

Chandra X-ray Observatory
The 2020 HRC Anomaly

Plan of action for the Side B Swap
Chandra Community Briefing
31 August 2020

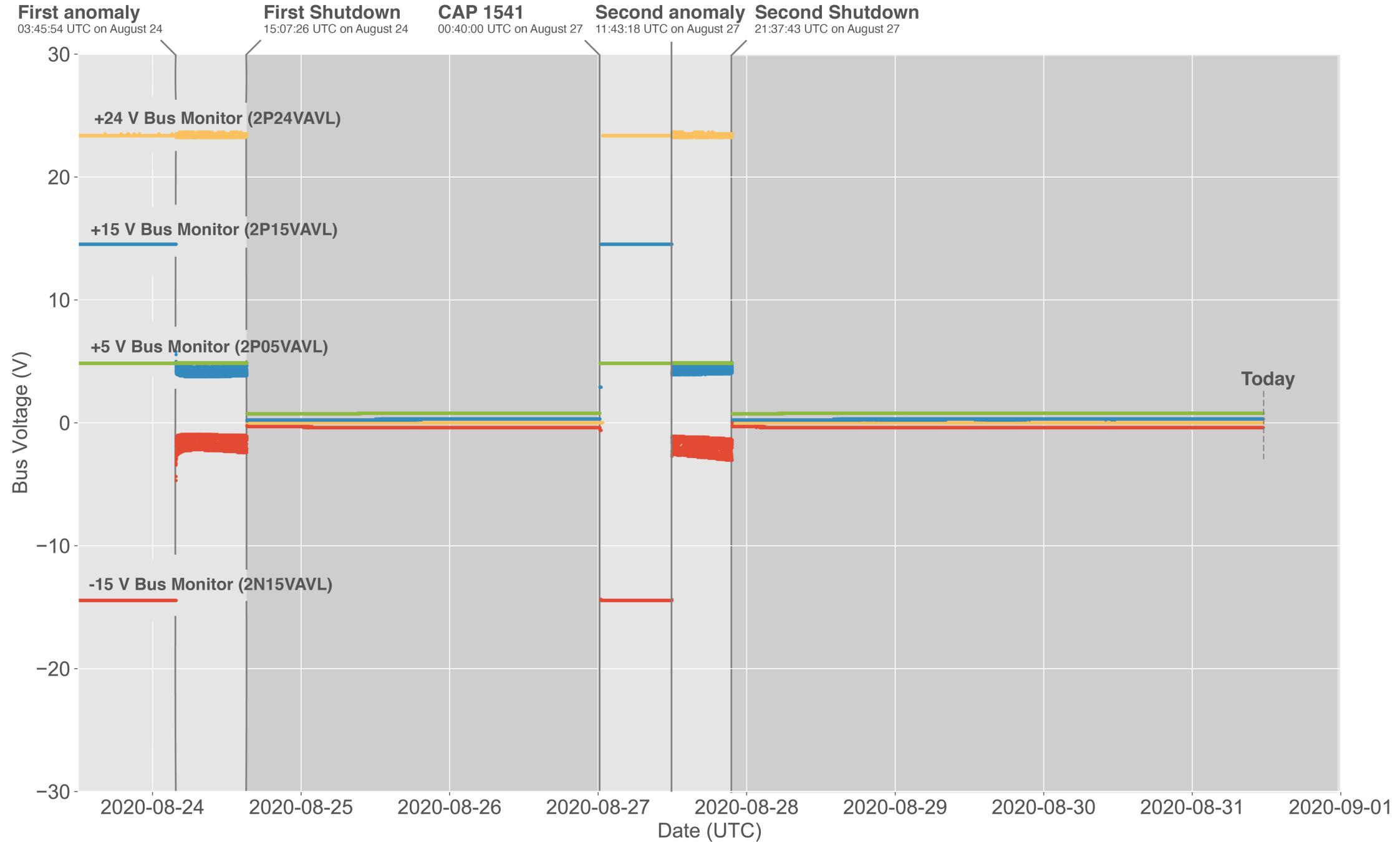
HRC Operations Team

D. Patnaude, R. Kraft, P. Nulsen, G. Tremblay, T. Gauron, A. Kenter, K. Gage, B. Bissell, G. Austin, J. Chappell

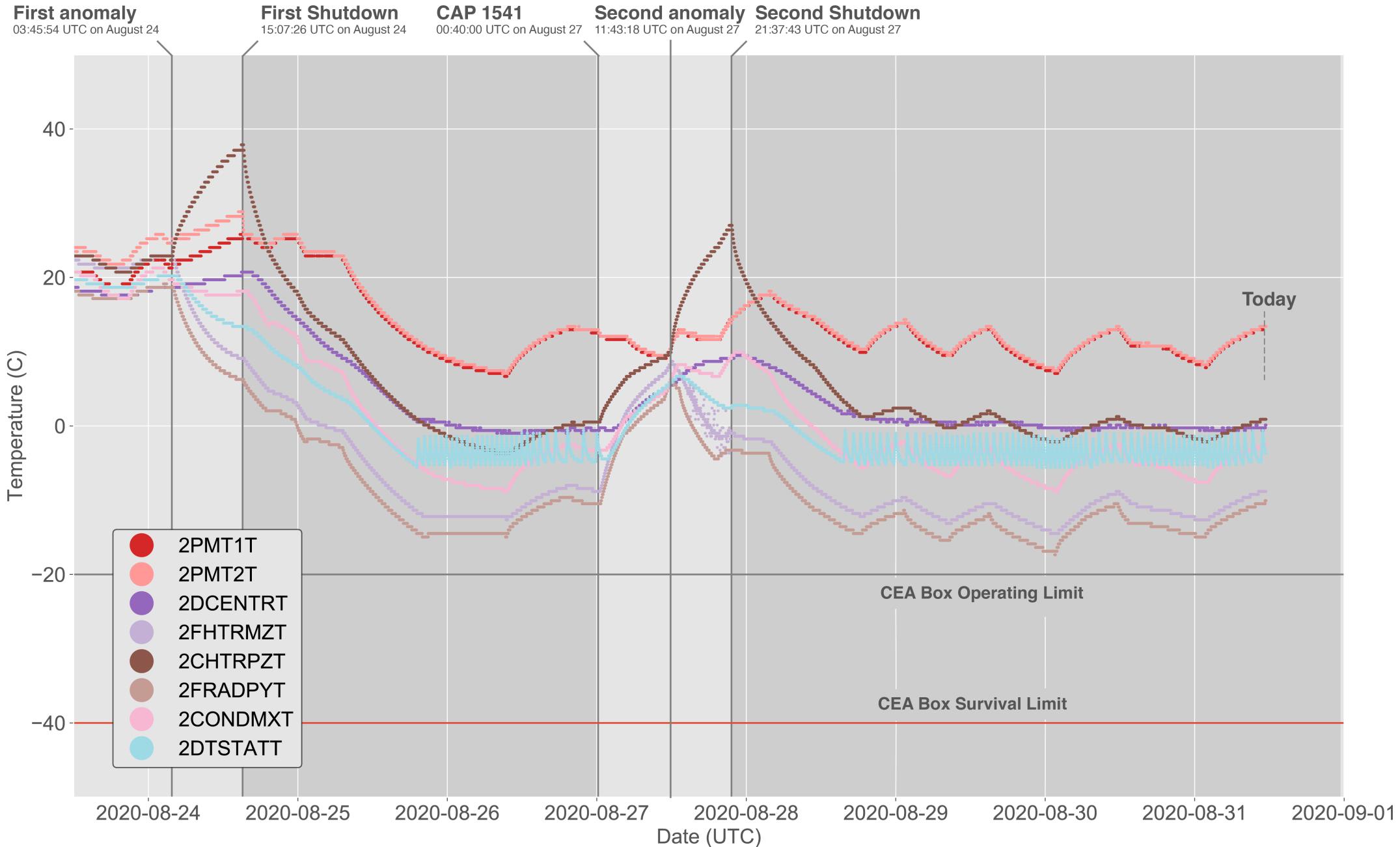
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The Anomaly

- Last Monday, the HRC suffered from an anomaly of unknown cause, leading to off-nominal voltages on its +/- 15 V bus. The HRC cannot be used for science in this state.
 - A detailed discussion of the anomaly and our subsequent actions can be found in our prior community briefings from last week, [linked here](#).
- Our first plan of action was to **attempt a reset of the Side A power supply bus**, which we successfully completed last Wednesday evening via CAP 1541.
- While the Side A reset did initially return the voltages to nominal values, **the anomaly occurred for a second time** ~11 hours later.
- Our next option is to **swap the HRC's power configuration to CEA B on the redundant bus**.



Current thermal status



Preparations for the Side B Swap

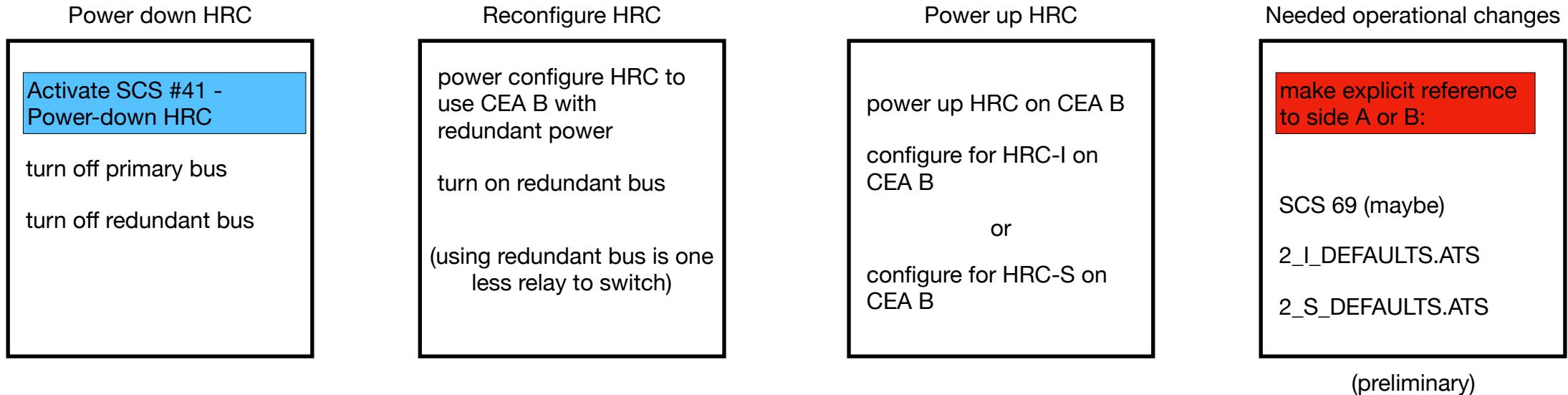
- For the past three days, the HRC Team has been reviewing, analyzing, and discussing the commanding and procedures necessary to make this change.
 - This includes an informative search through shift reports, early logs and notes, etc.
- We have now prepared **CAP 1543**, which will switch the +5 V, +/- 15 V, and +24 V power supplies to Side B electronics using the redundant +28 V power bus from the spacecraft.
 - The CAP is essentially a sequence of three known Standard Operating Procedures, **SOPs 62035, 62036, & 62021**, with breakpoints between them for operator and HRC Team confirmation. There has been a clear plan for a Side B swap since launch.
 - The CAP also performs a configuration of the instrument to its default state. It does *not* power up the voltages on the microchannel plates, nor does it bring up the anti-coincidence shield. This will be done after the HRC Team is satisfied with the health and stability of the instrument following the CAP.

Plan for today and this week

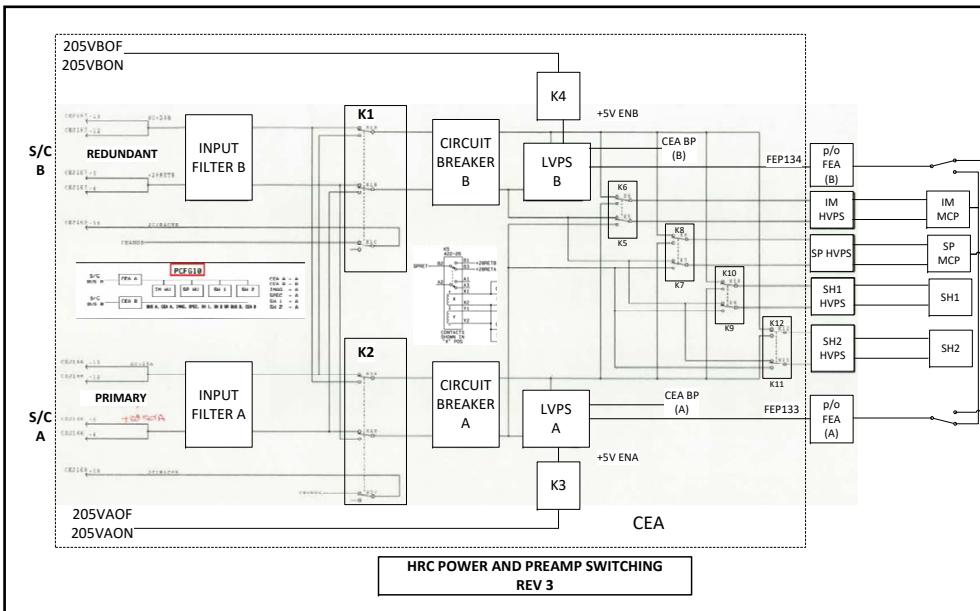
- Pending a successful review immediately following this meeting, the HRC Team and the FOT **are prepared to execute this CAP today**.
 - We will use this afternoon's 1:40pm EDT (BOT) extended (2h 35m) comm pass for this activity.
- **If the swap is fully successful**, our plan is to leave the instrument in its post-CAP configuration for a few days.
- We would then plan to power on the HRC anticoincidence shield following this “soak” period.
- A full turn-on of the HRC High Voltage can be arranged after the shield has been brought up (perhaps a ~week), after ACIS has returned to science.

EXTRA SLIDES

Top level diagram to switch from Side A on the Prime Bus to Side B on the Redundant Bus



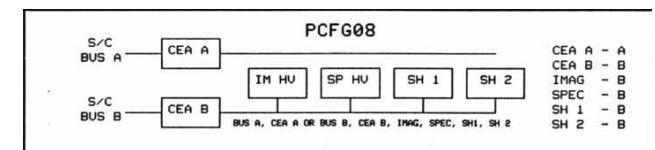
HRC Power Switching



Post-power up HRC

turn on PMT#2
turn on HRC-I/S HV
ramp up HRC-I/S HV - point at blank sky

Swap to side B on redundant bus is represented by power configuration PCFG08



Hypotheses from 8/28 tag

- The rapid reoccurrence of the anomaly **now disfavors a single event upset (SEU) scenario.**
- Timescales argue that **the thermal environment is one potential driver of whatever is causing the anomaly.**

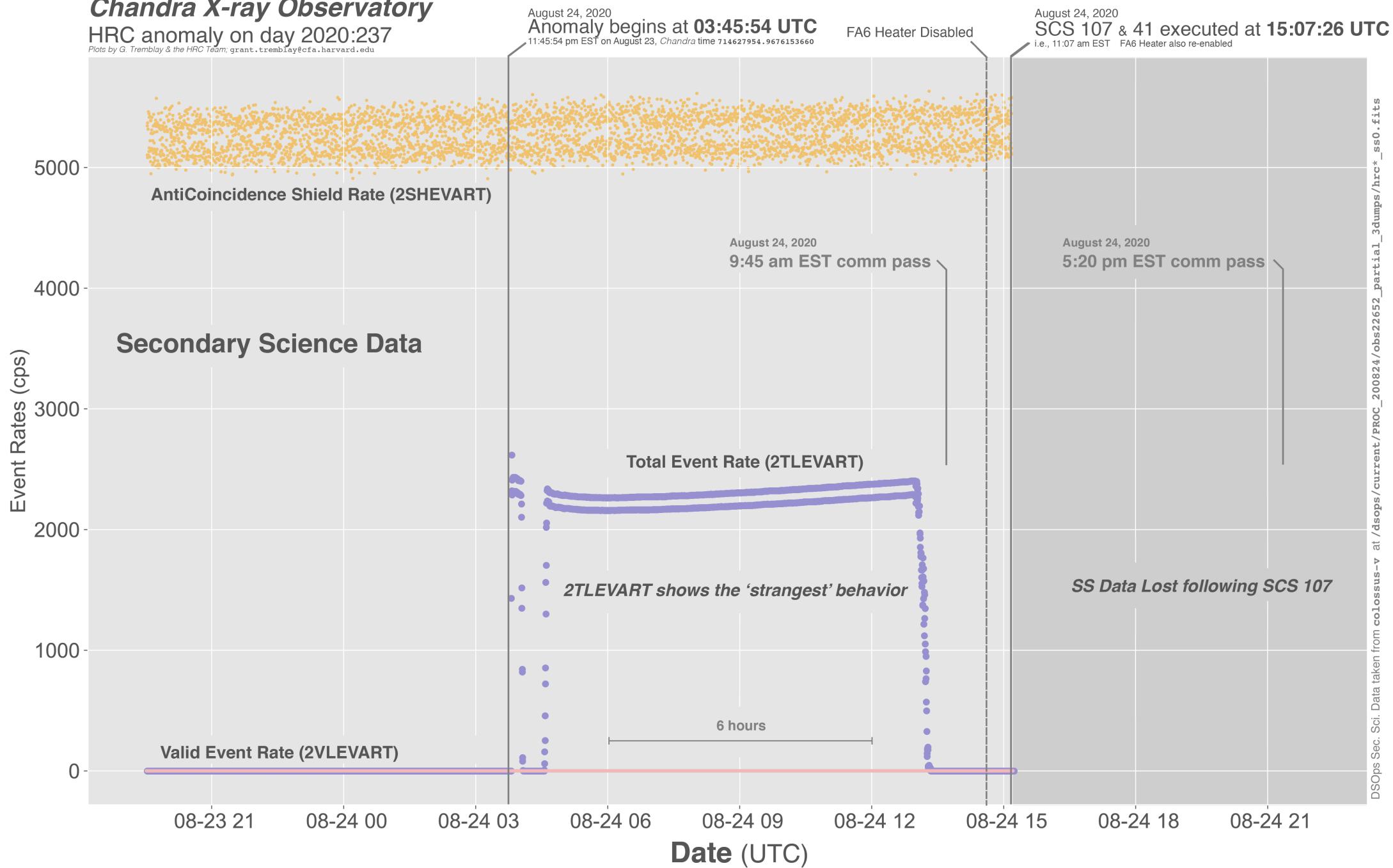
Hypotheses from 8/26 tagup

- The anomaly is due to a problem **with the +/- 15 V power supply bus on Side A**
 - **A problem in the +15 V bus would also take out the -15 V power supply due to DC-to-DC design**
 - A problem in the -15 V bus would not cause issues with the +15 V bus
 - **There could be a fault in the electronics on this bus**
 - A load fault that is transient in nature (e.g. an SEL). This should clear with a power cycle.
- ... or ...
- A failed component that is dragging down the +15V bus. This would not clear with a power cycle and would require an A/B swap.
- ... or ...
- A latched-up component downstream of DC-DC converter may clear with power cycle. Otherwise an A / B swap is indicated.

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HRC anomaly on day 2020:237

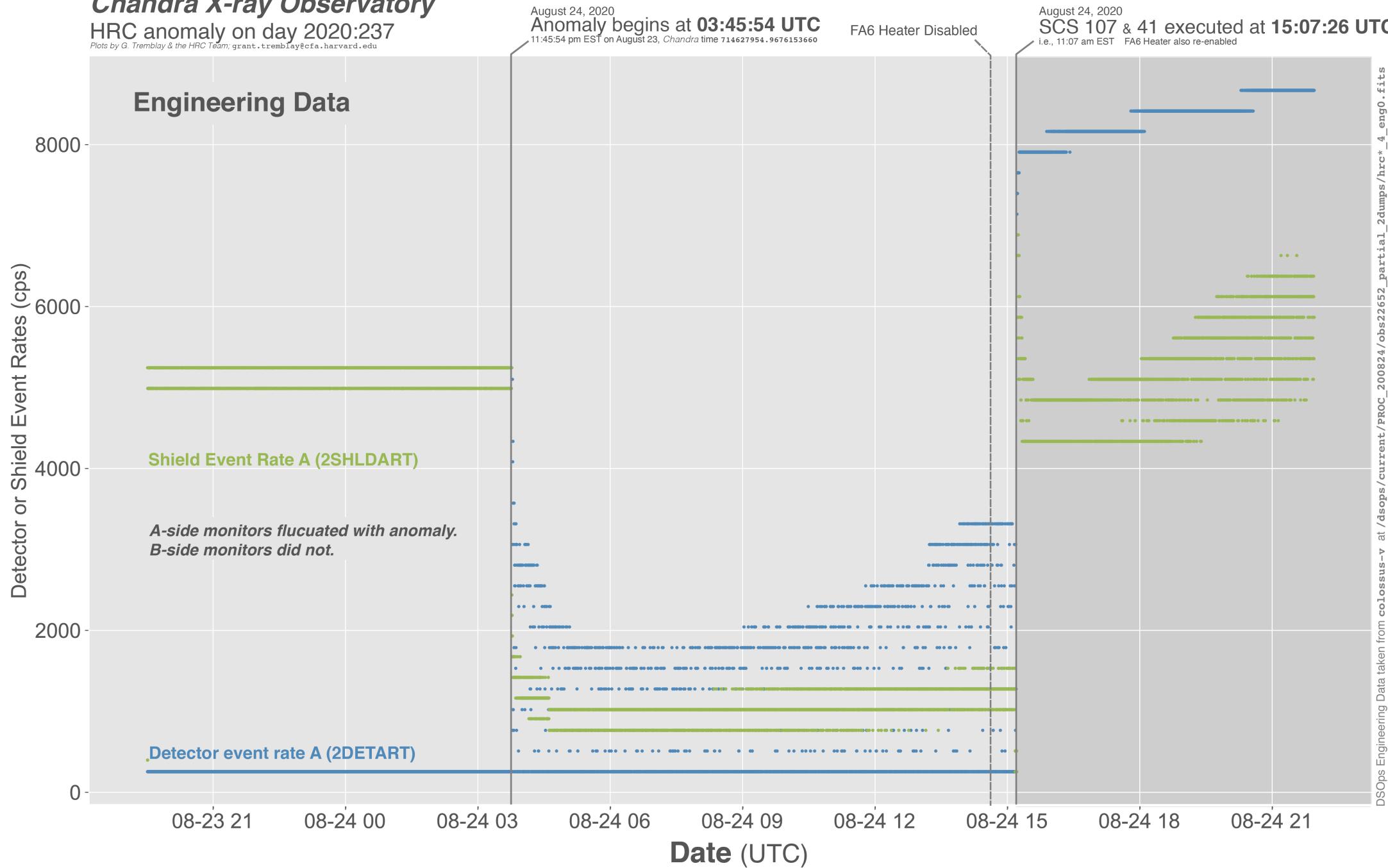
Plots by G. Tremblay & the HRC Team: grant.tremblay@cfa.harvard.edu



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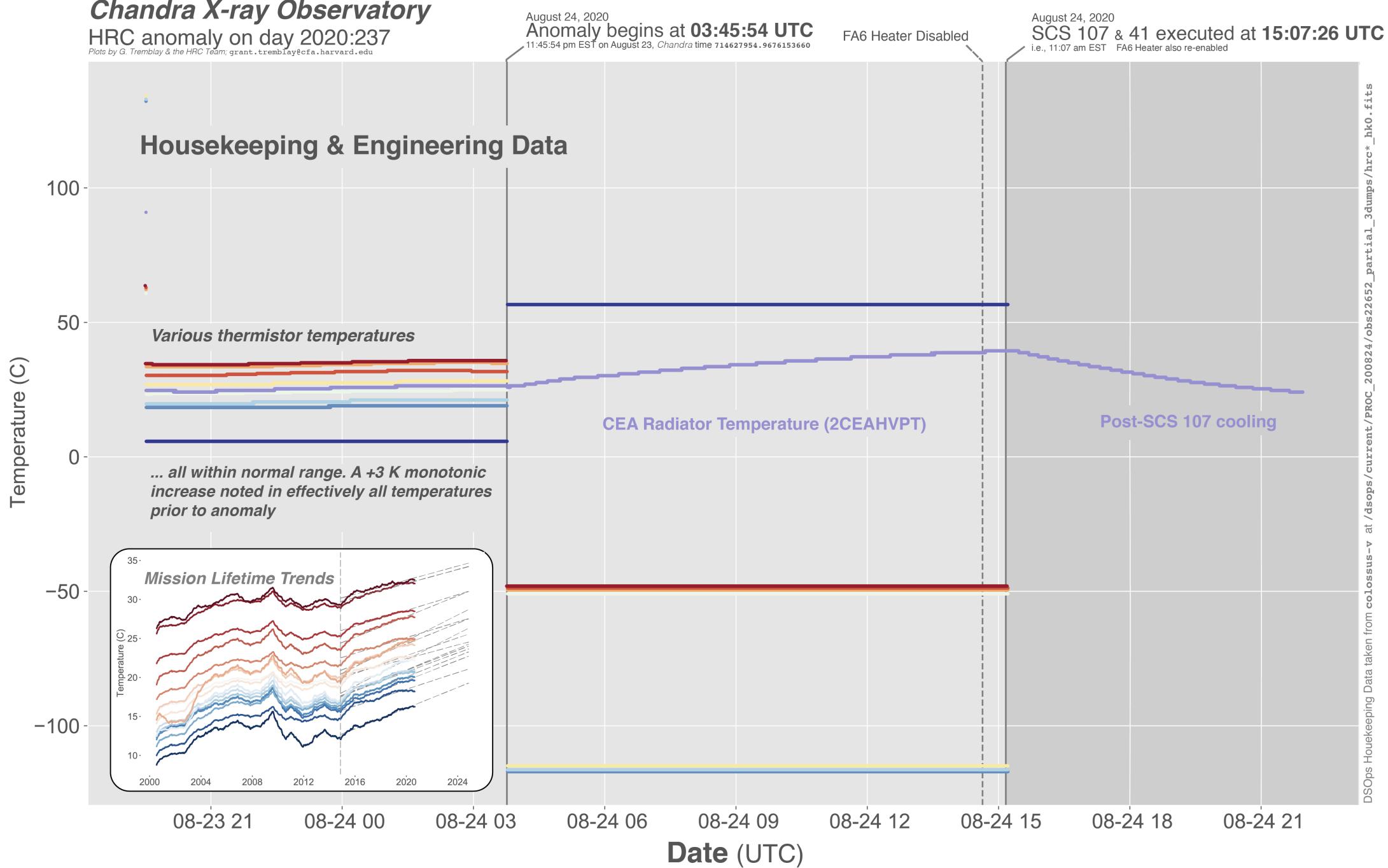
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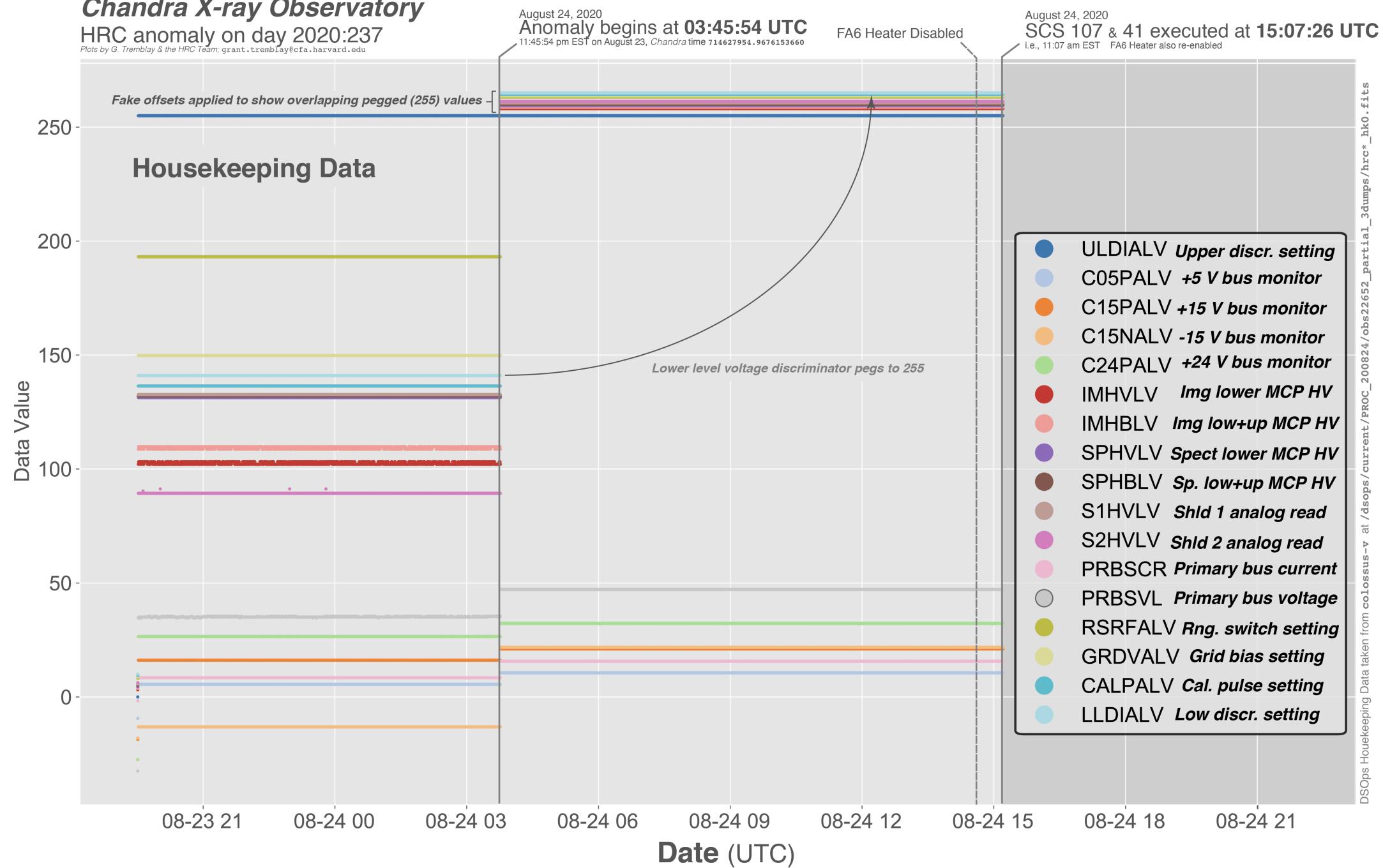
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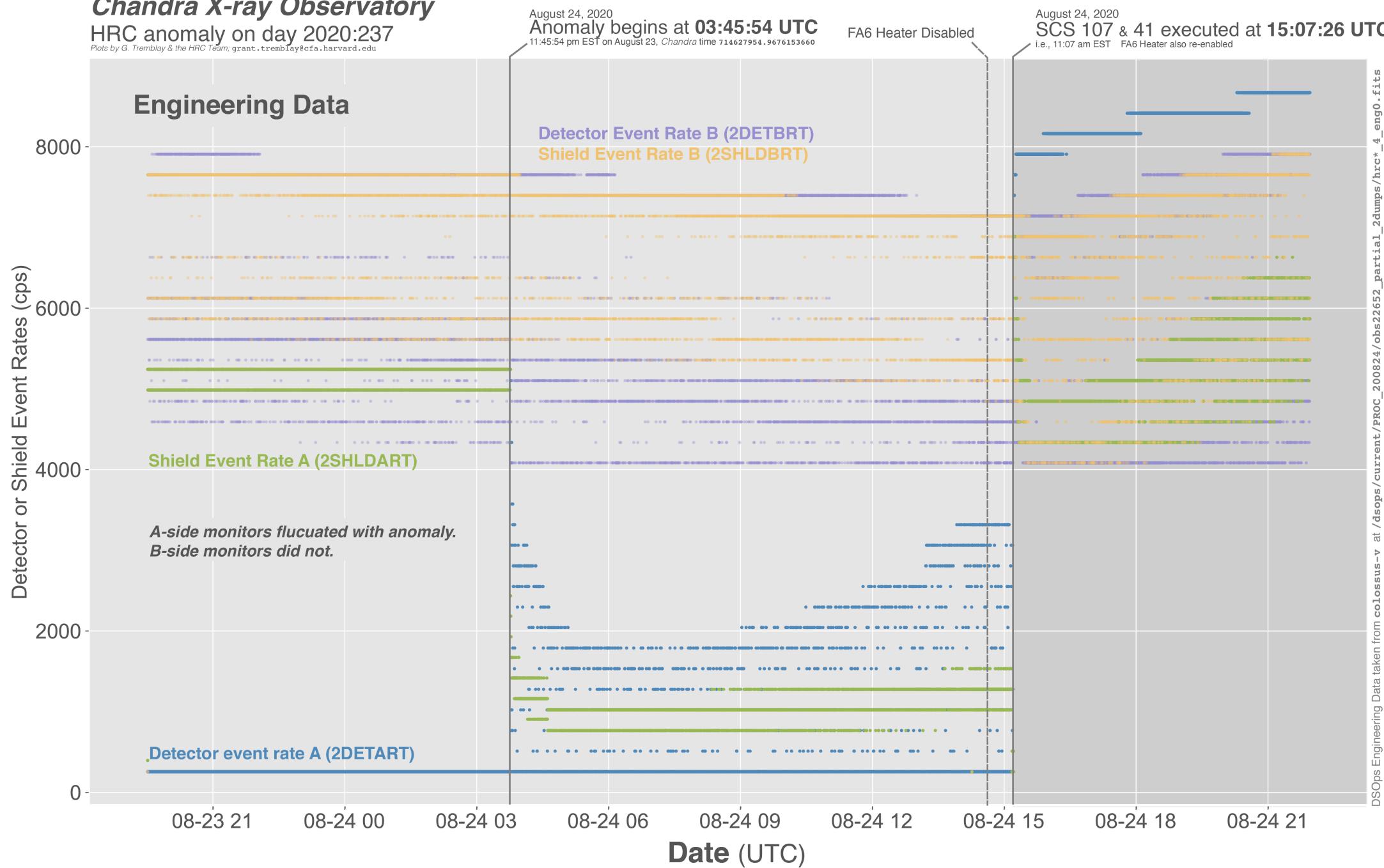
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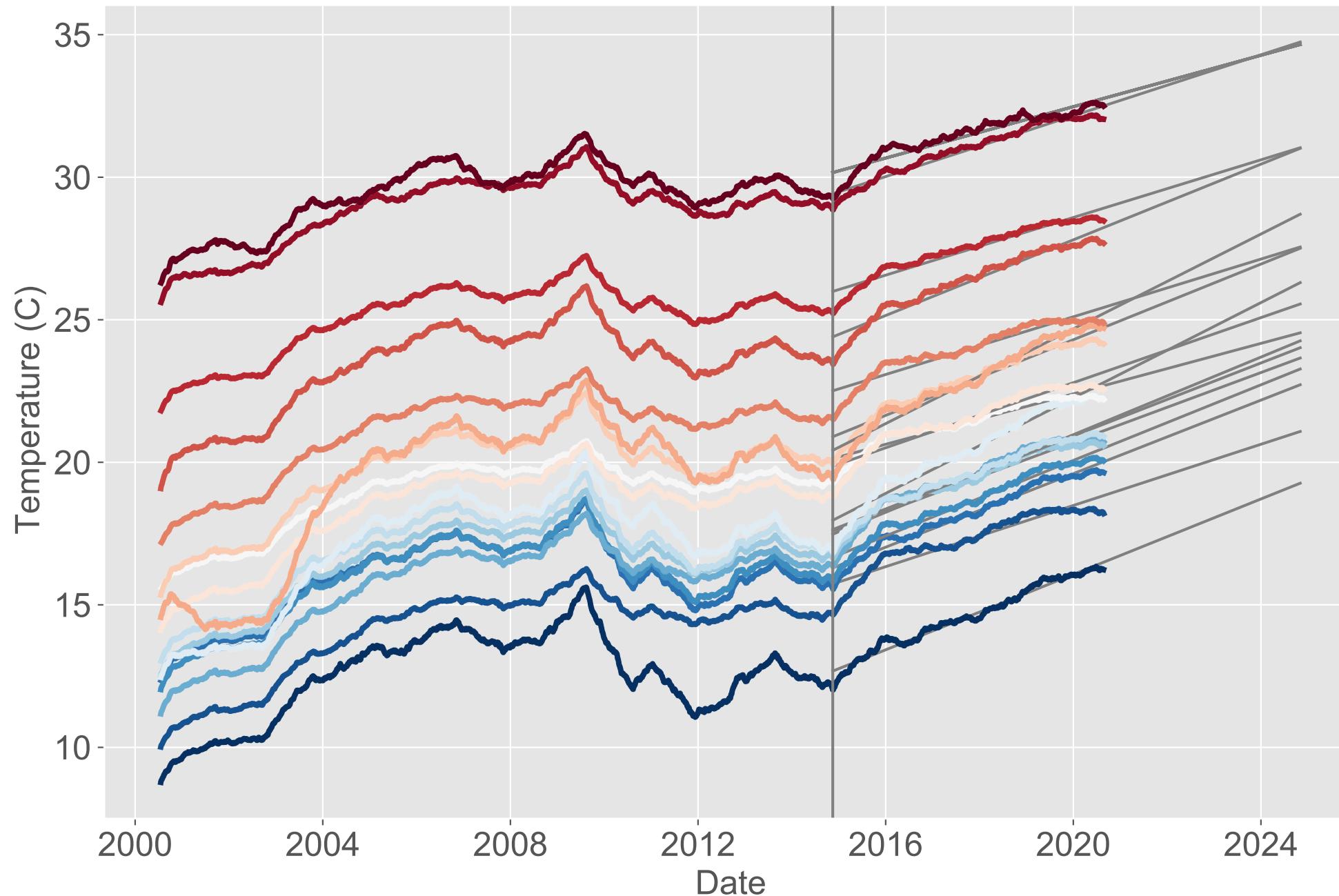
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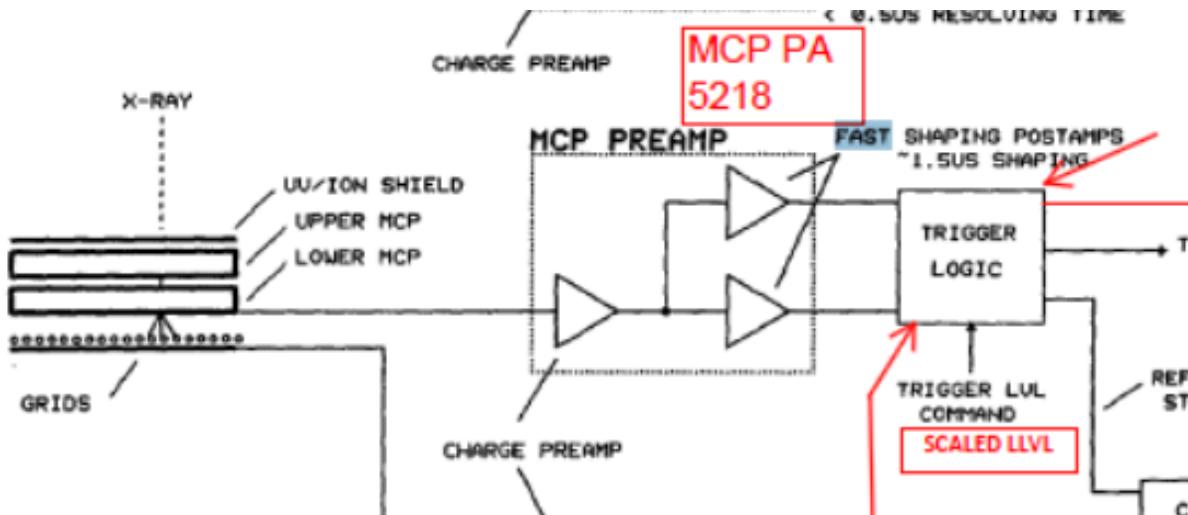
Forecasted HRC Thermistor Temperatures if Current Slopes Hold



Explanation of trigger noise

(T. Gauron)

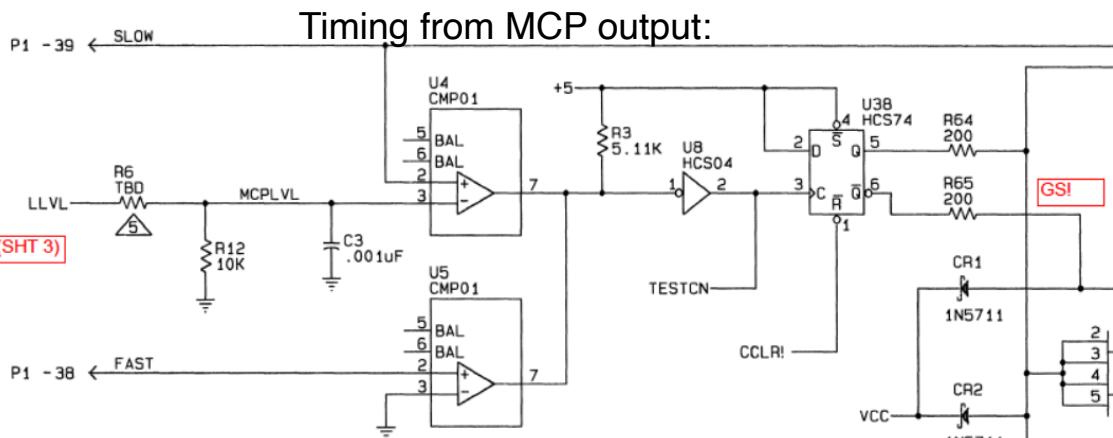
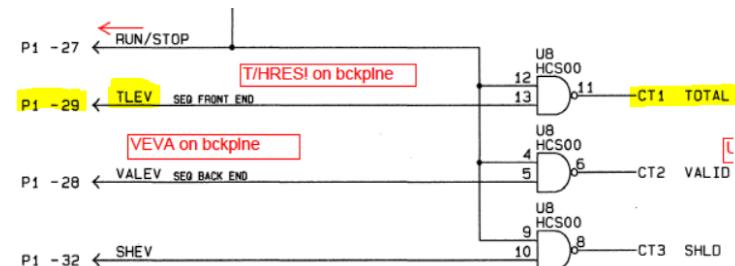
Top Level Trigger from MCP output:



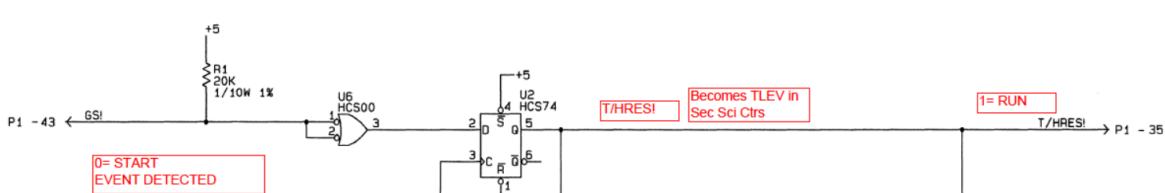
T/HRES! Routes to SEC_SCI_CTR pin 29 on backplane

CE	SLOT 11	SEC SCI CTR A
5209		
CEJ11	0 1	CE+15A
46	0 2	CEGND
47	0 3	CE-15A
48	0 4	CEGND
49	0 5	CE+5A
50	0 6	CE+5A
51	0 7	
52	0 8	
53	0 9	
54	0 10	
55	0 11	
56	0 12	
57	0 13	
58	0 14	
59	0 15	
60	0 16	
61	0 17	
62	0 18	
63	0 19	
64	0 20	
65	0 21	
66	0 22	
67	0 23	
68	0 24	
69	0 25	
70	0 26	
71	0 27	
72	0 28	
73	0 29	T/HRES!
74	0 30	SECCTC! A
75	0 31	1.024MHZ2A
76	0 32	

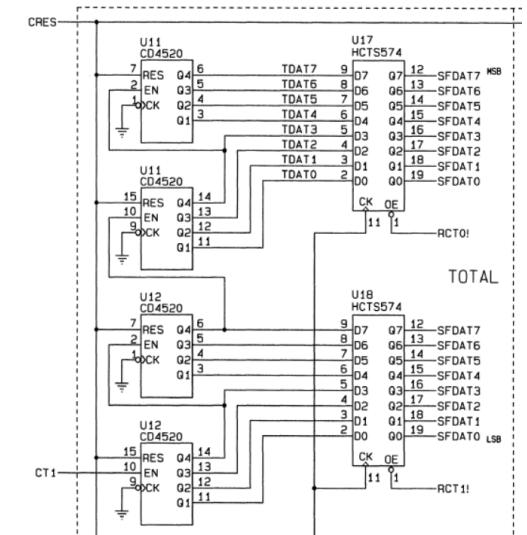
It's called TLEV on the SEC_SCI PWA



GSI! is synced with S/C clock and becomes T/HRES! in SEQUENCER



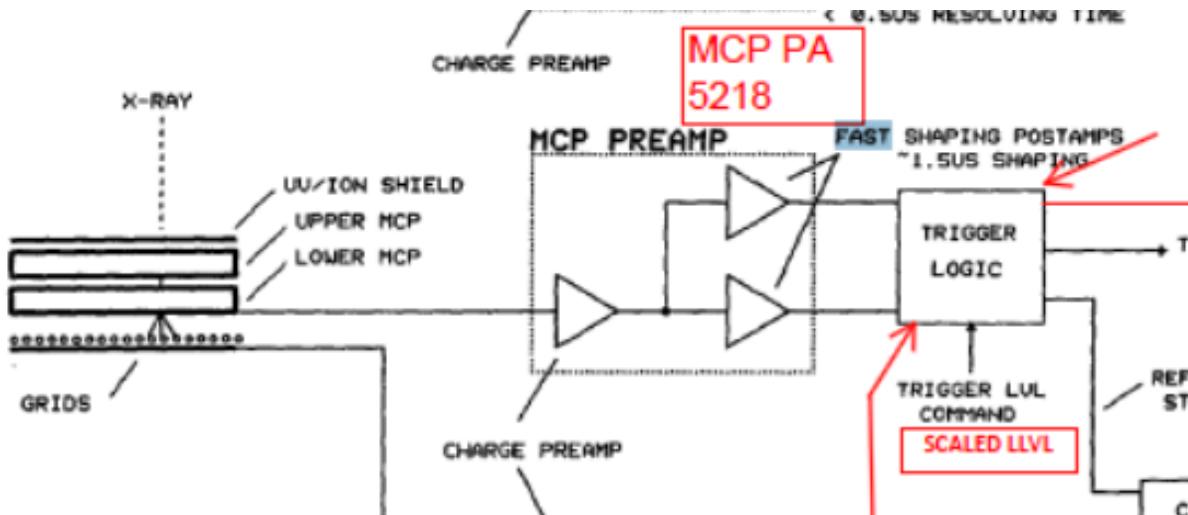
...and gets counted for TOTAL EVENTS



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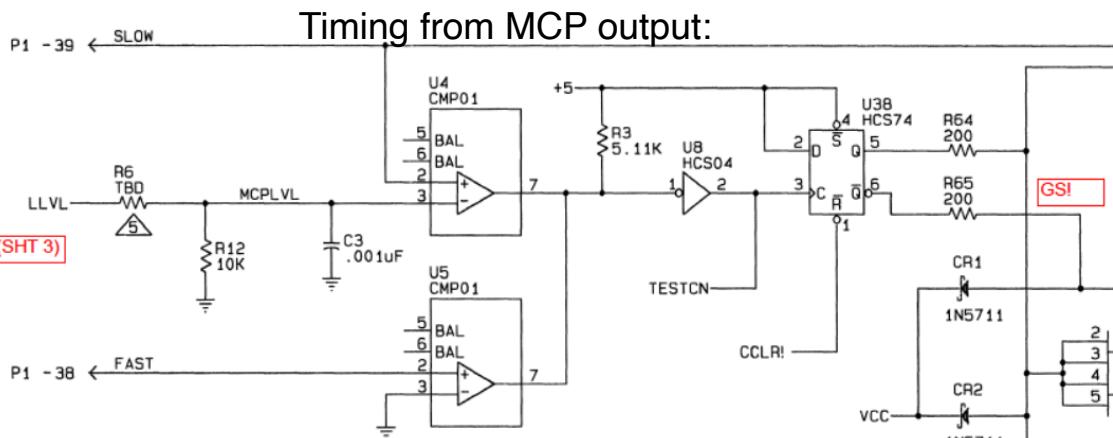
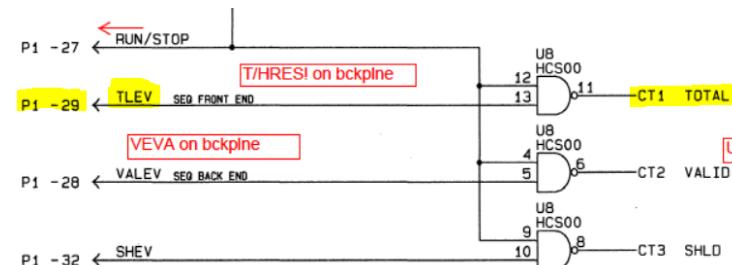
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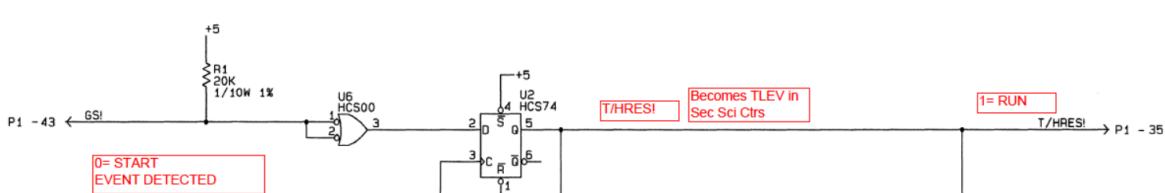
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53	0 8	
54	0 9	
55	0 10	
56	0 11	
57	0 12	
58	0 13	
59	0 14	
60	0 15	
61	0 16	
62	0 17	
63	0 18	
64	0 19	SFDAT7A
65	0 20	SFDAT6A
66	0 21	SFDAT5A
67	0 22	SFDAT4A
68	0 23	SFDAT3A
69	0 24	SFDAT2A
70	0 25	SFDAT1A
71	0 26	SFDAT0A
72	0 27	
73	0 28	VEVA
74	0 29	T/HRES! A
75	0 30	SECTIC! A
76	0 31	1.024MHZ2A
	0 32	

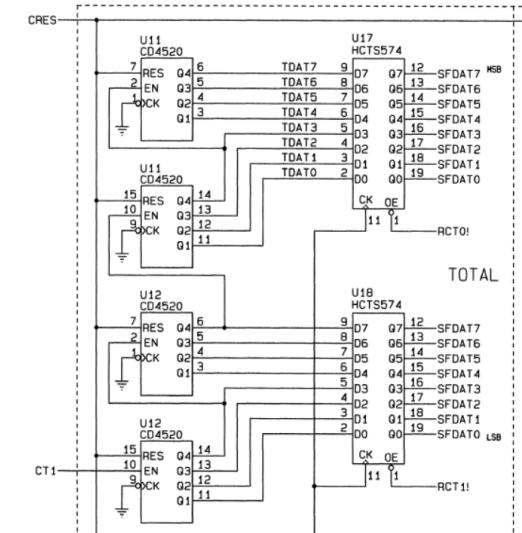
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GSI is synced with S/C clock and becomes T/HRES! in SEQUENCER



...and gets counted for TOTAL EVENTS



Prime and redundant side wiring

(T. Gauron)

