



# Chandra Flight Note

FLIGHT NOTE NO.	475
SUBJECT	HST ASC Failure
DATE	02-14-08
AUTHOR	Bradley Bissell

## 1.0 Summary

Between June 2006 and January 2007 the HST mission experienced failures with their ACS Side-1 and Side-2 electronics. Anomaly Review Boards (ARB) were formed to conduct ground tests and analyses to try to determine the root cause of the failures. For both the Side-1 and Side-2 failures, the ARB found that Interpoint DC/DC power converters were among the most likely candidates for the failures observed. While the ARB reports on both failures did not clearly indicate why the suspect components failed, their recommendations regarding the power and thermal cycles experienced by the ACS electronics might suggest these were factors that may have contributed to accelerated aging/stress on the HST ACS components.

This Flight Note focuses on the Interpoint DC/DC power converters used on Chandra and how the lessons learned from the HST failures might be applied to the Chandra mission. In contrast to the HST usage, the power converters onboard Chandra are not power cycled and experience thermal fluctuations over a smaller range. In addition the Chandra model numbers are different and they are used in an alternate circuit configuration. Due to the lack of power cycling and reduced thermal variations, the Chandra operating environment is possibly more benign and less stressing on the electrical components. Based on the available data at this time, there are no recommended changes to how the Chandra units are utilized. Should a power converter onboard Chandra fail in a similar manner to that seen on HST, a swap to the backup equipment could be accomplished to resume mission activities.

## 2.0 Background

### 2.1 ACS Side-1 Failure

On June 19, 2006, the ACS Side 1 experienced a failure and transitioned to Suspend Mode when its processor detected an out-of-limits condition. The ARB concluded that the most likely cause of the ACS Side 1 on-orbit anomaly was a result of the loss of the ACS Side 1 CEB +15V power rail in either an open or shorted condition. The most likely cause of the ACS failure was the MFL2815D

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Interpoint DC-DC converter within Low Voltage Power Supply LVPS Board #3. The next most likely cause is a short to ground in the transformer T6 on the same LVPS board. This conclusion was substantiated via engineering evaluations, focused ground tests, historical performance, and on-orbit telemetry collected at the time of the anomaly. As a result of the investigations the HST ARB recommended changes in the ACS operations to reduce thermal and power cycling.

For additional details concerning the ACS Side 1 failure, see **Appendix A**.

## **2.2 ACS Side-2 Failure**

On January 27, 2007, the ACS experienced a loss of power from the Power Distribution Unit (PDU) supporting ACS Side-2.

The ARB analysis of the various electrical components showed that the most likely candidates for a component failure were wet tantalum capacitors, EMI filters, or Interpoint DC/DC power converters. These components were used on all three LVPS boards and in the Auxiliary Power Box (APB), which powers the Anneal heaters. Currently anneals, raising the CCD temperature by 30°C for a limited period of time, are performed monthly to reduce the number of hot pixels on the science instruments. The identification of the most likely failure candidates was substantiated via engineering evaluations, focused ground tests, and on-orbit telemetry collected at the time of the anomaly.

In the report concerns were raised regarding possible resonances due to the HST ACS circuit configuration with multiple converters hanging off an under-damped EMI filter. The ARB recommended additional testing be performed in this area.

For additional details concerning the ACS Side-2 failure, see **Appendix B**.

## **2.3 NASA Action Item**

In February 2007, a NASA Action Item was opened for the Chandra program to investigate the use of Interpoint DC/DC converters onboard the Chandra spacecraft. The investigation found the use of Interpoint DC/DC converters in four units, the PEA, SEA, EIO, and HRC. Analysis continued on the individual units and, using the original HST ACS ARB findings, differences were found between the units used on HST and on Chandra.

### 3.0 Analysis Results/Findings

#### 3.1 DC/DC Converter Models

Tables 1 and 2 below outline the differences between Interpoint DC/DC converters used on HST and Chandra. The data is provided from vendor specification sheets as of mid-2006, but it is believed to be representative of units used on HST and Chandra.

HST Interpoint DC/DC converters are the source of regulated power for the ACS. They are separated among three boards. Each Board has more than one DC/DC converter connected to one EMI filter. See **Appendix C**: “*MFL Single and Dual DC/DC Converters*, Crane Aerospace & Electronics Power Solutions”, for more information regarding the MFL type Interpoint DC/DC converter.

**Table 1: HST DC/DC converters**

HST	Model #	#/Type of Output	Power Rating	Qty & Where Used	Allowable Temperature Range
	MFL2815D	1: +15V 1: -15V	65W	2: LVPS1 1: LVPS2 1: LVPS3	-55°C to +125°C
	MFL2812S	1: +12V	60W	1: LVPS2 2: LVPS3	-55°C to +125°C
	MFL2815S	1: +15V	65W	4: LVPS2	-55°C to +125°C
	MFL2805S	1: +5V	50W	2: LVPS1 2: LVPS2 1: LVPS3	-55°C to +125°C

Chandra Interpoint DC/DC converters are the source of regulated power within each of the PEA, SEA, EIO, and HRC units. They are single strung with one EMI filter connected to one DC/DC converter. See **Appendix D**: “*MTR Single, Dual, and Triple DC/DC Converters*, Crane Aerospace & Electronics Power Solutions”, for more information regarding the MTR type Interpoint DC/DC converter.

**Table 2: Chandra DC/DC converters**

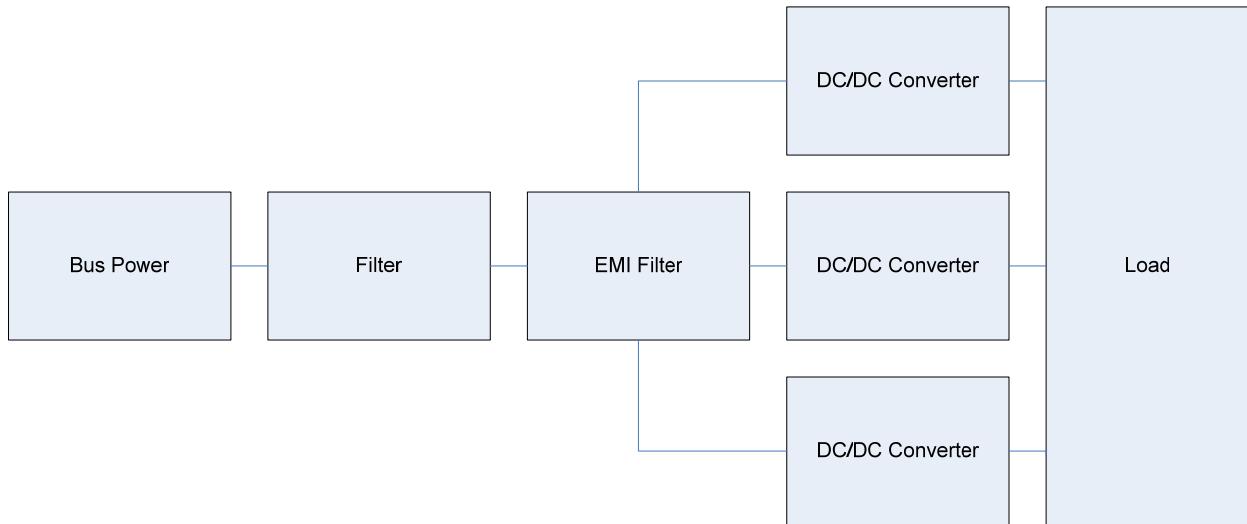
Chandra	Model #	#/Type of Output	Power Rating	Qty & Where Used	Allowable Temperature Range
	MTR28515TF	1: +5V 1: +15V 1: -15V	30W	2: PEA 1: EIO 2: SEA	-55°C to +125°C
	MTR2805SF	1: +5V	25W	2: HRC	-55°C to +125°C
	MTR2812SF	1: +12V	30W	4: HRC	-55°C to +125°C
	MTR2815DF	1: +15V	30W	2: HRC	-55°C to +125°C

While the MFL and MTR units have comparable output types and allowable temperature ranges, the MFL units have higher power ratings/power density values over the MTR units, and the MFL units can be operated with multiple units in a parallel configuration.

### 3.2 *Circuit Design*

The high level circuit design differs between HST and Chandra with regard to DC/DC converter use. HST uses one EMI Filter connected to multiple DC/DC converters to drive the load. Chandra uses one EMI Filter connected to one DC/DC converter to drive the load in all but one case. In the case of HRC two MTR2812SFs are stacked to provide +24V. It is speculated that the use of one EMI filter to one DC/DC converter may provide a more benign or stable operating environment for the units.

Figures 1 and 2 below provide a top level circuit diagram example of how the Interpoint DC/DC converters are wired on HST and Chandra.



**FIGURE 1: Top Level HST Unit Circuit Diagram (example)**



**FIGURE 2: Top Level Chandra Unit Circuit Diagram (example)**

See **Appendix E** for SEA design/reference information relative to the DC/DC converter usage within the unit.

See **Appendix F** for PEA design/reference information relative to the DC/DC converter usage within the unit.

See **Appendix G** for EIO design/reference information relative to the DC/DC converter usage within the unit.

See **Appendix H** for HRC DC/DC design/reference information relative to the DC/DC converter usage within the unit.

### **3.3 Operating Environment**

HST and Chandra experience different thermal effects due to orbit configuration and science instrument use. HST experiences higher thermal variance compared to Chandra. The ACS Side-1 final report questioned thermal cycling as being a potential stress to components on the LVPS boards, and recommended that the powering off of the HRC and ACS be minimized to reduce risk to the components through thermal degradation.

<b>Spacecraft</b>	<b>Component</b>	<b>Typical Temperature Variance</b>	<b>Reasons</b>
HST	LVPS Boards	~ 30°C	<ul style="list-style-type: none"><li>• Temperatures fluctuate per orbit due to LEO configuration.</li><li>• HRC is powered off when the SBC is powered causing thermal fluctuation.</li><li>• ACS is powered down approximately once every month to perform anneal operations</li></ul>
Chandra	SEA	~ 7°C	<ul style="list-style-type: none"><li>• The SEA Box and Power Supply experience minimal temperature cycling effects due to attitude.</li><li>• The SEA is not powered off during normal operations.</li></ul>
	PEA	~ 2°C	<ul style="list-style-type: none"><li>• The PEA Case and Power Supply see minimal temperature cycling effects due to attitude.</li><li>• The PEA is not powered off during normal operations</li></ul>
	EIO	~ 40°C	<ul style="list-style-type: none"><li>• The EIO experiences high temperature fluctuations due to attitude and mounting location on the outer -Z surface (sun facing)</li><li>• The EIO is not powered off during normal operations</li></ul>
	HRC	~ 3°C	<ul style="list-style-type: none"><li>• The HRC sees minimal temperature fluctuations due to attitude</li><li>• The HRC is not powered off during normal operations</li></ul>

### **3.4 Chandra Response to Unit Failure**

In the event of an Interpoint DC/DC converter failure onboard Chandra, the response is straightforward. Loss of a converter would shut down the box, and a manual swap to the redundant side (except for the EIO) is necessary to recover operations. A failure of any one converter within HRC would result in the loss of the A-side of the instrument; swapping to the B-side is necessary to continue HRC operations. In the case of the EIO, which powers EPHIN, there is no redundant unit, and a swap to using the HRC as a radiation monitor is necessary. Procedures are in place for making this EPHIN-to-HRC swap, if needed.

Long term, effort to create side-B swap procedures (where they do not already exist) has been added to the FOT Engineering activity planning list.

## **4.0 Conclusion**

In evaluating the usage and configuration of Interpoint DC/DC power converters on Chandra versus HST, the following differences were noted:

- Chandra and HST do not share the same model Interpoint DC/DC converter units (MFL vs. MTR).
- Chandra only has one DC/DC converter connected to one EMI Filter. HST has more than one DC/DC converter per EMI Filter.
- Chandra does not power cycle the units containing Interpoint DC/DC converters.
- HST DC/DC converters experience temperature fluctuations over a greater range because of eclipses due to the low Earth orbit, and power cycling of science instruments. Chandra DC/DC converters experience nearly constant thermal conditions due to the highly elliptical orbit, spacecraft orientation toward the sun, and uninterrupted operations.

Due to the lack of power cycling and reduced thermal variations, the Chandra operating environment is possibly more benign and less stressing on the electrical components. Based on the available data at this time, there are no recommended changes to how the Chandra units are utilized. While the possibility always exists for a failure due to workmanship, or other causes, should a power converter onboard Chandra fail in a similar manner to that seen on HST, a swap to the backup equipment could be accomplished to resume mission activities.

FOT Engineering monitors performance of the PEA, SEA, EIO, and HRC units reporting key statistics and trends in the Engineering Biannual Reports. To date, no trends suggesting degraded DC/DC converter performance have been observed.

## **5.0 Recommendations**

- Close Action Item (NASA #07-03)
- Continue to monitor key voltages/ currents, where possible, for signs of anomalous behavior and provide updated trending via engineering quarterly reports.

## **6.0 References**

- *Appendix A: Advanced Camera for Surveys (ACS) Side 1, Anomaly Review Board (ARB) Final Report, Document Number: LMSS/C060410, August 24, 2006*
- *Appendix B: Anomaly Review Board (ARB) Final Report, Advanced Camera for Surveys Side 2, June 1, 2007 [draft]*
- *Appendix C: MFL Single and Dual DC/DC Converters, Crane Aerospace & Electronics Power Solutions (Created Feb 09, 2007)*
- *Appendix D: MTR Single, Dual and Triple DC/DC Converters, Crane Aerospace & Electronics Power Solutions (Created Sep 18, 2006)*
- *Appendix E: SEA Design / Reference Information*
- *Appendix F: PEA Design / Reference Information*
- *Appendix G: EIO Design / Reference Information*
- *Appendix H: HRC Design / Reference Information*

## **Appendix A:**

*Advanced Camera for Surveys (ACS) Side 1, Anomaly Review Board (ARB)  
Final Report, Document Number: LMSS/C060410, August 24 2006*

**Advanced Camera for Surveys (ACS)**  
**Side-1**  
**Anomaly Review Board (ARB)**  
**Final Report**

**Document Number:**  
**LMSS/C060410**

**August 24, 2006**

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## Introduction

On June 19, 2006 at 1:15:19 PM EDT, ACS Side 1 transitioned to Suspend Mode when its processor detected an out-of-limits condition. Telemetry later showed that all 158 telemetry parameters sampled by the ACS Wide Field Channel (WFC) and the High Resolution Channel (HRC) Charge Coupled Device (CCD) Electronics Boxes (CEBs) began reporting 12-bit hexadecimal FFF values (twelve 1s) in the same sampling cycle. A Tiger Team was immediately formed to evaluate the anomaly. On June 21, 2006, the ACS Anomaly Resolution Board (ARB) was officially formed.

## ARB Charter

The ACS ARB was tasked to perform a detailed investigation into the ACS Side 1 Suspend Event. Refer to Attachment #1 for a copy of the ARB Charter Letter. The board membership was established by HST Code 440, with the caveat that membership could be adjusted at the discretion of the Chairperson. In addition to the ARB members listed in attachment #1, the Chairperson, Roger Chiei, also saw fit to call on and request contributions from the following added ARB team members:

Chuck Harguth	BATC
Ken Albin	BATC
James Simons	BATC
Andy Hunt	BATC
Lynette Marbley	Code 303/442
Henning Leidecker	Code 562

The ARB Charter requested that the following five objectives be addressed:

1. Assess risks and benefits of diagnostic flight testing of ACS  
Status: Completed. ARB presented an ACS Side 1 Test Proposal on July 13, 2006.

See Attachment #2 for test proposal meeting charts.

The ARB recommended against executing an ACS Side-1 test for the following reasons:

- There is a low probability risk associated with running an ACS Side 1 test that could result in a loss of remaining ACS Side 1 assets if ACS Side 1 20 Amp fuse were to blow during the test
- Executing ACS Side 1 test is not expected to produce any results that will change how we operate ACS Side 2
- There is only one possible test outcome that could vindicate the Interpoint MFL2815D device as the root cause of the original anomaly.

HST Project concurred with the recommendation. No Side-1 on-orbit testing was executed.

2. If possible, identify the reason for the saturation of CEB parameters  
Status: Completed. Engineering evaluations and ground test engineering data support the fact that the ACS Side 1 anomaly was caused by the loss, either an open or a short, of the +15V CEB Power. A number of potential fault locations have been evaluated by the ARB. They are evaluated in this final report.
3. Assess whether the anomaly stressed any of the ACS components  
Status: Completed. A potential for overstress was identified in one postulated failure mode where an internal fault in an Interpoint MFL2815D results in an overvoltage condition of the -15V rail. Refer to the Overstress section on page 50 of this report for details.
4. Assess the risks, if any, of operating ACS on Side 2.  
Status: Completed. ARB presented interim findings during ACS Side 2 Switch FRR on June 29, 2006.  
See Attachment 3 for the ARB inputs to the FRR. The ARB unanimously recommended proceeding with switching to ACS Side 2 operation. The switch to ACS Side-2 operations was successful.
5. Determine if the cause of the ACS anomaly is a failure mode that is present in any of the other HST instruments, especially COS and WFC3  
Status: Completed. All ACS ARB findings and recommendations have been reviewed with respect to the COS, WFC3 and STIS designs. Software and circuit design changes have resulted. Refer to the COS, WFC3 and STIS sections on pages 59-60 of this report for details on the circuit design changes. Refer to the Software Evaluation section on page 20 for recommended flight software changes.

In addition, the ARB was also requested to present findings and recommendations to the project for each objective area as soon as results became available. The ARB complied with this request, keeping HST Code 440, Code 441, and Code 442 apprised of all findings and concerns as they arose and were being investigated.

All ARB meetings have been documented on the ACS CEB ARB website on the HST EDOCS server. The web address of the ARB website is:

<http://edocs.hst.nasa.gov/hstsystm/ACSCEBARB>

## On-Orbit Anomaly Summary

At about 2006/170/17:05, HST entered a planned loss-of-signal (LOS) time period. During this time, engineering data was not available in real-time, but was recorded on the on-board engineering data solid state recorder (SSR). When HST reacquired signal around 17:35, ACS was observed to have suspended during the LOS. During this time, HST did not pass through the South Atlantic Anomaly (SAA). In addition, no commands were sent to ACS via the stored command timeline.

NSSC-I Status Buffers (STBs) received during the LOS indicated the cause of the suspend event:

- ☒ At 170/17:15:25.868 → ACS 715 with parameter 0804F hex
- ☒ At 170/17:15:25.868 → ACS 707 with parameter 00FFF hex
- ☒ At 170/17:15:26.368 → ACS 715 with parameter 08051 hex
- ☒ At 170/17:15:26.368 → ACS 707 with parameter 00FFF hex

The status buffers messages and associated parameters reported that engineering data items contained in the Operate limits monitor table were out of limits. It was the out-of-limit check that resulted in the suspend action.

- ☒ JWAS1P15 was reading 0FFF hex → ACS WFC3 CEB ASPC +15V
- ☒ JWAS1P5 was reading 0FFF hex → ACS WFC3 CEB ASPC +5V

At about 20:28, an ACS memory dump was taken. The engineering data SSR was dumped and merged so telemetry analysis could be done.

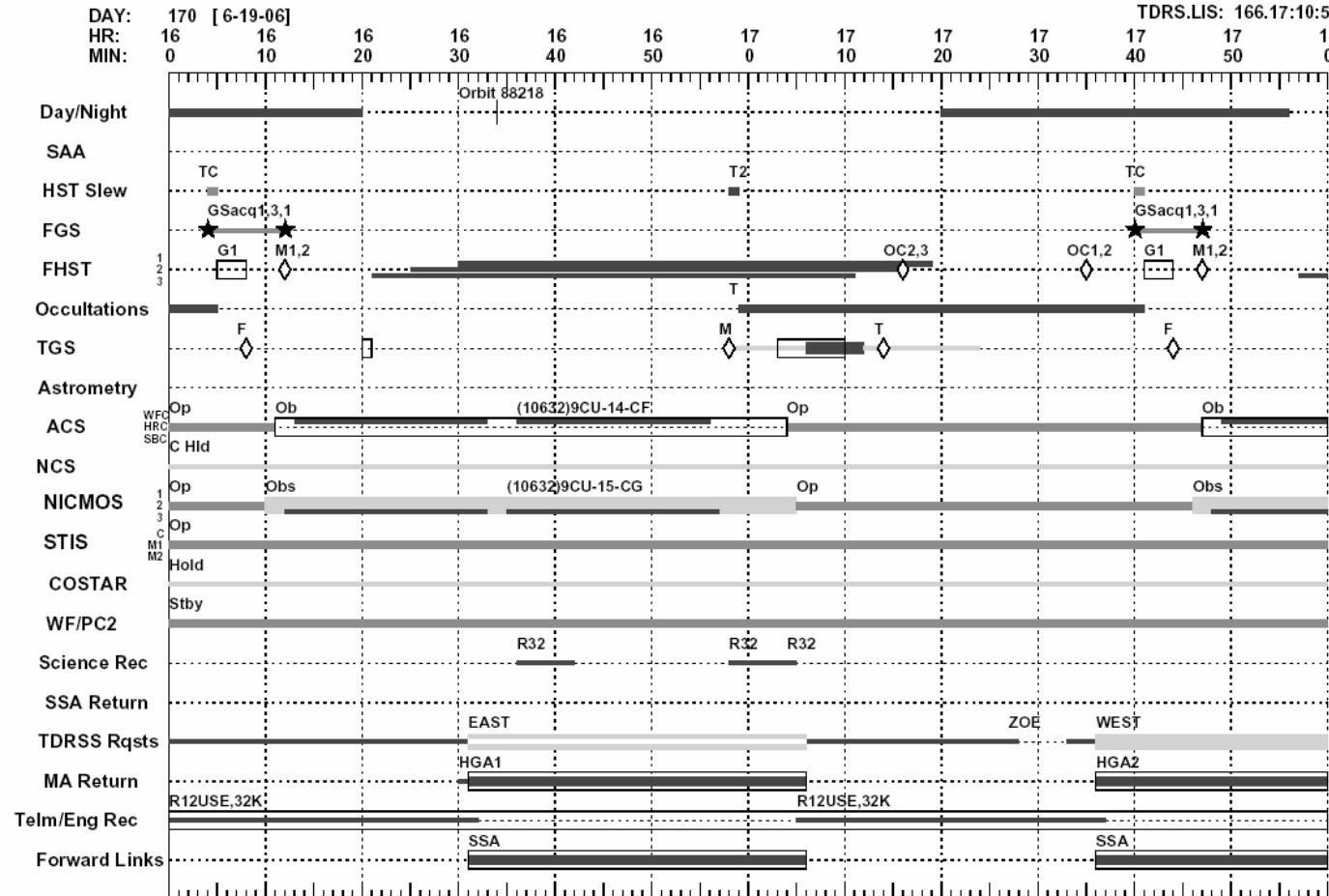


MEGG Version 32.65

## HST MISSION SCHEDULE EVENTS

sa170q01\_f

Page: 9  
SMSID: SA170Q01  
RUNID: m\_sa170q  
TDRS.LIS: 166.17:10:56



## On-Orbit Telemetry Data

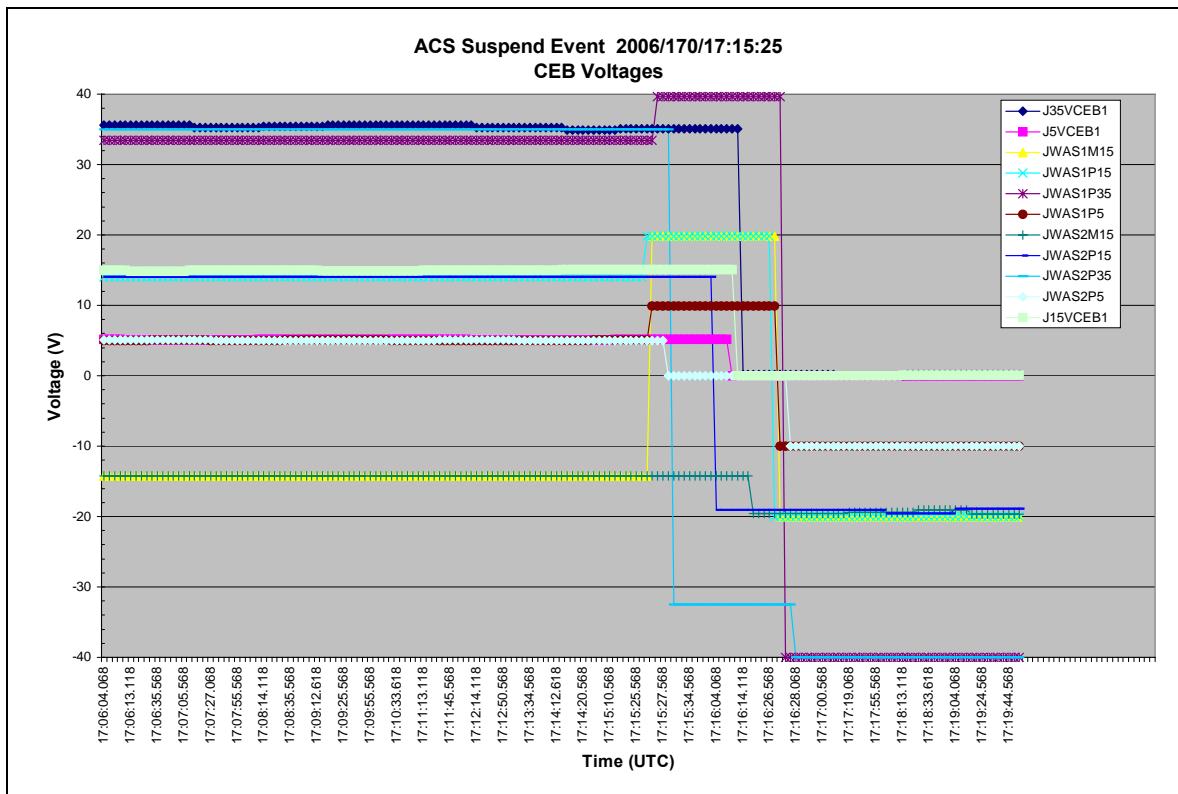
Once the Engineering SSR was dumped and merged, the analysis and trending of the telemetry data began. Analysis of the CEB voltages showed the voltages were stable until ACS suspended. The CEB voltages are turned off as part of an ACS suspend.

The following mnemonics are collected as RIU-direct telemetry:

- J35VCEB1
- J5VCEB1
- J15VCEB1

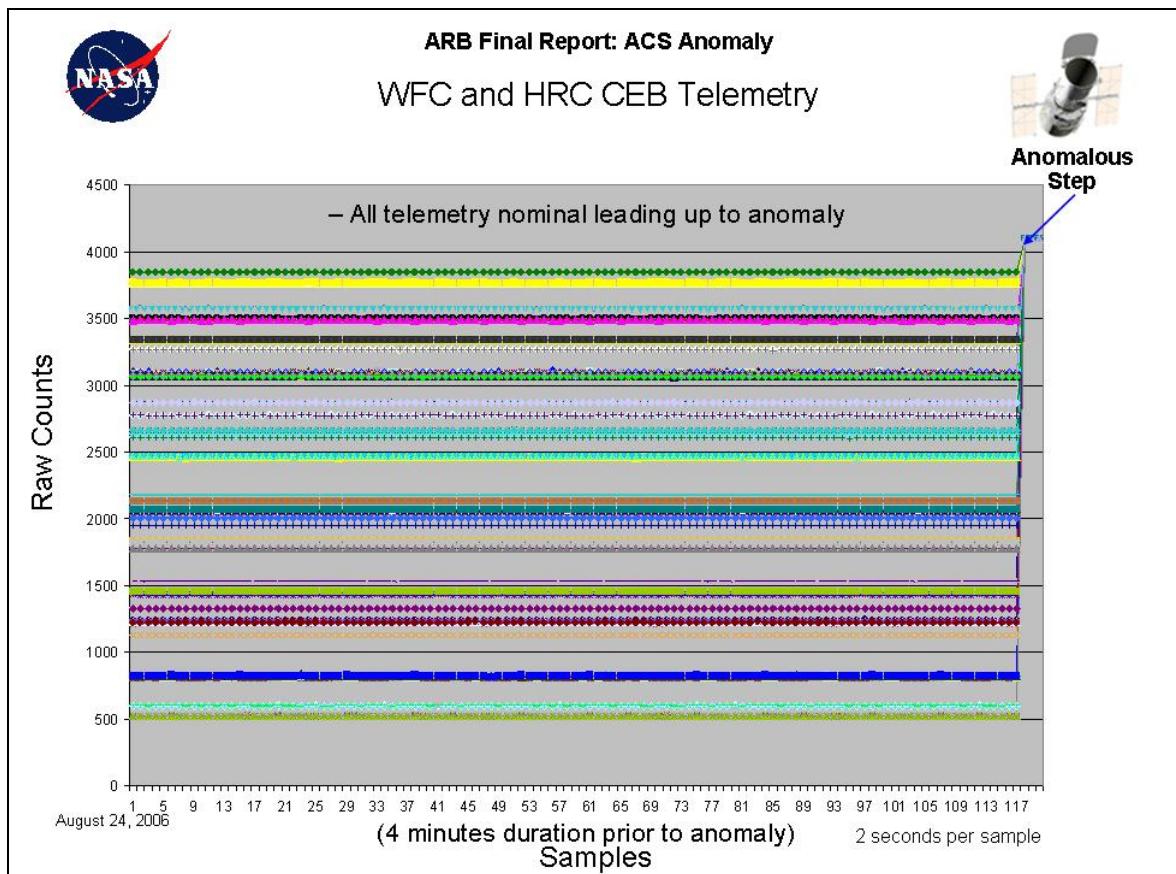
All other mnemonics are collected from the CEB via the Normal Engineering Data (NED) task.

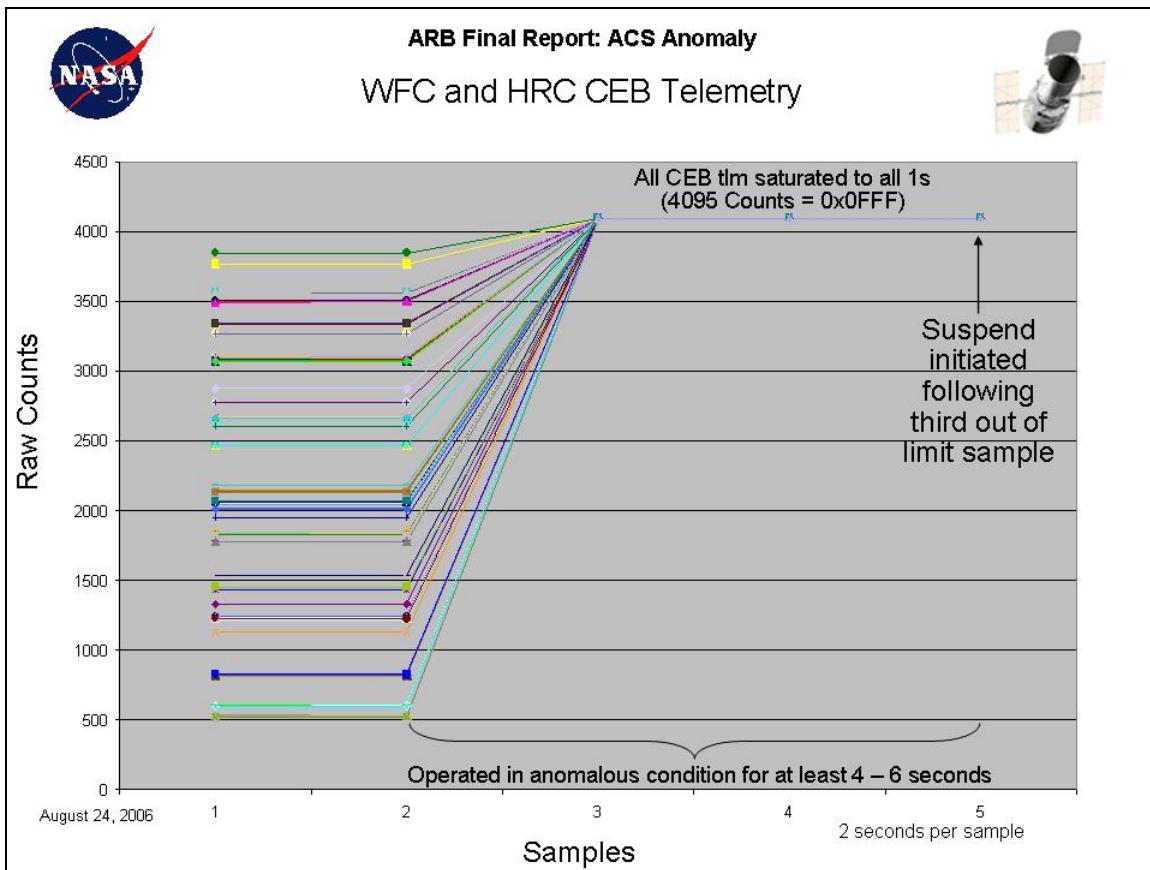
NED sampled data saturated to all ones prior to the Suspend. Once Suspended, all NED sampled data read zeros since it is not collected by Boot flight software. The Suspend sequence removes all power from the CEB. RIU-direct telemetry is valid throughout. Downlink time are staggered on the graph.



The analysis of the memory dump showed that, when the Suspend occurred, all telemetry items being limit checked from the WFC and HRC CEBs had been out-of-limits for 3 consecutive runs of the limit check task. The limit check task runs every 2 seconds.

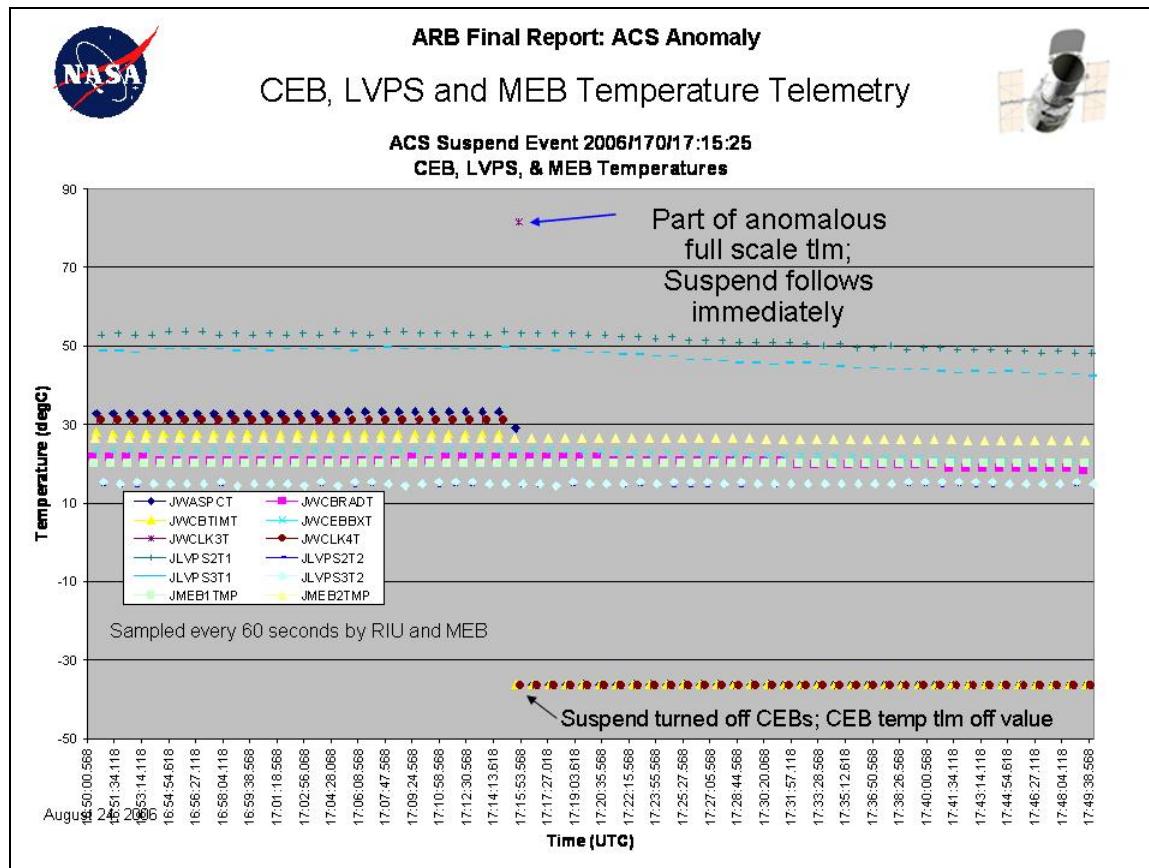
The memory dump also contains the Normal Engineering Data (NED) history buffer. NED is a task that runs every 2 seconds to collect engineering data from the WFC CEB, HRC CEB, and the support electronics system (SES). The NED history buffer contains the last 120 sample sets of data (last 4 minutes of data). The NED history buffer showed all data was nominal and steady up to the last 3 samples prior to the Suspend. The last 3 samples showed all WFC CEB and HRC CEB data were reading all ones (0FFF hex). The SES data remained nominal during the last 3 samples.



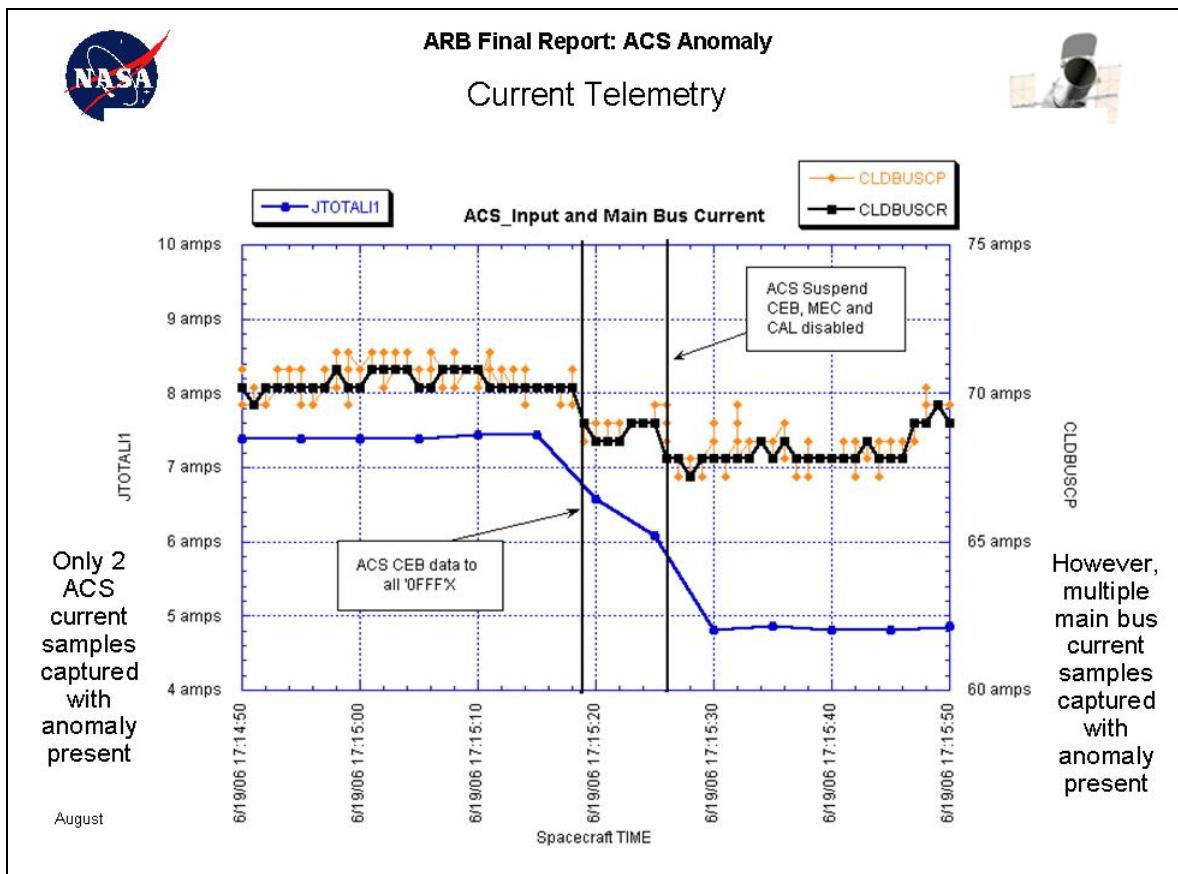


Thus, the all-ones telemetry data was sampled from both the WFC and HRC CEBs. This data failed limit checking three consecutive times, which caused the Suspend. Depending on when the limit checking was done, ACS remained in the anomalous state for about 4 to 6 seconds prior to initiating the Suspend. Up to another 2 seconds could have passed prior to CEB power being removed as a result of the Suspend sequence.

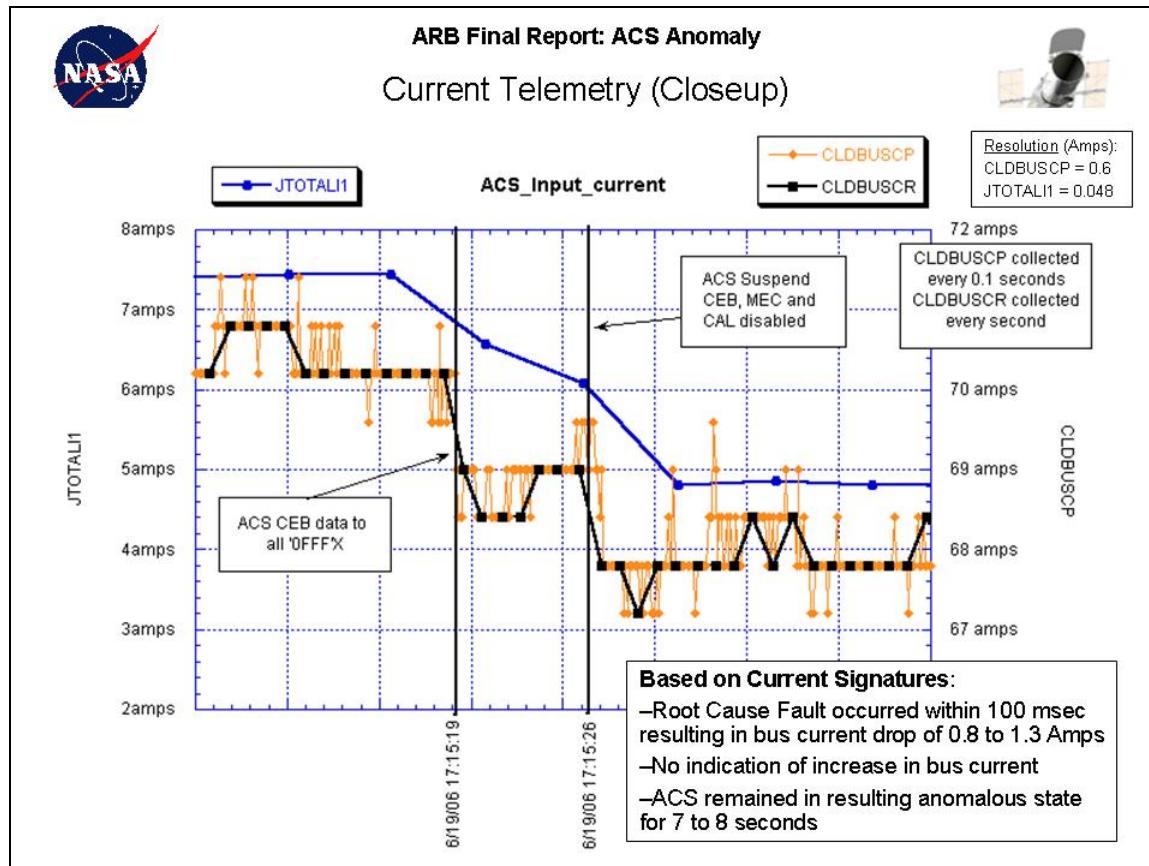
An analysis of temperature data showed that the MEB, LVPS, and CEB temperatures were all nominal up to the point of the Suspend.



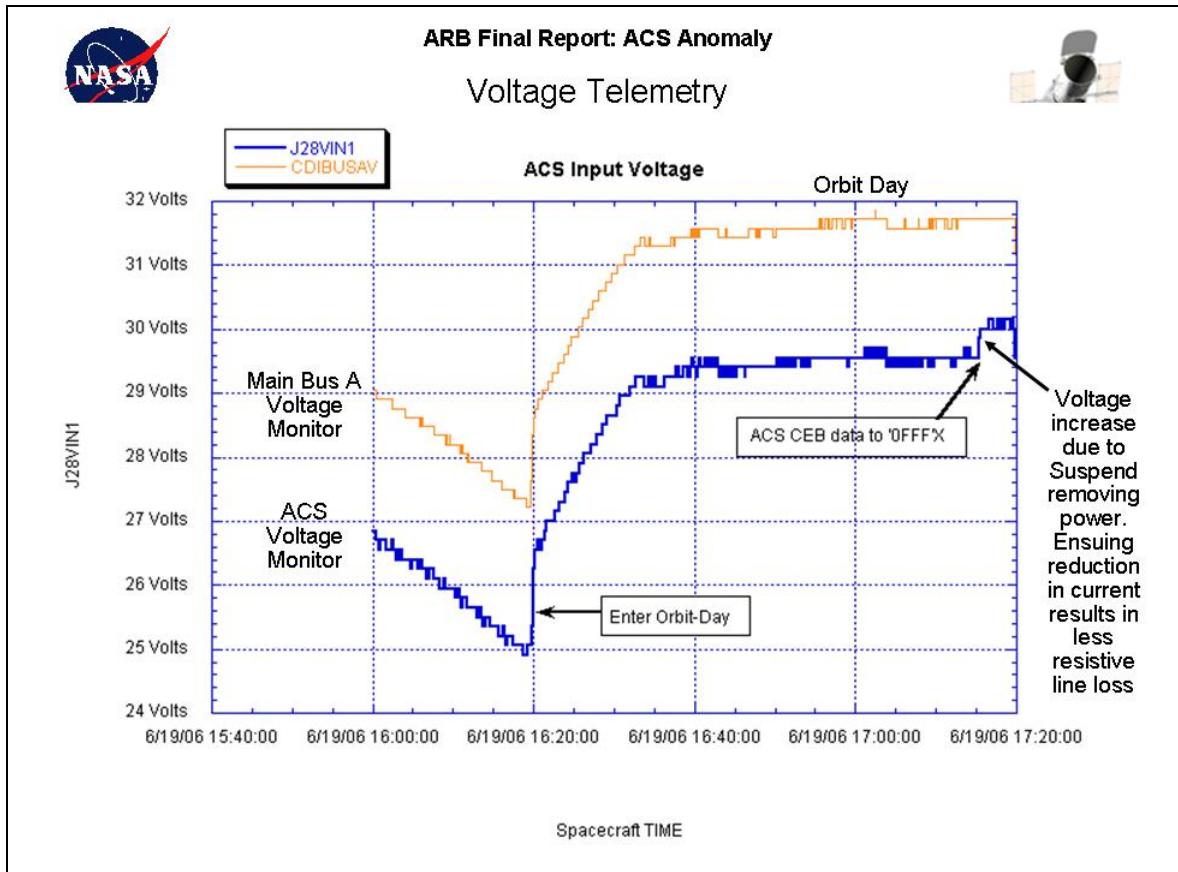
An analysis of the ACS input current and HST main bus current telemetry showed a decrease in current prior to the Suspend. The ACS input current is sampled and downlinked every 5 seconds. HST main bus current is sampled and downlinked every 0.1 seconds.

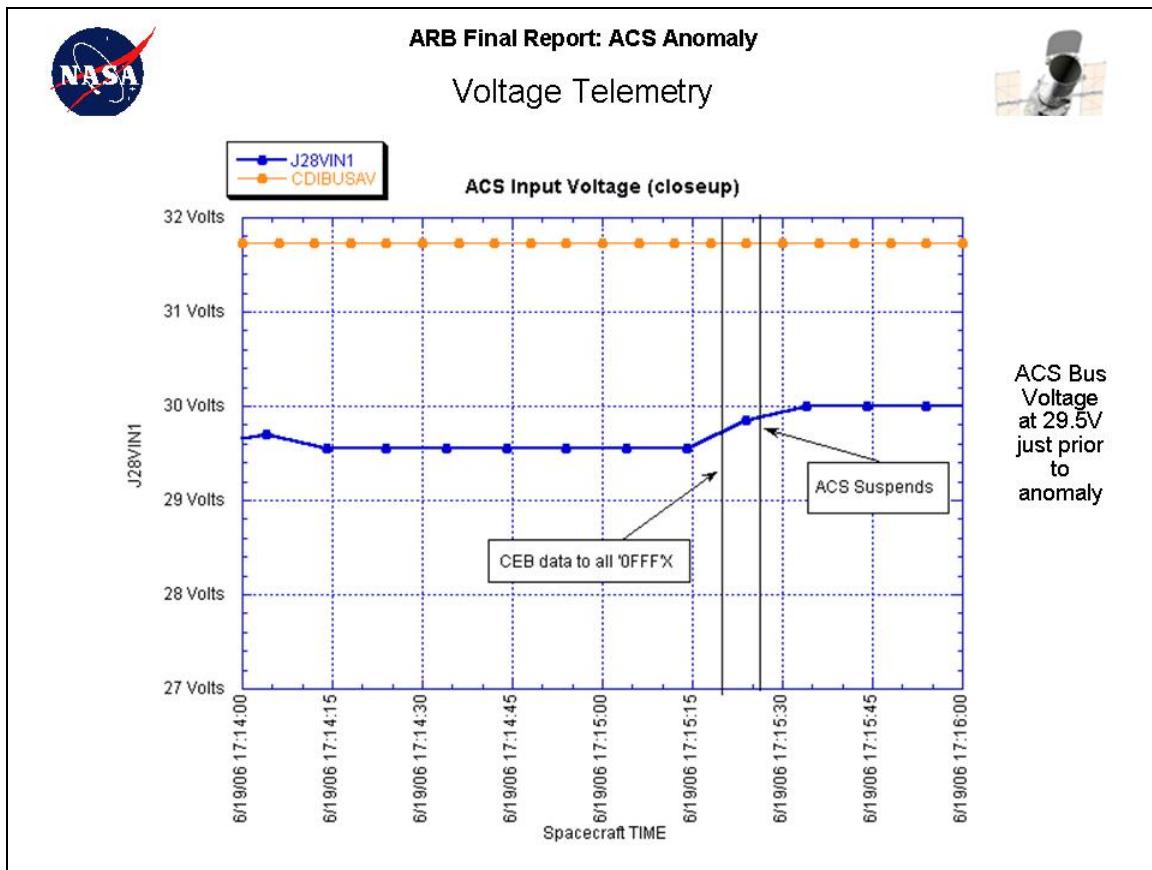


A more detailed analysis of the ACS input current and HST main bus current telemetry indicated that the root cause fault must have occurred within one HST main bus current sample time, or 100 msec. The total current decrease due to the anomaly was measured to be somewhere between 0.8 Amps and 1.3 Amps, based on the resolution of the available current monitors. In addition, the HST main bus current telemetry provided a more accurate evaluation of how long the circuitry had remained powered in the anomalous state. Approximately 7 to 8 seconds had elapsed prior to Suspend turning off the CEB power supplies.

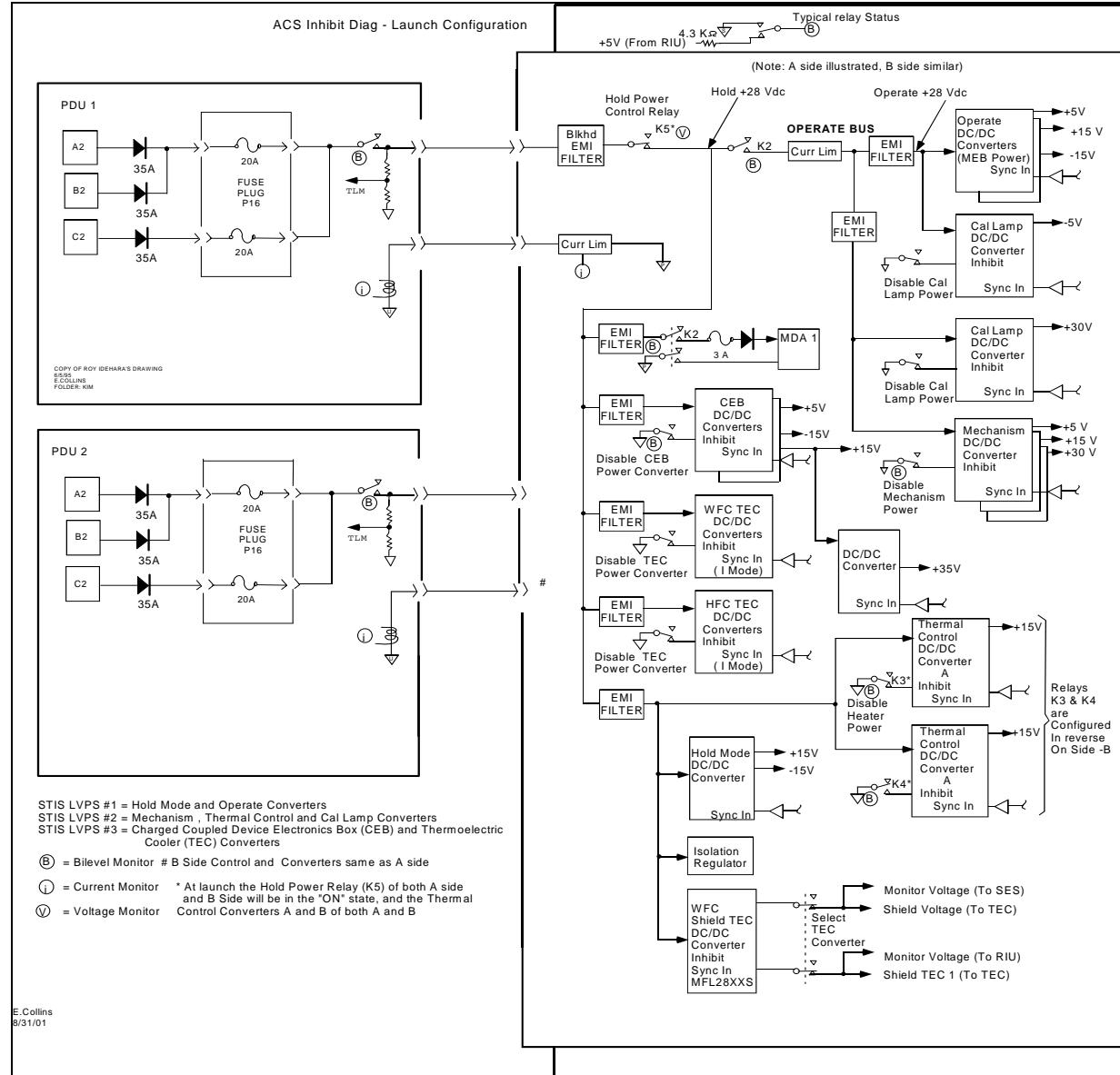


The ARB was interested to determine where the anomaly had occurred in the orbital day/night cycle. A previous ARB (STIS Side 2 ARB) determined that their failure with an Interpoint MFL2805S device responded to input bus voltage changes as a function of day/night cycles. In their failure, they determined that they had lost their +5V power supply output when the bus was below approximately +28V. However, as the bus approached and exceeded +28V after entering the orbit day transition, the Interpoint device responded by drawing current exponentially, which led to the internal destruction of the device. For ACS, the on-orbit telemetry indicates that the anomaly occurred when the ACS bus voltage was at approximately 29.5V, and thus higher than the voltage of concern in the STIS Side 2 ARB. In addition, the ARB later determined that one of the potential suspect Interpoint MFL2815D converters must have been functioning in some manner in order to produce the on-orbit signature of all 1s in CEB telemetry. Therefore, the previous anomaly mechanism on STIS Side 2 could not be related to the ACS anomaly.

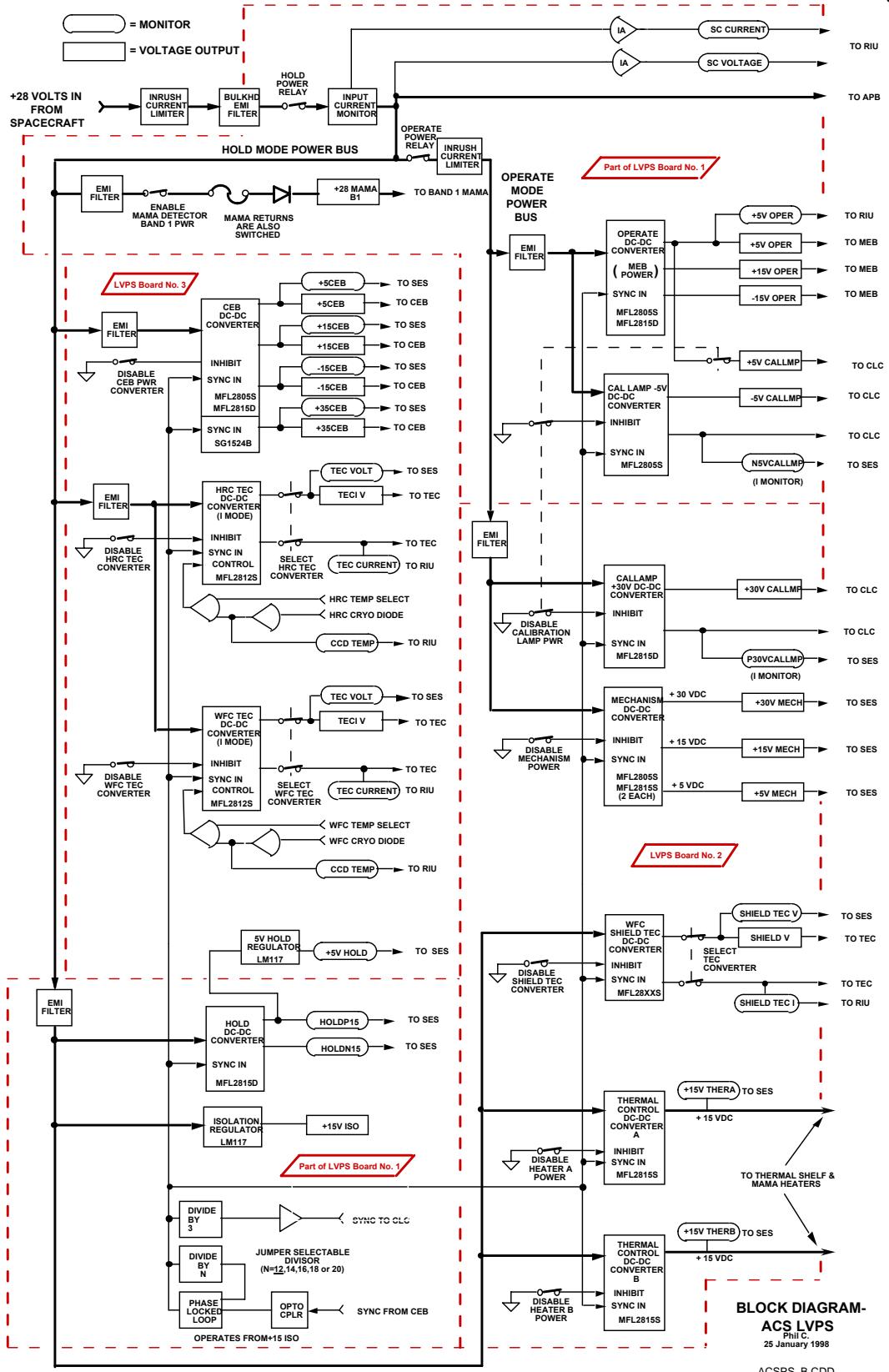




## Block Diagrams



The drawing applies to ACS, although notes on the drawing incorrectly indicate STIS.



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Note: Drawing incorrectly references an SG1524 as the CEB +35V PWM. The part is actually an SG1525A.

## Software Evaluation

NED (Normal Engineering Data) is an MEB software task that collects analog engineering data for the SES, HRC CEB, and WFC CEB from A/D electronics. The NED, running every 2 seconds for 4 minutes of total data collection, maintains a circular history buffer that holds 120 sample sets of Current Value Table (CVT) data. Upon detailed evaluation of the NED history buffer data, it was determined that all of the last 3 sample sets of HRC CEB and WFC CEB data (158 data values) showed all 0FFF (hex). The SES data was found to be nominal.

Preliminary Testing on ACS test bench (ESTIF) could not re-produce all “ones” condition with the CEB(s) off, as expected; 0000 (hex) is expected when the CEB(s) are powered off.

The NED data collection process was evaluated in detail and is presented below:

- Normal Engineering Data Collection
  - Enabled during CS operate transition
  - Collects Current Value table A/D telemetry items ( 80 for WFC, 78 HRC, 79 SES)
  - Collects 120 sample sets every 2 seconds for 4 minutes of history
  - History Buffer Data examined:
    - SES data appeared nominal
    - WFC & HRC: 5 most recent samples before buffer wrap showed 2 good samples and 3 maximum value (4095 counts) 0FFF hex values
    - A/D collection process
  - A/D collection process
    - Data sampled directly from A/D electronics for HRC CEB, WFC CEB, and SES
      - › Write to A/D Address FIFO (in WFC, HRC, SES order)
      - › Read from A/D Data FIFO (in SES, WFC, HRC order)
    - Collected data stored in NED history buffer and Current Value Table used by Limit task
    - Address FIFO (4K X 9):
      - › Check Address FIFO empty, if not empty suspend
      - › Check Data FIFO empty, if not empty suspend
      - › Reset Data FIFO (regardless of status register)
      - › Load Address FIFO with MUX addresses
      - › Enable A/D complete interrupt
    - Data FIFO 2(4K X 9):
      - › Wait for interrupt
      - › Read based on Address FIFO empty
      - › Converted data is 12 bits; unused bits 12-15 are pulled LO in h/w; upper 4 bits masked off in FSW regardless.
      - › Mask interrupt
      - › Loop while Data FIFO not empty, if empty suspend

- FIFO Status register (low 4 bits of 16-bit register used by h/w)
  - > Only reflects state of low order FIFO; FSW has no insight to status of high order FIFO (empty, not empty)
  - > The Data FIFO is reset prior to data collection for a known state
  - > No ability to reset the Address FIFO except by system reset

Evaluation of the NED software process determined it to be very robust, with numerous FIFO checks being conducted as part of the process. As can be seen in the above flow in the A/D collection process, the ADDR FIFO and DATA FIFO are checked to make sure they are empty. If not empty, a Suspend is executed. Since this was not the source of the Suspend, these two FIFOs must have been emptied or empty at this point of execution. The DATA FIFO data is collected as long as data is present. If data is not placed into the DATA FIFO, a Suspend is executed. Again, since this was not the source of the Suspend, the DATA FIFO must have been filled with data that was ultimately read by the processor.

Upon reading the 16 bit data FIFO, the software disregards the four most significant unused bits and masks them to an all 0 value. The ARB noted that the CEBs actually assign 0 values to these four most significant bits in hardware prior to transferring the data serially. However, the ARB, in attempting to narrow down the location of the root cause of the anomaly, would have preferred that the MSB values were not masked to 0 by the software. This would have aided the ARB in quickly evaluating and verifying that the MEB serial interfaces to the CEBs were functioning correctly. If the data in the MEB were all 0x0FFF, it would exonerate the circuitry downstream of the CEB's parallel-to-serial shift register. The 0x0FFF data pattern would not be possible if this circuitry failed to a logic '1', '0', or was intermittent or erratic.

**ARB Recommendation:** Store Normal Engineering Data in history buffer in raw form; do not software mask four most significant unused bits.

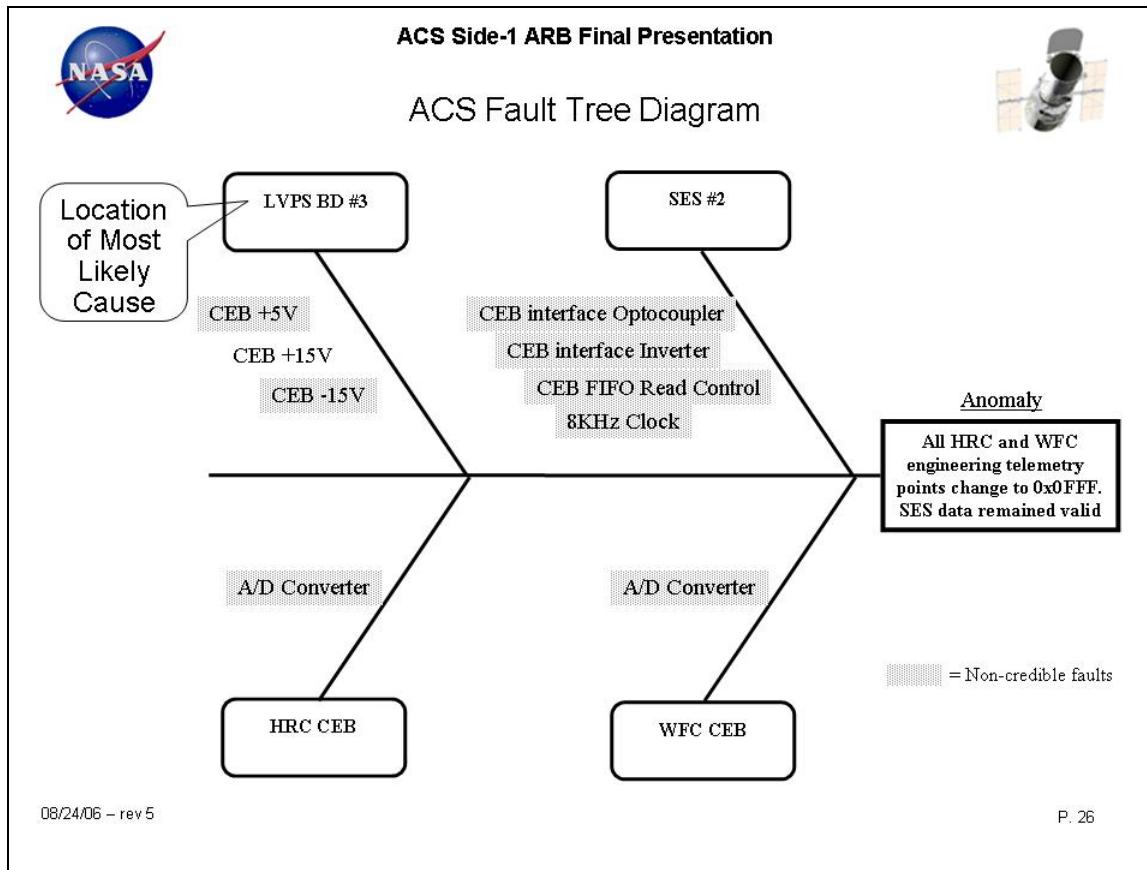
FSW change requests were submitted for ACS (J338), COS (C306), and WFC3 (W292) for the change to the instrument FSW to not mask the upper 4 bits of the NED History Buffer entries.

The description for each of the software change requests reads as follows: “Modify SI flight software so the NED history buffer contains 16-bit values exactly as read from the A/D FIFOs. Specifically, do not apply a bit-mask to the data prior to storage in the buffer. Storing the data in an unmodified form would allow insight to a possible failure in the opto-isolators.”

This change was approved for inclusion in the WFC3 flight software release version CS3.0C, scheduled for Nov 2006 delivery. The change for ACS and COS will be incorporated in future releases, tentatively later this year.

## Fault Tree Analysis

An ACS Fault Tree Diagram was developed in order to structure the ARB investigation. Potential causes of the ACS anomaly were evaluated, with non-credible failure modes ruled out via evaluation, analysis and testing.



A review of SES #2 indicated that it could not contain the cause of the ACS on-orbit anomaly for the following reasons:

- CEB Interface Optocoupler:
  - Theory: CEB to SES interface uses common 6N140A Optocoupler package (Schematic SC538458 sheets 10 and 11)
    - 16 Bit serial data interface
    - Valid data transfer window signal interface
  - Same Optocoupler package (U117) shared by both WFC and HRC CEB interfaces
  - RULED OUT:
    - On orbit transition to Operate1 resulted in all 0s data, consistent with CEBs in powered off state
    - Failure of U117 outputs all Low would have resulted in Software FIFO Management algorithm Suspend; no Valid Data Transfer signal thus no data in Data FIFO to collect

- Failure of U117 outputs all High would have resulted in all 0s data being read (similar to CEB powered off condition)
- CEB Interface Inverter:
  - Theory: CEB to SES Interface uses common AC14 Inverter package (SC538458 sheets 10 and 11)
    - 16 Bit serial data interface
    - Valid data transfer window signal interface
  - 3 of 6 AC14 Inverters in a package (U39) shared by both WFC and HRC CEB interfaces
    - 2 for WFC serial data and transfer signals, 1 for HRC transfer signal
    - Different AC14 (U118) used for HRC serial data path
  - RULED OUT:
    - On orbit transition to Operate1 resulted in all 0s data, consistent with CEBs in powered off state
    - Although AC14 package U39 common in both WFC and HRC interfaces, not common in Serial Data Path
      - Failure of U39 outputs all High would have resulted in Software FIFO Management algorithm Suspend; no Valid Data Transfer signal thus no data in either WFC or HRC Data FIFO to collect
      - Failure of U39 outputs all Low would have resulted in all 0s data being read from WFC Data FIFO and random, unsynchronized data read from HRC Data FIFO
- CEB FIFO Read Control:
  - Theory: Loss of FIFO data read control (SC538458 sheet 2)
  - would result in MEB reading undriven SES data bus that is pulled up by default, leading to all 1s data
- RULED OUT:
  - On orbit transition to Operate1 resulted in all 0s data, consistent with CEBs in powered off state, as opposed to the all 1s failure condition
  - Failure to read Data FIFO would have resulted in Software FIFO Management algorithm Suspend
    - Without a Data FIFO read, Data FIFO contents would not have indicated an Empty condition prior to next FIFO Address update and resulted in a Suspend

- CEB Interface 8KHz Clock:
  - Theory: CEB to SES interface uses common 8KHz Clock which is not used by SES data collection circuitry (Schematic SC538458 sheets 9, 10 and 11)
    - 8KHz used as primary CEB to SES interface state machine clock
    - Differs from SES data collection clock; SES data collection uses 4MHz as state machine clock
  - RULED OUT:
    - On orbit transition to Operate1 resulted in all 0s data, consistent with CEBs in powered off state and FIFO state machine functioning
    - Failure of 8KHz would have resulted in Software FIFO Management algorithm Suspend; no data in Data FIFO to collect

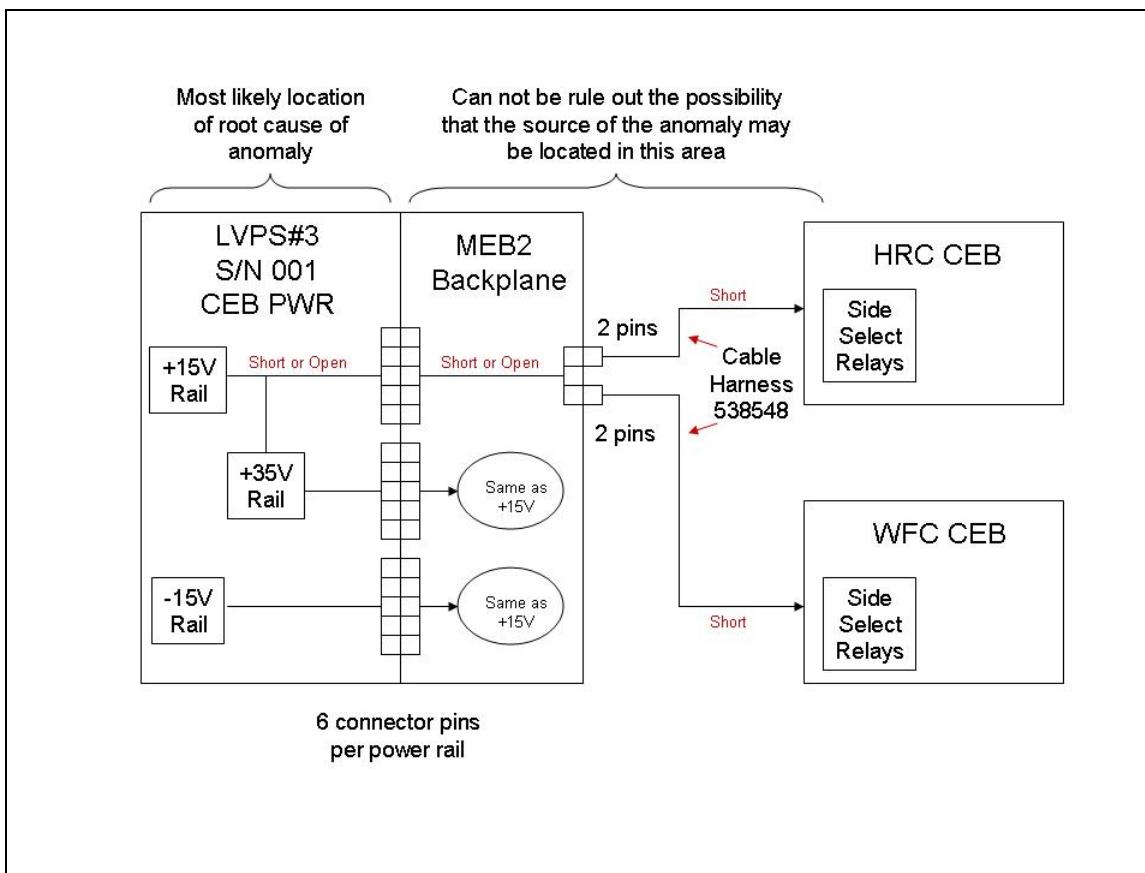
A review of the WFC and HRC CEBs indicated that it could not contain the cause of the ACS on-orbit anomaly for the following reasons:

- CEB A/D Converter and associated serial interface:
  - Theory: Anomaly with CEB to SES A/D Converter AD674B and/or associated Serial Shift register (HCS165) (Schematic SC538603 sheet 12) resulted in all 1s CEB data transmitted to SES
  - RULED OUT:
    - WFC and HRC CEBs are two identical, yet independent units in ACS. Anomaly of this type would require two independent failures in both of the CEBs simultaneously
    - Both CEBs fully functional on ACS Side 2

Finally, a review of the LVPS Board #3 indicated that it **most likely contains** the cause of the ACS on-orbit anomaly for the following reasons:

- Loss of CEB Power Rail:
  - Theory: Both WFC and HRC CEBs supplied with power from common LVPS +5V, +15V and -15V source (Schematic SC538463 Sheet 3). Loss of the +15V power rail, with or without degradation of the -15V power rail, results in uncharacteristic performance of CEB A/D conversion and associated serial data stream.
  - **Most Likely Cause:**
    - Ground testing of Engineering CEB unit resulted in reproduction of on orbit anomaly (refer to Engineering CEB Testing section of this report for details)

The LVPS Board #3 has been identified as most likely containing the cause of the ACS on-orbit anomaly since it contains all of the active components that produce and/or interface with the suspected +15V CEB power rail. However, it is also possible that a +15V trace to ground or +15V wire short to ground fault may have occurred on the MEB Backplane or in the MEB to CEB harnessing respectively.



## Engineering CEB Testing

The ARB's leading theory as to the reason for the ACS on orbit anomaly focused on the loss of a +15V or -15V CEB power rail. This theory was based on the knowledge that 1) the power rail was common to both WFC and HRC CEBs, 2) CEB A/D converters required +/-15V rails to operate, and 3) NED software operating in the SES section of MEB was evaluated and found to be very robust, with numerous FIFO checks being conducted as part of the process, substantiating that the root cause of the anomaly was not located in the SES.

Initial engineering evaluation of the CEB schematics supported the claim that loss of some combination of the +/-15V rail could possibly produce the anomalous all 1s signature detected at the time of the ACS anomaly. Engineering evaluation further

indicated that the +5V CEB power must have been present in order to transfer the all 1s data from the CEBs to the MEB.

Initially, a breadboard test with an A/D converter was set up and run to determine its response to various power rail combinations. The results indicated that the interaction of power loss on the hardware was more complicated and need to be evaluated at a higher level. The CEB contains analog muxes, operational amplifiers, sample and hold circuits, as well as the A/D converter, all of which are powered by the +/-15V CEB rails. Therefore, a loss or disruption of these rails will have a different response at the CEB assembly level as compared to the lower level piece part level.

The ARB therefore reviewed what ground assets were available to aid in the anomaly investigation. Ball Aerospace determined that they still had a CEB Test Set that contained a CEB Engineering Unit. Following discussions with HST Code 442 Management concerning the possible risk of hardware damage from subjecting the CEB Engineering Unit to off nominal power combinations, the decision was made to proceed with Engineering Unit evaluation. HST Code 442 Management accepted the risk, acknowledging that if the CEB Engineering Unit was damaged, it could be debugged, fixed, and returned to service if and when needed in the future.

CEB Engineering Unit testing commenced at Ball Aerospace. A number of test combinations were requested and executed over the course of the ARB. Essentially, each test required the operator start and verify a test with nominal power conditions, and then continue on with requested manipulations of the various power rail inputs using lab power supplies. Following each off nominal power combination test, a normal power combination test was re-executed to determine if the testing had inflicted signs of damage on the Engineering CEB. Ultimately, no signs of damage were ever detected in the nominal Engineering CEB telemetry response.

The CEB Engineering Unit test used the telemetry response read-out screen on the CEB Test Set to determine the CEB response to various power rail combinations. For nominal operation, it was expected that the ‘Actual’ LOW and HIGH RAIL CLOCK values would be in a repeatable mid range position. Refer to Attachment #4. An all 1s telemetry response, similar to that experienced during the on-orbit ACS anomaly, would produce an ‘Actual’ value of 10.00 or 19.99, depending on the telemetry point. Likewise, an all 0s telemetry response would produce an ‘Actual’ value of -10.00 or -20.00.

The ARB realized that a number of combinations of power rail tests would be required. Both shorts and opens were required to be executed, as well as intermediate voltage rails. A summary of the findings is shown in the following table:

<b>+15V Power</b>	<b>-15V Power</b>	<b>Results</b>	<b>Anomaly Match</b>	<b>Notes</b>
+15V	-15V	Nominal	-	
Open	-15V	All 1s	YES	
+15V to +2.5V	-15V	Various	-	
+2.5V to 0V	-15V	All 1s	YES	
Short	-15V to -5.9V	All 0s	-	
Short	-5.9V to -0.4V	All 1s	YES	
Short	-0.4V to 0V	All 0s	-	
+15V	Open	All 0s	-	COS TVac lid deflection anomaly (L5 open)
+15V	-15V to -5.5V	Various	-	
+15V	-5.5V to 0V	All 1s	YES	A short on the -15V rail will drag down the +15V rail
+15V to 0V	Short	All 0s	-	

The above table summarizes the ARB's attempt to fully characterize the CEB engineering unit's response to as many +/- 15V combinations as possible in the lab. Not all of these combinations are realistic when powering the CEB with an MFL-2815D converter. Refer to the MFL2815D Analysis and GIDEP Search Results section on page 31 for expected voltage combinations when using the converter.

In addition to the above test results, an additional test was configured in which an MFL-2815D Interpoint power converter was used to power the Engineering Unit CEB +/-15V rails. Once powered on and the Engineering CEB telemetry results were verified to be responding nominally, the MFL-2815D converter was inhibited while the CEB remained powered by the +5V Test Set power supply. The goal of this test was to determine if an anomaly related to the MFL-2815D inhibit, resulting in the loss of both the +15V and -15V rails with the unpowered output loads still connected, would reproduce the on orbit anomaly. The results of this test produced an All 0s telemetry response, thus ruling out an MFL-2815D inhibit related failure.

Ultimately, the Engineering CEB data was evaluated as a whole and the following two conclusions were drawn:

- 1) The CEB MFL2815D was not inhibited on orbit
- 2) The CEB MFL2815D did not fail in such a way that caused the primary input side to fuse open at the internal bond wires. In other words, the MFL2815D had to still be functioning in some capacity with respect to the -15V rail in order for the Engineering CEB to replicate the on orbit scenario.

The Ball Aerospace Engineering test details are included as Attachment #4.

## GSFC MFL2815D Lab Tests

The ACS +/- 15V CEB power supply design located on the LVPS#3 board utilizes an Interpoint MFL2815D DC/DC Converter. The MFL2815D input is connected to the ACS +28V Hold bus through an FME28 line filter. The ACS LVSP#3 board S/N 001 on LVPS Side 1 (physically located in ACS MEB 2) contains an MFL2815D converter with Interpoint part number of 5962-9319301HXC from lot date code 9443. A review of ACS Certification Logs revealed that the Interpoint Converter Serial Numbers were not recorded.

The ARB acquired an MFL2815D Interpoint converter (Serial Number 0643, Lot Date Code 9815) and performed bench testing to better understand the device's operation and dynamic response characteristics in the presence of an external anomaly.

A review of the Interpoint MFL series converter data sheets was conducted by the ARB. The MFL single output models (MFL2805S) clearly indicated that a no load condition is acceptable and that they are power limited for continuous short circuit operation on the output for case temperature <125C.

However, further review of the Interpoint MFL dual series converter data sheets (MFL2815D) indicated that the same conditions found in the single output converters were not so clear for the dual output models. The data sheets do indicate that no load is ok and a shorted output is also power limited for continuous short circuit operation. However, another statement requires that output loading between the two rails be balanced to within a 70%/30% range. This implies that the load of both outputs must be somewhere between 50/50 and 30/70 to provide the specified regulation output voltages. In other words, an MFL2815D must not be operated as a single output device leaving the other output open. Bench testing verified this finding.

Bench tests were executed that measured the response of the MFL2815D +15V and -15V rails in open and shorted conditions, with representative loads connected to the power rails. The load set utilized initially was 25 ohms, 15 ohms, and 6 ohms. Subsequent ARB evaluation of actual CEB ground test data (obtained from the Flight WFC3 CEB) provided characteristic current drawn information for a single representative CEB. Since the ACS LVPS CEB power supply supplies two CEBs with current nominally and (except when performing Solar Blind activities where the HRC CEB is turned off) as was the case at the time of the on-orbit anomaly, these current values need to be doubled. Thus, the characteristic loads on the CEB LVPS power supplies were determined to be as follows:

Voltage Rail (V)	CEB Current (A)	Total Current (2 CEBs) (A)	Load (Ohms)
+5	0.2	0.4	12.5
+15	0.575	1.15	13
-15	0.575	1.15	13

For the +15V and -15V voltage rails, the calculated 13 ohm load was determined to be extremely close in value to the previously used 15 ohm load. Therefore, the 15 ohm load condition was determined to provide the closest representation of the on-orbit system.

<b>+15V</b>				<b>-15V</b>			
<b>Simulated Fault</b>	<b>Load based Response (V)</b>			<b>Simulated Fault</b>	<b>Load based Response (V)</b>		
	<b>25 Ω</b>	<b>15 Ω</b>	<b>6 Ω</b>		<b>25 Ω</b>	<b>15 Ω</b>	<b>6 Ω</b>
None	n/a	15.08	n/a	None	n/a	-15.08	n/a
Short	0	0	0	None	-0.91	-0.91	-0.91
Open	15.08	15.08	15.08	None	-3.19	-11.29	-8.60
None	0.95	0.95	0.95	Short	0	0	0
None	15.08	15.08	15.08	Open	-16.25	-16.30	-16.36

The MFL2815D bench test data clearly indicated that the +15V output provided by the MFL2815D could only be forced out of regulation by either an external +15V power rail shorting event or an internal (within the MFL 2815D module itself) +15V power converter failure. The -15V output regulation was shown to vary as a function of either an external shorting event or changes to the +15V rail. Thus, it was determined that the +15V output of the MFL2815D is the Master closed loop regulator, with the -15V rail operating in a Slave mode. This Master/Slave regulation configuration within the MFL2815D was corroborated by follow up discussions with Interpoint technical representatives. It was also noted that the -15V output appeared to be limited to approximately 110% of its nominal output voltage, as seen in the -15V simulated open output condition.

In addition to the output voltage response of the MFL2815D, the ARB needed to better understand the input current characteristics of the device as a function of various output fault modes. This data can be compared to the on-orbit current signature to see if it matches the on-orbit anomaly. Input current measurements were thus conducted and are summarized as follows:

<b>MFL2815D Test Condition</b>				<b>30.0V In</b>	
				<b>Iin (A)</b>	<b>Pin (W)</b>
Nominal (32 W out)				1.27	38.1
Short +15V Rail				0.197	5.91
-15V Rail (Load -15V with +15V open)					
<b>R</b>	<b>Vo</b>	<b>Io (A)</b>	<b>Po (W)</b>		
10	9.35	0.94	8.74	0.39	11.7
12	9.62	0.80	7.71	0.36	10.8
13	10.11	0.78	7.86	0.37	11.1
15	11.28	0.75	8.48	0.39	11.7
16	11.99	0.75	8.99	0.41	12.3
17	12.54	0.74	9.25	0.42	12.6
18	12.39	0.69	8.53	0.3	9
19	9.35	0.49	4.60	0.27	8.1

This data indicated that the nominal current draw by the test MFL2815D was 1.27 Amps. When the +15V output was shorted to ground, the input current draw decreased to 0.197 Amps. For a +15V open condition with the -15V rail loaded with 13 ohms, the current draw decreased to 0.37 Amps. Thus, in both the +15V shorted and opened cases, the MFL2815D input current decreased. The current deltas expected at the input to the MFL2815D were calculated to be:

$$+15V \text{ Short: } 1.27 \text{ Amps} - 0.197 \text{ Amps} = 1.073 \text{ Amps} \text{ DELTA drop in current}$$

$$+15V \text{ Open: } 1.27 \text{ Amps} - 0.38 \text{ Amps} = 0.89 \text{ Amps} \text{ DELTA drop in current}$$

Therefore, the difference in current drop between a +15V shorted output and a +15V opened output is merely 0.137 Amps. A review of the orbital telemetry data at the time of the anomaly indicates that the +28V bus current dropped somewhere in the range of 0.8 Amp to 1.3 Amps. Thus, the on orbit data does correlate well with the assertion that the +15V output failed in either a shorted or opened fashion. However, the relatively small difference in current drop between the +15V shorted and opened cases make it impossible to reliably predict which of the two possible failure modes may be present on orbit.

Additional MFL2815D bench testing was conducted in order to further characterize the MFL2815D converter response, yet this set of testing was focused on the responses that would be obtained during a proposed ACS Side 1 on-orbit investigation test. Since the proposed test required the CEBs be off, the MFL2815D was characterized assuming no load on the +15V and -15V outputs. The results are summarized below:

The MFL2815D was tested with no load on either output and then a light load on the +15V to simulate the +35V circuitry. That light load on the +15V with no load on the -15V caused the -15V to increase in voltage slightly, but hardly more than 1V (-16.2V max).

Previous shorting data had been obtained with loads connected to the converter. For this test, the loads were removed. Surprisingly and in contrast with the loaded data set previously taken, there was a significant voltage present on the non-shorted output.

Outputs Unloaded (Open Circuit)		Outputs Loaded (previous data for comparison)	
+15V Rail	-15V Rail	+15V Rail	-15V Rail
Short	-6.8V	Short	-0.91
9.8V	Short	0.95	Short

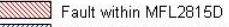
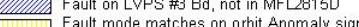
This data therefore indicated to the ARB that execution of an on-orbit test in the proposed no CEB load scenario would, in the event that a short was present, be able to discern which voltage rail contained the actual short. A Fault Response Summary Table was generated based on these results and presented as part of the ACS Side-1 Test Proposal Meeting (refer to Attachment #2)

**ACS Side-1 Test Proposal Meeting**

Benefits of Testing: Fault Response Summary Table




Case #	Failure Mode	Anomaly match based on ETU testing	Implicates	Expected Telemetry			
				+5V	+15V	-15V	+35V
1	All Nominal	no	Problem intermittent or +15V open beyond TLM sample point	+5V	+15V	-15V	+35V
2	+15V open (external)	YES	LVPS #3 Board	+5V	0V	-15V	0V
3	+15V open (internal)	YES	MFL2815D	+5V	0V	-18V to -20V	0V
4 or 5	-15V open (external or internal)	no	MFL2815D or LVPS #3	+5V	+15V	0V	+35V
6	+15V shorted (internal or external)	YES	MFL2815D or LVPS #3 or MEB Backplane or Harness to CEBs	+5V	0V	-6V to -8V	0V
7	-15V shorted (internal or external)	no	MFL2815D or LVPS #3 or MEB Backplane or Harness to CEBs	+5V	+8V to +11V	0V	+30V to +35V
8 or 9	MFL2815D inhibited or internally destroyed	no (additional testing in progress)	MFL2815D	+5V	0V	0V	0V



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## MFL2815D Analysis and GIDEP Search Results

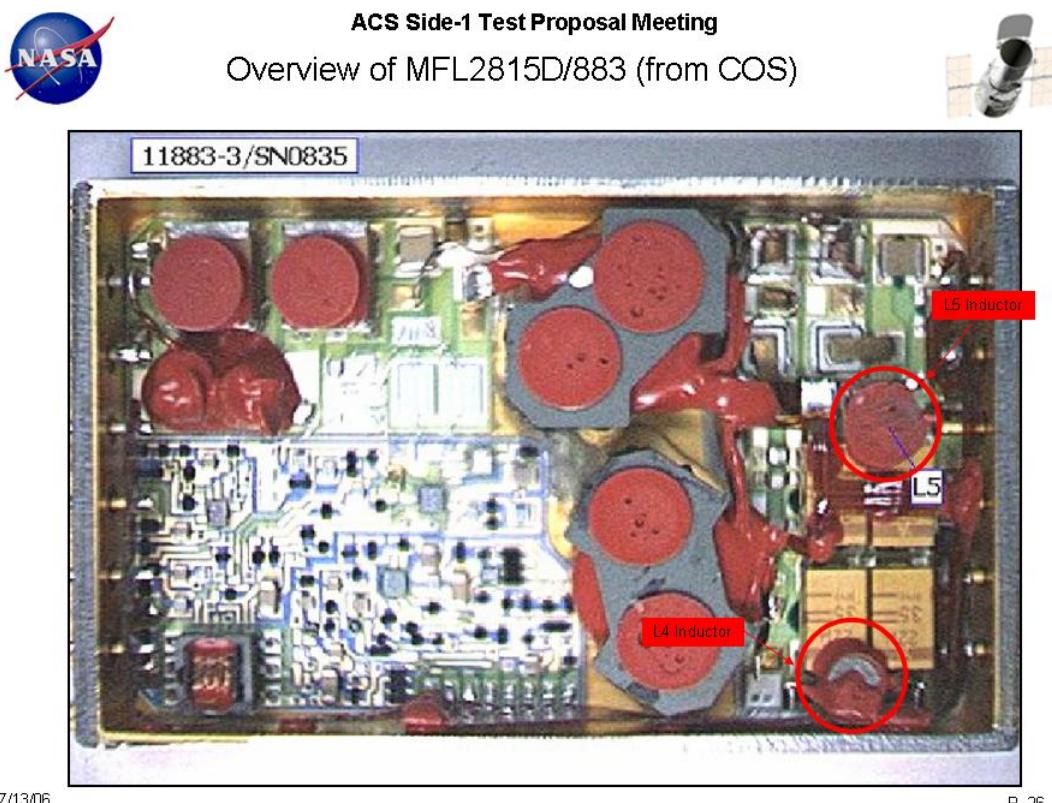
To identify all potential failure modes and weaknesses of the MFL2815D, several investigative paths were followed:

- Perform Government-Industry Data Exchange Program (GIDEP) search on Interpoint converters
- Establish sensitivity of the converter to radiation

- Review Mission Success bulletins related to Interpoint converters
- Perform internal MFL2815D fault testing as directed

A GIDEP search on Interpoint converters was conducted. GIDEPs MT2-P-00-01, MT2-P-01-01, MT2-P-01-01A, MT2-P-04-01, MT2-P-04-02, and MT2-P-04-03 were reviewed.

The only GIDEP alert that was found to affect the MFL2815D/883 converter was MT2-P-04-01, which related to a vacuum environment related mechanical stress issue that is transferred from the device lid through silicone adhesive to an output inductor (L5) on the -15V rail. A follow up conversation with Interpoint on this subject confirmed that the L5 output inductor was only related to the -15V rail. Loss of the -15V rail would not affect operation of the +15V output. This information agreed with previous GSFC anomaly data related to this concern. Interpoint pointed out that in order to fail the +15V rail in a similar manner, an L4 inductor would have to be displaced by lid deflection. However, it was noted that the L4 inductor is located next to a side wall in the cavity of the MFL2815D and therefore is exposed to very little lid deflection in comparison to the L5 inductor which is near the center line of the package. The GSFC Parts Engineering Branch further noted that the L4 inductor appears to be staked not only to the lid of the device, but also to the C80A and C80B +15V output tantalum capacitors (refer to photo below).



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GIDEP alert MT2-P-01-01A was not related to the MFL series of devices, but investigated further by the ARB nonetheless. This GIDEP related to the SMHF28XXX series of Interpoint converters. The concern raised was related to unusual test failure results as a function of low dose radiation testing. The anomalous behavior was attributed to the use of a TC4426 MOSFET driver in the SMHF28XXX converters. ARB parts engineering representatives verified that Interpoint did not use the TC4426 driver in their MFL series. Instead, they used the TC4429 driver which does not have the low dose radiation concern. Interpoint, when asked this question, replied that, "The MFL units used on the Hubble were "ES" standard power units. They did use the TC4429 driver chip, but they were not tested for radiation levels, nor was the entire unit. There were never any guarantees for radiation susceptibility on these units."

Low dose rate testing has the potential to affect devices that are built with bipolar technology. However, not all bipolar technology devices show sensitivity to low dose rate testing. Therefore, low dose rate testing is frequently being performed on bipolar devices to see if there is a problem.

The following devices were used in WFC3 and COS and had low dose rate testing performed by NASA.

<b>Device</b>	<b>Test Report</b>
MFL2805S	PPM-95-126
MFL2812S	PPM-95-128
MFL2815S	PPM-95-127
MFL2815D	PPM-95-135

These test reports can be found online by searching for the test report number at the following GSFC webpage:

<http://radhome.gsfc.nasa.gov/radhome/papers/TIDPart.html>

In each case, the output voltage increased slightly with radiation and only marginally exceeded the manufacturer's spec after 30krad. Ball used the fact that low dose rate testing had been performed on these part types to qualify these devices for WFC3 and COS. Refer to the following radiation test report PPM-95-135 regarding MFL2815D radiation testing results:

Generic Part No.	MFL2815D	Data Source	PPM-95-135 (Ball TD file 0184)
Part Description	65W Dual 15V dc/dc Converter	Rad Source	Cobalt 60
Technology	Hybrid	Sample Qty	3
Manufacturer	Interpoint	Dose Rate	0.04 – 0.18 rad(Si)/sec
Date Code	9443		

### General Summary of Part Radiation Tolerance

Test samples were biased with 9 or 18 W load during irradiation (not sure which, based on inconsistencies in the bias circuit diagram). The total dose levels were 2.5, 5, 10, 15, 20 and 30 krad(Si). No anneal tests were performed. Parameters measured include: full load positive & negative output voltage, efficiency, input current (no load), positive & negative load regulation, line regulation and output ripple. None of the parameters exhibited appreciable degradation following 30 krad(Si), except for positive & negative output ripple and Vout. Note that Vout exceeded the manufacturer's spec pre-rad and throughout testing ("mean +3sigma" values).

+Vout Full Load <b>(14.85 – 15.15 V)</b>	<b>Initial</b>	<b>5 krad</b>	<b>10 krad</b>	<b>15 krad</b>	<b>20 krad</b>	<b>30 krad</b>
<b>Mean</b>	15.04	15.05	15.06	15.08	15.06	15.06
<b>Std Dev</b>	0.08	0.09	0.09	0.09	0.12	0.12

-Vout Full Load <b>(-15.23 to -14.77</b>	<b>Initial</b>	<b>5 krad</b>	<b>10 krad</b>	<b>15 krad</b>	<b>20 krad</b>	<b>30 krad</b>
<b>Mean</b>	- 15.00	- 15.01	- 15.02	- 15.04	- 15.03	- 15.03
<b>Std Dev</b>	0.08	0.08	0.09	0.09	0.11	0.12

Pos. Output Ripple <b>(100 mVp-p)</b>	<b>Initial</b>	<b>5 krad</b>	<b>10 krad</b>	<b>15 krad</b>	<b>20 krad</b>	<b>30 krad</b>
<b>Mean</b>	61.0	80.9	79.1	77.8	79.2	80.5
<b>Std Dev</b>	6.9	8.7	7.5	7.2	7.8	8.1

Neg. Output Ripple <b>(100 mVp-p)</b>	<b>Initial</b>	<b>5 krad</b>	<b>10 krad</b>	<b>15 krad</b>	<b>20 krad</b>	<b>30 krad</b>
<b>Mean</b>	55.5	76.0	75.8	74.8	76.2	77.5
<b>Std Dev</b>	6.1	9.3	8.6	8.3	8.7	8.5

Lockheed Martin Mission Success Bulletin #04-01 dated February 5, 2004, relates to a potential catastrophic failure mode (double syncing) for Interpoint power converters. This bulletin indicates that testing showed that high synchronization signal amplitudes (peak-to-peak) can cause the Interpoint converter to synchronize on rising and falling edges of the external synchronization signal. This effectively doubles the synchronization frequency, which leads to a catastrophic converter failure. Users are recommended to review their designs and determine if their Interpoint sync pin inputs are operating in the 4.5 to 5.5 volt range. The ARB completed such an investigation previously as part of the STIS Side 2 ARB and in that case determined that the external sync waveforms met the recommended operating voltage range specified by Interpoint and this Mission Success bulletin. The ACS circuitry for providing external sync to the Interpoint converters was compared with that of the STIS design and found to be exactly the same. Thus, the ARB determined that the ACS design complies with the recommendations of this Mission Success bulletin.

A possible concern related to potential collateral damage in Interpoint devices caused by Shear Testing was forwarded to ARB from Ball Aerospace via email. The email indicated that Interpoint employs an in-process test on deliverable converters that may compromise the reliability of a small fraction of all delivered hybrids. This test involves shearing a number of components off the substrate, replacing them and then running the test sample through all remaining process steps for inclusion with the deliverable lot. The concern raised was that, during the die shear testing, there is considerable risk for collateral damage to nearby die on the substrate. This was believed to be evidenced in one DPA sample of a Ball Aerospace device as detailed in the following email extract.

From: O'Connor, Timothy  
Sent: Thursday, June 29, 2006 5:23 PM  
To: D'Ordine, Mary  
Cc: Lopez, Vicky; Mollenkopf, Christine  
Subject: Destructive bond pull failure in Interpoint SMTR2815TF triple output DC/DC converter...

...

Further questioning of Interpoint revealed that the only possible outside agent that might be responsible for the die-attach failure would be an inadvertent “knock-on” event from in-process die shear testing that Interpoint performs as an SPC measure of epoxy quality. This testing is normally performed on one sample of a deliverable lot and involves shearing 7 capacitors off the substrate. The shear forces are recorded, new capacitors are installed and the sample continues processing as a deliverable part. Interpoint keeps meticulous records on which serial number undergoes this die shear testing. S/N 176 turned out to be the single sample in our flight lot to experience this in-process operation. CR60 is adjacent to one of the capacitors that were sheared off. It was only happenstance that one of our 2 DPA samples was the die shear sample. Interpoint personnel remarked that this is the first time evidence of a possible negative consequence of their shear/repair procedure has surfaced with any customer and that they were reviewing cessation of the practice across all of their space product.

Interpoint has agreed to no longer fold their die shear samples back into BATC-deliverable lots for all future star tracker-related DC/DC converter procurements. To date, they have been cooperative in identifying the serial numbers of die shear samples of other flight lots of different converter types (single and dual output converters) delivered to other star tracker programs.

I recommend that all delivered lots of Interpoint converters at BATC be reviewed to identify the die shear sample serial numbers and that flight hardware be reviewed for the presence of these die shear samples on finished or in-process PWAs.

Tim O'Connor  
Mission Assurance Manager  
CT/Advanced Imaging  
Ball Aerospace & Technologies Corp.

The ARB attempted to investigate this potential concern further. Unfortunately, ACS build records do not contain specific serial numbers for the Interpoint converters. The only information known for sure, related to the MFL2815D Interpoint converter on the LVPS3 board S/N 001, is that it came from Lot Date code 9443. GSFC Parts Engineering records indicate that there were a total of 40 MFL2815D devices received with a lot date code of 9443. The ARB was hopeful that closeout photos would provide

sufficient resolution to discern the actual serial number marked on the MFL2815D. However, LVPS3 board close out photos could not be located. Therefore, the ARB was left with no choice but to abandon this course of investigation due to lack of S/N information.

Early discussions with Interpoint focused on understanding the MFL2815D internal operation and regulation, followed by ‘what if’ lines of questioning. The ACS on-orbit anomaly signature coupled with Engineering CEB ground testing indicated that the most likely cause of the anomaly was the loss of the +15V power rail in either an open or shorted condition. The +15V shorted condition, regardless of whether internal or external to the Interpoint converter, would result in the same MFL2815D internal current limit response. Refer to GSFC MFL2815D Lab Tests on page 28 of this report for those response characteristics.

Unlike the shorted +15V response, Interpoint stated that an open of the +15V rail within the MFL2815D package would produce a different signature than if an open had occurred on the +15V rail external to the MFL2815D. The rationale for this related to the fact that the MFL2815D relies on the +15V rail as the regulating authority, and thus both the +15V and the -15V rail depend on the +15V rail for regulation. Interpoint stated that if the +15V rail were to open internal to the MFL2815D and prior to the +15V regulation feed back point (which they stated is as close to the output of the device as possible), then the -15V rail would most likely climb in an unregulated manner to at or near the bus voltage being supplied to the MFL2815D at the time, and potentially could remain there for a relatively long duration. This finding was accepted by the ARB and presented in both the ACS Side 2 Switch FRR on June 29, 2006 and the ACS Side 1 Test Proposal on July 13, 2006.

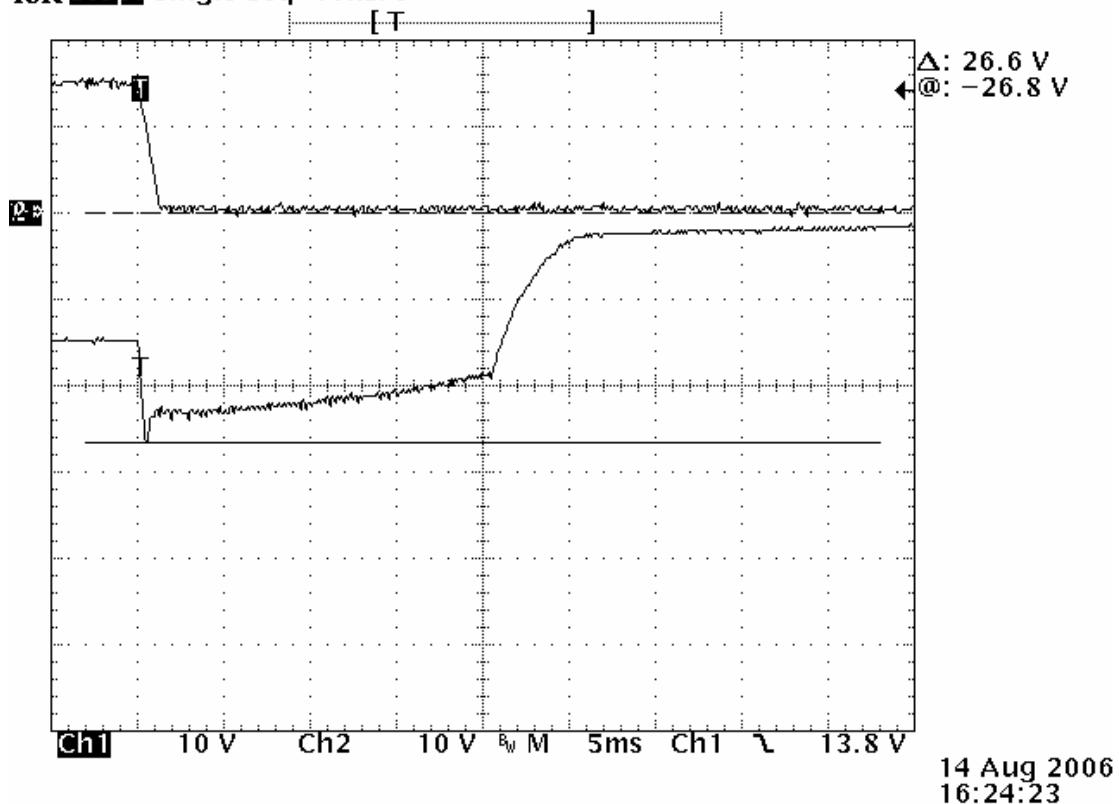
Following the ACS Side 1 Test Proposal presentation, the HST Project requested more information regarding the actual characteristic behavior of an open on the +15V rail inside the MFL2815D prior to the +15V feedback point. Specifically, the goal with this study was to answer the questions: what would it take and how long would it take for the device to fail under the previously stated condition. Thus, the ARB tasked Interpoint with running a lab test to simulate this scenario, record the results, and answer the following set of questions:

1. Will the -15V rail actually increase in voltage?
2. To what value will the rail voltage increase go?
3. How long will the -15V rail remain at the increased voltage level prior to destruction internal to the MFL2815D?

In addition, the ARB requested that Interpoint run this test with a device that is fabricated in the same manner as our MFL2815D/883 devices of Date Code 9443. In other words, Interpoint was requested to make sure they used 4, 5 mil Al bond wires to the input stage FETS.

Interpoint did run such a test. Below is a scope plot of the single test run that they executed:

Tek Stop: Single Seq 10kS/s



The above test was executed with the input bus set to approximately 28V. In the above scope plot, the top trace is the +15V output. The top trace signal transitions to 0V at the point where Interpoint opened the +15V power rail prior to their internal regulation feedback point (at inductor L4). Notice that as the +15V output is opened, the -15V rail, depicted in the lower trace, transitions from -15V to approximately -26.8V (as previously surmised by Interpoint) for a short duration, and then slowly decays from -24V to -18V over approximately 20ms. After 20ms, the device began to destroy itself, and the -15V rail collapsed to approximately -2V and is seen dropping. Interpoint stated that the negative rail remained at approximately -2V for the remainder of the testing, and was still at -2V following a power cycle. According to the data obtained in Engineering CEB Testing section of this report on page 22, as long as the -15V rail remains above -0.4V, the on-orbit anomaly signature would have been present. The potential overvoltage condition of the -15V rail is discussed further in the Overstress section of this report. However, Interpoint also measured the input current during this induced failure and reported that the input current jumped from 0.4 amps to over 8 amps peak and remained higher through the duration of the test. This increase in input current does not match the ACS on-orbit anomaly signature.

Interpoint determined that the response signature obtained above was due to the ultimate destruction of a Shottky diode on the +15V rail, upstream of the point where Interpoint induced the open failure of inductor L4. Interpoint pointed out that this response was only one of a number of possible response outcomes relating to expected duration of the

negative rail beyond its normal limits. Essentially, the duration of excessive voltage on the negative rail is extremely difficult to quantify since there are so many parts that are being pushed well beyond their design specifications; it is truly a race condition to see which internal component will fail first.

Interpoint was further requested to evaluate the MFL2815D internal design and identify open/short fault modes that could potentially lead to the loss of the +15V rail and match the ACS on-orbit signature (input current decrease). The following fault locations and components were identified as candidates:

<b>Circuit Description</b>	<b>Component</b>	<b>Failure Description</b>
+15V Output Section	C80A (Tantalum Capacitor; 22uF @ 35V rated)	Fails SHORT. Once shorted, tantalum capacitors tend to remain shorted.
	C80B (Tantalum Capacitor; 22uF @ 35V rated)	
	10 mil Copper Clip between substrate and output pin (voltage feedback connected to this same copper clip)	Fails OPEN. Causes open load fault response signature without affecting +15V voltage feedback

<b>Circuit Description</b>	<b>Component</b>	<b>Failure Description</b>
Overcurrent Detection Circuitry	<p>Two sets of two Cupron resistors in parallel (0.025 Ohm and 0.02 Ohm)</p> <p>For each of the two outputs (+/-), the sense resistor is actually composed of two Cupron resistors in parallel (0.025 Ohm and 0.02 Ohm), soldered to the substrate with high temperature solder. The summing node is with these two 0.011 Ohm sense resistors arranged in series, so that the Op-amp circuit monitors the total voltage (sum of two currents) developed across these two sense resistors. If one of these Cupron resistors becomes open, then the net increase in resistance (hence voltage) may trick the op-amp circuit into misinterpreting an over-current condition, resulting in reduced PWM duty cycle and reduced output voltages</p> <p>According to Interpoint, it is highly unlikely that these Cupron resistors will fail, either in the solder joints, or in the component itself.</p>	Fault mimics an external short circuit that persists. Device responds by executing short circuit protection. Output voltages fold back and input current is decreased.
	<p>Over Current Detection Circuitry op-amp</p> <p>The Over Current Detection op-amp could fail. It also receives input from the output voltage error-amplifier circuit as part of the Voltage Feedback Circuitry. Its purpose is to throttle the PWM duty cycle when either overvoltage or overcurrent occurs.</p>	Fault mimics an external short circuit that persists. Device responds by executing short circuit protection. Output voltages fold back and input current is decreased.

<b>Circuit Description</b>	<b>Component</b>	<b>Failure Description</b>
Voltage Feedback Circuitry	Precision voltage reference diode (2.5V)	<p>Fault falsely indicates that devices +15V rail is too high in voltage. Device responds by decreasing drive to output voltage rails, thus decreasing output voltage rails. Input current is decreased.</p> <p>The output voltage feedback circuit contains a precision voltage reference diode (2.5V). An error-amplifier (in the same dual op-amp package as the one above) samples the +15V output in reference to this voltage, and feeds this error-output to the op-amp described above, to throttle the PWM control. If this 2.5V reference fails short, it can be interpreted as an over-voltage condition, resulting in reduced output voltage.</p>
	Other elements including two Zener diodes and several bipolar transistors	<p>Fault falsely indicates that devices +15V rail is too high in voltage. Device responds by decreasing drive to output voltage rails, thus decreasing output voltage rails. Input current is decreased</p> <p>There are other elements within this complex feedback and control path that, if failed, can possibly trick the converter to give lowered output voltages, including two Zener diodes and several bipolar transistors.</p>

## Space Weather

An evaluation of Space Weather for June 19, 2006 was conducted. Ultimately, it was determined that the Space Weather was clear on June 19 and therefore most likely did not contribute to the ACS anomaly. Refer to Attachment #8 for the detailed Space Weather findings.

## ACS Side-2 Switch Flight Readiness Review

On June 29, 2006, the ACS ARB presented its preliminary findings and recommendation with regard to proceeding with ACS Side 2 operations. The ARB provided an overview of the investigation status at the time, an ACS hardware safety evaluation based on the status of the investigation and the knowledge acquired at the time, additional ARB recommendations, and a final conclusion. The Flight Readiness Review: ACS Side-2

Switch and ACS CS 4.02 Installation (JV0019) presentation material is provided in Attachment #3; refer to section 2.3 of the presentation materials.

At the Flight Readiness review, the ARB unanimously recommended proceeding with ACS Side 2 activation. Data and testing at the time indicated that the loss of the +15V CEB rail was most likely responsible for the on orbit anomaly. The ARB also determined that switching to ACS Side 2 was safe regardless of an open or shorted condition on the +15V CEB power rail.

The ARB also cautioned that, although deemed safe, switching to ACS Side 2 would not restore ACS CEB operation in all fault scenarios. Thankfully, these fault scenarios were ultimately ruled out, as both WFC and HRC CEB operation was successful on ACS Side 2. ACS Side 2 activation was successfully completed on June 30, 2006.

The ARB, at the time, recommended precluding Solar Blind Channel (SBC) operations while on ACS Side 2, due to unanswered questions relating to CEB ‘hybrid’ power configuration. CEB ‘hybrid’ power configuration occurs when one CEB (such as the HRC CEB) is powered off and the other CEB (such as the WFC CEB) remains powered on. In this configuration, it was determined that the ‘off’ CEB was still receiving +5V power into its Timing Board, yet its other boards were not powered, thus resulting in a ‘Hybrid’ power configuration within the off CEB. The ARB Electrical Engineers were not comfortable with this CEB ‘Hybrid’ power configuration and requested additional time to investigate if it is truly a safe operational configuration. The HST Management team complied with the ARB requested ban, removing SBC activities from the SMS. The ARB ultimately completed its review of CEB hardware safety in ‘Hybrid’ power configuration and the ban was lifted on July 6, 2006. Refer to CEB ‘Hybrid’ Power Configuration on page 43 of this report for details of the ARB investigation.

Another ARB recommendation that is found in the ACS Side-2 FRR package relates to EEPROM writes while in the SAA. A concern was raised by the ARB Parts Engineering representatives that EEPROM writes in a charged particle region of space, such as the South Atlantic Anomaly (SAA), have potential failure modes that could lead to permanent destruction of EEPROM memory locations that would require mapping around in the future. This concern was raised based on issues related to Hitachi EEPROMs. However, verification of the ACS EEPROMs indicated that the manufacturer was ‘SEI’. SEI repackaged SEEQ EEPROMs in RAD PAK packages. During the 1990s, SEEQ was the only qualified EEPROM manufacturer approved for space flight applications. NASA GSFC wrote specification G311P-783-200 for these parts. GSFC Radiation Engineering calculated the risk of upset or destructive events on ATMEL/SEEQ 28C256 EEPROMs in write mode in the HST orbit (for solar minimum activity). The risk of a destructive event was determined to be negligible (5.7E-12 event/device-s), and the risk of an SEU determined to be very low (2.6E-6 events/device-s). The radiation group added that there is no advantage to writing into the EEPROM outside of the SAA as heavy ion induced rates dominate the event rates. Based on these findings, this recommendation to not perform EEPROM writes to ACS while in the SAA

was verbally withdrawn at the time of the presentation based on the information provided by parts engineering and radiation engineering earlier that morning.

## CEB ‘Hybrid’ Power Configuration

The CEBs can and are configured with all +15V, -15V and +35V inputs opened via relays on the CEB boards, yet still allow +5V input power onto the CEB Timing Board. This power configuration has been referred to as the ‘Hybrid’ power configuration since one board can be powered in a CEB while all of the others are not.

An evaluation of the CEB ‘Hybrid’ power configuration was conducted by the ARB members. A detailed review of the CEB Timing Board schematics revealed that +5V applied to the CEB Timing Board will not be leaked to the unpowered CEB boards following CEB power on initialization. This is due to the use of AC244 and AC374 tri-state output drivers. The investigation determined that at power-on reset, the CEB Timing Board FPGA will set the CS\_BUS\_EN control line to 0V. This was verified in the “Test Procedure, Timing Board, ACS CEB”, drawing number 538217. 0V on the CS\_BUS\_EN through transistor inverter Q101 ensures the output control of the AC244s and AC374s are maintained in a tri-state (i.e. high impedance) configuration. In tri-state mode, these devices do not electrically drive and thus voltage is not provided at their outputs. Without drive voltage, there is no potential present to force current into the off side of the CEB through sneak paths created by the powered down configuration. Thus, this configuration is deemed safe.

However, further evaluation revealed that subsequent MEB commanding to the CEB to begin executing a timing profile would result in the CS\_BUS\_EN signal changing from 0V to an active 5V, thus activating the output drivers. This would eliminate the protection provided by the Timing Board output drivers in tri-state mode and could lead to overstress of the down stream receiving circuits, as current will be forced up through their input protection diodes to the unpowered rail. Thus, if the ‘Hybrid’ CEB power configuration is to be used, safeguards must remain in place to ensure the CEB hardware integrity. Note that the present operational software contains a virtual flag that indicates if a CEB is on or off. If deemed off, MEB commanding to the off CEB is disallowed and no commands will be issued. This implementation fully meets the ARB requirement that no commanding of the off CEB be conducted. However, the ARB felt it prudent to require a CARD item be added to ensure that future operational considerations do not inadvertently bypass this important CEB command disable feature.

Hot switching of the CEB power configuration relays has long been known by the Science Instrument Systems Engineers (SI SEs) to be avoided. Both ACS and STIS operational procedures are built such that they preclude hot switching of the CEB power configuration relays. However, the ARB also discovered that a specific CARD item on this topic had not been put in place for either ACS or STIS. The ARB, in the interest of ensuring that such an important item as not hot switching ACS or STIS CEB power configuration relays in the future was not overlooked, requested a dedicated ACS and STIS CARD item on this subject be added.

The ARB therefore recommended the addition of following CARD items:

- ACS only: Prevent commanding of the ‘off’ CEB
- ACS and STIS: Prevent hot switching of CEB power configuration relays

The SI SEs have the action to update the CARD. Currently these additional CARD items are in the internal review cycle and will be sent to the CCB upon this review.

A CARD item is already in place for WFC3 and all WFC3 operational procedures conform to these restrictions.

The moratorium on SBC activities, due to the use of CEB ‘Hybrid’ power operations, was lifted by the ARB on July 6, 2006.

## **ACS Side-1 Test Proposal**

On July 13, 2006, the ARB presented a comprehensive ACS Side-1 test proposal to a board consisting of HST Code 440, Code 441, Code 442, and STScI representatives (See Attachment #2).

## **Failure Mode Evaluation and Analysis (FMEA)**

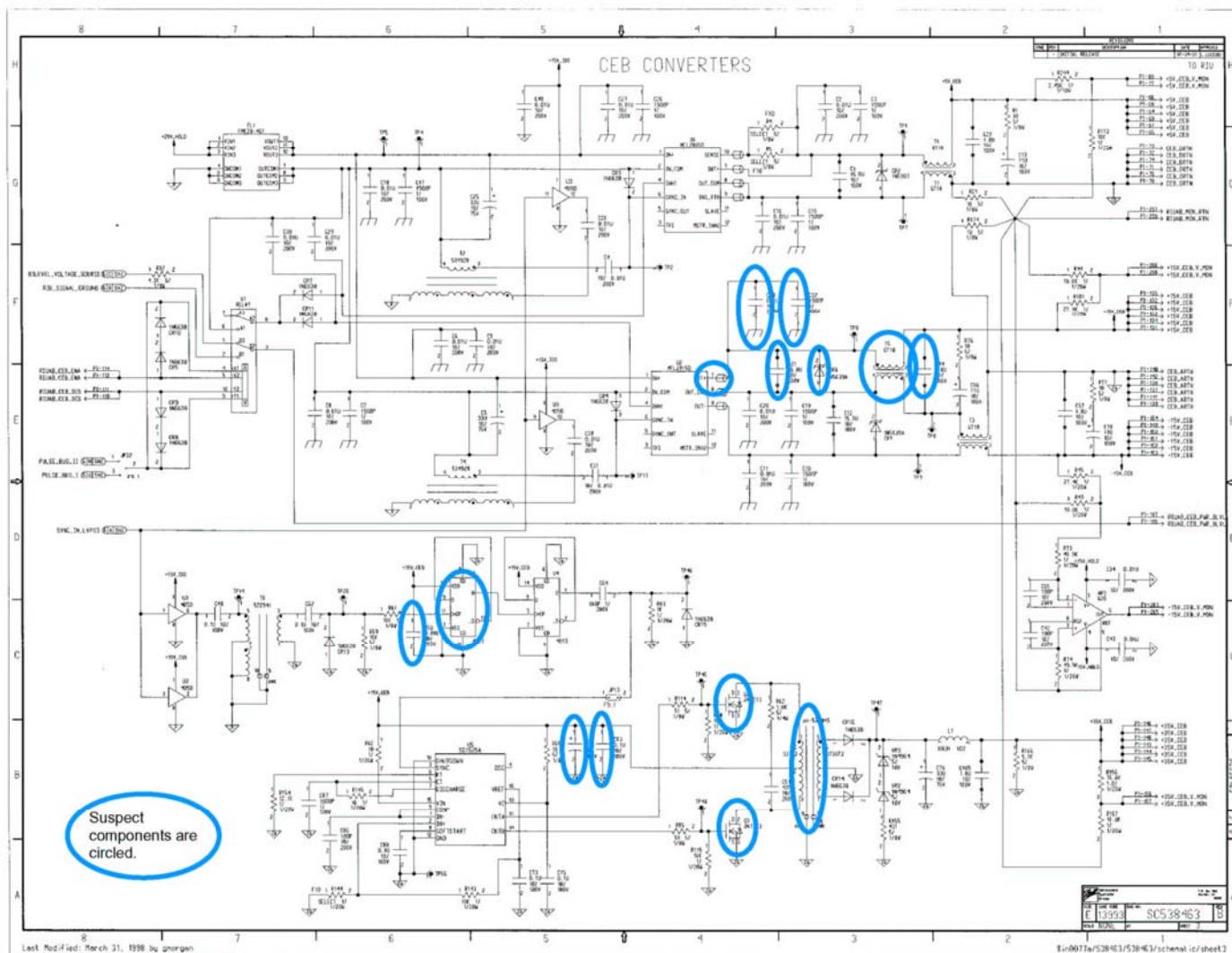
A thorough component level Failure Mode Evaluation and Analysis (FMEA) was conducted by the ARB on the ACS LVPS3 Board circuitry relating to the +/-15V CEB power rails. The goal of this FMEA was to evaluate each and every component connected to the +/-15V CEB power rails and determine the associated response based on postulated credible fault modes, such as shorts or opens. The FMEA resultant responses were then compared to the set of voltage rail responses obtained via CEB Engineering unit lab testing to determine if the postulated failure mode could have resulted in the ACS on orbit anomaly. Refer to Attachment #5 for the FMEA.

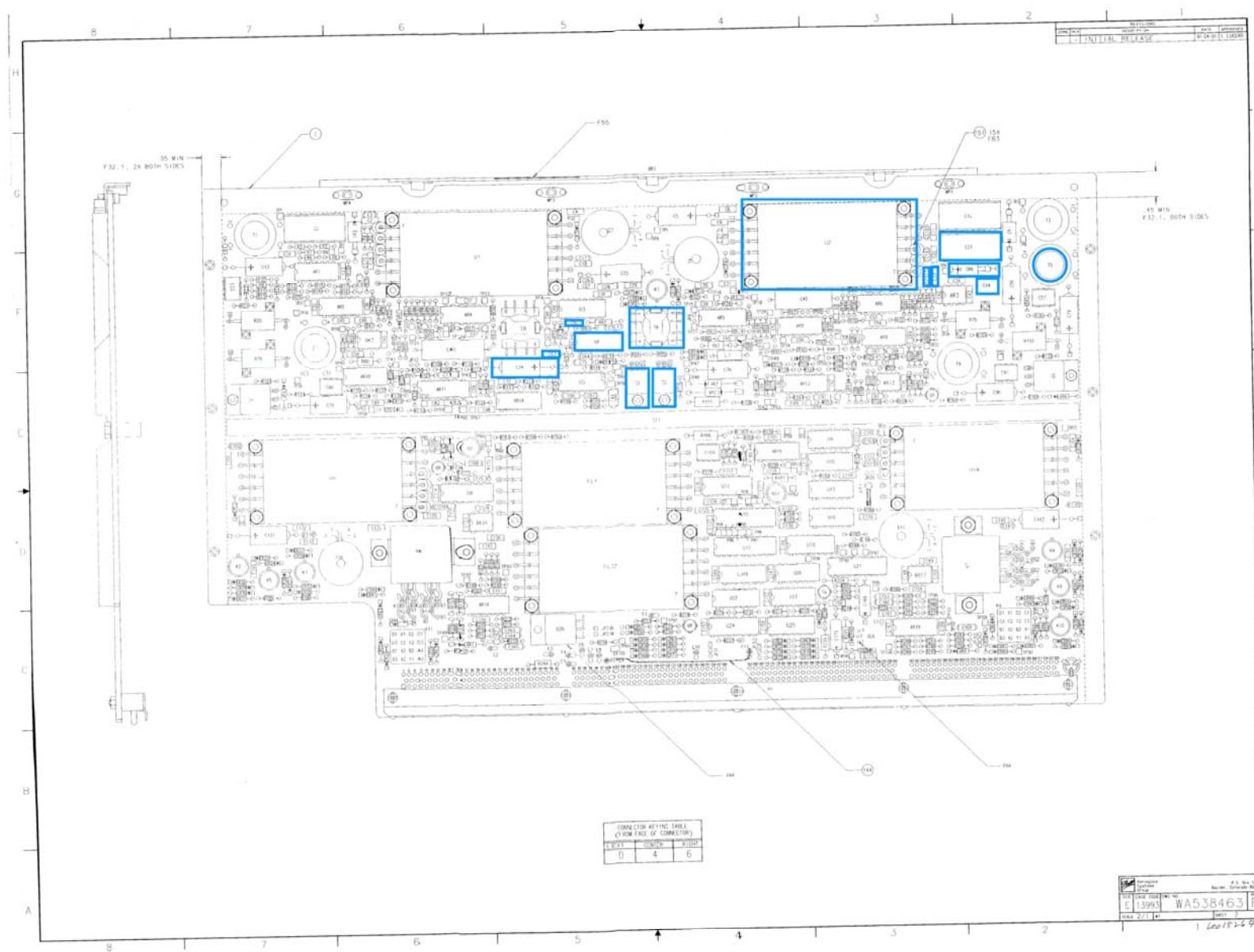
Based on the FMEA results, the following fourteen ACS LVPS3 board parts (comprised of nine distinct part types) and associated failure modes have been identified as possibly resulting in the ACS on-orbit anomaly.

Ref Des	Part No	Part type	Value	Failure	Effect	Condition Matches on Orbit Anomaly
U2-7	MFL2815D/883	Interpoint DC/DC	MFL2815SD: out+	short to chassis	Loss of +15V; -15V reduced to less than -1V	Yes
"	"	"	"	short common	Loss of +15V; -15V reduced to less than -1V	Yes
"	"	"	"	open	Loss of +15V; -15V reduced to approx -11V	Yes
C33	M39014/02-1338	Ceramic	0.01uF, 10%, 200V	Short	Loss of +15V; -15V reduced to less than -1V	Yes
C32	CCR05CG152FS	Ceramic	1500pF, 1%, 100V	Short	Loss of +15V; -15V reduced to less than -1V	Yes
C21	532857-011085	Multilayer Ceramic, 87106-085	15uF, 10%, 100V	short	Loss of +15V; -15V reduced to less than -1V	Yes
CR6	170525-018	diode, transient suppressor	JANTXV1N5639A	short	Loss of +15V; -15V reduced to less than -1V	Yes
C44	532857-011065	Multilayer Ceramic, 87106-065	1.8uF, 10%, 100V	short	Loss of +15V; -15V reduced to less than -1V	Yes
T5	522940-001	Inductor, Output Filter		winding-to-winding short	Loss of +15V; -15V reduced to less than -1V	Yes
"	"	"		winding 1-2 open	Loss of +15V; -15V reduced to approx -11V	Yes
C50	M39014/02-1338	Ceramic	0.01uF, 10%, 200V	Short	Loss of +15V; -15V reduced to less than -1V	Yes
U4	170501-003	Dual D F/F	CD4013, M38510R05151BCA	internal short VDD to gnd	Loss of +15V; -15V reduced to less than -1V	Yes
C74	M39006/22-628H	wet tantalum, polarized	11uF, 10%, 100V	Short	Loss of +15V; -15V reduced to less than -1V	Yes
C63	M39014/02-1338	Ceramic	0.01uF, 10%, 200V	Short	Loss of +15V; -15V reduced to less than -1V	Yes
Q2	171266-005	2N7273	12A, 100V MOSFET	Short D-to-S	Loss of +15V; -15V reduced to less than -1V, loss of +35V	Yes
Q3	171266-005	2N7273	12A, 100V MOSFET	Short D-to-S	Loss of +15V; -15V reduced to less than -1V, loss of +35V	Yes
T6	538445-001	Transformer		Primary-to-Secondary short	Loss of +15V; -15V reduced to less than -1V, loss of +35V	Yes

Table 1: FMEA Parts List

Pictorially, the identified suspect devices have been identified on the following LVPS3 schematic and assembly drawing.





A search for GIDEP alerts, Lockheed Martin Mission Success Bulletins and Lessons Learned was conducted for all suspect devices identified above by the FMEA. There were no findings, except for GIDEPs and Mission Success Bulletins related to Interpoint devices. Refer to MFL2815D Analysis and GIDEP Search Results on page 31 of this report.

The above suspect device information and all Ball source control drawings associated with the above identified components was provided to the GSFC Parts Engineering Branch. The GSFC Parts Engineering Branch was tasked with evaluating the likelihood of parts to fail based on historical part type failure rates while accounting for known source control document required pre-flight screening. The evaluation provided by GSFC Parts Engineering is as follows:

Dear Roger,

Your review board has located fourteen ACS LVPS3 board parts, and a failure mode for each, which could cause the observed ACS failure telemetry. These are presented [in Table 1 on page 45] of your report. You, Bruce Meinhold, and I met today to estimate the likelihood of failure of each of these parts, based on our experience with the robustness of these parts. This email is to document our conclusions.

### Summary

I rank the most likely cause of the ACS failure as residing within U2-7, the Interpoint DC-DC converter. The next most likely cause is the transformer T6. I cannot rank the chances of a second delamination of the pw-board and its heat-sink leading to the ACS failure, but I do not suppose it is "low likelihood" since (a) this delamination happened once and (b) it seems not to have been understood, but only repaired.

### Discussion

- 1) U2-7: MFL2815 --- This is a plausible cause of the ACS failure, since several of these have failed in ways that duplicate the ACS failure-signature over the course of the HST program.
- 2) C33 / C32 / C50 / C63 : M390014/xx and CCR05CGxx ceramic capacitors --- Each of these is highly unlikely to have failed short. The space industry has used a huge number of these, with no failures when screened as these have been, and not abused by their use (eg, these can be destroyed by mechanical stress); successful operation for 4+ years of operation in space implies absence of excessive stress, since failure under stress tends to be prompt.
- 3) C21 / C44 : multilayer ceramic capacitors --- When these fail, which is very rare (unless exposed to excessive mechanical stress), they "open"; failing "short" is highly unlikely.
- 4) CR6 : transient suppressing diode --- The failure mode is "open" and is rare; a "shorted" condition is much more rare, ie., is highly unlikely.
- 5) T5 / T6 : "magnetic" part --- These are curiously sensitive to heat. When kept below (roughly) 150C throughout their windings, these devices are robust. But this robustness melts away as any part of the windings exceed (roughly) 150C (for the insulations used here) since this increases the wire's resistance which leads to still more heating, and soon softens the insulation and allows the conductive metals to touch and short. The history of T6 (which failed short as a result of abusively high current until the wire insulation softened and allowed shorting, and was replaced, only to have the replacement subjected to the same abusively high current, but for a briefer time) suggests the possibility of a latent failure. Correct operation of the "as flown" T6 for 4+ years somewhat lessens the likelihood that this is the cause of the ACS failure, but does not by any means make it highly unlikely. I suggest it is a plausible cause of the ACS failure, perhaps only an order of magnitude behind the likelihood of an Interpoint failure. (These estimates of likelihoods are uncertain to perhaps half an order of magnitude.)
- 6) U4 : Dual Flip-Flop --- This device has seen wide use for more than 15 years, and is robust and failure-free (unless wickedly abused, when it fails promptly): an electrical short after 4+ years of correct operation is highly unlikely.
- 7) C74 : wet-slug tantalum capacitor --- This was purchased as a "established reliability" part, with a measured failure rate of no more than 0.01%/1000hr when operated at 85C and at rated voltage: when operated at less than 50C and at 50% (or less) of its rated voltage, its failure rate drops to "invisible in this application": its failure in ACS is highly unlikely. If it did fail, there is a reasonable chance that enough outgassing would happen that this event would be visible in telemetry data monitoring pressure in the aft shroud --- so, "no pressure event visible at the time of the ACS failure" ==> "no shorted C74".
- 8) Q2 / Q3 : 2N7273 --- this device is highly unlikely to fail when run at the voltages applied to it in ACS. This extends to the possibility of a "gate rupture" induced by a hi-energy heavy charged particle (single event effect): this is highly unlikely at the voltages applied to these two examples of this device in the ACS.

Not on the list of parts is your recounting of the delamination between a pw-board and a heat sink bonded to it. The stresses applied by the mis-matches (CTE-driven?) were large enough to rupture the aggressively-strong adhesive, and also to shear two rivets. The de-bond was addressed only by re-bonding, and not by re-design or (apparently) even analysis of the expectation of the success of the re-bonding. In particular, I don't see any reasons given to suppose that this repair will certainly result in a bond that is substantially stronger than the original bond. Also, these kind of stresses can "warp" the pair (pw-board and heatsink) into shapes like a potato-chip, and these can impose stresses on board-mounted parts that can fatigue them. (And also impose stresses on internal parts like plated-through holes.) I do not know enough about this situation to hazard an estimate for the probability of a second de-bonding that may have ruptured a wire. But this does seem to be a possibility, even if I cannot estimate a probability.

Sincerely,  
Henning Leidecker

Note that the above evaluation is solely based on piece part related data and historical failure rates. It does not account for potential circuit design stresses or manufacturing Quality and Test related issues that possibly occurred on the ground prior to launch. Refer to the Additional Design Issues and Concerns on page 57 and Quality Records on page 50 of this report for those inputs.

## Overstress

A review of the LVPS Board #3 schematics (SC538463 rev B) indicated the use of 'hefty' Transzorbs (1N5639A) on the +/-15V outputs from the MFL2815D converter. The 1N5639A data sheet shows that these devices will shunt current to ground when a voltage in the range of 17.1V to 18.9V is applied across them. Therefore, if the Interpoint MFL2815D failed in such a manner as to allow one or both of its output rails to exceed its maximum regulation value, the output voltage on the power bus would have been limited to 18V +/-5% by the Transzorb protection circuits.

A review of the down stream parts contained in the CEB indicated that all parts are rated to 20V or higher (greater than the worst case 18.9V Transzorb protection voltage) with two exceptions. The AD674B Analog to Digital Converter is rated for a maximum voltage of 16.5V, and the AD585 Sample and Hold Amplifier is rated for a maximum voltage of 18V. Thus, these two device types are the only parts that potentially could have been overstressed if this Interpoint MFL2815D overvoltage scenario were to have occurred.

It should also be noted that, even in light of the possible overstress to the previously stated two devices, the ARB does not recommend changing the Transzorb value to that of a lower voltage rated device. At present, the lower end of the Transzorb activates at 17.1V. Lowering the Transzorb value would move its lower end closer to the actual +/-15V operating rail, which could result in the Transzorbs conducting even when not desired. For this reason, the ARB does not recommend a change in the Transzorb values.

## Quality Records

The ARB requested that the ACS Quality Records be recovered from storage and made available for evaluation. This task was partially successful, as not all desired quality records were located.

The ARB requested the ACS closeout photos for the Side 1 LVPS3 board. Unfortunately, those photos could not be located. Instead, the ARB used recent COS LVPS photos as a reference example of what a typical LVPS instrument board looks like.

**Preliminary Failure Report number 2314.019 Rev. -**, referencing MDR A92311 12/3/1997, was written against ACS LVPS3 S/N 001 board due to an initial board level test failure. Board level testing discovered that the +28V dc supply was applied to the boards thermal plane. A visual inspection was performed and found pins 128 and 129 of the P1 connector were shorted together and also to the connector case via a solder splash.

A failure review stated that no parts were overstressed, including the Interpoint DC/DC converters, as the Interpoint converter chassis' are isolated from their internal circuitry. The ARB re-evaluated this failure scenario and contacted Interpoint to verify the previous finding. Interpoint concurred, stating via email response that, "All Interpoint converters are tested for 10 Meg-Ohm isolation at 500V (input/output, input/case, and output/case). Exposing the case to 28V potential will not create an overstress condition". Ultimately, the ARB found that all the correct actions had been taken with regard to this test anomaly and no overstress had occurred as a result of this test anomaly. Refer to Attachment #6 for a copy of this failure report.

**Test Anomaly Worksheets (TAWS) TAWS 33, TAWS 78, and TAWS 81B with Ball Failure Report 20314.024 Rev** – were reviewed by the ARB. This failure chain of events occurred during MEB box level TVac testing, but ultimately was attributed to a circuit design error on the LVPS board #3 S/N 001 board (the board that failed on orbit). The chain of events is extremely convoluted, so a synopsis follows (Note that LVPS Side 1 below refers to the LVPS#3 board that is suspected of containing the root cause of the failure on-orbit):

- TAWS 33

- It was noted that the +35V CEB supply was running a little higher than expected. This TAWS showed "minor" waggling of the +35 monitor for MEB 1 (LVPS Side 2) thermal cycling.
- The "Analysis and Conclusion" text indicates a safing limit of 37.5V (which comes into play for MEB 2 testing).
- TAWS closed stating, 'suspect it's ok' and that the procedure needs to be redlined to open tolerance to 35.5 +/- 1V.

- TAWS 78

- Generated against MEB 2 (LVPS Side 1) during thermal cycle testing (first hot cycle). This TAWS is the original sponsor of MDR A92365.
- Anomaly Description: Lost +15V/-15V and +35V CEB voltages during the hot soak
- Analysis and Conclusion: Found that the +35V transformer was overheated and shorted. The cause of the problem was found to be related to the +35V sync pulse that controls the PWM. The "Attached write-up" referenced in "Analysis and Conclusion" section was scanned in as part of TAWS 81B. (It was included as part of both TAWS' in binder). Thus, this conclusion was not actually arrived at until after TAWS 81B work was completed.
- Data extraction indicates that the CEB converter was powered on at 19:06:10. It SHOULD HAVE safed at 19:09:11 but did not, since software safing limits were not enabled. The part(s) failed at 19:29:11 after being energized for 23 minutes

and, per the extraction, it appears as though testing continued for at least another hour and a half (20:59:03).

- Although not stated specifically in the TAWS documentation, the failed transformer T6 and a number of other components (R84, R82, U4, C50, and Q2) were replaced following this failure and the unit returned to thermal cycle testing, which ultimately led to TWAS 81B. This rework is actually discussed in the disposition of TAWS 81B.
- TAWS 81B
  - Generated against MEB 2 (LVPS Side 1) during thermal cycle testing (first retest hot cycle)
  - Sponsored the part of the MDR which reads "During the next hot operate the 35V monitor again exceeded the limits and the MEB safed"
  - This test resulted in a safing event after three out-of-limit samples (3 minutes), as expected.
  - Note: TAWS 81A is unrelated to this TAWS. It refers to an operator error resulting in a memory dump error. Since these worksheets were handwritten, it is assumed that the number "81" was accidentally used twice and it was later corrected by assigning an "A" and a "B".
- Attached +35V Bias Converter Anomalies and Resolution Report, dated April 16, 1998
  - States that **visual inspection** of the newly replaced T6 transformer determined there was no evidence of overheating.
  - In an attempt to recreate the anomalous voltage observed during thermal cycle testing in the lab, the LVPS3 card was plugged into the LVPS test set and **subjected to hot air from a heat gun**.
  - Ultimately determined that the SG1525A Pulse Width Modulator (PWM) free run frequency required modification in order to not conflict with the external sync frequency. This conflict results in a double pulse condition to the PWM output FETS, resulting in extra long on periods that allow the T6 transformer core to saturate, resulting in a large increase in current through the transformer windings which will eventually lead to the destruction of the transformer. A design change was implemented; R154 was changed from 10K to 12.1K. The design change was implemented on all ACS LVPS3 boards.
  - Report states, "Because of the conditions observed during the second temperature test of the LVPS3 board in MEB2, and the short period of time that the +35 volt output was in an anomalous condition, there was not enough time to overheat the T6 transformer. In my opinion, no components were overstressed.".
  - Report also states, "Also, it appears that the connecting wires on Q3 pins 1 and 2 are extremely close to touching.". There is no further reference to this concern anywhere.

- Summary

- During the MEB 2 box level TVac test, the LVPS3 board ran for 23 minutes at a higher than expected 35V bus voltage (safing limits were disabled) and then failed due to a short caused by overheating of the T6 transformer. The failed T6 transformer and a handful of other parts were replaced, but the team failed to correctly identify the root cause. The post rework re-test resulted in safing after 3 minutes that, according to the authors of the anomaly resolution, presumably saved the parts from overstress and led to the identification of the root cause (R154 value needed to be increased in order to lower the SG1525A free run frequency).

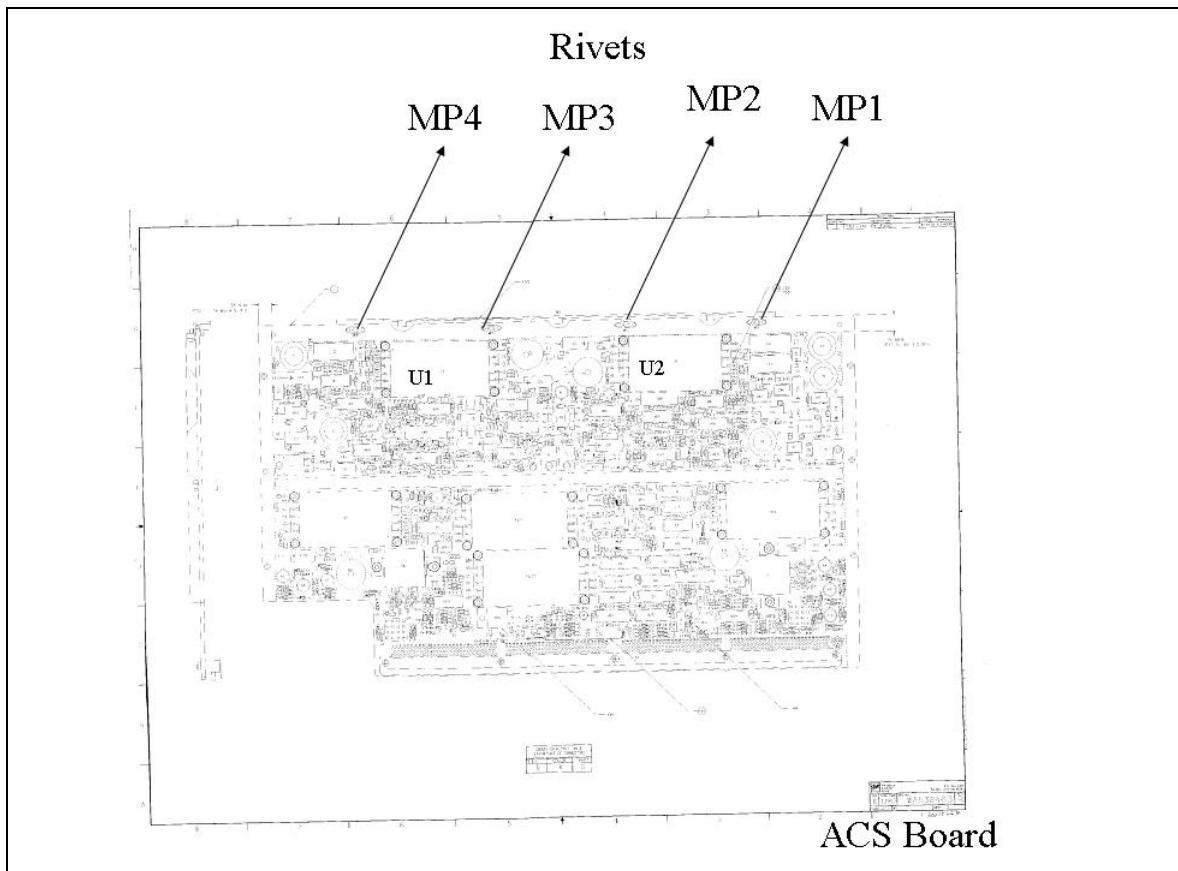
- ARB Evaluations resulting in Non-Concern Findings

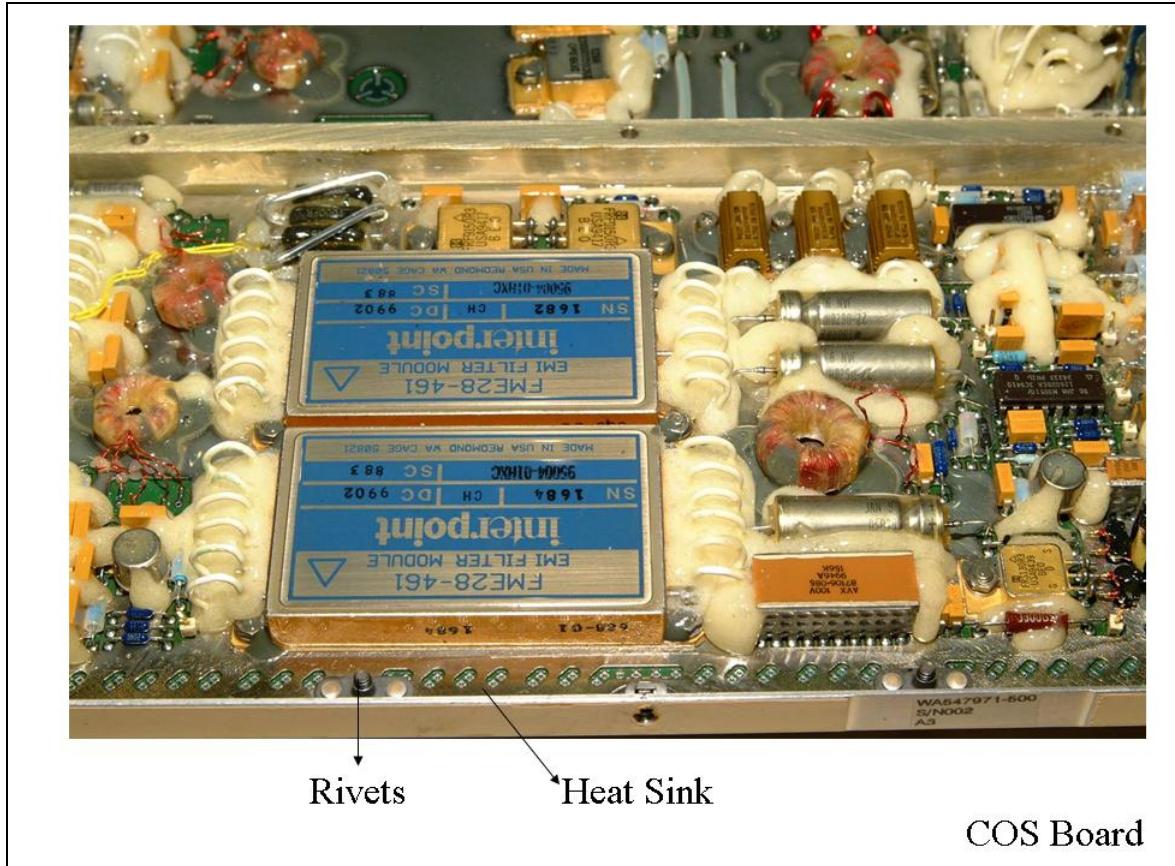
- The ARB evaluated if the SG1525A PWM synchronization circuit design change was adequately implemented. The ARB concluded that the correction to the circuit timing was implemented correctly. An old Silicon General Ap-note PS-7 from the SG1525A Synchronizing the SG1525A PWM states, "Program the SG1525A oscillator with Rt and Ct to free-run at a frequency 10% slower than the external clock frequency". The ARB determined that the original design with R154 at 10K did not in fact meet this requirement, but did meet this requirement with the modified design of R154 at 12.1K.
- The ARB reviewed the parts replaced following the initial test anomaly to determine if all potentially overstressed devices were replaced. The ARB concluded that the parts replaced do not make 100% sense. T6 was removed and replaced, as T6 was thermally shorted and sent to F/A. Also, devices Q2, R84, R82, U4, and C50 were also determined to have possibly been overstressed and were therefore replaced. However, evaluation by the ARB of these parts in the circuit design could not identify a reason why these devices actually required replacement. There is no write up supporting any of this, only a statement that they were replaced due to concerns that they may have been overstressed. FET Q2 was replaced for fear of overstress, yet the ARB noted that its companion FET Q3 was not replaced. A review by the ARB of the 2N7273 FET determined that its continuous Drain Current is specified to be 12 Amps at  $T_c = 25C$  and 7 Amps at  $T_c = 100C$ . Since the +15V Interpoint MFL2815D converter will enter current limit (below 4.5 Amps) long before the continuous drain current limits of the 2N7273 FET are reached, FETs Q2 and Q3 would not have been overstressed.
- The ARB was concerned to find the statement, "Also, it appears that the connecting wires on Q3 pins 1 and 2 are extremely close to touching." in the Anomaly Resolution report with no further reference to how this concern was addressed. Documentation reviewed by the ARB does not indicate that this concern was addressed at all. ARB assessment of a short between FET Q3 (one of the two switching FETS used by the SG1525A PWM to control current flow through transformer T6) Gate pin 1 and Drain pin 2 would result in Q3 being off at all time, which would lead to saturation of the T6 transformer through FET Q2. This would ultimately lead to the ARB postulated 7V motor boating of the +15V supply due to the SG1525A 7V internal shutdown limit. Note that the ARB FMEA and lab testing does not believe that the 7V motor boating condition matches the ACS on-orbit anomaly signature. In addition, Phil Christon of Ball verbally reported to ARB member Ken Albin that he recalls that the two points in question were physically close but not touching and that this was a workmanship issue that should have been addressed.

- ARB Concerns

- The ARB was concerned to find that after the initial replacement of transformer T6, the anomaly again repeated with the new transformer during re-testing with no further part removal and replacement. The report states, "Because of the conditions observed during the second temperature test of the LVPS3 board in MEB2, and the short period of time that the +35 volt output was in an anomalous condition, there was not enough time to overheat the T6 transformer. In my opinion, no components were overstressed.". The ARB has concluded that an opinion based on external visual observations of a transformer is insufficient to determine if the internal wiring insulation of the transformer was subjected to stress that may have eventually resulted in a latent type anomaly on orbit. The ARB notes that the single test sample original 'shorting' failure took 23 minutes to produce a hard short. The ARB also notes that the second transformer was subjected to the same conditions for less than 1/8<sup>th</sup> of that time, or about 3 minutes. However, the ARB has no way to determine qualitatively what potential stress and possible latent damage may have occurred within the T6 transformer over the 3 minutes of heating that it was subjected to. Also note that additional bench level anomaly investigation work was conducted with this flight board for an unspecified time duration.
- The ARB was concerned to find that the flight LVPS3 board was subjected to uncontrolled heating effects by a heat gun as part of the anomaly investigation. Due to lack of controls, the ARB cannot reasonably determine how much localized thermal gradient was applied to which components on the flight LVPS3 board during this anomaly investigation. It is conceivable that this anomaly investigation technique produced thermal stresses that resulted in a latent failure on the flight LVPS3 board in question.

Ball Material Discrepancy Report (MDR) A92295, identified a PWB defect around rivets associated with LVPS3 S/N 001 (refer to Attachment #6). Damaged MP1 through MP4 were noted to be crushed and split. Nut plates were warped slightly and the board had separated between the Ground/Thermal Plane and the fiberglass board. The separation was written up as confined to the edge of the board, with two rivets almost touching vias. The defect disposition indicated that the chassis ground and rivets are both to chassis ground, thus no effect if they had touched. Also, repair of the separated edges of the Ground/Thermal Plane and the fiberglass board was accomplished by injecting BPS 26.05 Type II, Class 3, grade A, Style A and clamping the edges of the board during cure. It was also stated that the thermal dispartitive surface plane is clamped to PWB by the nut plate and rivets for mechanical support and will prevent propagation of the separation.

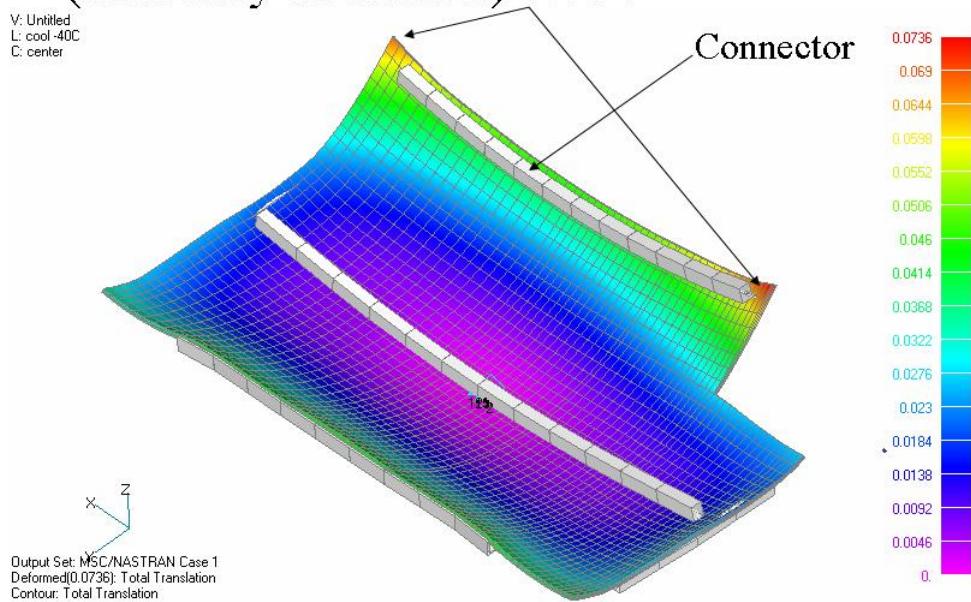




Upon ARB review of MDR A92295, the ARB was concerned with regard to potential on-orbit board deflection issues and the possible on-orbit re-separation of the Ground/Thermal Plane from the fiberglass board. A recent Thermal Distortion analysis completed by Bart Drake for the STIS repair effort indicated that the warpage and twist of an unconstrained LVPS board is substantial due to dissimilar properties between the Ground/Thermal Plane and the fiberglass board itself. In this analysis, a room temperature (20C) to -40C delta thermal change was applied to the model for a 60C total delta T. Thus the ARB cannot help but wonder if a Ground/Thermal Plan to fiberglass board separation could have occurred that ultimately led to a shorting condition or a stressed component solder joint that resulted in the ACS on-orbit anomaly. The suspected circuit components associated with this on-orbit anomaly are primarily located in the region where this MDR identified the initial board separation. In addition, ACS is powered down approximately once every month to perform anneal operations, at which time the LVPS board temperatures transition approximately 30 degrees C during the current 6-hour anneals. During previous 24-hour anneals, the transition was about a 40 degree C delta.

# Analysis Results

- Maximum displacement from center (boundary constraint) 0.074”



Requests were made of Ball Aerospace to provide qualification documentation on the process and design of the Ground/Thermal Plane to fiberglass board. None has been located at the time of this writing.

## Additional Design Issues and Concerns

A detailed ARB review of the U5 SG1525A Pulse Width Modulator implementation in the ACS circuit identified two concerns related to the external synchronization signal input. These concerns related to external sync signal amplitude and pulse width. Review of an SG1525A ap-note revealed the following with regard to reliable external synchronization, “Drive the SG1525A SYNC terminal (pin 3) with the external clock. Input impedance is 2K. The clock amplitude should be greater than 2 volts and less than 5 volts. Pulse width should be at least 300nsec for reliable triggering, but it should not exceed the free-running oscillator clock pulse width by more than 200nsec.”

A review of the ACS SG1525A circuit implementation revealed that the External Sync Input pin (pin 3) is driven by a CD4013 device that is powered by +15V. Thus, the sync input will be seeing +15V pulses. However, the SG1525A application note specifies that the Sync input voltage range should be between 2V to 5V. **Thus, +15V external sync signal input voltage into the SG1525A is well over the +5V recommendation of the device.** A review of the SG1525A Oscillator Schematic (as depicted in the data sheet) does indicate that the oscillator section is connected to Vref which is a +5V input. Thus,

a +15V Sync input would in fact be larger than the Vref supplied to the circuit. The ARB contacted Texas Instruments to discuss this concern. The TI representative ultimately stated that the 5V limit should not be exceeded into the external sync input; no further information was supplied.

The ARB attempted to evaluate the risk to the on-orbit ACS side 2 circuitry as a function of this finding. The SG1525A specification sheets as well as the ap-note indicate that the external sync input contains an internal 2K series resistor. The power through this series resistor based on the ACS sync input pulse width and amplitude at 150 KHz was then determined to be 215 uWatts. The ARB believes that this extremely small power value will not lead to degradation of the SG1525A external sync input. One unknown that the ARB cannot determine is the trace to trace breakdown voltage limits provided by the SG1525A design. If the SG1525A sync input design assumes 5V, it is unclear how it will respond and continue to respond to a higher voltage pulsed input of +15V max over time.

The other concern related to the external sync signal input pulse width. The SG1525A ap-note clearly states that the, “Pulse width should be at least 300nsec for reliable triggering, ...”. ARB evaluation of the external sync signal pulse width circuitry revealed that the pulse width is function of the U5 CD4013 +15V output signal passing through a series capacitor (C64 at 100 pF) with a resistor (R83 at 1K) to ground. This circuit technique is valid for shortening pulse widths. However, a PSpice simulation of this sync input circuitry into the SG1525A indicated that the SG1525A would see an external sync pulse width of only 150ns at the minimum 2V level. Thus, based on the recommendation provided by the SG1525A ap-note, this pulse width is far too short (150ns actual vs 300ns recommended) to provide reliable synchronization. Ultimately, unreliable synchronization could lead to a double pulse condition similar to the one described in the Quality Records section of this report under the TAWS 81B box level TVac test anomaly. Unreliable synchronization could thus result in a double pulse condition to the PWM output FETS, resulting in extra long on periods that allow the T6 transformer core to saturate, resulting in a large increase in current through the transformer windings which could eventually lead to the destruction of the transformer.

The ARB performed an engineering test using the ACS Test Bench located in the GSFC VSTIF facility. All testing was conducted at ambient conditions. The goal of the test was to verify that the PSpice findings related to the external sync pulse amplitude and width were accurate, as well as attempt to identify if PWM double clocking was occurring due to the less than recommended external sync pulse width. Scope traces of the SG1525A external sync signal did in fact verify that the sync signal pulse had a peak amplitude of approximately 9V and a pulse width of approximately 150ns when measured at the 2V level. This matched the findings of the PSpice model. Scope traces of the PWM A output driver phase were monitored for signs of double clocking. None were detected. The ACS Test Bench 28V power supply was then manually adjusted, at varying rates, within a +24V to +29V range to see if input bus voltage disturbances would produce signs of PWM output double clocking. Again, none were detected. Although no signs of double clocking were detected with the VSTIF ACS bench, the

ARB did note that that testing was conducted at ambient, whereas the original indication of problems with external syncing during the flight acceptance ACS ground test program were not detected until MEB box level hot thermal cycle testing.

## COS

In light of the ACS Side 1 on-orbit anomaly and the previous two anomalies on STIS Side 1 and STIS Side 2 relating to power rail/supply concerns, the HST project decided proactively to change all COS (and WFC3) Interpoint converters from the present MFL/883 type to a more reliable space qualified SMFL type (the STIS Repair Board was previously slated to be fabricated with the SMFL type parts already). Note that this action was taken independent of the ACS ARB activity, since the analysis does not point rigorously to one unique part as the certain cause of the problem Refer to Attachment #7 for detailed differences between Interpoint MFL/883 devices and Interpoint SMFL devices and for a thorough explanation as to how the increase in reliability is achieved.

In light of the ARB findings regarding the excessively high external sync signal amplitude into the SG1525A, a review of the COS circuitry verified that they were subjected to the same excessive voltage issue. COS is presently in the process of preparing an MDR as defined in the following email extract below to remove and replace all existing SG1525A devices due to the potential for overstress:

Program: COS

Item: WA547971-500;      Description: PWA, LVPS #1

s/n 001 & 002 (to be confirmed)

The circuit configuration and component values on the flight boards have subjected the SG1525A Sync input to voltages as high as ~8V in short pulses. Nonetheless, the datasheet Absolute Max. limits digital inputs to 5.5V, maximum. This occurred, presumably, because the previous designer(s) considered this to be an Analog input which are spec'ed to handle up to the power supply rail voltage, as opposed to a Digital input that can handle only 5.5V, max.

James Simons contacted Texas Instruments Applications Engineering for clarification of a previous ambiguous response and learned this. Their 'official' response was that this input is considered Digital, and must be limited to 5.5V input voltage. At the time, our focus was to correct this new-found problem, so inadvertently delayed reporting this potential part overstress. It affects one part on the LVPS#1 boards, U9; both side 1 & 2.

U9 is item 115, part no. 532797-002, reference no. M38510/126C2BEA.

regards,  
Ken Albin  
Ball Aerospace & Technologies Corp.

In addition, Ball is in the process of generating EOs that will modify the external sync amplitude at the SG1525A in order to comply with the 5.5V absolute maximum limit. In

the same EO, Ball is working to ensure that the SG1525A external sync minimum pulse width recommendation of 300ns is met as well.

## **WFC3**

In light of the ACS Side 1 on-orbit anomaly and the previous two anomalies on STIS Side 1 and STIS Side 2 relating to power rail/supply concerns, the HST project decided to proactively change all WFC3 (and COS) Interpoint converters from the present MFL/883 type to a more reliable space qualified SMFL type (the STIS Repair Board was previously slated to be fabricated with the SMFL type parts already). Note that this action was taken independent of the ACS ARB activity, since the analysis does not point rigorously to one unique part as the certain cause of the problem. Refer to Attachment #7 for detailed differences between Interpoint MFL/883 devices and Interpoint SMFL devices and for a thorough explanation as to how the increase in reliability is achieved.

On WFC3, the hardware change that resulted from the ACS ARB findings were:

- Replacement of 200pF sync coupling capacitor to 470pF to address the SG1525A external sync pulse width.

HAR 2156 was opened to document the change. The resolution plan (part replacement) was HAR board approved, and then followed up with EOs on the relevant drawings and schematics. Then, SOWs were written for J&T to perform the work. Cert Logs were updated with the work performed. The HAR will be closed on conclusion of board and box-level tests.

Unlike ACS and COS, the WFC3 external sync signal was already fed by a +5V circuit, thus meeting the signal amplitude requirements of the SG 1525A. No further changes were required to comply with the amplitude requirement.

## **STIS**

The STIS Repair Board (STIS LVPS 2) was previously slated to be fabricated with the higher reliability SMFL Interpoint converter type parts. A review of the STIS LVPS 2 board has determined that it does not contain any SG1525A PWM devices, and therefore does not require further investigation with respect sync pulse width and amplitude.

The ARB did evaluate the circuitry that is located on the two remaining STIS LVPS boards presently on-orbit, namely STIS LVPS1 and STIS LVPS3. These two boards are not slated for replacement on the next servicing mission, as the STIS Side 2 failure was localized to be within an Interpoint MFL2805S/883 located on STIS LVPS2. The ACS ARB did determine that the STIS design does not utilize an SG1525A. However, the STIS LVPS3 board was found to utilize an earlier version of that PWM, namely an SG1524B.

The STIS SG1524B PWM external sync circuit, located on SC522951 sheet 3, is driven by a CMOS 4013 D-type flip-flop (U3) powered by +15V\_CEB. Since the SG1524B PWM device, like the SG1525A device, requires that the external sync amplitude to not

exceed 5.5V absolute maximum amplitude, the STIS design does possess the excessively high external sync signal amplitude issue.

The STIS SG1524B external sync pulse width is determined by a 47pF cap (C6) and a 1K (R1) to ground. An ap-note on the SG1524B was located and reviewed. The SG1524B ap-note recommends the external sync pulse width should be at least 200 nsec (100ns less than the minimum recommendation for the SG1525A device) for reliable synchronization. It also showed the equivalent circuit having a 3.2K resistor from pin 3 to ground inside the chip, which is different from the SG1525A. A PSpice analysis was executed using these parameters and showed the external sync pulse width to be 100 nsec at the 2.0 volt level. Therefore, according to the application note, the STIS SG1524B external sync pulse width is too short (100ns actual vs 200ns recommended) to provide reliable synchronization.

## ACS WFC Bias Offsets

During the course of the ACS ARB, ARB representatives from the Space Telescope Science Institute informed the ARB that ACS (on Side-2) is occasionally exhibiting seemingly random, low-level jumps in the WFC CCD bias levels recorded in full frame bias (zero second) images. These jumps manifest themselves as either discrete or smoothly varying changes in the bias level inferred when summing the bias levels of the individual WFC CCD columns, which are read out in parallel (see Figure 1 on page 62). The bias jumps can also be seen in the two-dimensional bias images if a hard stretch of the color scale is adopted (see Figure 2 on page 63). These bias offsets are small - typically less than 1 DN. In some cases, multiple bias offsets are present in the images. The bias offsets can also be seen in some (800-1000 second) dark images obtained for calibration purposes. Here again, the effect is subtle and most easily seen by collapsing the full frame. The ACS WFC bias offsets are orders of magnitude smaller than those recently identified for the WFPC2 WF4 detector.

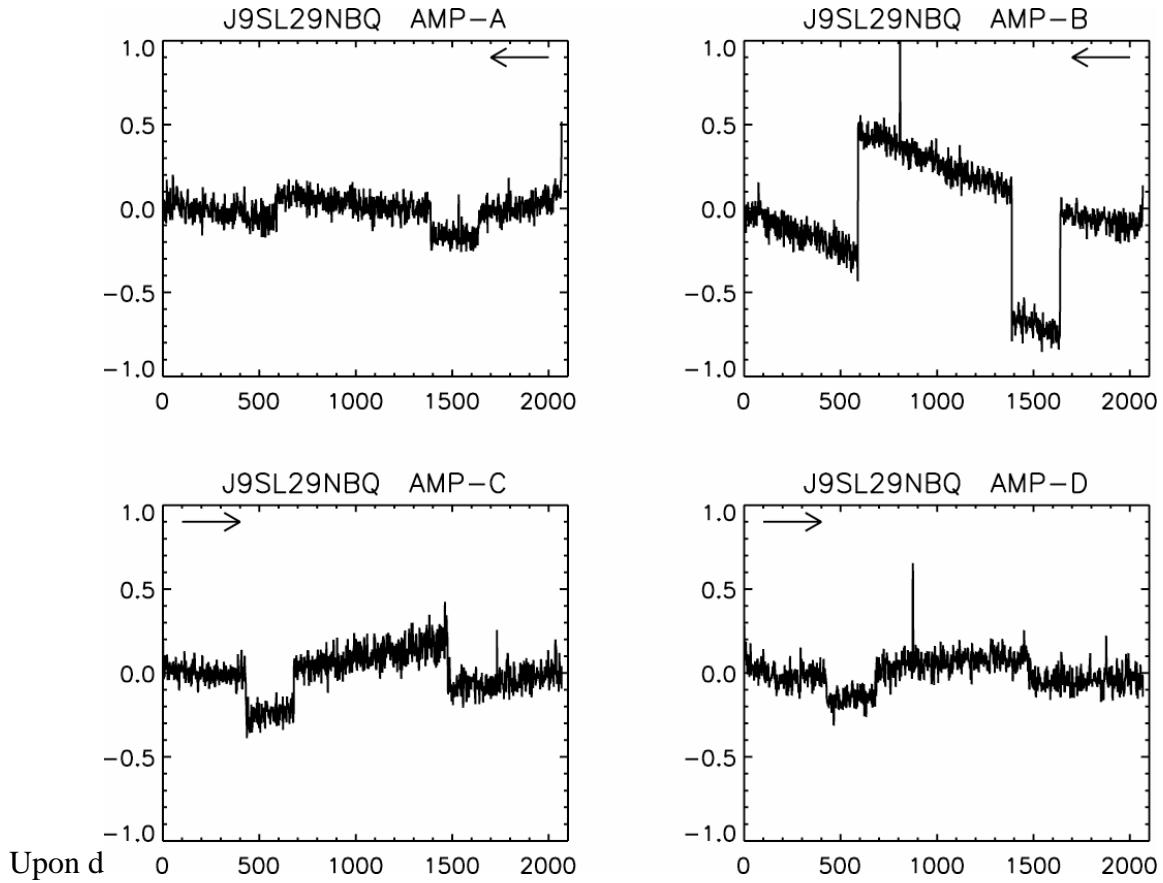


Figure 1: An example of a typical bias jump seen in ACS WFC data. The arrows at the top of each panel indicate the direction of the readout in each amplifier. Y-axis values are DN. X-axis values are pixels.

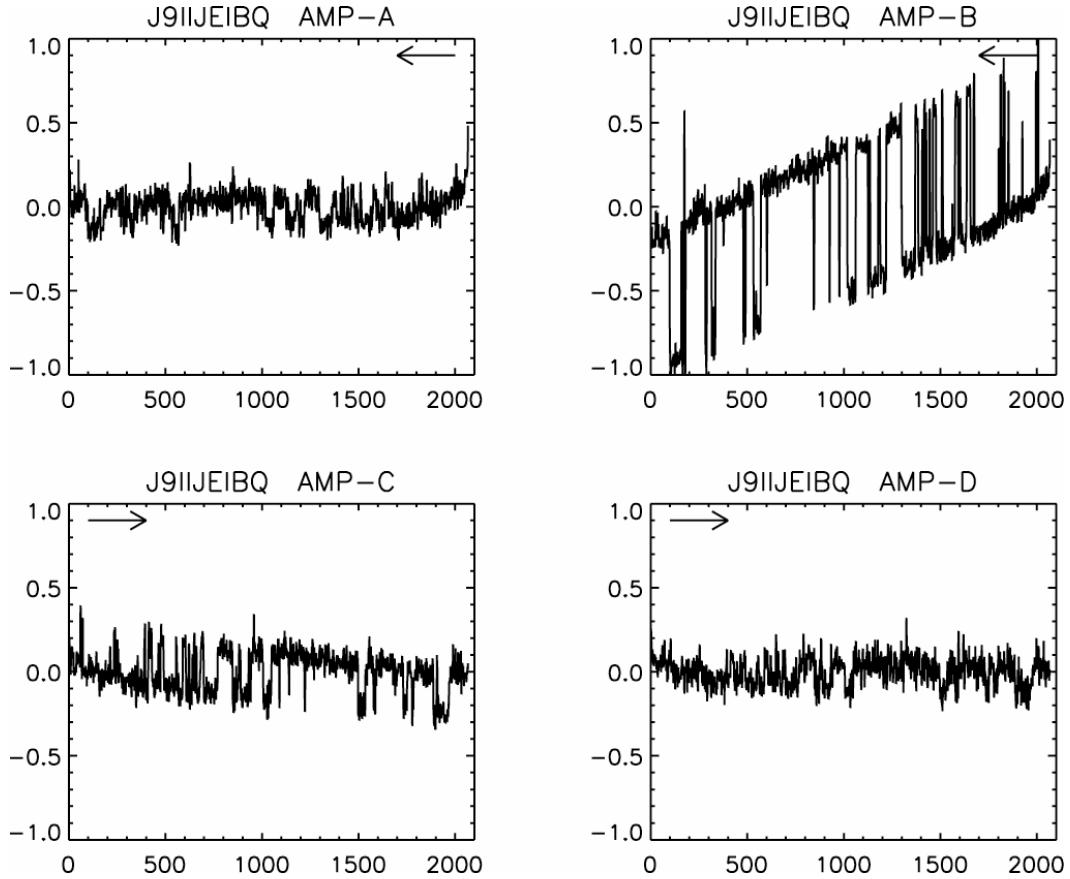
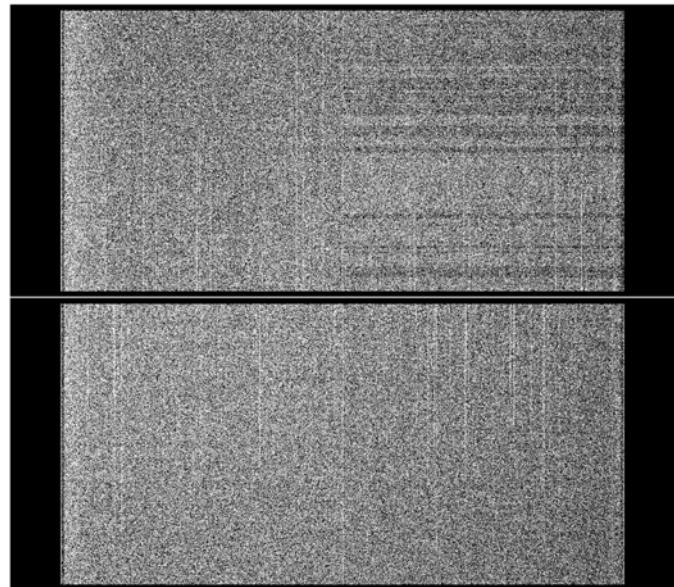


Figure 2: *Above:* An example of an atypical bias jump seen in ACS WFC data. The arrows at the top of each panel indicate the direction of the readout in each amplifier. Y-axis values are DN. X-axis values are pixels. *Below:* Two-dimensional image, with the grayscale stretched to show the bias jumps. Orientation of amplifiers (clockwise from upper left) is A, B, D, C.



Upon delving more deeply into this issue, the ACS Team at STScI found that similar jumps also occasionally occurred within the bias images obtained previously on ACS Side-1. Looking back to June 1, 2005, they noted that 20 out of 917 Side-1 bias images (~2.2%) contained these types of bias offsets. This can be compared to a total of 11 out of the 47 bias images examined for ACS Side-2 through July 28, 2006 (or ~23%, a factor of ten higher frequency of occurrence than Side-1). Qualitatively, the bias jumps on both Side-1 and Side-2 look similar. In most cases, the bias jumps on either side are most pronounced in the data read out through WFC amplifier B. However, the jumps are often seen in multiple amplifiers, and are sometimes obvious in all four amplifiers. They occur simultaneously when they are present in more than one amplifier. There does not appear to be a strong dependence of the frequency of bias offset occurrence upon the gain of the readout.

Bias offsets have not been detected in data obtained with the HRC CCD, either on Side-1 or Side-2. It is more difficult to detect subtle effects like this with the HRC since the CCD is smaller (fewer columns to sum) and only one amplifier per readout. Still, offsets of the type and magnitude of those seen for the WFC would have been detectable in HRC data had they been present.

The small WFC bias offsets must either be corrected, or the images removed, when constructing the ACS “superdark” and “superbias” reference frames used in the ACS data calibration pipeline to avoid introducing the imprint of the offsets into the calibrated science data. There is a straight-forward process for doing so that the STScI ACS Team employs. However, it is quite likely that offsets such as these are occasionally present in the raw science data collected.

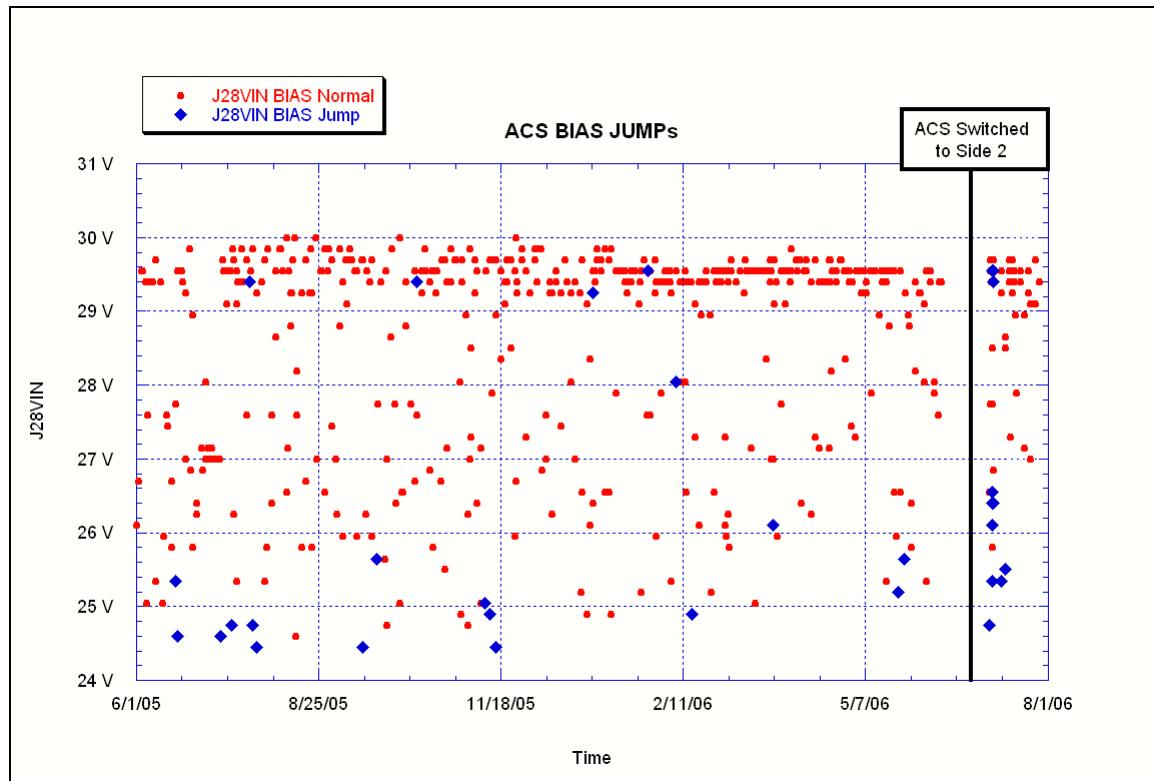
**At their current levels, the bias offsets do not significantly affect the quality of the science data for several reasons:**

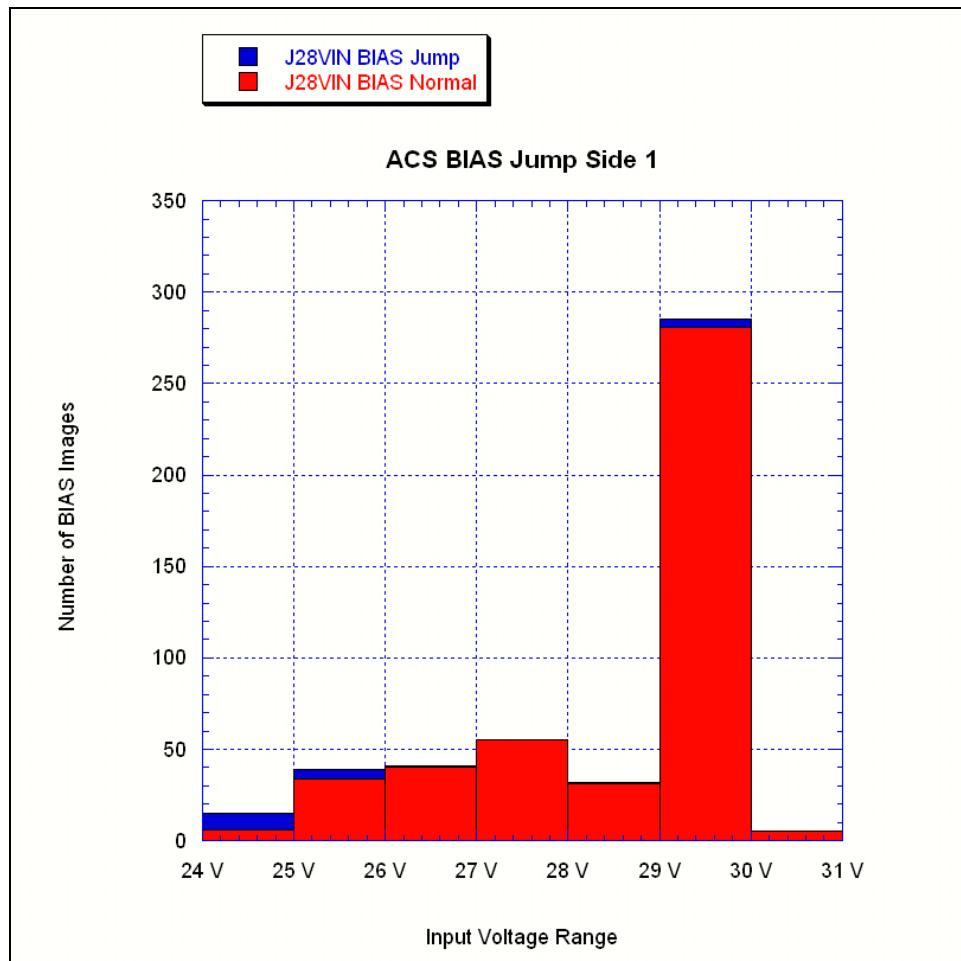
- 1) The current offsets are small (<1 DN), so they would contribute significantly to the image noise only for science programs interested in detecting very faint objects in deep ACS exposures. Other sources of noise dominate.
- 2) The offsets appear to be random, at least as far as the science observation is concerned. Programs designed to detect faint objects typically take many (often dozens of) exposures to achieve their desired sensitivity. Thus, the noise contribution of the offsets in individual images is reduced accordingly in the summed image used to study faint objects.

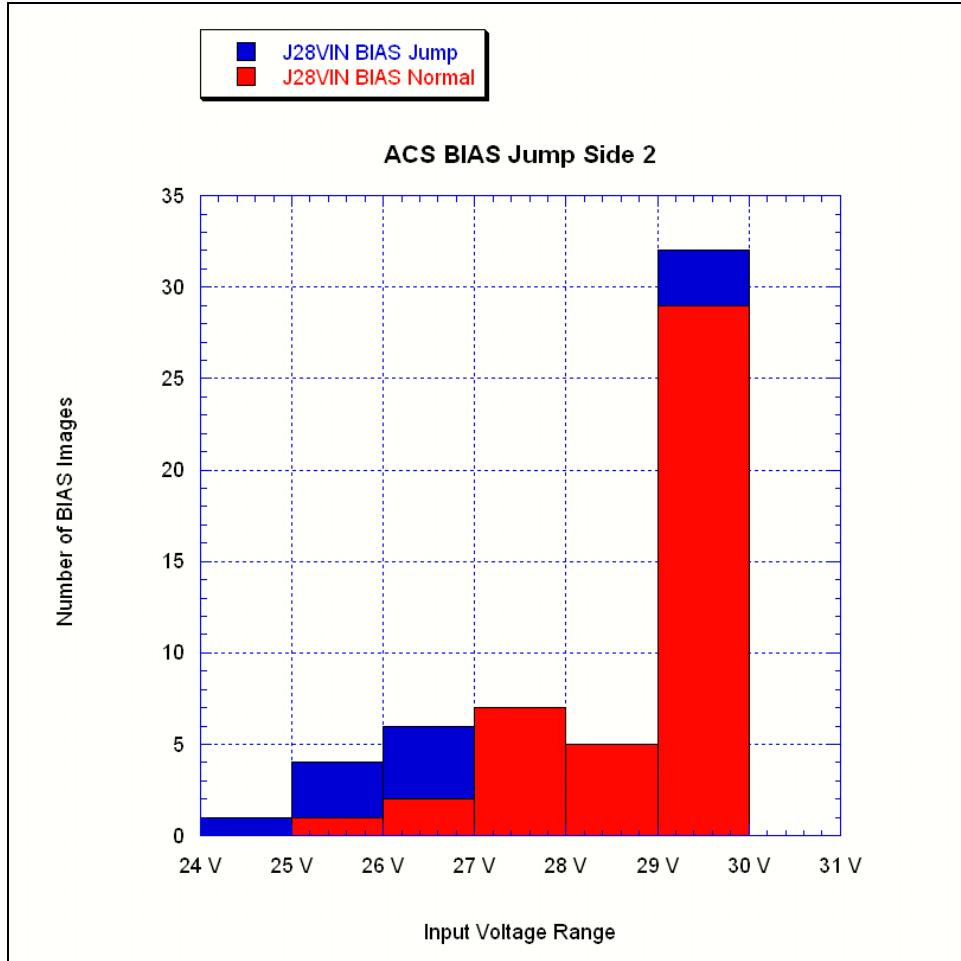
The ARB attempted to explore the possibility that the ACS WFC noise issue could possibly be a secondary effect of the previously raised concern related to the +35V ACS Pulse Width Modulator SG1525A circuit synchronization. This theory assumes that occasional unstable synchronization of the SG1525A results in double clocking of the PWM output FETs, which ultimately results in voltage ripple on the +35V bus to the CEBs resulting in image bias noise during readout. An attempt to provide evidence that

would corroborate the possibility of this theory was conducted using the VSTIF ACS Test bench. The test, executed at ambient conditions, did not produce double clocking results. Refer to Additional Design Issues and Concerns on page 57 of this report for more details.

Efforts are presently underway to determine the cause of these bias offsets. A preliminary examination of the ACS +28V bus timeline shows that the bias offsets tend to occur preferentially when the bus voltage is low (+24V to +27V). Only two of the Side-2 events and five of the Side-1 events occurred when the voltage was +28V or higher. The ACS Team will continue to monitor the bias jump frequency and level to be sure that they remain within acceptable ranges.







## Operational Recommendations

In considering operational responses to the ACS ARB findings, the ARB recommends two additional areas of investigation.

1. In current ACS operations, the HRC is powered off when the SBC is powered. Reducing power cycles of the HRC CEB may minimize potential power converter aging and stress due to thermal cycling. Leaving the HRC CEB on when the SBC is on could have thermal and power implications that require further investigation. The reduced number of cycles would be minimal as the SBC observations only account for about 10% of the total ACS observations in Cycle 15. The ARB recommends that this be studied as part of the ACS Hybrid LEI task.
2. Additional thermal and power cycling occurs on ACS during the monthly Anneal cycles. The ARB recommends two additional investigations for reducing power cycles during Anneals.

- a. Reduce the frequency of anneals. Currently, anneals are done monthly. With the new lower WFC TEC set point, the WFC anneals could be reduced with no adverse affects. The HRC anneals, however, are still required monthly. It might be possible to reduce the HRC anneals if the HRC TEC point is lowered. The frequency of anneals is not anticipated to increase over time. The ARB recommends that the STScI ACS Team evaluate the possibility of reducing the frequency of anneals.
- b. Under current operations, the LVPS board temperatures drop about 30 degC during an Anneal cycle. These temperature swings can be reduced to about 5 to 10 degC by doing the Anneal using the Side-1 Hold and Anneal relays, which are still functioning. This “hybrid” Anneal mode would consist of:
  - Leave most ACS Side-2 relays closed
  - Turn off the TECs on Side-2
  - Close the Side-1 Hold and Anneal relays

This mode would increase the net power load on HST, but reduce ACS Side-2 thermal and power swings. There are thermal and power implications that require further study. In addition, the NSSC-I safing and limit check tables would need modification since the relay configuration is not deemed by NSSC-I FSW to be a valid configuration. The ARB recommends that this be studied as part of the ACS Hybrid LEI task.

Finally, the ARB has not identified any operational workarounds related to the SG1525A PWM external synchronization pulse width and amplitude failing to meet recommendations. The susceptibility to synchronization problems might occur any time the CEB power is on. The ARB cannot determine the long-term risk associated with this specification discrepancy. Further evaluation of this risk would require comprehensive engineering tests that are beyond the scope of the ARB.

## Conclusion

The ARB has concluded that the most likely cause of the ACS Side 1 on-orbit anomaly was a result of the loss of the ACS Side 1 CEB +15V power rail in either an open or shorted condition. This conclusion is substantiated via engineering evaluations, focused ground tests, historical performance, and on-orbit telemetry collected at the time of the anomaly.

The following facts have been concluded based on on-orbit data at the time of the anomaly:

1. All CEB telemetry collected by the Normal Engineering Data (NED) task went from valid data to all ones within one sample period.
2. No indication of anomalous secondary voltages prior to ACS Suspend
3. No indication of thermal rise prior to and following the anomaly
4. Anomaly nearly instantaneous; occurred within 100 ms window
5. +28V Bus current decreased on the order of 0.8 Amps to 1.3 Amps as a function of the anomaly

6. No out-of-family behavior was observed in the science data prior to the Suspend event.

The LVPS Board #3 S/N 001 has been identified as **most likely location of** the cause of the ACS on-orbit anomaly since it contains all of the active components that produce or interface with the suspected +15V CEB power rail. However, it is also possible that a +15V trace to ground or +15V wire short to ground fault may have occurred on the MEB Backplane or in the MEB to CEB harnessing respectively.

The following conclusions have been derived as a function of ground testing:

1. Ground testing verified loss of +15V rail and resulting variations of -15V rail would match the on-orbit signature.
2. The CEB MFL2815D was not inhibited on-orbit by the anomaly
3. The CEB MFL2815D did not fail in such a way that caused the primary input side to fuse open at the internal bond wires. In other words, the MFL2815D had to still be functioning in some capacity with respect to the -15V rail in order for the Engineering CEB to replicate the on-orbit scenario.
4. A short or open of either the CEB MFL2815D +15V or -15V outputs would result in a decrease in converter input current.

A thorough component-level Failure Mode Evaluation and Analysis (FMEA) was conducted by the ARB on the ACS LVPS3 Board circuitry related to the +/-15V CEB power rails. The FMEA evaluated each component connected to the +/-15V CEB power rails and determined the associated response based on postulated credible fault modes, such as shorts or opens. The FMEA resultant responses were then compared to a set of voltage rail responses obtained via CEB Engineering Unit lab tests to determine if the postulated failure mode could have resulted in the ACS on-orbit anomaly. Based on the FMEA results, fourteen ACS LVPS3 board parts (comprised of nine distinct part types) and associated failure modes have been identified as possibly resulting in the ACS on-orbit anomaly.

After analyzing the fourteen suspect parts identified in Table 1 on page 45, the GSFC Parts Branch provided this assessment:

The most likely cause of the ACS failure resides within LVPS Board #3, component U2-7, the MFL2815D Interpoint DC-DC converter. The next most likely cause is a short to ground in the transformer T6 on the same LVPS board.

## ***Summary of Additional Concerns and Findings***

A number of concerns were identified by the ARB:

1. Quality record review
  - a. Identified an MEB level thermal cycle test failure that matched the on-orbit failure scenario exactly. A short occurred on the +15V rail at the +35V T6 step-up transformer.
    - i. The ARB was concerned to find that after the initial replacement of transformer T6, the anomaly again repeated with the new transformer during re-testing with no further part removal and replacement. The ARB has concluded that unaided visual inspection of the transformer's exterior is insufficient to determine if the internal wiring insulation of the transformer was subjected to stress that may have eventually resulted in a latent-type anomaly on orbit. However, the ARB has no way to determine quantitatively what potential stress and possible latent damage may have occurred within the T6 transformer over the 3 minutes of heating that it was subjected to during the re-test.
    - ii. The ARB was concerned to find that the flight LVPS3 board was subjected to uncontrolled heating effects by a heat gun as part of the anomaly investigation. It is conceivable that this anomaly investigation technique produced thermal stresses that resulted in a latent failure on the flight LVPS3 board in question.
  - b. Ball Material Discrepancy Report (MDR) A92295, identified a PWB defect around rivets associated with LVPS3 S/N 001. Nut plates were warped slightly and the board had separated between the Ground/Thermal Plane and the fiberglass board. The ARB cannot help but wonder if a Ground/Thermal Plane to fiberglass board separation could have occurred that ultimately led to a shorting condition or a stressed component solder joint that resulted in the ACS on-orbit anomaly. Such separation could have been aggravated by thermal transitions. For example, ACS is powered down approximately once every month to perform anneal operations, at which time the LVPS board temperatures transition approximately 30 degrees with the current 6-hour anneals.

A detailed ARB review of the U5 SG1525A Pulse Width Modulator implementation in the ACS LVPS3 circuit identified two concerns related to the external synchronization signal input. The SG1525A external sync signal amplitude was found to exceed the vendor's specification. In addition, the external sync signal pulse width was found to not meet the minimum recommended pulse width to ensure reliable external synchronization of the SG1525A. Unreliable synchronization could result in a double pulse condition to the PWM output FETS, resulting in extra long "On" periods that allow the T6 transformer core to saturate, resulting in a large increase in current through the transformer windings which could eventually lead to the destruction of the transformer. The COS, WFC3, and STIS designs were thoroughly evaluated with respect to the SG1525A findings.

## ***Summary of ARB Recommendations***

The ARB has made the following recommendations:

- Modify ACS flight software so the NED history buffer contains 16-bit values exactly as read from the A/D FIFOs. Specifically, do not apply a bit-mask to the data prior to storage in the buffer. Storing the data in an unmodified form would allow better insight into the MEB/CEB interface. Make similar flight software changes to COS and WFC3. (NICMOS and STIS do not have NED history buffers.)
- New CARD items should be written to prevent invalid “hybrid” power configurations. These include:
  - ACS only: prevent commanding of the “off” CEB
  - ACS and STIS: prevent hot switching the CEB internal relays.
- Investigate reducing thermal and power cycling by:
  - Leaving the HRC CEB powered on while doing SBC operations.
  - Reducing the number of anneals
  - Performing anneals in a “hybrid” mode that would leave Side-2 electronics powered while annealing from Side-1

Investigations have been referred to the Hybrid LEI Task and the STScI ACS Team.



## **Attachment 1: ARB Charter**



June 21, 2006

440

TO: Distribution  
FROM: 440/Associate Director for Astrophysics Division  
SUBJECT: Formation of an Anomaly Review Board (ARB) to Investigate Advanced Camera for Surveys (ACS) June 19, 2006 Suspend Event

At 170/17:15:19 (June 19, 2006), all 158 CCD Electronics Box (CEB) engineering telemetry parameters stepped to saturation (observed via dump of the Normal Engineering Data (NED) history buffer). The ACS flight software suspended the instrument at 17:15:26.368 after three out of limit samples of the 36 limit checked parameters were registered.

The ARB formed herewith is requested to address the following objectives:

1. Assess the risks and benefits of diagnostic flight testing of ACS.
2. If possible, identify the reason for the saturation of the CEB parameters.
3. Assess whether the anomaly stressed any of the ACS components.
4. Assess the risks, if any, of operating ACS on Side 2.
5. Determine if the cause of the ACS anomaly is a failure mode that is present in any of the other HST instruments, especially COS and WFC3.

The members of this ARB are identified below. The membership may be adjusted at the discretion of the chairperson:

Roger Chie, Chairperson	LMTO/Code 442
Randy Stevens, Secretary	LM IS&S/Code 441
Steve Arslanian	HTSI/Code 441
Wilbur (Dale) Brigham	Code 563
Ken Carpenter	Code 667/441
Ed Cheung	J&T/Code 442
Randy Kimble	Code 667/442
Olivia Lupie	Code 581/441
Mal Niedner	Code 667/440
Mike Prior	Code 441
Art Rankin	J&T/Code 441
Tim Schoeneweis	BATC
Ken Sembach	STScI
Beverly Serrano	RSTX/Code 441
Noman Siddiqi	QSS/Code 562
Hsiao Smith	Code 442
Renee Taylor	Code 303/442
Tom Wheeler	STScI

The ARB shall present findings and recommendations to the project for each objective area as soon as results become available. The ARB shall complete the investigation and present the final report to the HST Project no later than July 24, 2006.

Preston Burch

Distribution:

ARB Members

cc:

300/Mr. M. Watkins  
400/Mr. A. Obenschain  
400/Mr. G. Morrow  
400/Mr. J. Greaves  
400/Ms. S. Cauffman  
440/Mr. E. Ruitberg  
440/Mr. M. Weiss  
440/Dr. A. Whipple  
440/Dr. D. Leckrone  
441/Mr. M. Ahmed  
441/Dr. K. Kalinowski  
441/Mr. M. Prior  
442/Mr. F. Cepollina  
442/Mr. M. Kienlen  
500/Mr. O. Figueroa  
500/Mr. S. Scott  
560/Mr. J. Day  
563/Mr. T. Yi  
600/Dr. L. Leshin  
LMTO/Mr. D. Connolly  
LMTO/Mr. T. Cruz  
Vantage Systems Inc./Mr. L. Dunham  
STScI/Dr. M. Mountain  
STScI/Dr. R. Doxsey

## **Attachment 2: ACS Side-1 Test Proposal Meeting Charts**





## ACS Side-1 Test Proposal Meeting

**July 13, 2006**  
1:00 pm EDT B3/S107A



## ACS Side-1 Test Proposal Meeting



### Agenda

Introduction

(R. Chiei)

Test Plan and Schedule

(R. Stevens)

Benefits of Testing

(R. Chiei)

Risks of Testing

(R. Chiei)

ARB Recommendation

(R. Chiei)



## ACS Side-1 Test Proposal Meeting



### Introduction

- Meeting Purpose
  - Discuss proposal for ACS Side 1 Testing
- ARB Charter identifies the following objectives that are related to a potential ACS Side 1 Test:
  - Assess risks and benefits of diagnostic flight testing of ACS
    - » Completed: Risk and benefit of executing an ACS side 1 test are addressed in this presentation
  - If possible, identify the reason for the saturation of CEB parameters
    - » To be Completed: Additional data obtained from an ACS Side 1 test would aid the ARB in more accurately identifying the root cause of the anomaly through process of elimination
  - Assess whether the anomaly stressed any of the ACS components
    - » To be Completed: Same as above
  - Determine if the cause of the ACS anomaly is a failure mode that is present in any of the other HST instruments, especially COS and WFC3
    - » To be Completed: Additional data obtained from an ACS Side 1 test would aid the ARB in more accurately identifying the root cause of the anomaly through process of elimination. Most likely Root cause will then be evaluated with regard to applicability to COS and WFC3.

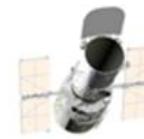
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## ACS Side-1 Test Proposal Meeting

### Introduction

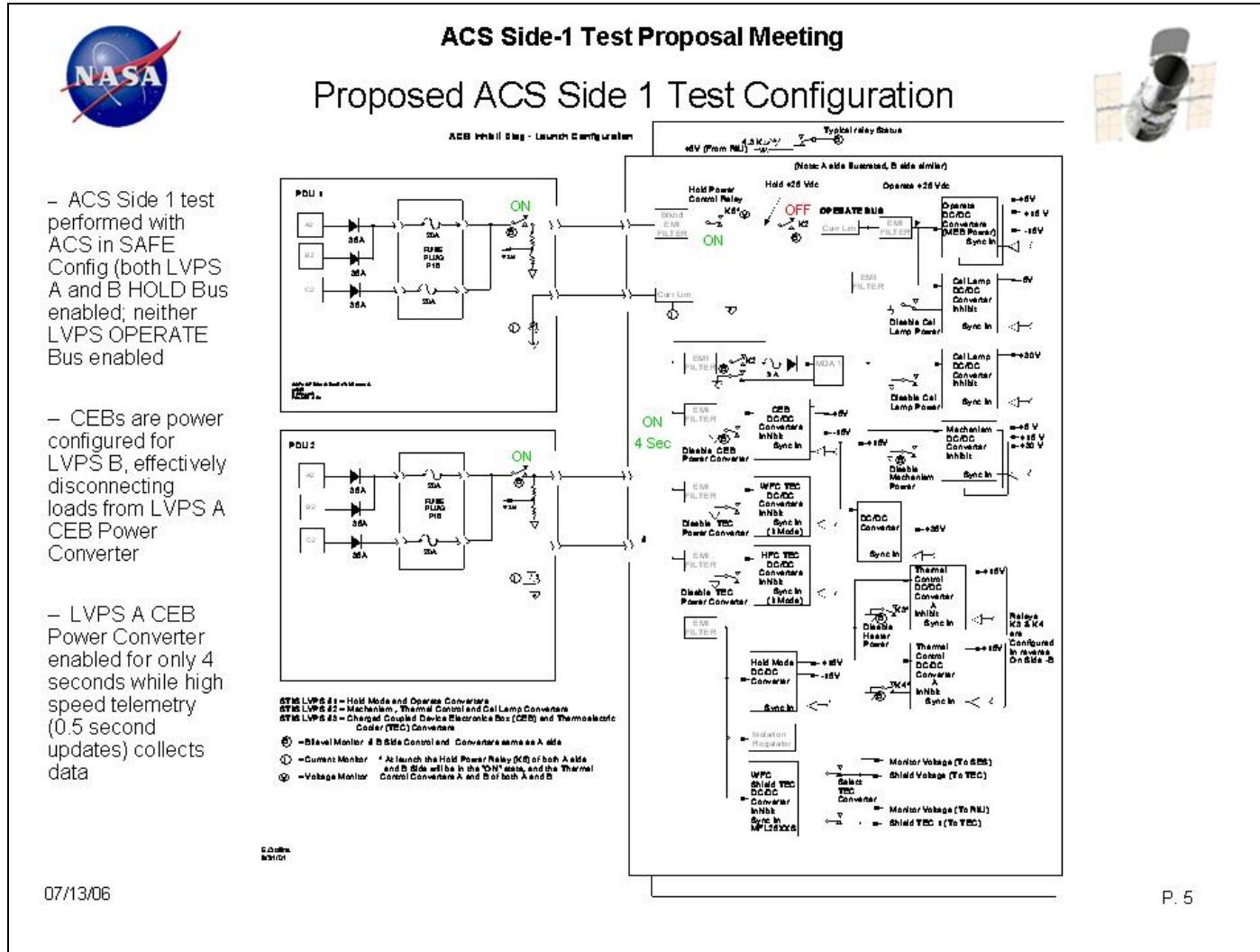


- ACS Hardware Status Update

- Successful switch to ACS Side 2 operations has eliminated the ACS CEBs (both HRC and WFC CEBs) as a potential root cause anomaly fault site
  - LVPS #3 (and associated MFL2815D CEB power converter), MEB mother board, and MEB to CEB harness remain as possible root cause fault sites
- ARB has completed an evaluation of CEB 'Hybrid' power mode operation
  - CEBs can and are configured with all +15V, -15V and +35V inputs opened via relays on CEB boards, yet still allow +5V input power onto CEB Timing Board
  - ARB and Ball personnel performed an in depth analysis and concluded no safety concerns exist
    - CEB Timing board Power-on Reset (POR) ensures Timing Board output drivers are configured in a tri-stated High-Z mode. This safe configuration is maintained until CEB is commanded by MEB to begin executing timing profiles
    - ARB has requested the addition of two CARD items
      - Prevent commanding of the 'off' CEB
      - Prevent hot switching of CEB power configuration relays
  - CEB 'Hybrid' power mode now deemed safe; moratorium on SBC activities was lifted on 7/6/06
  - CEB 'off' power configuration can now be proposed for ACS Side 1 testing

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## ACS Side-1 Test Proposal Meeting



### Test Plan and Schedule

#### Test Overview

- ☒ HST String Configuration
  - ☒ Transition to Safe (Side-2) via SMS.
  - ☒ Reconfigure NSSC-I telemetry collection
  - ☒ Close the Side-1 CEB relay
  - ☒ Restore NSSC-I telemetry collection
  - ☒ Recover from Safe (Side-2) via SMS
- Total test time < 1 hour

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## ACS Side-1 Test Proposal Meeting



### Test Plan and Schedule

#### HST String Configuration

- ☒ Commanding would be done on an Operational String
  - No changes required to operational database to support new telemetry
  - Quick update CCLs to improve commanding efficiency and accuracy
  - New faster telemetry data can be obtained in raw format – 30-day archive available in raw format
- ☒ Monitoring of new telemetry would be done on Test String
  - New mnemonics for faster telemetry built into a test database
  - Allows calibrated values to be extracted and plotted.
  - Data available on that string even after test database has been switched out

#### Transition to Safe (Side-2) via SMS

- Standard reconfiguration transition
- Planned during non-ACS proposals (non-interference)
  - » GO Proposal 10538 – 14 SAA-free orbits



## ACS Side-1 Test Proposal Meeting



### Test Plan and Schedule

#### Reconfigure NSSC-I Telemetry Collection

- ☒ 10 bytes of telemetry are downlinked for ACS every 0.5 seconds
  - 2 bytes externally subcommutated data – “RIU Direct”
  - 1 byte of NSSC-I generated data
  - 7 bytes of internally subcommutated data – contains data read from MEB flight software
- ☒ Since MEBs are off in Safe mode, we would “steal” the 7 bytes of internally subcommutated data and replace them with the following:
  - J5VCEB1
  - J15VCEB1
  - JM15VCEB1
  - J35VCEB1
  - JTOTALI1
  - J28VIN1
  - JCEBPWR1 (and associated bi-levels)

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## ACS Side-1 Test Proposal Meeting



### Test Plan and Schedule

#### Reconfigure NSSC-I Telemetry Collection (continued)

- ☒ Establish memory monitors
  - View Engineering Data Request Buffer prior to patching with new telemetry addresses
  - Confirm expected, nominal values for telemetry addresses
- ☒ Execute patches to Engineering Data Request Buffer via quick-updated CCL
  - CCL ensures that patches are exactly as tested
- ☒ Patches confirmed
  - Via memory monitors (Ops and Test String)
  - Via new telemetry (Test String)

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## ACS Side-1 Test Proposal Meeting



### Test Plan and Schedule

#### Close the Side-1 CEB Relay

- ¤ Relay commanding would be done via an RTCS
  - Ensures accurate timing of relay closure: 4 seconds
  - Ensures relay would be commanded open, even if communications is lost
- ¤ RTCS Overview
  - Command all internal CEB relays to point to Side-2
    - » Ensures Unloaded Side-1
    - » Should already be in this state from Safing
  - Close the Side-1 CEB relay
  - Wait 4 seconds
    - » To allow telemetry sampling
  - Open the Side-1 CEB relay

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## ACS Side-1 Test Proposal Meeting



### Test Plan and Schedule

#### Restore NSSC-I Telemetry Collection

- ☒ Execute patches to restore Engineering Data Request Buffer via quick-updated CCL
  - CCL ensures that patches are exactly as tested
  - Restores the 7 locations back to their internally subcommutated values for collecting data from the MEB
- ☒ Patches confirmed
  - Via memory monitors (Ops and Test String)
  - Via new telemetry (Test String)

#### Recover from Safe (Side-2) via SMS

- Standard SMS transition



## ACS Side-1 Test Proposal Meeting

### Test Plan and Schedule



#### Post-Test Analysis

- ☒ Capture extractions and plots from Test String
- ☒ If required, archive CCS raw telemetry archives for the time the relay was closed.

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## ACS Side-1 Test Proposal Meeting



### Test Plan and Schedule

#### Schedule

- ☒ July 10: proof of concept demonstrated in ESTIF
- ☒ July 11: requirements for RTCS specified to ST Scl
- ☒ July 14-19: Dry runs in VEST
- ☒ July 18: Ops Acceptance Test script review
- ☒ July 20: Cut-off day for SMS212
- ☒ July 20: Ops Acceptance Test
- ☒ July 21: Ops Acceptance Test backup day
- ☒ July 26: pre-FRR
- ☒ July 28: FRR
- ☒ July 31: Beginning of SMS212 containing large non-ACS proposal (GO10538)
- ☒ July 31 or August 4: execute on-orbit test (depends on scheduling)
- ☒ August 1-3: Battery Capacity Test
- ☒ August 7-13: next planned Anneal (SMS219)

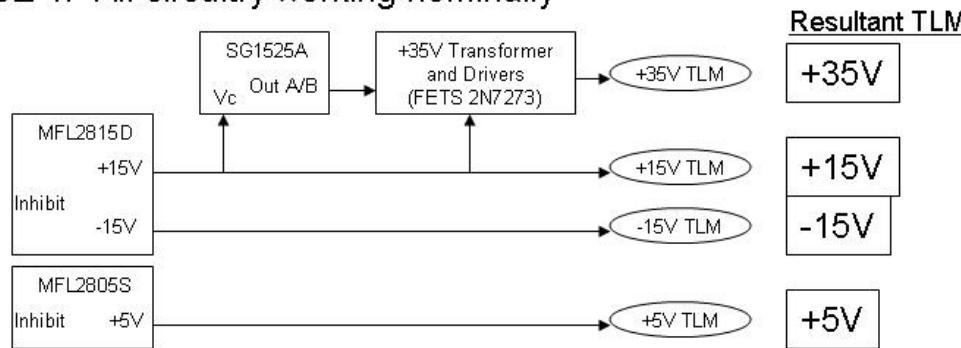


## ACS Side-1 Test Proposal Meeting



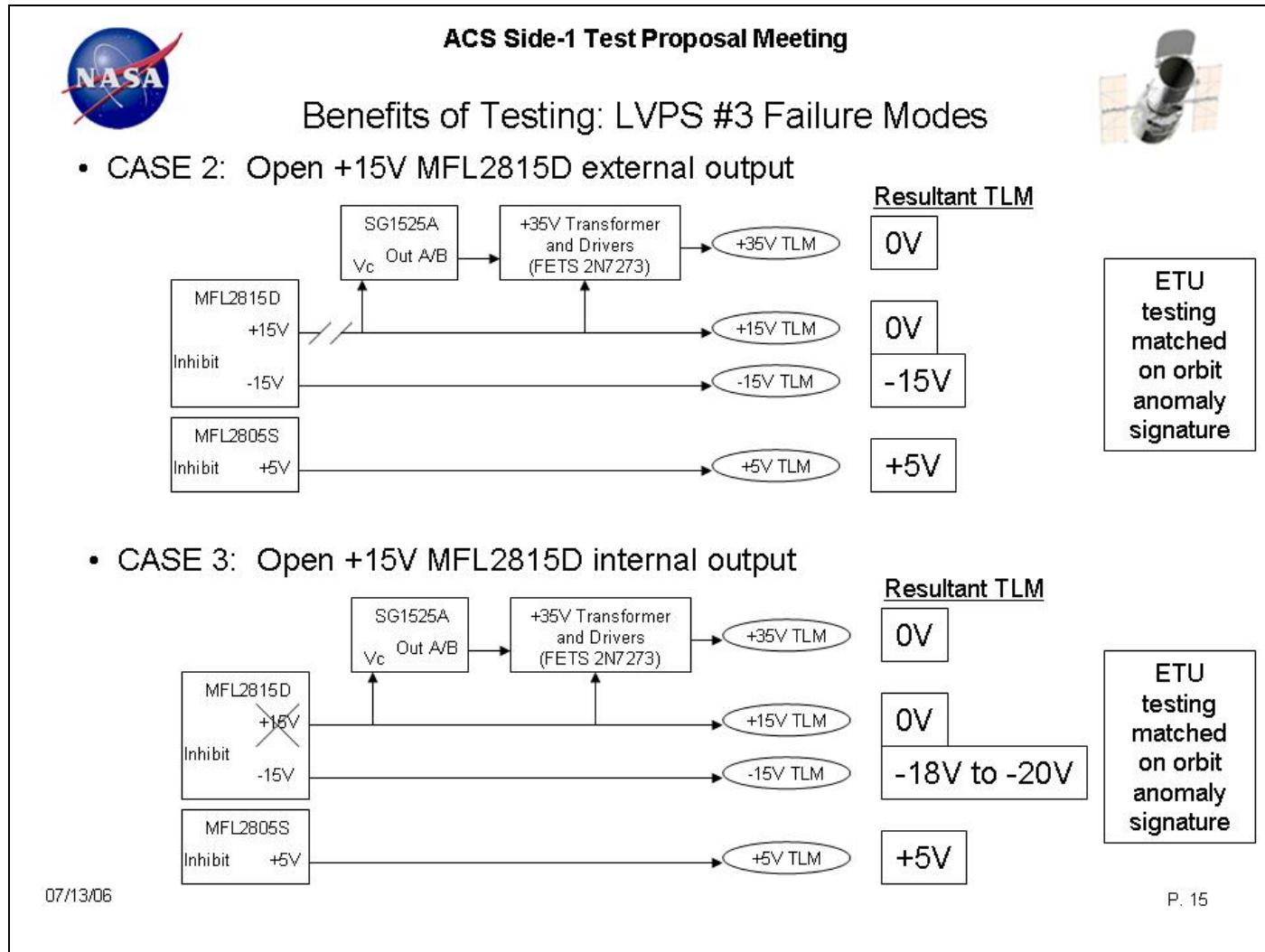
### Benefits of Testing: LVPS #3 Failure Modes

- Enabling ACS Side 1 CEB power converters will provide a definitive set of resultant telemetry responses
  - Resultant telemetry response is dependant on fault mode
  - Aids the ARB in more accurately identifying the root cause of the anomaly
- Nine fault mode Cases with associated Resultant Telemetry have been defined
  - Assumes +15V, -15V, and +35V CEB loads are disconnected in compliance with the proposed Side 1 Test configuration
- CASE 1: All circuitry working nominally



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**ACS Side-1 Test Proposal Meeting**

**Benefits of Testing: LVPS #3 Failure Modes**

**• CASE 4: Open -15V MFL2815D external output**

The diagram illustrates the power supply architecture for Case 4. It shows the MFL2815D and MFL2805S power modules, their respective inhibit signals, and the connections to the SG1525A voltage controller and the +35V Transformer and Drivers (FETS 2N7273). The resulting TLM values are listed on the right.

Resultant TLM
+35V
+15V
0V
+5V

**• CASE 5: Open -15V MFL2815D internal output**

The diagram illustrates the power supply architecture for Case 5, similar to Case 4 but with a crossed-out -15V connection from the MFL2815D module. The resulting TLM values are listed on the right.

Resultant TLM
+35V
+15V
0V
+5V

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**ACS Side-1 Test Proposal Meeting**

**Benefits of Testing: LVPS #3 Failure Modes**

• CASE 6: Shorted +15V MFL2815D output (internal or external)

The diagram shows the power supply architecture. On the left, there is a box labeled "MFL2815D" with "+15V" and "-15V" outputs, and an "Inhibit" input. This connects to a "SG1525A" chip, which has an "Out A/B" output. This output goes to a "Transformer and Drivers (FETS 2N7273)" stage, which then provides three types of TLM signals: "+35V TLM", "+15V TLM", and "-15V TLM". On the right, these TLM signals are mapped to "Resultant TLM" values: "+35V TLM" maps to "0V", "+15V TLM" maps to "0V", and "-15V TLM" maps to "-6V to -8V". Below the main stage, there is another "MFL2805S" component with an "Inhibit" input and a "+5V" output, which also provides a "+5V TLM" signal. A callout box on the right states "ETU testing matched on orbit anomaly signature".

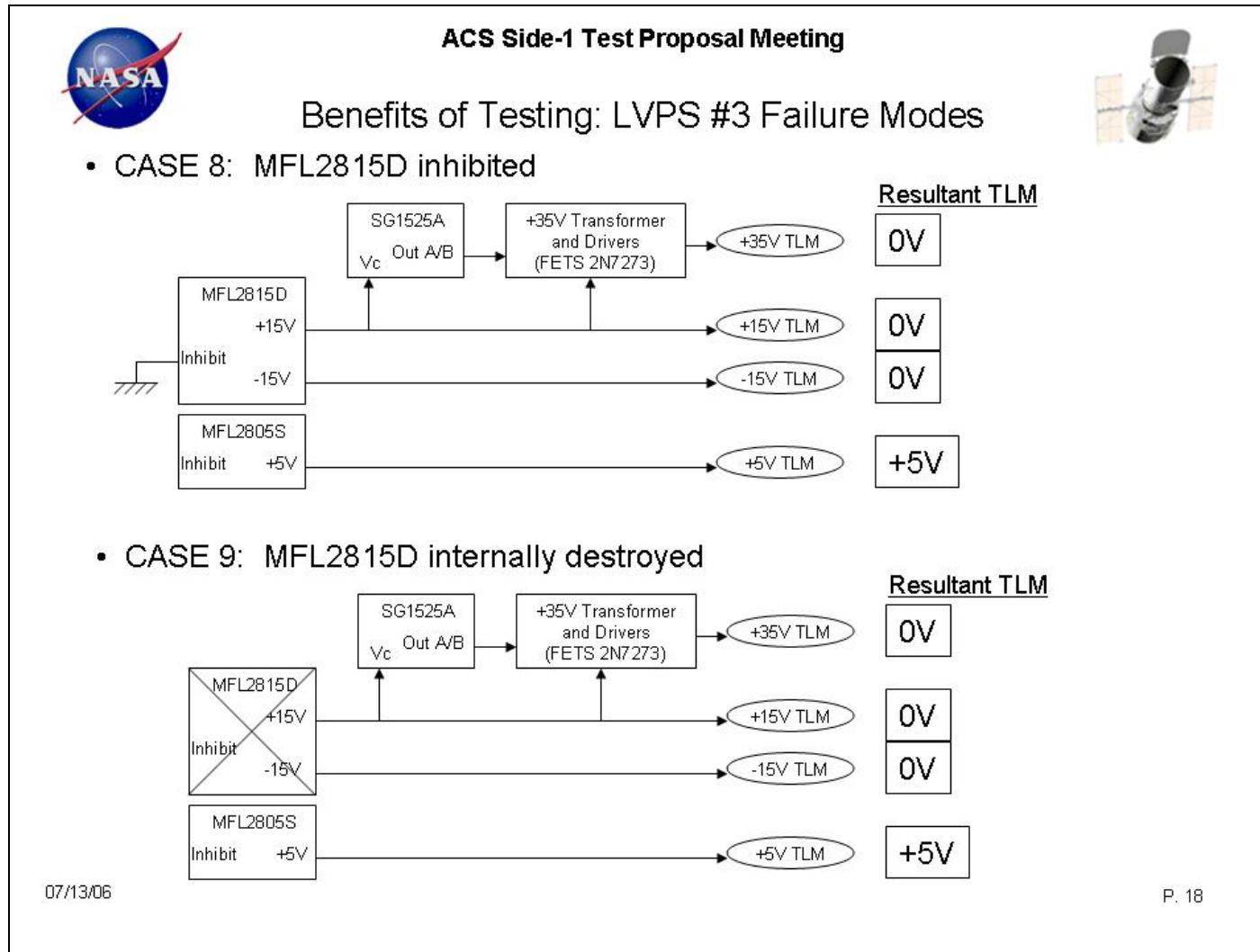
Resultant TLM
0V
0V
-6V to -8V
+5V

• CASE 7: Shorted -15V MFL2815D output (internal or external)

The diagram is similar to Case 6 but with different voltage assignments. The "MFL2815D" component now has "+15V" and "-15V" inputs, and its "Inhibit" output connects to the "SG1525A" chip. The "SG1525A" chip's "Out A/B" output goes to the "Transformer and Drivers (FETS 2N7273)" stage, which provides three types of TLM signals: "+35V TLM", "+15V TLM", and "-15V TLM". The resulting "Resultant TLM" values are: "+35V TLM" maps to "+30V to +35V", "+15V TLM" maps to "+8V to +11V", and "-15V TLM" maps to "0V". The "MFL2805S" component remains the same, providing a "+5V TLM" signal.

Resultant TLM
+30V to +35V
+8V to +11V
0V
+5V

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**ACS Side-1 Test Proposal Meeting**

**Benefits of Testing: Fault Response Summary Table**




Case #	Failure Mode	Anomaly match based on ETU testing	Implicates	Expected Telemetry			
				+5V	+15V	-15V	+35V
1	All Nominal	no	Problem intermittent or +15V open beyond TLM sample point	+5V	+15V	-15V	+35V
2	+15V open (external)	YES	LVPS #3 Board	+5V	0V	-15V	0V
3	+15V open (internal)	YES	MFL2815D	+5V	0V	-18V to -20V	0V
4 or 5	-15V open (external or internal)	no	MFL2815D or LVPS #3	+5V	+15V	0V	+35V
6	+15V shorted (internal or external)	YES	MFL2815D or LVPS #3 or MEB Backplane or Harness to CEBs	+5V	0V	-6V to -8V	0V
7	-15V shorted (internal or external)	no	MFL2815D or LVPS #3 or MEB Backplane or Harness to CEBs	+5V	+8V to +11V	0V	+30V to +35V
8 or 9	MFL2815D inhibited or internally destroyed	no (additional testing in progress)	MFL2815D	+5V	0V	0V	0V

 Fault within MFL2815D  
 Fault on LVPS #3 Bd, not in MFL2815D      P. 19  
 Fault mode matches on orbit Anomaly signature

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## ACS Side-1 Test Proposal Meeting

### Risk Assessment: Remaining ACS Resources



- Many possible combinations of ACS Side-1 and Side-2 assets are possible to maintain science if the need arises
- ACS Side-1
  - ACS Side-1 remains a valuable resource except for the CEB power converters
  - While operating on ACS Side-2, the following ACS Side-1 assets are available and obtainable in the event of a future ACS Side-2 anomaly (requires closing the Side-1 hold relay):
    - » Power MAMA
    - » Power and control either/both TECs including WFC shield TEC
    - » Power thermal shelf heaters
    - » Power window and interface plate heaters
  - Additional potential configurations are possible, requiring further investigation
    - » Power calibration lamps
      - Requires closing both operate relays; currently a CARD item in place preventing this
- ACS Side-2
  - ACS Side-2 is presently fully functional
  - If ACS Side-2 experienced a power converter failure (except the CEB converters) or some other non-catastrophic failure (e.g., not a blown main bus fuse), ACS Side-1 can be re-activated using the ACS Side-2 CEB power converters (requires closing the Side-2 hold relay):
    - » Evaluation of science image noise related to lack of CEB Sync signal to be determined



## ACS Side-1 Test Proposal Meeting



### Risk Assessment

- ¤ Re-activation of suspected faulty ACS Side-1 CEB power converters inherently carries risk
  - CEB Power Converter Outputs
    - » Risk: Out of tolerance power supply outputs could overstress/damage downstream components in ACS CEBs
    - » Risk Mitigation: +15V, -15V, and +35V CEB loads disconnected via open relays from CEB loads. +5V will be supplied to CEB timing boards, however, +5V is supplied via a separate DC/DC converter that the ARB has absolutely no reason to suspect at this time (+5V required in CEBs in order to transmit all 1's data to MEB SES).
  - CEB Power Converter Inputs
    - » Risk: Fault leads to high current draw on main bus that blows ACS Side-1 PDU 20 Amp Fuse
    - » Risk Mitigation: Current telemetry (sampled every 100ms) at time of anomaly indicates current decreased; no indication of current spike. Side-1 remained in fault configuration for an additional 7 to 8 seconds with no indication of change in input current. Analysis completed during STIS Side 2 FRB determined that there was a very low probability (<1%) of blowing a PDU 20 Amp fuse due to the Interpoint Converter input stage bond wire configuration (refer to next set of charts).

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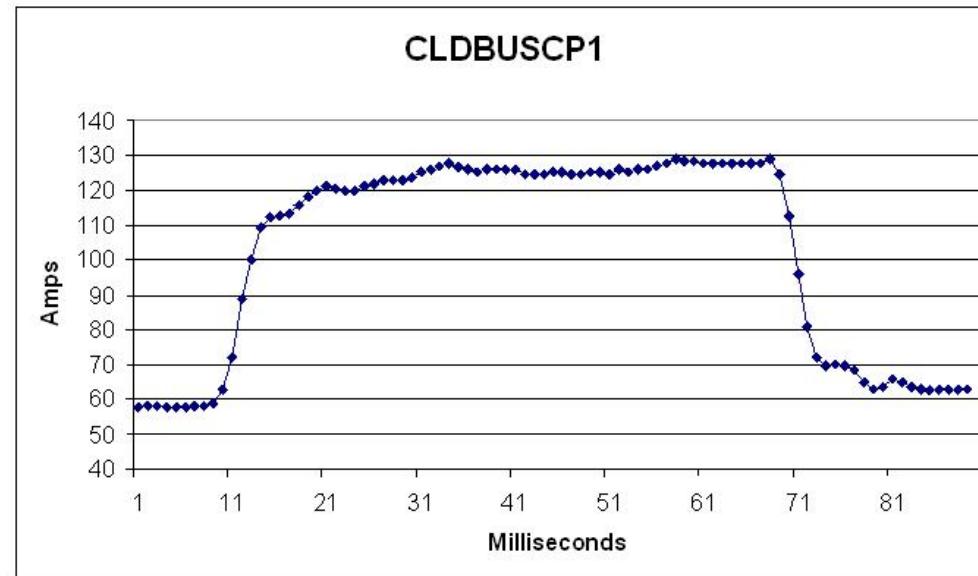


## ACS Side-1 Test Proposal Meeting



### PDU 20 Amp Fuse Current

- 20A Fuse blows at  $200 \text{ A}^2\cdot\text{sec}$  +/- 30%
  - From STIS Side 1 investigation (Leidecker)
- Bus C fuse observed to blow at  $\sim 215 \text{ A}^2\cdot\text{sec}$  during STIS Side 1 on-orbit anomaly investigation



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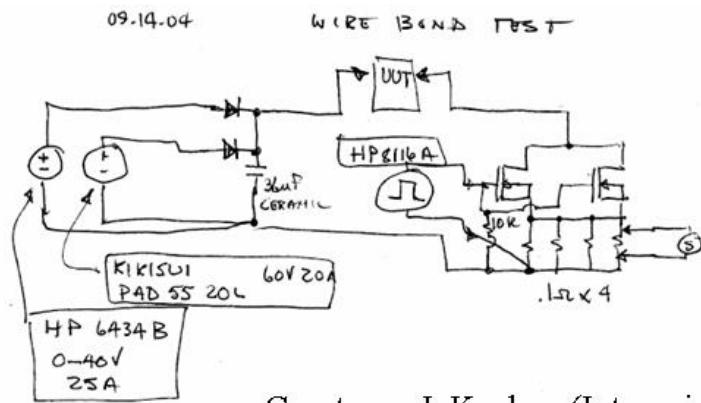


## ACS Side-1 Test Proposal Meeting



### Interpoint Fusing Test

- ¤ Experiments performed for STIS Side 2 FRB to measure fusing current of bond wires in 2805 primary
  - MFL2805S bond wires: Qnty 4, 5 mil Al wires ( $4 \times 5.37A = 21$  Amps)
  - MFL2815D bond wires: Identical
- ¤ Results show fusing at  $\sim 130$  A<sup>2</sup>.sec
  - Interpoint confirmed that the fusing analysis completed for the MFL2805S is 100% applicable to the MFL2815D



### Results

Peak Current (Amperes)	Pulse Width at bond failure (milliseconds)
150	6
104	12
80	23
60	150

Courtesy : J. Kuehny (Interpoint)

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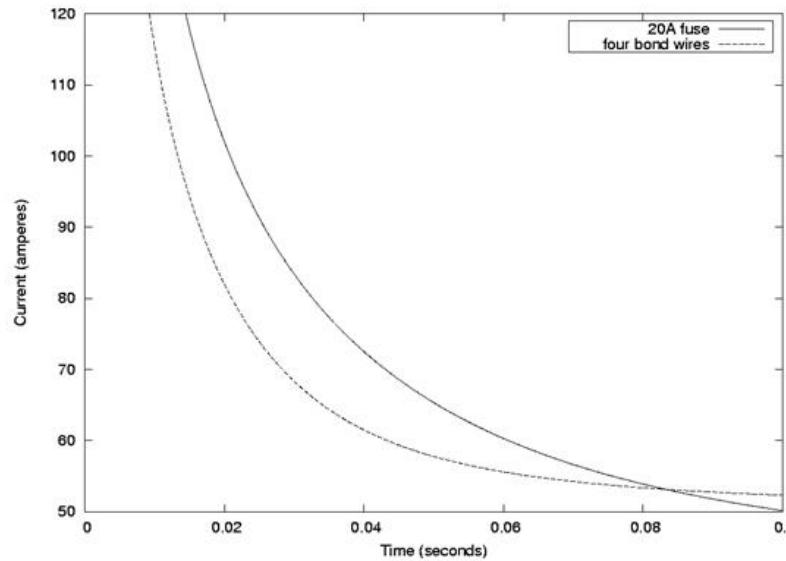


## ACS Side-1 Test Proposal Meeting



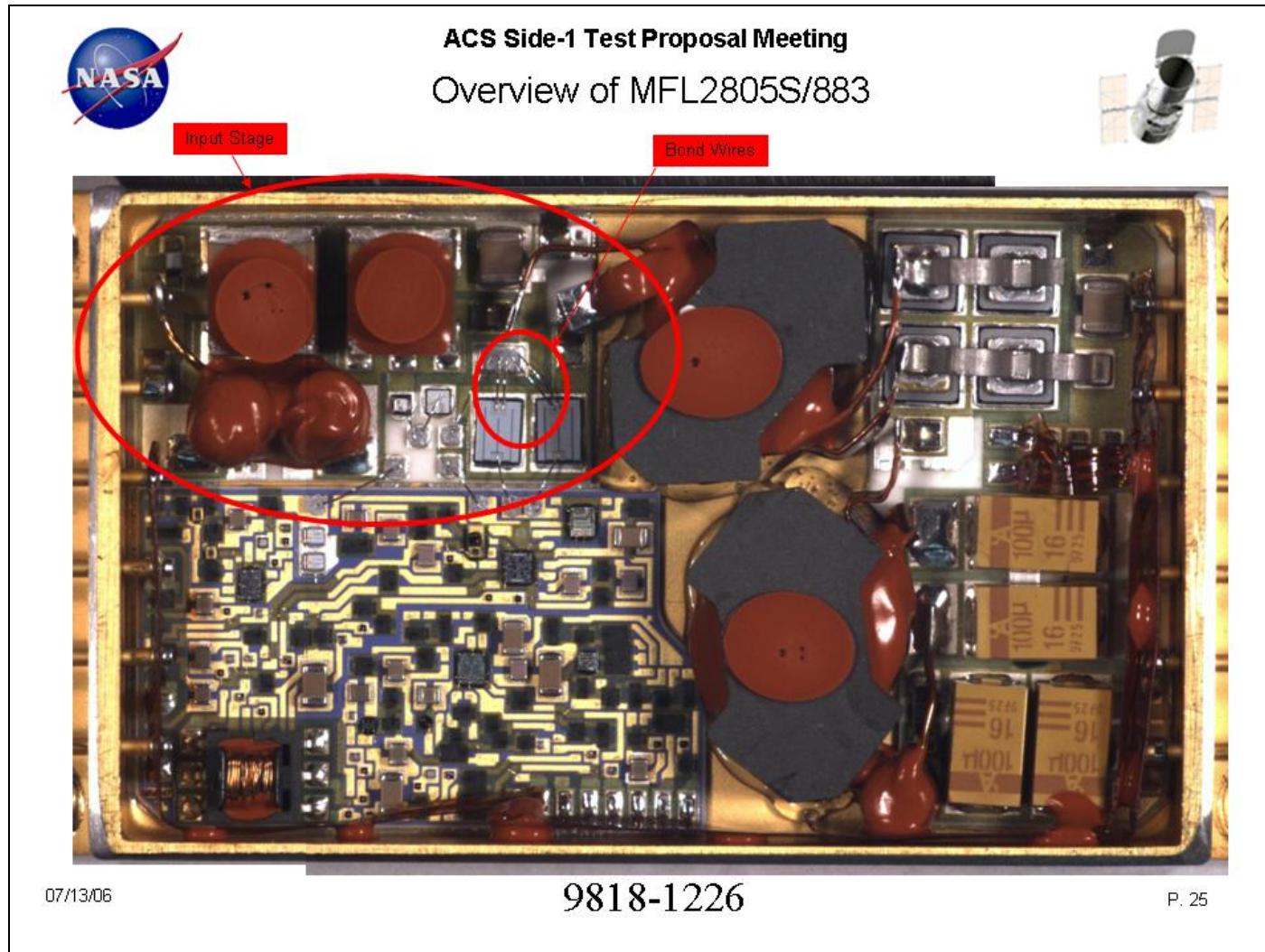
### MFL2815D vs 20 Amp Fuse

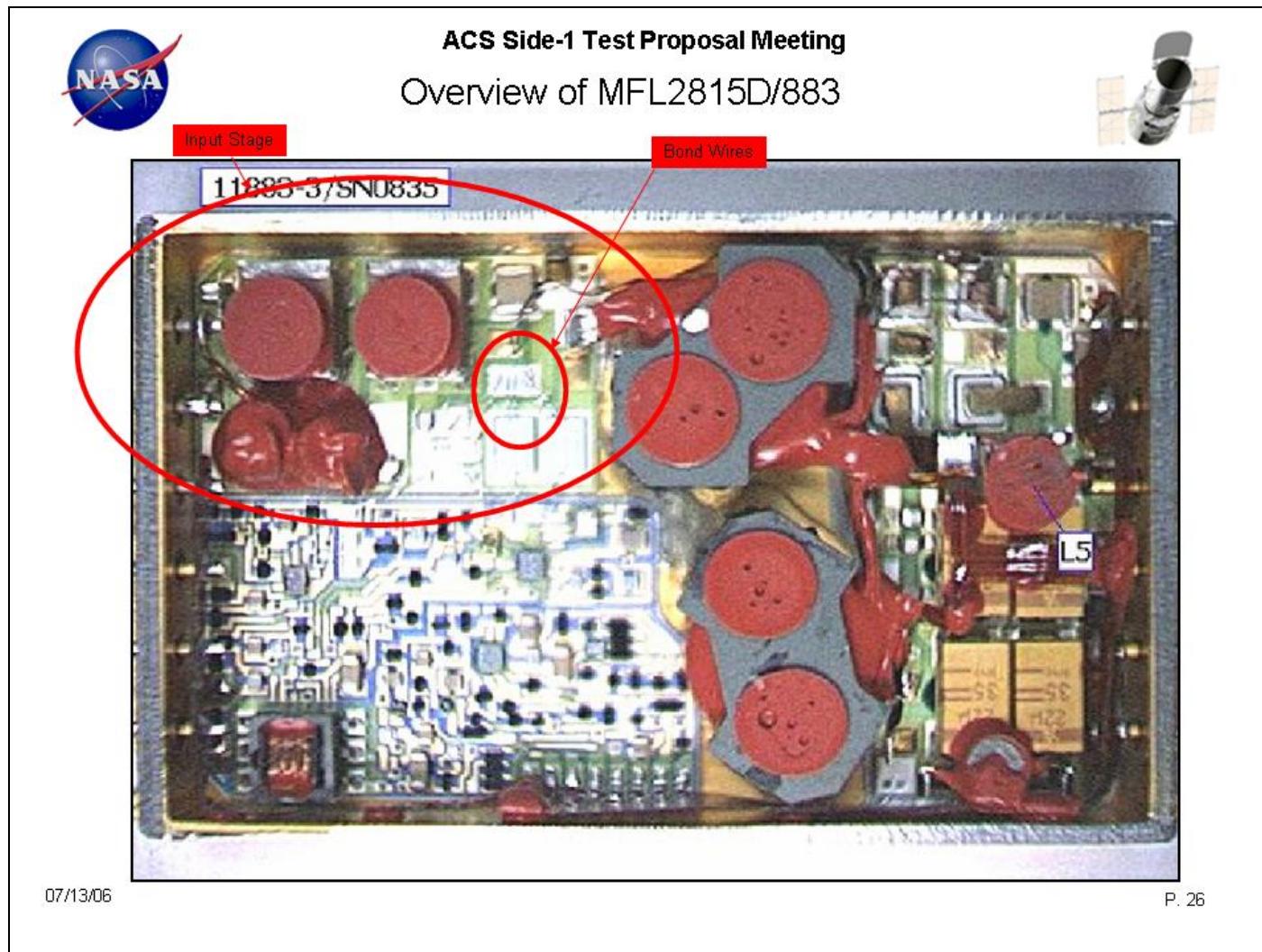
- ☒ Conclusions from STIS Side 2 FRB:
  - The MFL2805S Interpoint bond wires protect the fuse by interrupting sooner, over almost the entire domain of possible times
  - The risk of damage is less than 1%, and probably much less
- ☒ STIS Side 2 FRB findings stated above are 100% applicable to the MFL2815D used on ACS LVPS #3 board



07/13/06

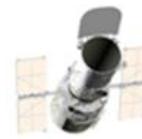
P. 24







## ACS Side-1 Test Proposal Meeting



### ARB Recommendation

- ¤ ACS ARB split with respect to executing an ACS Side 1 test
  - Based on vote (5 for, 10 against), ARB strongly leaning toward not running ACS Side 1 test for following reasons:
    - » There is a low probability risk associated with running an ACS Side 1 test that could result in a loss of remaining ACS Side 1 assets if ACS Side 1 20 Amp Fuse were to blow
    - » Executing ACS Side 1 test is not expected to produce any results that will change how we operate ACS Side 2
    - » There is only one possible test outcome that could vindicate the Interpoint MFL2815D device as the root cause of the original anomaly
      - However, there are two other test outcomes that would place the failure within the Interpoint MFL2815D

07/13/06

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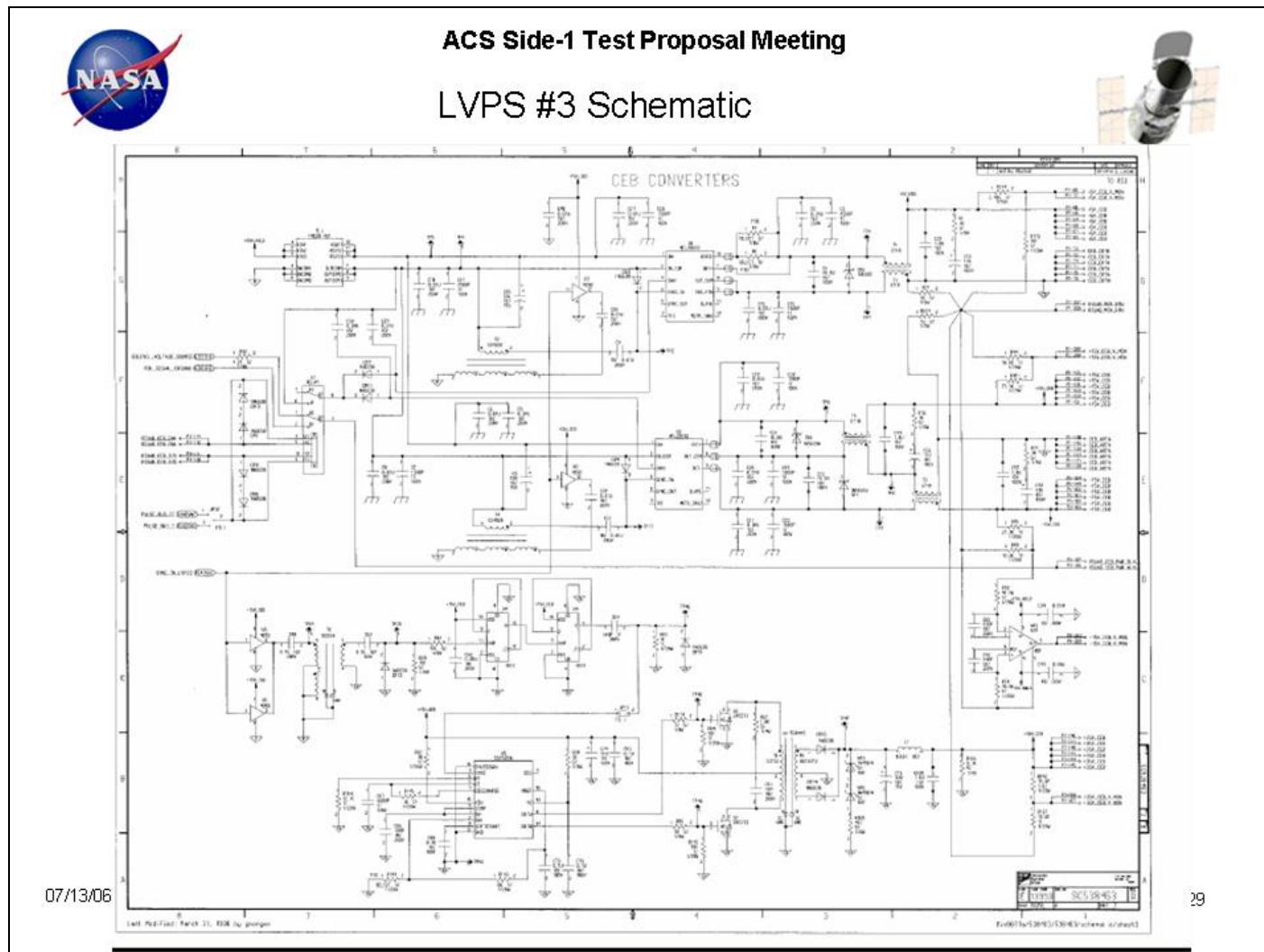
## ACS Side-1 Test Proposal Meeting

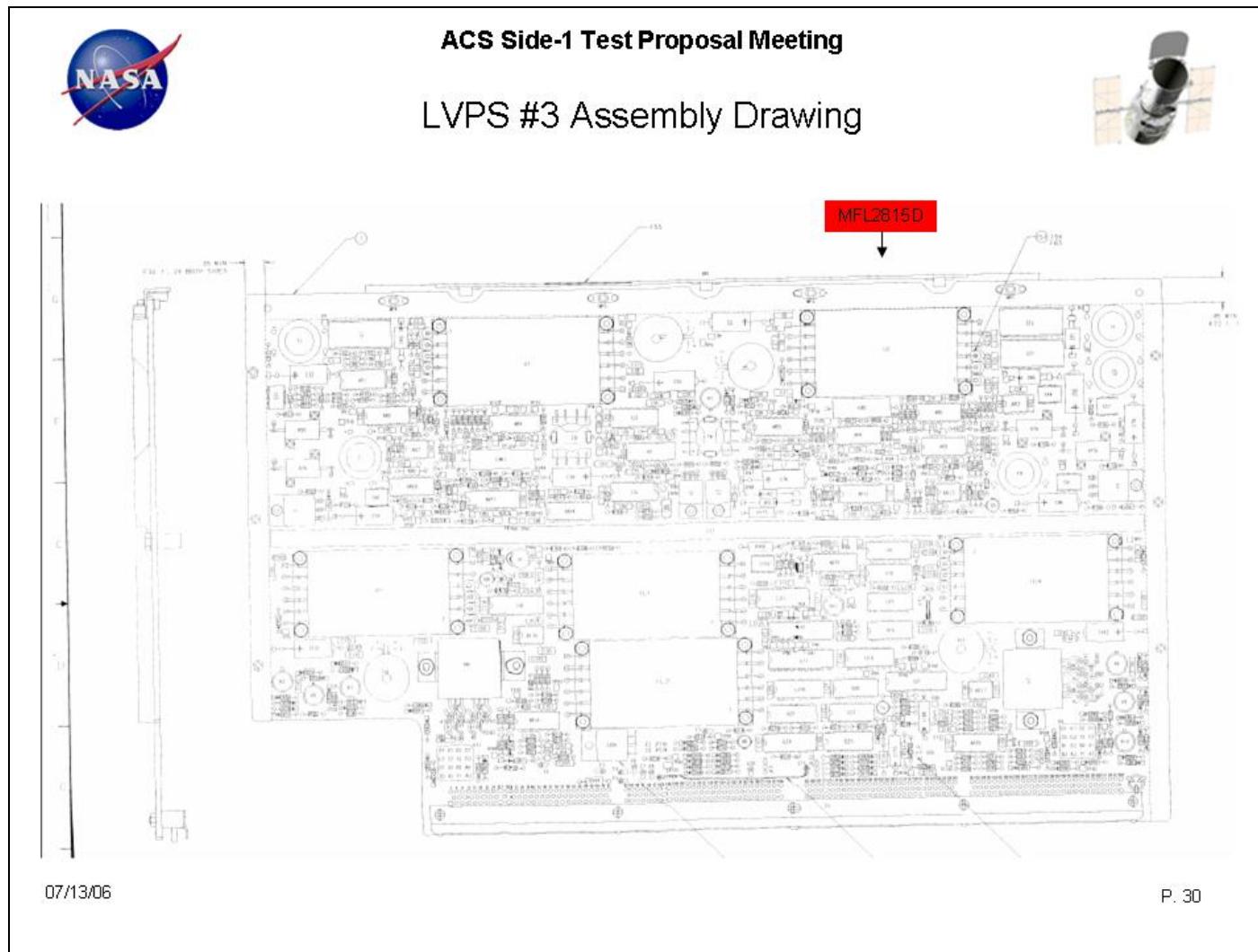


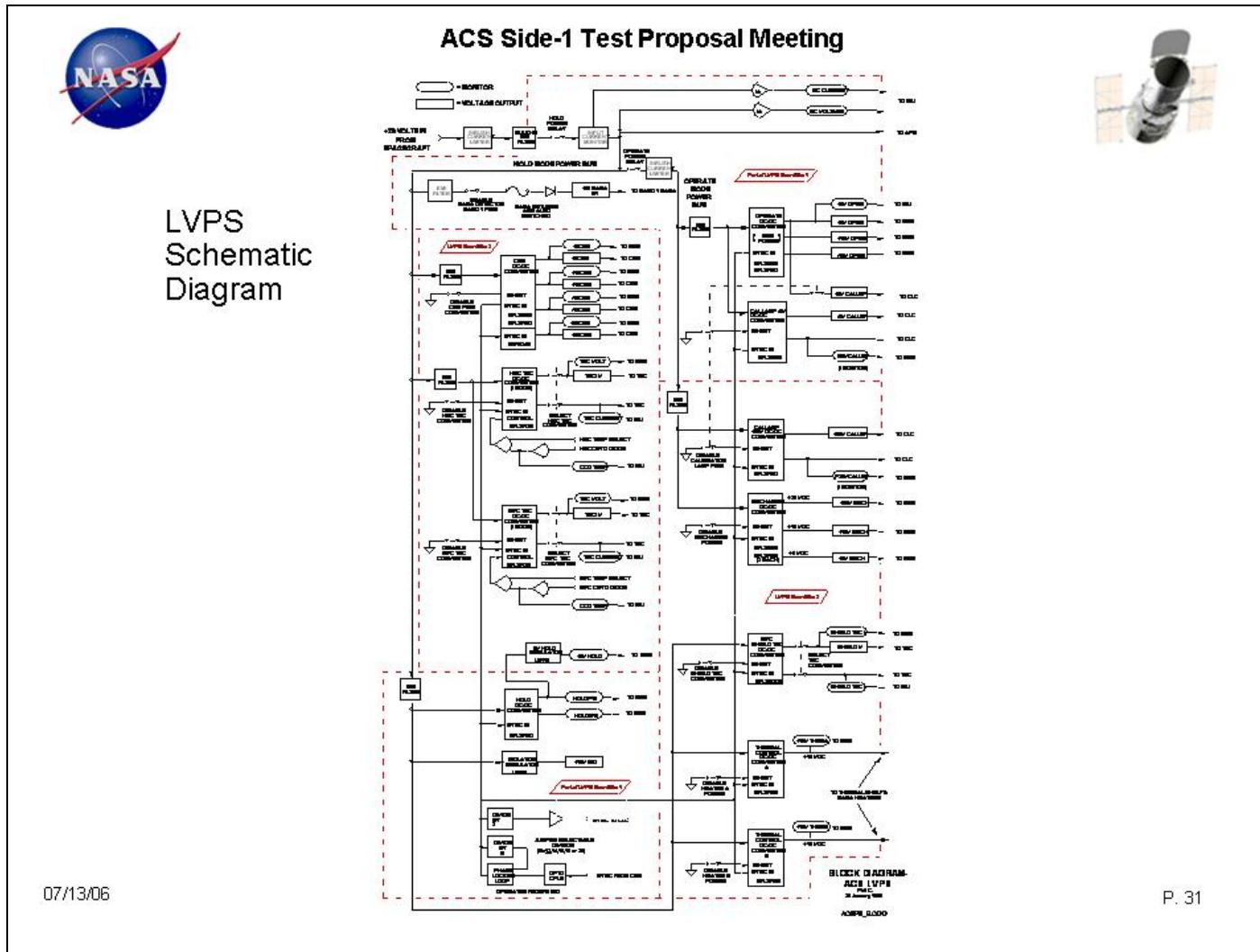
### Backup Charts

07/13/06

P. 28









## **Attachment 3: ACS Side-2 Switch and ACS CS 4.02 Installation FRR charts**

The following pages contain the first 13 charts of the FRR presentation for switching to ACS Side-2. Only the first 13 charts are included here since those highlight the ARB activities. For the complete set of charts see the following link on the HST EDOCS website:

[http://edocs.hst.nasa.gov/MOP/Shared%20Documents/FRR/ACS\\_Side2\\_CS4\\_02\\_FRR\\_rev0.ppt](http://edocs.hst.nasa.gov/MOP/Shared%20Documents/FRR/ACS_Side2_CS4_02_FRR_rev0.ppt)





**Flight Readiness Review:  
ACS Side-2 Switch  
and  
ACS CS 4.02 Installation (JV0019)**

**June 29, 2006**  
1:00 pm EDT B3/S107A



## FRR: ACS Side-2 Switch and CS 4.02 Installation

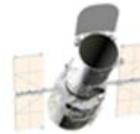


### Agenda

- 1.0 Engineering Team *(R. Stevens)*
- 2.0 Introduction/Overview *(R. Stevens/R. Chie)*
- 3.0 FSW, S/C H/W Changes and Implementation *(B. Serrano)*
  - 3.1 FSW and/or S/C H/W Functional Changes
  - 3.2 FSW Software Structure/Resource Changes
  - 3.3 Supporting Ground System Changes
  - 3.4 Supporting Documentation Changes
  - 3.5 Release Messages
  - 3.6 Unit and Build Level Testing/Results
  - 3.7 System Level Testing/Results
  - 3.8 H/W Interfaces Impact & Verification Matrix



## FRR: ACS Side-2 Switch and CS 4.02 Installation



### Agenda

- |  |                       |
|--|-----------------------|
| 4.0 Engineering Test / Installation                    | <i>(S. Arslanian)</i> |
| 4.1 Overview and Initial Conditions                    |                       |
| 4.2 Script Review                                      |                       |
| 4.3 Standalone Testing                                 |                       |
| 4.4 Operations Acceptance Testing Results              |                       |
| 4.5 Differences between Flight and Test Configurations |                       |
| 4.6 Summary of SMS Observing Plans                     |                       |
| 4.7 Timeline Review – MEGG                             |                       |
|  |                       |
| 5.0 Monitoring and System Impacts                      | <i>(S. Arslanian)</i> |
| 5.1 On-orbit Validation / Monitoring                   |                       |
| 5.2 System Impacts                                     |                       |
| 5.3 Supporting Operations Changes                      |                       |
| 5.4 Supporting PRD Changes                             |                       |
| 5.5 Training Module Changes (if any)                   |                       |
|  |                       |
| 6.0 Constraints and Restrictions Review                | <i>(S. Arslanian)</i> |
| 6.1 CARD   |                       |
| 6.2 OLD  |                       |



## FRR: ACS Side-2 Switch and CS 4.02 Installation

### Agenda



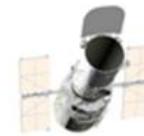
- |                                      |                                 |
|--------------------------------------|---------------------------------|
| 7.0 Contingency Planning             | <i>(S. Arslanian)</i>           |
| 7.1 Vehicle Contingencies            |                                 |
| 7.2 Ground Contingencies             |                                 |
|                                      |                                 |
| 8.0 Engineering Support Requirements | <i>(S. Arslanian)</i>           |
| 8.1 Personnel                        |                                 |
| 8.2 Communications / Data            |                                 |
| 8.3 CCS                              |                                 |
|                                      |                                 |
| 9.0 Liens                            | <i>(S. Arslanian)</i>           |
|                                      |                                 |
| 10.0 Follow-on Activities            | <i>(R. Stevens, K. Sembach)</i> |
| 10.1 ACS Side-2 SMOV                 |                                 |
| 10.2 Other Follow-on Activities      |                                 |

<b>FRR: ACS Side-2 Switch and CS 4.02 Installation</b>			
1.0 Engineering Team			
HST Project	Olivia Lupie	ST Scl	Kerry Clark Ilana Dashevsky Alan Welty Tom Wheeler Ken Sembach
SI FSW	Darryl Dye Dennis Garland Mike Kelly Peter Lien Wendy Lindboe Lily Liu Bev Serrano Colleen Townsley	HITT	June Atwell Stuart Bozievich Tony Foster Nick Lazio Armina Raufi
SI SE	Steve Arslanian John Bacinski Dave Hickey Art Rankin Holly Richardson Randy Stevens Scott Swain Morgan Van Arsdall	VEST	Eric Barksdale Ed Claybrooks Bill Kantonki Marvin Kent Jay Smith
DMS	Ben Teasdel	Sys Mgt	Pat Coleman Joe Cooper Pete Pataro Sujee Haskins Mark Slater
ACS ARB	Roger Chiei		



## FRR: ACS Side-2 Switch and CS 4.02 Installation

### 2.0 Introduction / Overview



#### 2.1 Objectives

- Configure ACS for Side-2 operations
- Install ACS CS 4.02 FSW into the control section (EEPROM version JV0019) of the ACS Side-2 MEB

#### 2.2 Testing and preparation adhered to administrative procedures

- AD 2-16: Operations Acceptance Testing
- AD 2-17: Spacecraft Configuration Change Process



## FRR: ACS Side-2 Switch and CS 4.02 Installation

### 2.0 Introduction / Overview



#### 2.3 Background

##### Anomaly History

- On 6/19/06 ACS suspended with ESBs 707 and 715 – HSTAR 10319
- Tiger Team investigations showed all ones (x0FFF) being read back from both HRC and WFC CEB A/D telemetry FIFOs
- On 6/20/06, HST Project gave direction to prepare for a Side-2 switch
- On 6/22/06, HST Project gave “go” for a Side-2 switch, unless ARB determined it was not safe to do so.
  - » 6/29/06 – FRR scheduled
  - » 6/30/06 – Uplink and realtime switch to Side-2
  - » 7/02/06 – Begin Side-2 SMS commanding
- On 6/22/06, Tiger Team transitioned investigation to the ACS CEB ARB
  - » ARB held first meeting
  - » ACS CEB ARB website (EDOCS Sharepoint):  
<http://edocs.hst.nasa.gov/hstsystman/ACSCEBARB/default.aspx>
- On 6/22/06, ACS transitioned to CS Operate mode on Side-1 (JBOOTOP1)
  - » On-orbit test recommended by Tiger Team and given Project concurrence



## FRR: ACS Side-2 Switch and CS 4.02 Installation



### 2.0 Introduction / Overview

#### 2.3 Background (continued)

##### ARB Status

- ARB has been actively investigating ACS On Orbit anomaly
  - On orbit telemetry has been extracted and analyzed:
    - ACS instrument level current data indicates current decreased approximately 1.2 – 1.8 amps during the anomaly based on CLDBUSCP sampled every 0.1 seconds and JTOTAL1 sampled every 5 seconds
    - Current data indicates anomaly lasted approximately 7 seconds prior to Suspend; a refinement over previous 4 to 6 second duration based on software telemetry collection routine.
    - All other parameters extracted thus far looked nominal
      - Bus Voltage was approximately 31.7V
  - A number of potential root cause fault theories have been identified and ruled out based on circuit evaluations, software evaluations, and additional ACS Side 1 to Operate1 testing
    - MEB1 SES hardware:
      - WFC and HRC CEB interface Optocouplers in common package
      - WFC and HRC CEB FIFO read control
      - WFC and HRC CEB common 8KHz sequencer clock that drives A/D data collection
    - CEB hardware:
      - A/D Converters



## FRR: ACS Side-2 Switch and CS 4.02 Installation



### 2.0 Introduction / Overview

#### 2.3 Background (continued)

##### ARB Status

- One remaining potential root cause fault theory remains at this time
  - Theory: Both WFC and HRC CEBs are supplied with power from a common LVPS +5V, +15V and -15V source. Loss of a 15V power rail(s) results in uncharacteristic performance of CEB A/D conversion, resulting in a CEB Engineering Telemetry stream consisting of all 1's data.
  - Lab testing with Engineering CEB unit has repeatedly reproduced the on orbit anomaly data signature of all 1's data by manipulating the input rail voltages.
    - Bench testing of an MFL2815D (Dual +/- 15V converter) has characterized the converter's output characteristics as a function of short circuit operation and open load operation
    - Engineering CEB test data clearly indicates reproduction of the on orbit anomaly in the following two configurations:
      - +15V open
      - +15V shorted to ground
    - Engineering CEB test data that does not reproduce the on orbit anomaly signature:
      - -15V open
    - Engineering CEB testing with -15V shorted to ground



## FRR: ACS Side-2 Switch and CS 4.02 Installation



### 2.0 Introduction / Overview

#### 2.3 Background (continued)

##### ARB Status – Hardware Safety

- It is safe to power up ACS Side 2, assuming fault related to loss (open or short) of +15V CEB power rail:
  - Open +15V fault
    - An open fault would be located in either:
      - MEB mother board
        - Switch to side 2 will safely bypass anomaly
      - Side 1 LVPS 3 board
        - Switch to side 2 will safely bypass anomaly
    - Internal to the MFL2815D converter on the Side 1 LVPS 3 board
      - Switch to side 2 will safely bypass anomaly
      - Depending on location of anomaly within Side 1 MFL2815D, worst case scenario during anomaly would have resulted in -15V rail jumping up to -20V (-15V rail controlled by +15V regulation within MFL2815D). LVPS 3 board provides protection in range of -17.1V to -18.9V, however, this exceeds absolute max rating of two CEB devices (A/D Converter AD674B @ 16.5V and Sample and Hold AD585 @ 18V) Additional investigation ongoing with Interpoint. Dr. Henning Leidecker investigating potential for overstress if this worst case scenario occurred



## FRR: ACS Side-2 Switch and CS 4.02 Installation



### 2.0 Introduction / Overview

#### 2.3 Background (continued)

#### ARB Status – Hardware Safety (continued)

- It is safe to power up ACS Side 2, assuming fault related to loss (open or short) of +15V CEB power rail (continued):
  - Shorted +15V fault
    - A short can be located in any one of the following locations:
      - Internal to the MFL2815D on the Side 1 LVPS 3 board
        - Switch to side 2 will safely bypass anomaly
      - On the side 1 LVPS 3 board
        - Switch to side 2 will safely bypass anomaly
      - On the MEB mother board
        - Switch to side 2 will safely bypass anomaly
      - In WFC CEB
        - Switch to side 2 will NOT bypass anomaly. Anomaly will still be present resulting in Suspend within 10 seconds of CEB power application. MFL2815D designed and rated for continuous output short circuit operation; no damage to side 2 hardware will result.
      - In HRC CEB
        - Identical to WFC CEB response above



## FRR: ACS Side-2 Switch and CS 4.02 Installation



### 2.0 Introduction / Overview

#### 2.3 Background (continued)

##### **ARB Status – Additional ARB Recommendations**

- Provide a temporary moratorium on ACS Solar Blind (SBC) operation
  - SBC operation presently disables power from the HRC CEB and leaves the WFC CEB fully powered
  - Disabling power from the HRC CEB removes all power from the HRC CEB Clock1, Clock2, and ASPC cards, but does not remove all +5V power from the HRC CEB Timing card, thus resulting in a 'hybrid' power configuration within the HRC CEB
  - ARB is not comfortable with this CEB 'hybrid' power configuration and requires additional time to investigate if it is truly a safe operational configuration for the CEB hardware
- Temporarily preclude EEPROM write operations while in South Atlantic Anomaly (SAA)
  - ARB Parts Engineering representatives in conjunction with GSFC radiation branch are reviewing data that indicates that EEPROM writes in a charge particle region of space, such as the SAA, have potential failure modes that could lead to permanent destruction of EEPROM memory locations that would require mapping around in the future.
  - Parts Engineering and radiation branch are investigating further
  - Initial assessment indicates an extremely low probably of upset to ACS parts in the HST orbit



## FRR: ACS Side-2 Switch and CS 4.02 Installation



### 2.0 Introduction / Overview

#### 2.3 Background (continued)

#### **ARB Status – Conclusion: ARB Side 2 Switch Recommendation**

- ARB unanimously recommends proceeding with switching to ACS Side 2 Operation at this time
  - Data and testing to date indicates loss of +15V CEB rail most likely responsible for on orbit anomaly
  - ARB has determined that switching to ACS Side 2 is safe regardless of an open or shorted condition on the +15V CEB power rail
  - ARB cautions that, although deemed safe, switching to ACS Side 2 will not restore ACS CEB operation in all fault scenarios
  - As a precautionary measure, do not perform a write to EEPROM while in the SAA until a detailed assessment and recommendation is provided by Parts Engineering and the GSFC Radiation Branch. This recommendation is applicable to all HST hardware containing EEPROMs
  - While on ACS Side 2, preclude SBC activities with either CEB powered until ARB completes review of CEB hardware safety in 'hybrid' power configuration



## Attachment 4: CEB Engineering Testing at Ball

### Test 1

Conducted 6/22-23 by Tim Schoeneweis, Chuck Harguth, Jed Gladieux, Andy Hunt, James Simons.

Results not included here – noted for context.

### Test 2

James Simons and I ran the test that Roger Chiei requested, setting the -15V supply to -1V, with the +15V supply shorted to GND.

The text describes the steps, and we captured screen shots of the telemetry at each one to be complete.

The screenshots lost some content in the transfer from the CEB Test computer, but still clearly show what's going on with the CEB telemetry. If the full screenshot is required for some reason, I can do the transfer differently upon request. Email me at [kalbin@ball.com](mailto:kalbin@ball.com).

Conditions:

- Test conducted in the RA-1 HST Lab at Ball Aerospace by James Simons and Ken Albin.
- EM CEB with CEB Test Setup.
- +5V & +35V power supplied by the custom Acopian power supply – unperturbed during this test.
- ±15V power was supplied by a separate Power Designs lab supply to allow variation.
- All power was run through a BTB to allow manipulating the ±15V.

## Test steps & screenshots

### 1. Power up CEB & interface. Nominal $\pm 15V$ .

**UVIS EVU CEB**

LOW RAILCLOCKS			HIGH RAILCLOCKS			CCD BIASES			VOLTAGE
Select One	Set Point	Actual	Select One	Set Point	Actual	Select One	Set Point	Actual	Voltage Name
RG AB Low	-5.65	-7.97	RG AB High	10.12	1.93	VDD AB	22.35	18.93	ASPC X +5
RG CD Low	0.00	-7.95	RG CD High	13.79	1.93	VDD CD	25.20	18.85	ASPC X +15
S1 AB Low	-3.00	-7.97	S1 AB High	3.16	2.03	VOD AB	16.03	11.53	ASPC X -15
S1 CD Low	-6.08	-7.96	S1 CD High	7.04	2.04	VOD CD	14.74	11.52	ASPC X +3
S2 A Low	-5.94	-7.97	S2 A High	6.88	2.04	VLG AB	-0.80	-4.08	CLK X +5
S2 B Low	-5.95	-7.96	S2 B High	6.89	2.03	VLG CD	-4.56	-4.08	CLK X +15
S2 C Low	-3.08	-7.97	S2 C High	6.07	2.04	VOFD AB*	14.74	13.05	CLK X -15
S2 D Low	-5.95	-7.96	S2 D High	6.89	2.03	VOFD CD*	14.73	12.99	CLK Y +5
S3 A Low	-6.08	-7.96	S3 A High	3.16	2.03				CLK Y +15
S3 B Low	-6.04	-7.97	S3 B High	5.11	2.03				CLK Y -15
S3 C Low	-7.50	-7.97	S3 C High	6.90	2.04				ASPC OFS1
S3 D Low	-5.95	-7.96	S3 D High	6.90	2.04				ASPC OFS1
SW A Low	-9.32	-10.00	SW A High	14.70	2.04				ASPC OFS1
SW B Low	-6.20	-7.94	SW B High	6.92	2.05				ASPC OFS1
SW C Low	-5.95	-7.97	SW C High	6.89	2.05				
SW D Low	-5.95	-10.00	SW D High	6.91	2.04				
P1 AB Low	-7.61	-8.92	P1 AB High	5.50	3.02				
P1 CD Low	-9.92	-8.88	P1 CD High	4.26	3.03				

\* Only valid for w/FCD

VOLTAGE

- ASPC X +5
- ASPC X +15
- ASPC X -15
- ASPC X +3
- CLK X +5
- CLK X +15
- CLK X -15
- CLK Y +5
- CLK Y +15
- CLK Y -15
- ASPC OFS1
- ASPC OFS1
- ASPC OFS1
- ASPC OFS1

Timing Brd

2. Remove +15V, leave open; -15V nominal

LOW RAILCLOCKS			HIGH RAILCLOCKS			CCD BIASES			VOLTAGE NAMES
Select One	Set Point	Actual	Select One	Set Point	Actual	Select One	Set Point	Actual	
RG AB Low	-5.65	10.00	RG AB High	10.12	19.99	VDD AB	22.35	41.98	ASPC X +5
RG CD Low	0.00	10.00	RG CD High	13.79	19.99	VDD CD	25.20	41.98	ASPC X +1
S1 AB Low	-3.00	10.00	S1 AB High	3.16	10.00	VOD AB	16.03	21.00	ASPC X -1!
S1 CD Low	-6.08	10.00	S1 CD High	7.04	10.00	VOD CD	14.74	21.00	ASPC X +3
S2 A Low	-5.94	10.00	S2 A High	6.88	10.00	VLG AB	-0.80	10.00	CLK X +5
S2 B Low	-5.95	10.00	S2 B High	6.89	10.00	VLG CD	-4.56	10.00	CLK X +15
S2 C Low	-3.08	10.00	S2 C High	6.07	10.00	VOFD AB*	14.74	42.14	CLK Y +5
S2 D Low	-5.95	10.00	S2 D High	6.89	10.00	VOFD CD*	14.73	42.07	CLK Y +15
S3 A Low	-6.08	10.00	S3 A High	3.16	10.00				CLK Y -15
S3 B Low	-6.04	10.00	S3 B High	5.11	10.00				ASPC OFS
S3 C Low	-7.50	10.00	S3 C High	6.90	10.00				ASPC OFS
S3 D Low	-5.95	10.00	S3 D High	6.90	10.00				ASPC OFS
SW A Low	-9.32	10.00	SW A High	14.70	10.00				ASPC OFS
SW B Low	-6.20	10.00	SW B High	6.92	10.00				
SW C Low	-5.95	10.00	SW C High	6.89	10.00				
SW D Low	-5.95	10.00	SW D High	6.91	10.00				
P1 AB Low	-7.61	19.99	P1 AB High	5.50	10.00				
P1 CD Low	-9.92	19.99	P1 CD High	4.26	10.00				

\* Only valid for WFC

3. Short +15V to GND; -15V nominal

LOW RAILCLOCKS			HIGH RAILCLOCKS			CCD BIASES			VOLTAGE NAMES
Select One	Set Point	Actual	Select One	Set Point	Actual	Select One	Set Point	Actual	
RG AB Low	-5.65	-10.00	RG AB High	10.12	-20.00	VDD AB	22.35	-42.00	ASPC X +5
RG CD Low	0.00	-10.00	RG CD High	13.79	-20.00	VDD CD	25.20	-42.00	ASPC X +1
S1 AB Low	-3.00	-10.00	S1 AB High	3.16	-10.00	VOD AB	16.03	-21.01	ASPC X -1!
S1 CD Low	-6.08	-10.00	S1 CD High	7.04	-10.00	VOD CD	14.74	-21.01	ASPC X +3
S2 A Low	-5.94	-10.00	S2 A High	6.88	-10.00	VLG AB	-0.80	-10.00	CLK X +5
S2 B Low	-5.95	-10.00	S2 B High	6.89	-10.00	VLG CD	-4.56	-10.00	CLK X +15
S2 C Low	-3.08	-10.00	S2 C High	6.07	-10.00	VOFD AB*	14.74	-42.16	CLK Y +5
S2 D Low	-5.95	-10.00	S2 D High	6.89	-10.00	VOFD CD*	14.73	-42.09	CLK Y +15
S3 A Low	-6.08	-10.00	S3 A High	3.16	-10.00				CLK Y -15
S3 B Low	-6.04	-10.00	S3 B High	5.11	-10.00				ASPC OFS
S3 C Low	-7.50	-10.00	S3 C High	6.90	-10.00				ASPC OFS
S3 D Low	-5.95	-10.00	S3 D High	6.90	-10.00				ASPC OFS
SW A Low	-9.32	-10.00	SW A High	14.70	-10.00				ASPC OFS
SW B Low	-6.20	-10.00	SW B High	6.92	-10.00				
SW C Low	-5.95	-10.00	SW C High	6.89	-10.00				
SW D Low	-5.95	-10.00	SW D High	6.91	-10.00				
P1 AB Low	-7.61	-20.00	P1 AB High	5.50	-10.00				
P1 CD Low	-9.92	-20.00	P1 CD High	4.26	-10.00				

\* Only valid for WFC

#### 4. Short +15V to GND; set -15V supply to -10V

**LOW RAIL CLOCKS**

Select One	Set Point	Actual
ØRG AB Low	-5.65	-10.00
ØRG CD Low	0.00	-10.00
ØS1 AB Low	-3.00	-10.00
ØS1 CD Low	-6.08	-10.00
ØS2 A Low	-5.94	-10.00
ØS2 B Low	-5.95	-10.00
ØS2 C Low	-3.08	-10.00
ØS2 D Low	-5.95	-10.00
ØS3 A Low	-6.08	-10.00
ØS3 B Low	-6.04	-10.00
ØS3 C Low	-7.50	-10.00
ØS3 D Low	-5.95	-10.00
ØSW A Low	-9.32	-10.00
ØSW B Low	-6.20	-10.00
ØSW C Low	-5.95	-10.00
ØSW D Low	-5.95	-10.00
ØP1 AB Low	-7.61	-20.00
ØP1 CD Low	-9.92	-20.00

**HIGH RAIL CLOCKS**

Select One	Set Point	Actual
ØRG AB High	10.12	-20.00
ØRG CD High	13.79	-20.00
ØS1 AB High	3.16	-10.00
ØS1 CD High	7.04	-10.00
ØS2 A High	6.88	-10.00
ØS2 B High	6.89	-10.00
ØS2 C High	6.07	-10.00
ØS2 D High	6.89	-10.00
ØS3 A High	3.16	-10.00
ØS3 B High	5.11	-10.00
ØS3 C High	6.90	-10.00
ØS3 D High	6.90	-10.00
ØSW A High	14.70	-10.00
ØSW B High	6.92	-10.00
ØSW C High	6.89	-10.00
ØSW D High	6.91	-10.00
ØP1 AB High	5.50	-10.00
ØP1 CD High	4.26	-10.00

**CCD BIASES**

Select One	Set Point	Actual
ØVDD AB	22.35	-42.00
ØVDD CD	25.20	-42.00
ØVOD AB	16.03	-21.01
ØVOD CD	14.74	-21.01
ØVLG AB	-0.80	-10.00
ØVLG CD	-4.56	-10.00
ØVOFD AB*	14.74	-42.16
ØVOFD CD*	14.73	-42.09

**VOLTAGE NAMES**

Voltage Name
ØASPC X +5
ØASPC X +1
ØASPC X -15
ØASPC X +3
ØCLK X +5
ØCLK X +15
ØCLK Y -15
ØCLK Y +5
ØCLK Y +15
ØCLK Y -15
ØASPC OFS
ØASPC OFS
ØASPC OFS
ØASPC OFS

\* Only valid for WFC

Transition to the following telemetry state occurs at approx. voltage of -5.9V, dialing -15V supply from -10V to -1V.

#### 5. Short +15V to GND; set -15V supply to -1V

**LOW RAIL CLOCKS**

Select One	Set Point	Actual
ØRG AB Low	-5.65	10.00
ØRG CD Low	0.00	10.00
ØS1 AB Low	-3.00	10.00
ØS1 CD Low	-6.08	10.00
ØS2 A Low	-5.94	10.00
ØS2 B Low	-5.95	10.00
ØS2 C Low	-3.08	10.00
ØS2 D Low	-5.95	10.00
ØS3 A Low	-6.08	10.00
ØS3 B Low	-6.04	10.00
ØS3 C Low	-7.50	10.00
ØS3 D Low	-5.95	10.00
ØSW A Low	-9.32	10.00
ØSW B Low	-6.20	10.00
ØSW C Low	-5.95	10.00
ØSW D Low	-5.95	10.00
ØP1 AB Low	-7.61	19.99
ØP1 CD Low	-9.92	19.99
ØP2 AR Low	-7.61	19.99

**HIGH RAIL CLOCKS**

Select One	Set Point	Actual
ØRG AB High	10.12	19.99
ØRG CD High	13.79	19.99
ØS1 AB High	3.16	10.00
ØS1 CD High	7.04	10.00
ØS2 A High	6.88	10.00
ØS2 B High	6.89	10.00
ØS2 C High	6.07	10.00
ØS2 D High	6.89	10.00
ØS3 A High	3.16	10.00
ØS3 B High	5.11	10.00
ØS3 C High	6.90	10.00
ØS3 D High	6.90	10.00
ØSW A High	14.70	10.00
ØSW B High	6.92	10.00
ØSW C High	6.89	10.00
ØSW D High	6.91	10.00
ØP1 AB High	5.50	10.00
ØP1 CD High	4.26	10.00
ØP2 AR High	-2.00	10.00

**CCD BIASES**

Select One	Set Point	Actual
ØVDD AB	22.35	41.98
ØVDD CD	25.20	41.98
ØVOD AB	16.03	21.00
ØVOD CD	14.74	21.00
ØVLG AB	-0.80	10.00
ØVLG CD	-4.56	10.00
ØVOFD AB*	14.74	42.14
ØVOFD CD*	14.73	42.07

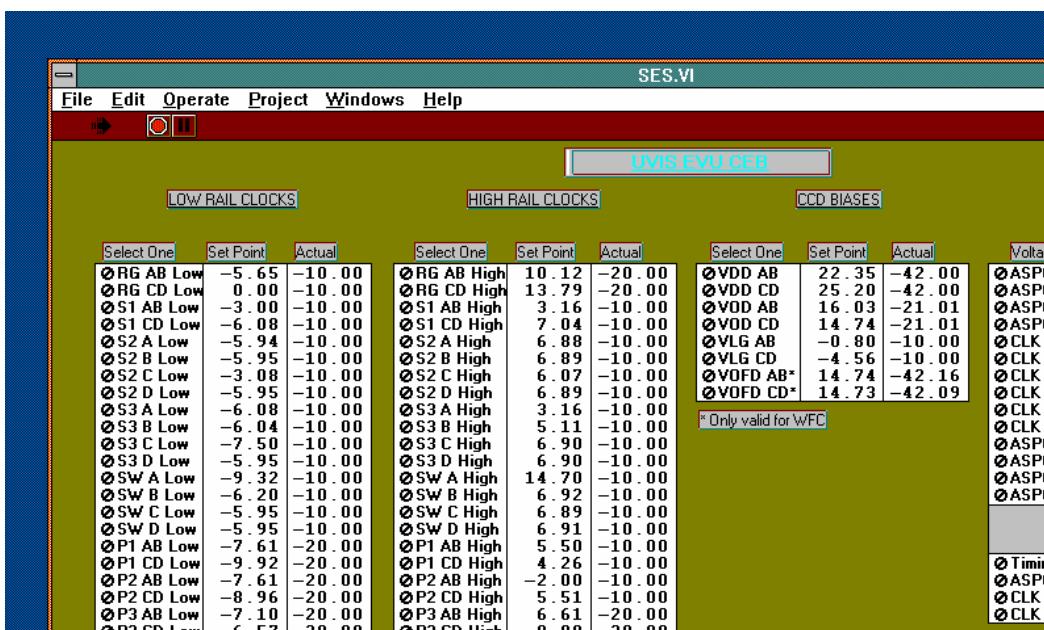
**VOLTAGE NAMES**

Voltage Name
ØASPC X +5
ØASPC X +1
ØASPC X -15
ØASPC X +3
ØCLK X +5
ØCLK X +15
ØCLK Y -15
ØCLK Y +5
ØCLK Y +15
ØCLK Y -15
ØASPC OFS
ØASPC OFS
ØASPC OFS
ØASPC OFS

\* Only valid for WFC

Transition to the following telemetry state occurs at approx. voltage of -0.4V, while dialing -15V supply from -1V to 0V.

## 6. Short +15V to GND, set -15V supply to 0V



### Test 3

I ran the next test that Roger Chiei requested, shorting the -15V supply to GND, and varied the +15V supply from +15V down to GND.

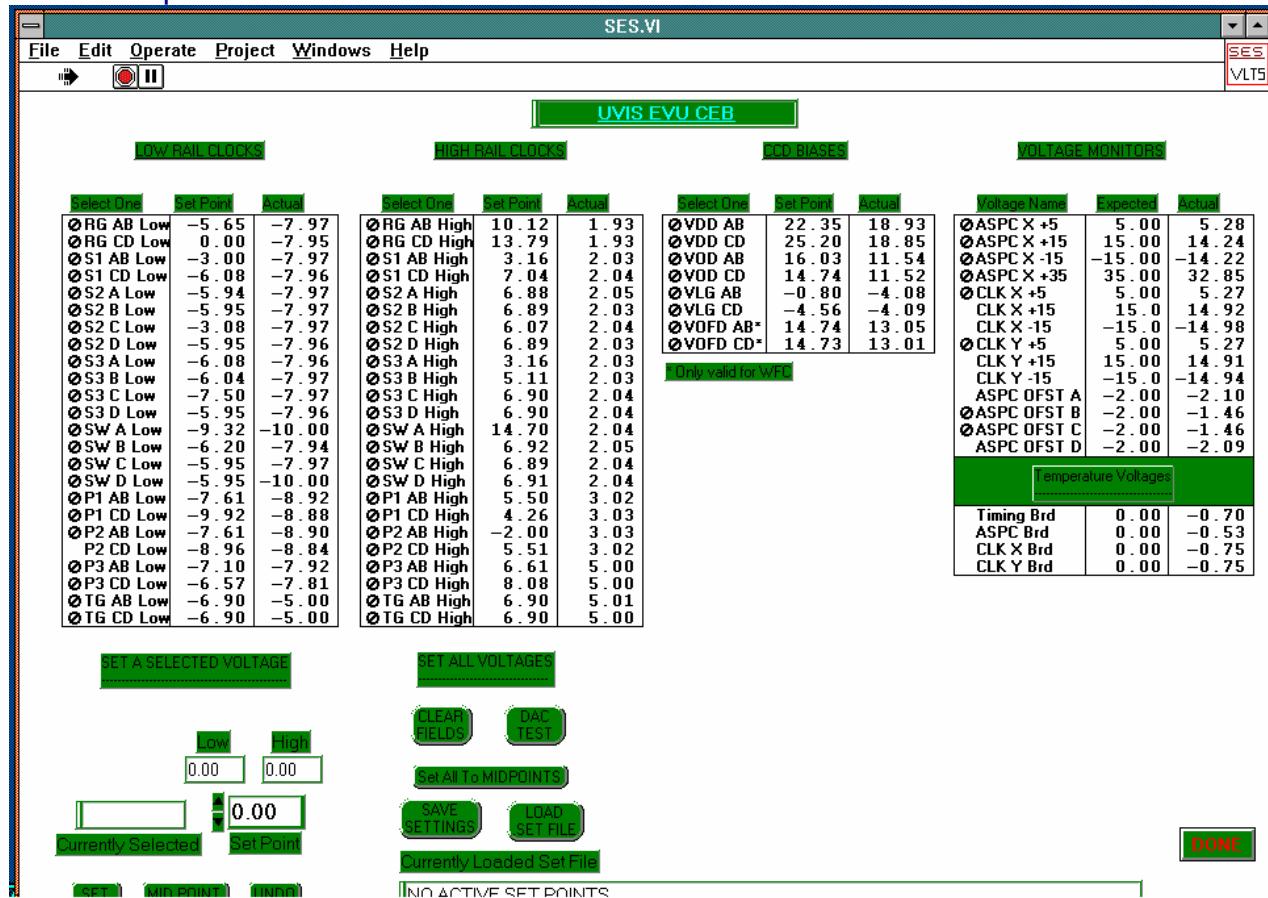
I'm attaching only two screen shots since nothing changed after disconnecting the -15V from power.

Conditions:

- Test conducted in the RA-1 HST Lab at Ball Aerospace by Ken Albin.
- EM CEB with CEB Test Setup.
- +5V & +35V power supplied by the custom Acopian power supply – unperturbed during this test.
- ±15V power was supplied by a separate Power Designs lab supply to allow variation.
- All power was run through a BTB to allow manipulating the ±15V.

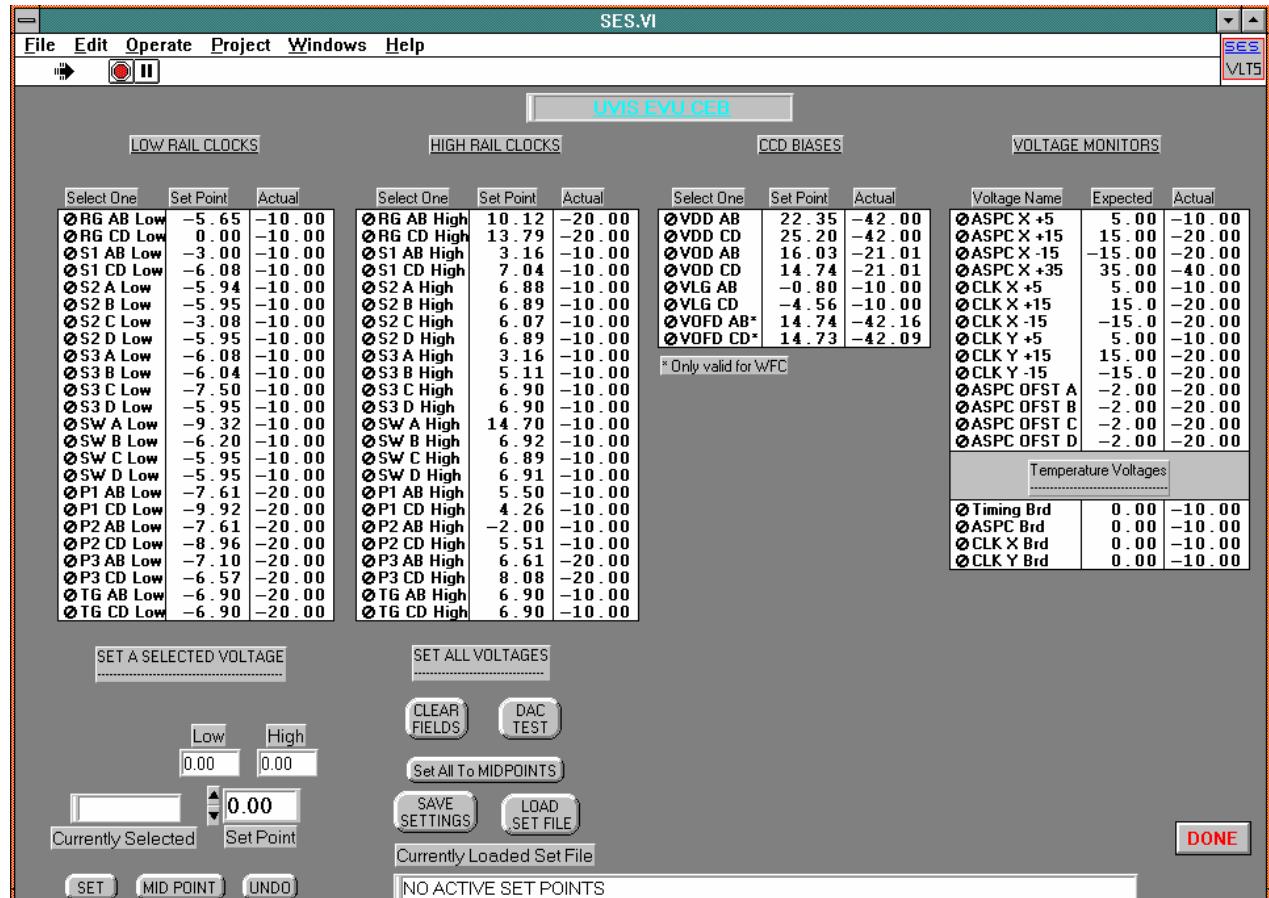
### Test steps & screenshots

#### 1. Power up CEB & interface. Nominal ±15V.



2. Remove -15V, leave open; +15V nominal
3. Short -15V to GND; +15V nominal
4. Short -15V to GND; vary the +15V supply from +15V to 0V

Note that the following screen capture applies to steps 2, 3 & 4, as no changes observed.





## Attachment 5: Detailed FMEA Analysis

Ladd Gillies                      Reference WA 538463B                      22-Jul-06  
James Simons                      Reference SSC538463B

Task:	Investigate each component (SC5384663) that is associated with the ±15V on ACS LVPS#3. Look for faults that can be attributed to the observed anomaly Assume normal operation when fault occurs, do not consider PWB trace failure, strictly look at the piece parts. Do not look internal to DC/DC converter other than I/O
Observed Anomaly:	Telemetry of the ADC = all 1's, e.g. complete lose of +15V, particle loss of -15V

In some cases with "no difference" noted, it was assumed that changes in operations would not be detected. Subtle changes that do not adversely change circuit operation.



	<b>Ref Des</b>	<b>Part No</b>	<b>Part type</b>	<b>Value</b>	<b>Failure</b>	<b>Effect</b>	<b>Condition Matches on Orbit Anomaly</b>	<b>Comment</b>
<b>Input</b>	C18	M39014/02-1338	Ceramic	0.01uF, 10%, 200V	Short	potential increase in input noise	No	shunts ground side of filter; not detectable
					Open	potential increase in input noise	No	not detectable
	C17	CCR05CG152FS	Ceramic	1500pF, 1%, 100V	Short	potential increase in input noise	No	shunts ground side of filter; not detectable
					Open	potential increase in input noise	No	not detectable
	C7	CCR05CG152FS	Ceramic	1500pF, 1%, 100V	Short	potential increase in input noise	No	shunts ground side of filter; not detectable
					Open	potential increase in input noise	No	not detectable
	C8	M39014/02-1338	Ceramic	0.01uF, 10%, 200V	Short	potential increase in input noise	No	shunts ground side of filter; not detectable
					Open	potential increase in input noise	No	not detectable
	C25	M39006/22-628H	wet tantalum, polarized	33uF, 10%, 75V	Short	28V hold current increases, loss of 28V, 5V and ±15V	No	Need to know current capability of 28V hold to determine if short clears
					Open	potential increase in input noise	No	not detectable
	C5	M39006/22-628H	wet tantalum, polarized	33uF, 10%, 75V	Short	28V hold current increases, loss of 28V, 5V and ±15V	No	Need to know current capability of 28V hold to determine if short clears
					Open	potential increase in input noise	No	not detectable
	C27	M39014/02-1338	Ceramic	0.01uF, 10%, 200V	Short	28V hold current increases, loss of 28V, 5V and ±15V	No	Need to know current capability of 28V hold to determine if short clears
					Open	potential increase in input noise	No	not detectable
	C26	CCR05CG152FS	Ceramic	1500pF, 1%, 100V	Short	28V hold current increases, loss of 28V, 5V and ±15V	No	Need to know current capability of 28V hold to determine if short clears
					Open	potential increase in input noise	No	not detectable
	C6	M39014/02-1338	Ceramic	0.01uF, 10%, 200V	Short	28V hold current increases, loss of 28V, 5V and ±15V	No	Need to know current capability of 28V hold to determine if short clears
					Open	potential increase in input noise	No	not detectable

	<b>Ref Des</b>	<b>Part No</b>	<b>Part type</b>	<b>Value</b>	<b>Failure</b>	<b>Effect</b>	<b>Condition Matches on Orbit Anomaly</b>	<b>Comment</b>
	C9	M39014/02-1338	Ceramic	0.01uF, 10%, 200V	Short	28V hold current increases, loss of 28V, 5V and ±15V	No	Need to know current capability of 28V hold to determine if short clears
					Open	potential increase in input noise	No	not detectable
	FL1	11015	EMI Filter	FME28-461/ES	Input short (internal)	28V hold current increases, loss of 28V, 5V and ±15V	No	Need to know current capability of 28V hold to determine if short clears
			EMI Filter	FME28-461/ES	Output short (internal)	28V hold current increases, loss of 28V, 5V and ±15V	No	Need to know current capability of 28V hold to determine if short clears
			EMI Filter	FME28-461/ES	Input open	28V hold current decrease, Loss of 28V, 5V and ±15V	No	no recovery
			EMI Filter	FME28-461/ES	Output Open	28V hold current decrease, Loss of 28V, 5V and ±15V	No	no recovery
	CR10	180616	Diode	0.3A, 150V - JANTXV1N6638	short	no impact	No	redundant diode
					open	possible damage to RIU CEB Enable driver	No	back emf protection
	CR5	180616	Diode	0.3A, 150V - JANTXV1N6638	short	no impact	No	redundant diode
					open	possible damage to RIU CEB Enable driver	No	back emf protection
	CR9	180616	Diode	0.3A, 150V - JANTXV1N6638	short	no impact	No	redundant diode
					open	possible damage to RIU CEB Enable driver	No	back emf protection
	CR8	180616	Diode	0.3A, 150V - JANTXV1N6638	short	no impact	No	redundant diode
					open	possible damage to RIU CEB Enable driver	No	back emf protection
	R32	RCR05G432JS	resistor, composition	4.3K, 5%, 1/8W	Short	No impact to ±15V	No	Tlm status, possible Impact to RIU Telemetry
					Open	loss of inhibit tlm status	No	
	C30	M39014/02-1338	Ceramic	0.01uF, 10%, 200V	short	inhibits ±15V, equivalent to both ±15V loss	No	
					open	no impact	No	
	C29	M39014/02-1338	Ceramic	0.01uF, 10%, 200V	short	inhibits +5V, loss of +5V only	No	

	<b>Ref Des</b>	<b>Part No</b>	<b>Part type</b>	<b>Value</b>	<b>Failure</b>	<b>Effect</b>	<b>Condition Matches on Orbit Anomaly</b>	<b>Comment</b>
					open	no impact	No	
	CR7	180616	Diode	0.3A, 150V - JANTXV1N6638	short	no impact	No	
					open	no impact	No	can't inhibit +5V
	CR11	180616	Diode	0.3A, 150V - JANTXV1N6638	short	no impact	No	
					open	no impact	No	can't inhibit ±15V
	K1	170570-005	Relay, DPDT	M39016/12-060M	open contact - "A"	no impact	No	normal operation is open
					Short A1-A2	inhibits ±15V & +5V, equivalent to both ±15V and +5V loss	No	
					open contact - "B"	loss of inhibit tlm status	No	
					Short B1-B2	change of telemetry status only	No	
					coil failure	no impact	No	
	C49	M39014/02-1338	Ceramic	0.01uF, 10%, 200V	short	shorts +15V_ISO supply, increase current on +15V_ISO, potential increase in detector noise. loss of sync on all supplies +5V, ±15V, +35V	No	
					open	no impact	No	decoupling cap, not detectable
	U3	170515-004	Hex Buffer/converter	CD4050B - M38510R05554BEA	output stuck high	loss of sync, potential increase in detector noise	No	loss of sync to a specific converter depends on which bit is stuck.
					output stuck low	loss of sync, potential increase in detector noise	No	loss of sync to a specific converter depends on which bit is stuck.
					Vdd open	loss of sync to all converters, potential increase in detector noise	No	

	<b>Ref Des</b>	<b>Part No</b>	<b>Part type</b>	<b>Value</b>	<b>Failure</b>	<b>Effect</b>	<b>Condition Matches on Orbit Anomaly</b>	<b>Comment</b>
					Vdd internal short	shorts +15V_ISO supply, increase current on +15V_ISO, potential increase in detector noise. loss of sync on all supplies +5V, ±15V, +35V	No	
	C28	M39014/02-1338	Ceramic	0.01uF, 10%, 200V	short	saturate sync xfmr - draw more current from 15V_ISO, loss of sync, potential increase in detector noise	No	
					open	loss of sync on +5V, potential increase in +5V	No	
	C38	M39014/02-1338	Ceramic	0.01uF, 10%, 200V	short	saturate sync xfmr - draw more current from 15V_ISO, loss of sync, potential increase in detector noise	No	
					open	loss of sync on ±15V, potential increase in ±15V noise	No	
	C4	M39014/02-1338	Ceramic	0.01uF, 10%, 200V	short	no impact	No	
					open	loss of sync on +5V, potential increase in +5V noise	No	
	C31	M39014/02-1338	Ceramic	0.01uF, 10%, 200V	short	no impact	No	
					open	loss of sync on ±15V, potential increase in ±15V noise	No	
	T2	534928-001	transformer		Short in winding	loss of sync on +5V, potential increase in +5V noise	No	
					Open Winding	loss of sync on +5V, potential increase in +5V noise	No	
					pri-to-sec short	loss of sync on +5V, potential increase in +5V noise	No	
	T4	534928-001	transformer		Short in winding	loss of sync on ±15V, potential increase in ±15V noise	No	
					Open Winding	loss of sync on ±15V, potential increase in ±15V noise	No	

	<b>Ref Des</b>	<b>Part No</b>	<b>Part type</b>	<b>Value</b>	<b>Failure</b>	<b>Effect</b>	<b>Condition Matches on Orbit Anomaly</b>	<b>Comment</b>
					pri-to-sec short	loss of sync on $\pm 15V$ , potential increase in $\pm 15V$ noise	No	
	CR3	180616	Diode	JANTXV1N6638	short	loss of sync on $+5V$ , potential increase in $+5V$ noise	No	
					open	no impact	No	exceed maximum input voltage rating to sync_in
	CR4	180616	Diode	JANTXV1N6638	short	loss of sync on $\pm 15V$ , potential increase in $\pm 15V$ noise	No	
					open	no impact	No	exceed maximum input voltage rating to sync_in
	U2 -1	11012	DC/DC	MFL2815SD - in+	short to chassis	28V hold current increases, loss of 28V, 5V and $\pm 15V$	No	
					short common	28V hold current increases, loss of 28V, 5V and $\pm 15V$	No	
					open	loss of $\pm 15V$	No	
	U2 -2		DC/DC	MFL2815SD - in_com	short to chassis	potential increase in input noise	No	shunts ground side of filter; not detectable
					short common	nothing	No	
					open	loss of $\pm 15V$	No	
	U2 -3		DC/DC	MFL2815SD - tri	short to chassis	no impact	No	
					short common	no impact	No	
					open	no impact	No	
	U2 -4		DC/DC	MFL2815SD -inhibit	short to chassis	loss of $\pm 15V$	No	
					short common	loss of $\pm 15V$	No	
					open	no impact	No	
	U2-5		DC/DC	MFL2815SD -sync out	short to chassis	no impact	No	
					short common	no impact	No	
					open	no impact	No	

	<b>Ref Des</b>	<b>Part No</b>	<b>Part type</b>	<b>Value</b>	<b>Failure</b>	<b>Effect</b>	<b>Condition Matches on Orbit Anomaly</b>	<b>Comment</b>
	U2-6		DC/DC	MFL2815SD - sync_in	short to chassis	loss of sync on ±15V, potential increase in ±15V noise	No	
					short common	loss of sync on ±15V, potential increase in ±15V noise	No	
					open	loss of sync on ±15V, potential increase in ±15V noise	No	
	U2-7		DC/DC	MFL2815SD - out+	short to chassis	Loss of +15V; -15V reduced to less than -1V	<b>Yes</b>	
					short common	Loss of +15V; -15V reduced to less than -1V	<b>Yes</b>	
					open	Loss of +15V; -15V reduced to approx -11V	<b>Yes</b>	
	U2-8		DC/DC	MFL2815SD - out_com	short to chassis	no impact	No	potential increase in noise
					short common	no impact	No	
					open	loss of gnd reference	No	
	U2-9		DC/DC	MFL2815SD - out -	short to chassis	Loss of -15V; +15V reduced to less than 1V	No	
					short common	Loss of -15V; +15V reduced to less than 1V	No	
					open	Loss of -15V only	No	
	U2-10		DC/DC	MFL2815SD - N/C	short to chassis	no impact	No	
					short common	no impact	No	
					open	no impact	No	
	U2-11		DC/DC	MFL2815SD - slave	short to chassis	loss of ±15V	No	equivalent to inhibit
					short common	loss of ±15V	No	equivalent to inhibit
					open	no impact	No	
	U2-12		DC/DC	MFL2815SD msrt_inh2	short to chassis	loss of ±15V	No	equivalent to inhibit
					short common	loss of ±15V	No	equivalent to inhibit

	<b>Ref Des</b>	<b>Part No</b>	<b>Part type</b>	<b>Value</b>	<b>Failure</b>	<b>Effect</b>	<b>Condition Matches on Orbit Anomaly</b>	<b>Comment</b>
					open	no impact	No	
	U1 -1		DC/DC	MFL2805SD	short to chassis	28V hold current increases, loss of 28V, 5V and ±15V	No	
					short common	28V hold current increases, loss of 28V, 5V and ±15V	No	
					open	loss of +5V	No	
	U1-2		DC/DC	MFL2805SD	short to chassis	potential increase in input noise	No	shunts ground side of filter; not detectable
					short common	no impact	No	
<b>Output</b>					open	loss of +5V	No	
	C33	M39014/02-1338	Ceramic	0.01uF, 10%, 200V	Short	Loss of +15V; -15V reduced to less than -1V	<b>Yes</b>	
					Open	potential increase in +15V noise	No	
	C32	CCR05CG152FS	Ceramic	1500pF, 1%, 100V	Short	Loss of +15V; -15V reduced to less than -1V	<b>Yes</b>	
					Open	potential increase in +15V noise	No	
	C11	M39014/02-1338	Ceramic	0.01uF, 10%, 200V	Short	Loss of -15V; +15V reduced to less than 1V	No	
					Open	potential increase in -15V noise	No	
	C10	CCR05CG152FS	Ceramic	1500pF, 1%, 100V	Short	Loss of -15V; +15V reduced to less than 1V	No	
					Open	potential increase in -15V noise	No	
	C20	M39014/02-1338	Ceramic	0.01uF, 10%, 200V	Short	no impact	No	potential increase in noise
					Open	potneital increase in noise on both ±15V	No	
	C19	CCR05CG152FS	Ceramic	1500pF, 1%, 100V	Short	no impact	No	
					Open	potneital increase in noise on both ±15V		
	C21	532857-011085	Multilayer Ceramic, 87106-065	15uF, 10%, 100V	short	Loss of +15V; -15V reduced to less than -1V	<b>Yes</b>	
					Open	potential increase in +15V noise	No	

	<b>Ref Des</b>	<b>Part No</b>	<b>Part type</b>	<b>Value</b>	<b>Failure</b>	<b>Effect</b>	<b>Condition Matches on Orbit Anomaly</b>	<b>Comment</b>
	C12	532857-011085	Multilayer Ceramic, 87106-065	15uF, 10%, 100V	short	Loss of -15V; +15V reduced to less than 1V	No	
					Open	potential increase in -15V noise	No	
	CR6	170525-018	diode, transient suppressor	JANTXV1N5639A	short	Loss of +15V; -15V reduced to less than -1V	<b>Yes</b>	
					Open	no impact	No	ovp
	CR1	170525-018	diode, transient suppressor	JANTXV1N5639A	short	Loss of -15V; +15V reduced to less than 1V	No	
					Open	no impact	No	ovp
	C44	532857-011065	Multilayer Ceramic, 87106-065	1.8uF, 10%, 100V	short	Loss of +15V; -15V reduced to less than -1V	<b>Yes</b>	
					Open	potential increase in +15V noise	No	
	R76	RCR05G101JS	Resistor, Composition	10, 5%, 1/8W	Short	no impact	No	lose output noise filter damping
					Open	potential increase in +15V noise	No	underdamped
	C56	M39006/22-628H	wet tantalum, polarized	11uF, 10%, 100V	short	1.5A increase in +15V current, 22W increase in R76 power dissipation (rated at 1/8W).	No	Depends on what happens to R76 when current and power rating are exceeded. Will it open? How long will it take to open?
					open	potential increase in +15V noise	No	underdamped
	C57	532857-011065	Multilayer Ceramic, 87106-065	1.8uF, 10%, 100V	short	Loss of -15V; +15V reduced to less than 1V	No	
					Open	no impact		
	R77	RCR05G101JS	Resistor, Composition	10, 5%, 1/8W	Short	no impact	No	lose output noise filter damping

	<b>Ref Des</b>	<b>Part No</b>	<b>Part type</b>	<b>Value</b>	<b>Failure</b>	<b>Effect</b>	<b>Condition Matches on Orbit Anomaly</b>	<b>Comment</b>
					Open	potential increase in -15V noise	No	underdamped
C78	M39006/22-628H	wet tantalum, polarized	11uF, 10%, 100V		short	1.5A increase in +15V current, 22W increase in R77 power dissipation (rated at 1/8W).	No	Depends on what happens to R77 when current and power rating are exceeded. Will it open? How long will it take to open?
					open	potential increase in +15V noise	No	underdamped
T5	522940-001	Inductor, Output Filter			short in winding, pri or sec	potential increase in +15V noise	No	
					winding-to-winding short	Loss of +15V; -15V reduced to less than -1V	Yes	
					winding 1-2 open	Loss of +15V; -15V reduced to approx -11V	Yes	
					winding 3-4 open	loss of ground reference	No	
T3	522940-001	Inductor, Output Filter			short in winding, pri or sec	potential increase in -15V noise	No	
					winding 1-2 open	loss of ground reference	No	
					winding 2-4 open	Loss of -15V only	No	
					winding-to-winding short	Loss of -15V; +15V reduced to less than 1V	No	
R174	RCR05G101JS	resistor, composition	10, 5%, 1/8W		short	no impact	No	monitor rtn/ceb rtn
					open	no impact	No	
R44	RNC50J1002FS	Resistor, Film	10.0k, 1%, 1/20W		short	changes TLM voltage - 0V on CEB +15V monitor	No	
					open	changes TLM voltage - full scale on CEB +15V monitor	No	
R101	RNC50J2742FS	Resistor, Film	27.4k, 1%, 1/20W		short	changes TLM voltage - full scale on CEB +15V monitor	No	
					open	changes TLM voltage - 0V on CEB +15V monitor	No	

	<b>Ref Des</b>	<b>Part No</b>	<b>Part type</b>	<b>Value</b>	<b>Failure</b>	<b>Effect</b>	<b>Condition Matches on Orbit Anomaly</b>	<b>Comment</b>
	R45	RNC50J2742FS	Resistor, Film	27.4k, 1%, 1/20W	short	changes TLM voltage - full scale on CEB -15V monitor	No	
					open	changes TLM voltage - 0V on CEB -15V monitor	No	
	R43	RNC50J1002FS	Resistor, Film	10.0k, 1%, 1/20W	short	changes TLM voltage - 0V on CEB -15V monitor	No	
					open	changes TLM voltage - full scale on -15V monitor	No	
	R73	RNC50J4992FS	Resistor, Film	49.9k, 1%, 1/20W	short	no impact	No	
					open	changes TLM voltage - loss of -15V monitor	No	
	C50	M39014/02-1338	Ceramic	0.01uF, 10%, 200V	Short	Loss of +15V; -15V reduced to less than -1V	<b>Yes</b>	
					Open	no impact	no	decoupling cap, not detectable
	U4	170501-003	Dual D F/F	CD4013, M38510R05151BCA	internal short VDD to gnd	Loss of +15V; -15V reduced to less than -1V	<b>Yes</b>	
					any other failure	loss of Sync for +35V, possibly higher noise in detector	No	
	C64	M39014/02-1338	Ceramic	0.01uF, 10%, 200V	Short	no impact	No	
					Open	loss of Sync for +35V, higher +35V noise	No	
	R83	RNC50J1001FS	Resistor, Film	1.0k, 1%, 1/20W	Short	loss of Sync for +35V, higher +35V noise	No	
					Open	no impact	No	
	CR15	180616	Diode	JANTXV1N6638	short	loss of Sync for +35V, higher +35V noise	No	
					open	possible Damage to U5, exceed maximum voltage ratings	No	
	R82	RNC50J10R0FS	Resistor, Film	10, 1%, 1/20W	Short	no impact	No	
					open	loss of 35V	No	
	R60	RCR05G101JS	Resistor, Composition	10, 5%, 1/8W	Short	No impact	No	

<b>Ref Des</b>	<b>Part No</b>	<b>Part type</b>	<b>Value</b>	<b>Failure</b>	<b>Effect</b>	<b>Condition Matches on Orbit Anomaly</b>	<b>Comment</b>
				Open	loss of 35V	No	
C74	M39006/22-628H	wet tantalum, polarized	11uF, 10%, 100V	Short	Loss of +15V; -15V reduced to less than -1V	Yes	
				Open	potential increase in +35V noise	No	
C63	M39014/02-1338	Ceramic	0.01uF, 10%, 200V	Short	Loss of +15V; -15V reduced to less than -1V	Yes	
				Open	potential increase in +35V noise	No	
C75	M39014/02-1350	Ceramic	0.1uF, 10%, 100V	Short	1.5A increase in +15V current, 22W increase in R60 power dissipation (rated at 1/8W).	No	Depends on what happens to R60 when current and power rating are exceeded. Will it open? How long will it take to open?
				Open	loss of +35V	No	
C73	M39014/02-1350	Ceramic	0.1uF, 10%, 100V	Short	Loss of +35V	No	Possible damage to U5
				Open	no impact	No	
C88	M39014/02-1350	Ceramic	0.1uF, 10%, 100V	Short	Loss of +35V	No	
				Open	no impact	No	
R143	RNC50J1002FS	Resistor, Film	10.0k, 1%, 1/20W	Short	no impact	No	
				Open	Loss of +35V	No	
R144	RNC50JXXXXFS	Resistor, Film	SELECT, 1%, 1/20W	Short	Loss of +35V	No	sets output pulse width
				Open	no impact	No	efficiency, noise
C86	M39014/02-0975	Ceramic	100pF, 10%, 200V	Short	Loss of +35V	No	
				Open	no impact	No	
R145	RNC50J10R0FS	Resistor, Film	10, 1%, 1/20W	Short	no impact	No	
				Open	Loss of +35V	No	
R154	RNC50J1212FS	Resistor, Film	12.1k, 1%, 1/20W	Short	Loss of +35V	No	One of U5's outputs latches high which pulls down the +15V to U5's UVLO threshold (7V) which then resets both outputs, thereby allowing the +15V to recover.

	<b>Ref Des</b>	<b>Part No</b>	<b>Part type</b>	<b>Value</b>	<b>Failure</b>	<b>Effect</b>	<b>Condition Matches on Orbit Anomaly</b>	<b>Comment</b>
					Open	Loss of +35V	No	One of U5's outputs latches high which pulls down the +15V to U5's UVLO threshold (7V) which then resets both outputs, thereby allowing the +15V to recover.
	C87	M39014/02-1011	Ceramic	1000pF, 10%, 100V	Short	Loss of +35V	No	One of U5's outputs latches high which pulls down the +15V to U5's UVLO threshold (7V) which then resets both outputs, thereby allowing the +15V to recover.
					Open	Reduction in 35V output voltage	No	Increased oscillator frequency; narrow output pulses.
	U5-1	532797-011	Pulse Width Modulator - in-	SG1525A	Short to gnd	Loss of +35V	No	
					Open	no impact	No	
	U5-2		in +		Short to gnd	Loss of +35V	No	
					Open	Loss of +35V	No	
	U5-3		SYNC		Short to gnd	Loss of +35V	No	
					Open	loss of Sync for +35V, potential increase in +35V noise	No	
	U5-4		OSC		Short to gnd	no impact	No	
					Open	no impact	No	
	U5-5		CT		Short to gnd	Loss of +35V	No	One of U5's outputs latches high which pulls down the +15V to U5's UVLO threshold (7V) which then resets both outputs, thereby allowing the +15V to recover.
					Open	Loss of +35V	No	
	U5-6		RT		Short to gnd	Loss of +35V	No	One of U5's outputs latches high which pulls down the +15V to U5's UVLO threshold (7V) which then resets both outputs, thereby allowing the +15V to recover.

	<b>Ref Des</b>	<b>Part No</b>	<b>Part type</b>	<b>Value</b>	<b>Failure</b>	<b>Effect</b>	<b>Condition Matches on Orbit Anomaly</b>	<b>Comment</b>
					Open	Loss of +35V	No	One of U5's outputs latches high which pulls down the +15V to U5's UVLO threshold (7V) which then resets both outputs, thereby allowing the +15V to recover.
	U5-7		Discharge		Short to gnd	Loss of +35V	No	One of U5's outputs latches high which pulls down the +15V to U5's UVLO threshold (7V) which then resets both outputs, thereby allowing the +15V to recover.
	U5-8		SOFTSTART		Open	Loss of +35V	No	
					Short to gnd	Loss of +35V	No	
	U5-9		COMP		Open	no impact	No	
					Short to gnd	Loss of +35V	No	
	U5-10		Shutdown		Open	no impact	No	
					Short to gnd	No impact	No	
	U5-11		Output A		Open	No impact	No	Depends on what happens to R60 when current and power rating are exceeded. Will it open? How long will it take to open?
					Short to gnd	0.75A increase in +15V current, 11W increase in R60 power dissipation (rated at 1/8W).	No	
					Open	+35V DC value slight decrease, output ripple increase	No	
					Stuck High	+15V will drop down to approximately +5V.	No	The +15V output will fold back to whatever Q2 gate-to-source voltage will sustain the available drain current.
	U5-12		Ground		Short to gnd	no impact	No	
					Open	Loss of +35V	No	
	U5-13		VC		Short to gnd	1.5A increase in +15V current, 22W increase in R60 power dissipation (rated at 1/8W).	No	Depends on what happens to R60 when current and power rating are exceeded. Will it open? How long will it take to open?

	<b>Ref Des</b>	<b>Part No</b>	<b>Part type</b>	<b>Value</b>	<b>Failure</b>	<b>Effect</b>	<b>Condition Matches on Orbit Anomaly</b>	<b>Comment</b>
					Open	Loss of +35V	No	
	U5-14		Output B		Short to gnd	0.75A increase in +15V current, 11W increase in R60 power dissipation (rated at 1/8W).	No	Depends on what happens to R60 when current and power rating are exceeded. Will it open? How long will it take to open?
					Open	+35V DC value slight decrease, output ripple increase	No	
					Stuck High	+15V will drop down to approximately +5V.	No	The +15V output will fold back to whatever Q2 gate-to-source voltage will sustain the available drain current.
	U5-15		Vin		Short to gnd	1.5A increase in +15V current, 22W increase in R82 power dissipation (rated at 1/8W).	No	Depends on what happens to R82 when current and power rating are exceeded. Will it open? How long will it take to open?
					Open	Loss of +35V	No	
	U5-16		Ref		Short to gnd	Loss of +35V	No	Possible damage to U5
					Open	Loss of +35V	No	
	R114	RCR50G510JS	Resistor, Composition	51.0, 5%, 1/8W	Short	no impact	No	
					Open	Slight Reduction +35V and output ripple will increase	No	
	R85	RCR50G510JS	Resistor, Composition	51.0, 5%, 1/8W	Short	no impact	No	
					Open	Slight Reduction +35V and output ripple will increase	No	
	R84	RNC50J1002FS	Resistor, Film	10.0k, 1%, 1/20W	Short	Slight Reduction +35V and output ripple will increase	No	
					Open	no impact	No	
	R115	RNC50J1002FS	Resistor, Film	10.0k, 1%, 1/20W	Short	Slight Reduction +35V and output ripple will increase	No	
					Open	no impact	No	
	Q2	171266-005	2N7273	12A, 100V MOSFET	Short D-to-S	Loss of +15V; -15V reduced to less than -1V, loss of +35V	Yes	

	<b>Ref Des</b>	<b>Part No</b>	<b>Part type</b>	<b>Value</b>	<b>Failure</b>	<b>Effect</b>	<b>Condition Matches on Orbit Anomaly</b>	<b>Comment</b>
					Short D-to-G	0.5A increase in +15V current, 7W increase in R114 power dissipation (rated at 1/8W).	No	Depends on what happens to R114 when current and power rating are exceeded. Will it open? How long will it take to open?
					Short G-to-S	Slight Reduction +35V and output ripple will increase; 1.1W increase in R114 power dissipation (rated at 1/8W).	No	Depends on what happens to R114 when current and power rating are exceeded. Will it open? How long will it take to open?
					Open	Slight Reduction +35V and output ripple will increase	No	
Q3	171266-005	2N7273	12A, 100V MOSFET		Short D-to-S	Loss of +15V; -15V reduced to less than -1V, loss of +35V	Yes	
					Short D-to-G	0.5A increase in +15V current, 7W increase in R85 power dissipation (rated at 1/8W).	No	Depends on what happens to R85 when current and power rating are exceeded. Will it open? How long will it take to open?
					Short G-to-S	Slight Reduction +35V and output ripple will increase; 1.1W increase in R85 power dissipation (rated at 1/8W).	No	Depends on what happens to R85 when current and power rating are exceeded. Will it open? How long will it take to open?
					Open	Slight Reduction +35V and output ripple will increase	No	
R62	RCR07G102JS	Resistor, Composition	1.0K, 5%, 1/4W		Short	potential increase in +35V noise	No	
					Open	potential increase in +35V noise	No	
C51	M39014/01-1333	Ceramic	47pF, 10%, 200V		Short	potential increase in +35V noise	No	
					Open	potential increase in +35V noise	No	

	<b>Ref Des</b>	<b>Part No</b>	<b>Part type</b>	<b>Value</b>	<b>Failure</b>	<b>Effect</b>	<b>Condition Matches on Orbit Anomaly</b>	<b>Comment</b>
	C76	M39006/22-0611H	wet tantalum, polarized	33uF, 10%, 75V	Short	+15V will drop down to approximately +7V (U5's UVLO threshold) and limit cycle.	No	The limit cycle is brought about by an over current on the +15V output that pulls it down to the UVLO threshold of U5 at which point the outputs turn off thereby removing the over current condition. The +15V begins to increase since the over current condition clears. The outputs are then free to turn on but are delayed a bit by the soft-start function of U5. Once the outputs turn on the over current condition returns and again pulls down the +15V. This cycle continues indefinitely. Possible damage to CR16 and CR14.
					Open	increase ripple on +35V	No	
	I1	M39010/07A100KP	Inductor	10uH, 10%	Short	potential increase in +35V noise	No	
					Open	loss of +35V	No	
	C109	532857-011065	Multilayer Ceramic	1.8uF, 10%, 100V	Short	+15V will drop down to approximately +7V (U5's UVLO threshold) and limit cycle.	No	The limit cycle is brought about by an over current on the +15V output that pulls it down to the UVLO threshold of U5 at which point the outputs turn off thereby removing the over current condition. The +15V begins to increase since the over current condition clears. The outputs are then free to turn on but are delayed a bit by the soft-start function of U5. Once the outputs turn on the over current condition returns and again pulls down the +15V. This cycle continues indefinitely. Possible damage to CR16 and CR14.
					Open	potential increase in +35V noise	No	

	<b>Ref Des</b>	<b>Part No</b>	<b>Part type</b>	<b>Value</b>	<b>Failure</b>	<b>Effect</b>	<b>Condition Matches on Orbit Anomaly</b>	<b>Comment</b>
	R166	RCR20G512JS	Resistor, Composition	5.1K, 5%, 1/2W	Short	+15V will drop down to approximately +7V (U5's UVLO threshold) and limit cycle.	No	The limit cycle is brought about by an over current on the +15V output that pulls it down to the UVLO threshold of U5 at which point the outputs turn off thereby removing the over current condition. The +15V begins to increase since the over current condition clears. The outputs are then free to turn on but are delayed a bit by the soft-start function of U5. Once the outputs turn on the over current condition returns and again pulls down the +15V. This cycle continues indefinitely. Possible damage to CR16 and CR14.
					Open	no impact	No	
	R156	RNC50J7682FS	Resistor, Film	76.8K,1%, 1/20W	Short	Changes TLM Voltage: +35V Tlm reads full scale	No	
					Open	Changes TLM Voltage: +35V Tlm reads zero	No	
	R167	RNC50J1002FS	Resistor, Film	710.0K,1%, 1/20W	Short	Changes TLM Voltage: +35V Tlm reads zero	No	
					Open	Changes TLM Voltage: +35V Tlm reads full scale	No	
	T6	538445-001	Transformer		Primary adjacent-turn short	150ma increase in +15V current; Slight reduction in 35V output.	No	Shorted turn will dissipate about 2W.
					Secondary adjacent-turn short	115ma increase in +15V current; Slight reduction in 35V output.	No	Shorted turn will dissipate about 1W.

	<b>Ref Des</b>	<b>Part No</b>	<b>Part type</b>	<b>Value</b>	<b>Failure</b>	<b>Effect</b>	<b>Condition Matches on Orbit Anomaly</b>	<b>Comment</b>
					Primary layer-to-layer short	+15V will drop down to approximately +7V (U5's UVLO threshold) and limit cycle.	No	The limit cycle is brought about by an over current on the +15V output that pulls it down to the UVLO threshold of U5 at which point the outputs turn off thereby removing the over current condition. The +15V begins to increase since the over current condition clears. The outputs are then free to turn on but are delayed a bit by the soft-start function of U5. Once the outputs turn on the over current condition returns and again pulls down the +15V. This cycle continues indefinitely.
					Secondary layer-to-layer short	+15V will drop down to approximately +7V (U5's UVLO threshold) and limit cycle.	No	The limit cycle is brought about by an over current on the +15V output that pulls it down to the UVLO threshold of U5 at which point the outputs turn off thereby removing the over current condition. The +15V begins to increase since the over current condition clears. The outputs are then free to turn on but are delayed a bit by the soft-start function of U5. Once the outputs turn on the over current condition returns and again pulls down the +15V. This cycle continues indefinitely.
					Primary-to-Secondary short	Loss of +15V; -15V reduced to less than -1V, loss of +35V	Yes	
					Open winding	Slight Reduction +35V and output ripple will increase	No	

	<b>Ref Des</b>	<b>Part No</b>	<b>Part type</b>	<b>Value</b>	<b>Failure</b>	<b>Effect</b>	<b>Condition Matches on Orbit Anomaly</b>	<b>Comment</b>
	CR14	180616-002	Diode	0.3A, 150V - JANTXV1N6638	Short	+15V will drop down to approximately +7V (U5's UVLO threshold) and limit cycle.	No	The limit cycle is brought about by an over current on the +15V output that pulls it down to the UVLO threshold of U5 at which point the outputs turn off thereby removing the over current condition. The +15V begins to increase since the over current condition clears. The outputs are then free to turn on but are delayed a bit by the soft-start function of U5. Once the outputs turn on the over current condition returns and again pulls down the +15V. This cycle continues indefinitely. Possible damage to CR16.
					Open	+35V DC value slight decrease, output ripple increase	No	
	CR16	180616-002	Diode	0.3A, 150V - JANTXV1N6638	Short	+15V will drop down to approximately +7V (U5's UVLO threshold) and limit cycle.	No	The limit cycle is brought about by an over current on the +15V output that pulls it down to the UVLO threshold of U5 at which point the outputs turn off thereby removing the over current condition. The +15V begins to increase since the over current condition clears. The outputs are then free to turn on but are delayed a bit by the soft-start function of U5. Once the outputs turn on the over current condition returns and again pulls down the +15V. This cycle continues indefinitely. Possible damage to CR14.
					Open	more ripple on 35V	No	
	VR3	524655-009	Zener	18V, 5%, 5W* - JANTXV1N4964	Short	100ma increase in +15V current; Slight reduction in 35V output.	No	OVP
					Open	no impact	No	



## **Attachment 6: Ball Quality Records**





**Ball Aerospace  
& Technologies Corp.**  
Aerospace Systems Division

### Preliminary Failure Report

Number: 2314.019 Rev. -

Page 1 of 2

Project	Project No.	Failure Date MM/DD/YY	Reportable Failure?	Safety Related?
ADVANCED CAMERA	2314	12/4/97	No	No

Test Details				Customer Traceability
MDR	Test Procedure Number:	Rev:	Paragraph No.	Failure Traceability Number:
A92311				

### Configuration Details

System	Component	Assembly	Part
Name	Name	Name	Name
		LVPS No. 3	
Ident No.	Ident No.	Ident No.	Ident No.
		538463-500	
S/N	S/N	S/N	Ckt Ref
	Mfr	Mfr	Mfr
			Generic Mfr Part No.

### Failure Summary

Failure Detected During:	Environment When Failed:	Hardware Level When Failed:	Failure Symptom:	Cause of Failure:
In-Process	Ambient	Assembly	Inoperative ±28 Volt short to GND	Workmanship

### Description of Failure

The +28 volt dc supply was shorted to chassis ground via a solder splash, that connected P1-129 and P1-128 to the thermal plane.

### Detailed Analysis

The thermal plane on this board is not chassis ground until the board is integrated into the higher MEB level of assembly. During this anomaly the +28 volts were connected to the thermal plane at connector pins P1-127, 128, 129, and 130. The +28 volts are connected to P1-128 and 129 via the test set through the test set cable. The solder splash bridged pins P1-128 and 129 to the thermal plane, which also connected pins P-127 and 130 to the thermal plane. All these pins are designed to be floating connections at this assembly level, they were not connected to any circuitry. This short connected the cases of the following parts to +28 volts via the mounting screws on the thermal plane:

Four (4) Interpoint DC/DC Converters  
U1, MFL2805S  
U2, MFL2815D  
U6 & U14, MFL2812S

These DC/DC Converters' cases are isolated from the internal circuitry. No pins/terminals were connected to chassis ground during this level of assembly, except for pin 2 (IN\_COM), where it is tied to ground through two capacitors for EMI purposes. The thermal plane, however, is not a part of the chassis ground at this level, until it is integrated into the next higher level of assembly (MEB). Thus, the thermal plane in this instance was floating. In this configuration, the converter's case was totally isolated from the internal circuitry (these devices are 100% tested for dc isolation by



**Ball Aerospace  
& Technologies Corp.  
Aerospace Systems Division**

**Preliminary Failure Report**

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the manufacturer). These devices could not have been affected as a result of this short.

Two (2) EMI Filters FL1 and FL2, FME28-461

These devices' cases are also isolated from chassis ground during the short, as in the DC/DC Converters' instance.

Two 2N7292 N-Channel power MOSFETS, Q1 & Q4, and two 2N7273 N-Channel power MOSFETS, Q2 & Q3

These FET transistors' terminals are ceramic isolated from their case. They could not have been affected as a result of the short.

Two Relays K6 and K7. These are latching relays with a floating and isolated case. They also could not have been affected as a result of the short.

The +28 volts were still measurable at the location of the short. This implies that there were very little current draw at the time of the anomaly. The test set was current limited to 500 mA, and the power supply did not trip.

Based on this investigation, no parts on this board could have been affected, as electronic parts, with their cases connected to the thermal plane, were isolated from the short. No other hardware were affected, this is the only board that was tested at the time of the anomaly.

---

**Cause of Failure**

The cause of the failure was a solder splash that bridged two pins on a connector.

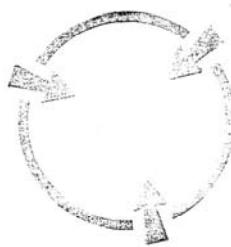
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**Corrective Action, Recurrence Control and Effectivity**

- Detailed visual inspection of every board on the ACS program should be performed before power is applied to prevent similar occurrences. Continuity check between connector pins is another measure that should be undertaken to check for similar shorts before power is applied.

<b>Approval Signatures:</b>	<b>Date</b>	<b>Date</b>
Reliability Engineer F. Sibai	12/4/97	Reliability Manager/Designee R. King
PEQA: J. Meadows		

Distribution: Reliability File  
C&DM



HANDLE PER



Test  
Anomaly  
Work  
Sheet

ITEM NAME & PART NUMBER					
PROCEDURE NO.	TAWS NO	TYPE OF TEST	PROJECT	DATE	PAGE OF
538359	33	MEB 1 Cold Cycle 1 Functional Test	ACS	3/18/98	1 of 1
<b>DESCRIPTION OF ANOMALY:</b> Running section 4.2.22.42 (CEB Load Tests, Step 070, the telenetry monitor J35VCEB1 showed 35.94 V when $35.0 \pm .5$ V was expected. Saw it toggle to 35.42 V and 36.11 Volts.					
ORIGINATOR: J. Puglione			CONCURRENCE: James R. Schmitz		
<b>ACTION TAKEN:</b> (Attach continuation pages as necessary.) - Suspect it's O.K. and just a procedure redline of the tolerance allowed or a calibration problem w/telenetry in database. - At the Load Box, the Voltage measured 35.68 V which is well within the $\pm 2.0$ Volt spec in the procedure. This being the case, we continued test.					
TEST CONDUCTOR: J. Puglione			QUALITY CONTROL: JRM		
<b>ANALYSIS AND CONCLUSION:</b> 35V CEB supply runs a little higher than exactly 35V, due to its load conditions. The safety limit is set at 37.5. The procedure needs to be redlined to open the tolerance to $35.5 \pm 1$ V.					
RETEST: <input type="checkbox"/> CONTINUE TEST <input checked="" type="checkbox"/> TRANSFER TO MDR NO. _____ OTHER <input type="checkbox"/> (EXPLAIN) _____					
TEST CONDUCTOR:			PEQA:		
FINAL: <input checked="" type="checkbox"/>			REVIEW AND APPROVALS:		
APPROVE <input checked="" type="checkbox"/>			SYSTEM ENGINEER: <i>James R. Schmitz</i>		
DISAPPROVE <input type="checkbox"/>			PEQA: <i>John Meadow</i>		

BR-527 2/84





Test  
Anomaly  
Work  
Sheet

ITEM NAME & PART NUMBER						
PROCEDURE NO.	TAWS NO	TYPE OF TEST	PROJECT	DATE	PAGE OF	
538359D	78	MEB2 Hot Cycle	ACS	4/10/98	1 of 3	
<b>DESCRIPTION OF ANOMALY:</b> lost +15 V f-15V, and +35V CEB voltages during the hot soak - possible loss of +15V converter						
ORIGINATOR: Randy Stevens			CONCURRENCE: Steve Arslanian			
<b>ACTION TAKEN:</b> (Attach continuation pages as necessary.) dumped ESB, extracted BSS data test stopped, safed and powered down						
TEST CONDUCTOR:			QUALITY CONTROL:			
<b>ANALYSIS AND CONCLUSION:</b> Found that the 35 V transformer was overheated & shorted. The cause of this problem was found to be related to the 35 V sync pulse that controls the PWM. See attached write up.						
RETEST	<input type="checkbox"/>	CONTINUE TEST	<input checked="" type="checkbox"/>	TRANSFER TO MDR NO.	_____	
OTHER	<input type="checkbox"/>	(EXPLAIN)	Changed Transformer and resistor			
TEST CONDUCTOR:	PEQA:					
FINAL:	REVIEW AND APPROVALS:					
APPROVE	<input checked="" type="checkbox"/>	SYSTEM ENGINEER: <u>J. R. Silve</u>				
DISAPPROVE	<input type="checkbox"/>	PEQA: <u>J. Meadow</u>				

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Test  
Anomaly  
Work  
Sheet

ITEM NAME & PART NUMBER					
PROCEDURE NO.	TAWS NO	TYPE OF TEST	PROJECT	DATE	PAGE OF
538359(D)	81B	MEB 2 FT HotCycle 1 Retest	ACS	4/15/98	1 of 4
DESCRIPTION OF ANOMALY: 3 minutes after enabling CEB relay MEB safed due to CEB +35V out of limits too many consecutive times (ESB 402, p. 3015' actual.)					
ORIGINATOR: J. Pugliano			CONCURRENCE:		
ACTION TAKEN: (Attach continuation pages as necessary.)  - Stopped Test - Instructed Thermal Chamber Ops folks to return chamber to ambient for troubleshooting next day - Appears that the problem that caused TAWS 78 is still there and is thermally related					
TEST CONDUCTOR: J. Pugliano			QUALITY CONTROL:		
ANALYSIS AND CONCLUSION: same as TAWS 78. See attached analysis & conclusion					
RETEST: <input checked="" type="checkbox"/>	CONTINUE TEST <input type="checkbox"/>	TRANSFER TO MDR NO. _____			
OTHER <input checked="" type="checkbox"/>	(EXPLAIN) _____	changed Resistor value.			
TEST CONDUCTOR:		PEQA:			
FINAL: APPROVE <input checked="" type="checkbox"/> DISAPPROVE <input type="checkbox"/>		REVIEW AND APPROVALS: SYSTEM ENGINEER: <u>Jerry L. Shen</u> PEQA: <u>JMudrow</u>			

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TAWS & LK

## +35 V Bias Converter Anomalies and Resolution

April 16, 1998

Notification was made that the LVPS3 board, located in MEB 2 (LVPS 1) had shown an overvoltage condition on the +35 Volt output while the MEB2 was in thermal test. The MEB had been raised to approximately 50 degrees C with all power off, then power was enabled to all circuits in the LVPS. The SITS had been programmed to SAFE the MEB if it detected a high voltage (greater than approx. 39 volts) on the 35 Volt output. The safing process was programmed to respond if the excessive voltage was detected three times in succession. When power was applied, this condition was detected, with the voltage at approximately 40 volts. The MEB was immediately safed, and operations suspended.

The detected condition was similar to a condition that had previously been observed for the +35 Volt converter. In the previous incident, it was determined that the T6 transformer in the 35 volt converter had seen temperatures that were high enough to damage the transformer. When the LVPS3 board was removed from the MEB, the transformer was visually inspected, and it was determined that there was no evidence of overheating.

An extender card was inserted into the MEB, and the load resistors for the 35 volt output was measured. The resistances were 700 ohms (Minimum load), 350 ohms (nominal load), and 234 ohms (Maximum load). These values are consistent with the expected current loads of 50, 100, and 150 milliamperes.

The LVPS3 card was taken to the ACS lab and plugged into the LVPS test set, which contained an EMU LVPS1 card. When power was applied, the output of the 35 volt converter was measured at 35.99 volts. In an attempt to recreate the anomalous voltage that was observed in the thermal chamber, an ionized blower was aimed at the suspect area, and the blower was set for heated air. Additionally, hot air from a heat gun was aimed through the ionized air stream at the suspect circuitry. A thermocouple temperature sensor was taped to the Q3 transistor so temperature could be monitored (see SC538463, sheet 3, zone 4/B). As the temperature at Q3 approached 50 degrees C, it was noted that the measured voltage went down to 35.91 volts. This is consistent with an increase in  $R_{dsOn}$  for the Q2 and Q3 FETs. During this time, an oscilloscope was monitoring the waveform at TP45. The waveform during the test remained nominal.

At that time, the decision was made to remove the Flight LVPS3 board from the LVPS Test set, and replace it with an EMU board. The EMU LVPS1 board was also installed on an extender card. Power was applied to the two boards, and the 35 volt output was monitored, as was the waveform at TP45. At ambient temperature, the frequency of the waveform at TP45 was measured at 64.9 kHz, indicating that the Phase-Locked Loop on the LVPS1 board was operating at 519.5 kHz (8 times the TP45 frequency). The heat gun was used to raise the temperature of the R49 resistor, while the thermocouple was used to monitor the temperature in the area of R49. Nearly as soon as heat was applied to R49, the waveform on the oscilloscope was observed as behaving erratically, and the voltage output measured by the DVM was also seen to be behaving erratically. The voltage was measured at several different levels, but 39+

volts was noted several times. The waveform frequency was measured during this time, and was found to be approximately 63.3 kHz, which translates to 506.3 kHz at the PLL. When the temperature of R49 was increased further, the TP45 waveform was observed in a double-pulse condition, that is, almost as soon as it switched OFF, it would turn back ON for another period. Unfortunately, there was no opportunity to capture any of the waveforms. During the “double-pulse” time, the output voltage was measured as high as +45 volts. **This double-pulse condition will have a nasty effect on the performance of the transformer. The extra-long ON period will allow the transformer core to saturate, resulting in a large increase in current through the transformer windings. The increased current flow will cause a temperature increase in the transformer.** Over time, the transformer temperature will increase to the point that the coating on the magnetic wire will melt and windings will begin to short out, resulting in a death spiral for the transformer.

Power was then removed from the boards under test, and jumper JP13 on LVPS3 was cut. This removed the external sync signal from the (U5) SG1525A PWM circuit, allowing it to operate at its own frequency. The free-running frequency is determined by R154 and C87. Using the TP45 waveform on the oscilloscope, the free-running operating frequency was measured at 129.87 kHz (2 times the TP45 frequency). This is essentially the same as the frequency supplied by the PLL. As JP13 was opened and closed, the only difference observed in the TP45 waveform was a slightly “cleaner” waveform when JP13 was closed. There was no discernible difference in frequency. For proper operation of the SG1525A circuit, it is important that the free-running frequency **ALWAYS** be lower than the external sync frequency.

Power was again removed from the boards, and the R154 resistor (10 k ohms) was opened and replaced by a decade resistor box set at 11K. Power was re-applied, and the TP45 waveform frequency was measured. The free-running frequency was calculated at 117.6 kHz, which would translate into an allowable 470.4 kHz PLL frequency. The decade box was changed to 12 k, and the free-running frequency was measured at 108.7 kHz, translating into a 434.8 kHz frequency allowable from the phase locked loop. At this frequency, the TP45 waveform showed no signs of degradation, the output voltage was measured at 35.9 volts, and the R49 resistor on the LVPS1 board could be heated to greater than +65 degrees C with no effect on the TP45 waveform.

**Based on these tests, the decision was made to permanently change R154 to a value of 12.1 k ohms on both of the Flight LVPS3 boards. This is a mandatory change.**

Because of the conditions observed during the second temperature test of the LVPS3 board in MEB2, and the short period of time that the +35 volt output was in an anomalous condition, there was not enough time to overheat the T6 transformer. In my opinion, no components were overstressed.

During testing, the following points on the Flight LVPS3 board were probed through the conformal coat: Q2, pins 1 and 2; Q3, pins 1 and 2; TP8, TP45, and TP48. Also, it appears that the connecting wires on Q3 pins 1 and 2 are extremely close to touching.



MATERIAL(S) DISCREPANCY REPORT  
AND RELIABILITY DATA REPORT

Page 1 of \_\_\_\_\_

MDR A 92365

Part No. 538450-501	Part Name MEB Assy	Supplier Name & Number BATC	
Serial/Lot # 0001	Project # 20314	Order # 4560D op 48 8	
Lot/Qty 1	Qty Insp. 1	Qty/Rej 1	
SPECIFICATION DESCRIPTION		DEFECT DESCRIPTION	
TP 538359 Para 4.2, 22.4, 2-030 Should measure CEB load test current ≈ 500 mA		measured 56 mA ohm milli check shows +15V CEB Converter is 1 ohm to ground.	
Type of Test/Inspection: Functional Test Thermal Cycle Hot operate	Environment: Static Sensitive Clean Thermal Cycle Hot operate		
Insp Procedure/Spec T0538359	Reject Stamp No. 30	Date 4-13-98 QA Representative John Meadow	Refer to Q/E Yes <input checked="" type="checkbox"/> No <input type="checkbox"/>
Direct Cause T6 component failure.		Organization/Department Causing Defect: T6 Manufacturer	
Defect Disposition Interim Disposition ① shut down MEB and Ramp temp to ambient. Interim ② Notify Reliability of failure. Interim ③ Remove LVPS 3 PWA from MEB perform visual for possible cause. Interim ④ Troubleshoot to determine cause. John Meadow 98-4-13 Results see attached Memo: Rework U2-7 Rework by removing and replacing T6, R84, R82, U4, C50, Q2 Touch up conformal coat on these components and those points listed on the memo. Route T6 to reliability for failure analysis. Interm ⑤ Check John Meadow 98-4-14 CR16 CR14 for function. Results: diodes OK Continuous w/tests - See continuation sheets.			
Acceptable per Inspection/Test - Meets Dwg Reqmts:		Qty <input type="text"/>	MRB Req'd Yes <input checked="" type="checkbox"/> No <input type="checkbox"/>
Use as is <input checked="" type="checkbox"/>	Rework to Dwg Rev A.	Other as Specified Above	Scrap
Reject	Refer to Purchasing	Retest/Reinp/Repair	Initial for Approval Customer BALL
Customer Rep Sign & Date N/A	Design Sign & Date N/A	Quality Assurance Sign & Date John Meadow	
Corrective Action WA538463-500 Rev A.			
John Meadow Sign & Date: 98-5-27		Dwg Change to be Made Yes <input type="checkbox"/> No <input checked="" type="checkbox"/> None	
CA To Be Completed By N/A	CA Responsibility N/A	Shipping Order	
Date: S/N: Lot No.	Person: Org:		

BR/4/067 4-89



### **Material(s) Discrepancy Report**

Continuation Sheet

Page 2 of

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Retain Original — Record Copy

BB-067-1 5/84



**Ball Aerospace  
& Technologies Corp.**

### Failure Report

No: 20314.024 Rev. -

Page 1 of 2

Project	Project No.	Failure Date MM/DD/YY	Reportable Failure?	Safety Related?
ADVANCED CAMERA	20314	4/13/1998	No	No

#### Test Details

#### Customer Traceability

MDR A92365	Test Procedure Number: 538359	Rev:	Paragraph No. 4.2.22.4.2-030	Failure Traceability Number:
---------------	----------------------------------	------	---------------------------------	------------------------------

#### Configuration Details

System	Component	Assembly	Part
Name	Name Main Electronics Box (MEB) 1	Name LVPS 3 PWA	Name
Ident No.	Ident No. 538450-501	Ident No. 538463	Ident No.
S/N	S/N 0001	S/N 0001	Ckt Ref
	Mfr BATC	Mfr BATC	Mfr
			Generic Mfr Part No.
			Part S/N:
			Part Date Code:

#### Failure Summary

Failure Detected During:	Environment Temp:	Environment When Failed:	Hardware Level When Failed:	Failure Symptom:	Cause of Failure:
Pre-Acceptance	Thermal-Vacuum	Component	No Output	Part Failure	

#### Description of Failure

During the hot portion of the MEB thermal cycle test, the test current measured 56mA, it should be around 500mA.

#### Detailed Analysis

Further troubleshooting revealed that the +15 volt CEB DC/DC Converter output is 1 ohm to ground. This converter is on the LVPS 3 PWA. Trouble shooting found that the transformer T6 was shorted and exhibited extensive heating. The transformer was removed from the circuit and the initial condition went away. After further analysis R84, R82, U4, C50, & Q2 were further replaced due to possible overstress. After rework the MEB Thermal Cycle Test was repeated. At approximately 50 degrees C the power was enabled to the LVPS again. At this point a similar condition as the first failure occurred. This test was performed however with a "safing process" that forced a "shut-down" of the test if more than +39V was detected on the +35V line. The LVPS 3 was removed at this point and another inspection of T6 was made. There appeared to be no adverse effects (i.e. heat) evident. Further test evaluation was made of the LVPS 3 on the bench while applying heat (approx. 50 degrees C) to various associated parts in the circuit. It was found that when R49 was raised in temperature both the waveform at TP45 behaved erratically, as well as the output voltage measured on the DVM also became erratic. Upon an increase of temperature to R49 it was observed that the waveform at TP45 would double-pulse. This condition would cause the transformer T6 core to saturate,



**Ball Aerospace  
& Technologies Corp.**

**Failure Report**

Number: 20314.024 Rev. -

Page 2 of 2

resulting in an increase of current through the windings, and thus an increase in operating temperature. This over the course of time would eventually cause damage to the transformer magnet wire insulation, resulting in a short circuit condition. Resistor value of R154 will change the driving frequency output to the transformer. After experimentation, the value for R154 was changed to 12.1 K to lower the initial frequency. After this change no other erratic conditions were observed on the +35V line, or in the frequency to T6 while elevating the temperature to R49. A mandatory design change was made on both Flight LVPS3 boards and R154 was changed to a 12.1K resistor. Since the second event of this original failure was performed using voltage limitation controls it is believed that no other components were overstressed, so there is no need to replace any parts other than R154.

---

**Cause of Failure**

R154 in the original design was too low in value to provide a driver frequency to T6 that would be compatible at elevated temperature operation.

---

**Corrective Action, Recurrence Control and Effectivity**

EO issued to change the value of R154 from 10K ohms to 12.1K ohms. All parts believed to have been overstressed were replaced.

<b>Approval Signatures:</b>	Date		Date
Reliability Engineer F. Sibai	4/13/1998	Reliability Manager/Designee R. King	
PEQA: J. Meadows			

Distribution: Reliability File  
C&DM

A/N 8640/4

BR-04, 8/89

JUL-18-2006 12:04 From:BATC AR744

303 939 7451

To:301 286 1779

P.2/2



## MATERIAL(S) DISCREPANCY REPORT

Page 1 of \_\_\_\_

### AND RELIABILITY DATA REPORT □

MDR A 92295

No WA538463	Part Name LVPS No.3 PWA	Supplier Name & Number Jackson & Tull
Serial/Lot # 0001	Project # 20314	Order # 8767 B
Qty/Qty	Qty Insp	Qty/Rej
1	1	1
Lot Rejected Yes <input checked="" type="checkbox"/> No <input type="checkbox"/>		Item Location RA 2 insp.

#### SPECIFICATION DESCRIPTION

Workmanship DWG note F13.7  
install nut plates per BPS 1.04 except  
use existing holes.

#### DEFECT DESCRIPTION

PWB around rivets - damaged MP1ThnMP4  
crushed and split. nut plates warped (slightly)  
Board separated at Ground/Thermal plane and  
fiberglass Board. Separation confined to edge of board.  
two rivets almost touching via's

Type of Test/Inspection Workmanship	Environmental Static Sensitive
Test Procedure/Spec DWG	Reject <input type="checkbox"/> Yes <input checked="" type="checkbox"/> Stamp No 1 Date 11/10/97 QA Representative John Meadow
Defect Cause J&T personnel used improper set up of riveting press	Refer to Q/E Yes <input checked="" type="checkbox"/> No <input type="checkbox"/> Organization/Department Causing Defect Jackson & Tull

Defect Disposition Intake: Refer to M&P for recommended disposition. John Meadow 97-11-12  
Via's in that area are to chassis ground - rivets are to chassis ground. - no effect if they touch  
OK to continue processing. Repair separated edges by injecting BPS 26.05 Type II, Class 3,  
grade A, Style A, Clamp edges during cure. USE AD 13 Crazing at rivet holes  
Design Lini created 12/14/97 PEQA. John Meadow 12-4-97 DCMC Standard 97/06

Thermal dissipative surface plane is clamped to PWB by the nut plates and rivets for mechanical  
support and will prevent propagation of the separation.

Acceptable per Inspection/Test - Meets Dwg Requirements.		Qty <input type="checkbox"/> MRB Read Yes <input checked="" type="checkbox"/> No <input type="checkbox"/>
Use as is	Rework to Dwg	X Other as Specified Above
Reject	Refer to Purchasing	Anlysis/Rmp/Repair
Customer Rep. Ray Colucci	Sign & Date 11/10/97	Initial for Approval Customer BALL
	John Johnson 98-2-12	Quality Assurance Sign & Date John Meadow 97-12-

Corrective Action J&T personnel used manual press on subsequent PWAs

CA To Be Completed By N/A	CA Responsibility Y/A	Dwg Change to be Made Yes <input type="checkbox"/> No <input checked="" type="checkbox"/>
Date S/N	Lot No.	Org
Shipping Order 08/4/007		

JUL 18 2009 14:33

303 939 7451

PAGE.22



## **Attachment 7: Interpoint Converter Quality**





## **Quality Differences, Quality Screening, and Parts Burn-In**

Noman Siddiqi



## Interpoint Converters

### MFL and SMFL DC to DC converters



- Interpoint makes two types of converters.
  - 1) Space Grade: QML Class K and Class H
  - 2) Military Grade: MIL-STD-883 Class H parts
- Space Grade Parts manufactured in Interpoint Redman, WA
- Military Grade parts manufactured in Taiwan

Interpoint P/N	Generic #	Lot Date Code
5962-9316301HXC	MFL2805S	9442
5962-9319301HXC	MFL2815D	9443
5962-9316101HXC	MFL2815S	9442
5962-9316201HXC	MFL2812S	9442
<b>5962-9319301HXC</b>	<b>MFL2815D</b>	9846,47,49,51
5962-9316301HXC	MFL2805S	9506
5962-9316101HXC	MFL2815S	9846,48,49,9905,9911
5962-9316301HXC	MFL2805S	9848
5962-9316101HXC	MFL2815S	9846,48,49,9905,9911
5962-9316201HXC	MFL2812S	9445

All of the HST existing Interpoint parts have been verified by Interpoint to be /883 Military Grade, built in their Taiwan facility



## Interpoint Converters



### **Interpoint Class K -**

Highest Reliability with All Quality Control By QML Manufacturer as required By  
MIL-PRF-38534

### **Interpoint Class H -**

High Reliability with All Quality Control By QML Manufacturer as required By MIL-  
PRF-38534

### **Interpoint Class H /883 -**

Reliability based on Manufacturer Quality Control as required By MIL-STD-883



## Interpoint Converters

	MIL-PRF-38534	MIL-PRF-38534	MIL-STD-883
	Interpoint Space Class K	Interpoint Space Class H	Interpoint Military Class H /883
Serialization	Allows traceability of electrical tests results	Required	Required
Element Evaluation	Requires 100% die electrical and visual inspection.  Each element lot in Hybrid screened and qualified	Requires 100% die electrical and visual inspection.	Requires 100% die electrical and visual inspection.
SEM Inspection	Performed on each lot of Semiconductor and Microcircuit	Not Required	Not Required
Non Destructive Bond Pull Test	100 percent non-destructive bond pull test performed	Not Required	Not Required
Destructive Bond Pull Test	Required	Required	Required
Internal visual	Required	Required	Required
Pre-Cap Inspection	Required	Required	Not Required
Temperature Cycling	Required	Required	Required
PIND	Required	Not Required	Not Required
Pre-Burn-in Electrical	Required	Required	Required
Burn-in	Required - 240 hours	Required – 160 hours	Required – 160 hours
Final Electrical	Required	Not Required	Not Required
Seal Test	Required	Required	Required
External Visual	Required	Required	Required



## Interpoint Converters



- **Interpoint Space Grade Class K Product Provides:**

- 1) 100% Screening testing of each element Lot.
- 2) Qualification on sample Lot.
- 3) Serialized test data.
- 4) SEM inspection on each Microcircuit and Semiconductor Lot.
- 5) 100% Non-Destructive Bond Pull Testing.
- 6) 100% Radiation performed on each element to meet Class K "R" level radiation requirements

- **Interpoint Class H**

- 1) 100% visual Inspection of each lot
- 2) Die level electrical testing.
- 3) 100% Radiation performed on each element to meet Class K "R" level radiation requirements

- **Interpoint Class H /883**

- 1) 100% visual Inspection of each lot
- 2) Die level electrical testing.



## Interpoint Converters



### MTBF Calculations

MIL-HDBK-217F

#### SMFL2812D MTBF CALCULATIONS - SPACE QUALITY (Class K)

$\pi^0$	0°C	25°C	50°C	75°C	100°C	125°C
S <sub>F</sub>	8,881,523	5,415,619	3,214,842	1,716,668	7,895,254	326,601

#### MFL2812D/883 MTBF CALCULATIONS - MILITARY QUALITY

$\pi^0$	0°C	25°C	50°C	75°C	100°C	125°C
S <sub>F</sub>	2,220,381	1,353,905	803,710	429,167	197,313	81,650



## Interpoint Converters



### Critical Parts

Element Part Number	Test Level	Class KR/HR	Class H	/883
IRFC7130	K Rad hard	Yes		
IRF130	H tested		Yes	Yes
SC125H100S	K tested	Yes		
SC125H100S	H tested		Yes	Yes
LM136-2.5	K rad tested	Yes		
LM136-2.5	H tested		Yes	Yes
MC35072	K rad tested	Yes		
MC35072	H tested		Yes	Yes
LM119	K rad tested	Yes		
LM119	H tested		Yes	Yes
MC34161	K rad tested	Yes		
MC34161	H tested		Yes	Yes
TC4429	K rad tested	Yes		
TC4429	H tested		Yes	Yes
Ceramic Caps	K tested	Yes		
Ceramic Caps	H tested		Yes	Yes
Tantalum Caps	K tested	Yes		
Tantalum Caps	H tested		Yes	Yes



## Interpoint Converters



### Summary

- Use of Interpoint Class K DC-DC Converters will provide Maximum Quality and Reliability of the end item.
- Use of Interpoint Class H DC-DC Converters will provide Good Quality and Reliability of the end item.
- Use of Interpoint Class H /883 DC-DC Converters will provide some Quality and Reliability of the end item.

## Attachment 8: Space Weather



**Space weather was clear at time of ACS suspend  
event on June 19, 2006**

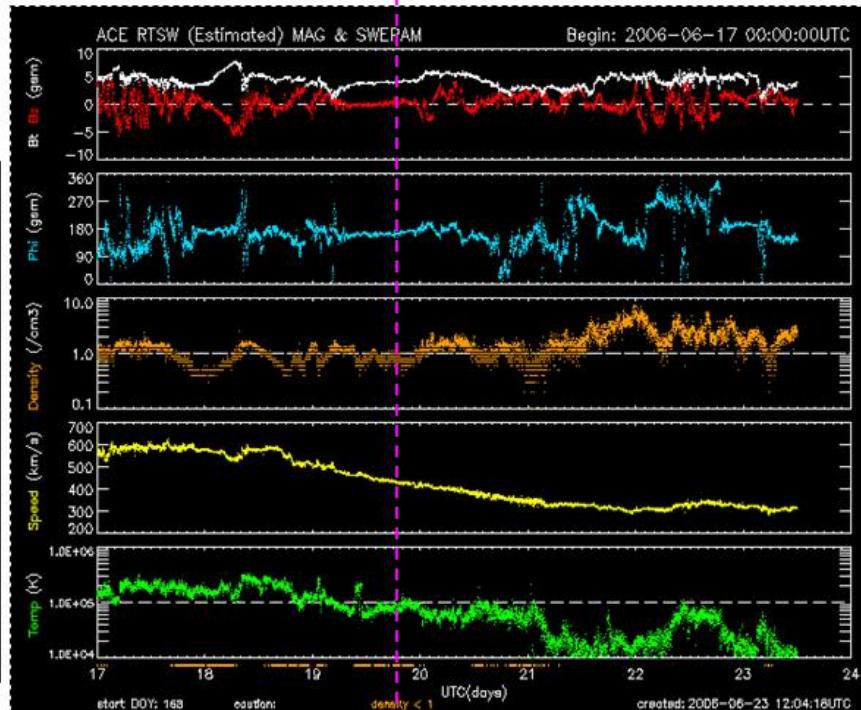
Mal Niedner

for the ARB

## Solar-wind & IMF parameters

### Comments on conditions near June 19.72 UT

- Plasma and field parameters normal and well-behaved
- Earth region was on trailing edge of high-speed stream, densities were low ( $< 1 \text{ cm}^{-3}$ )
- Quiet conditions consistent with lack of interplanetary shocks and strong X-ray flares (cf. next charts)

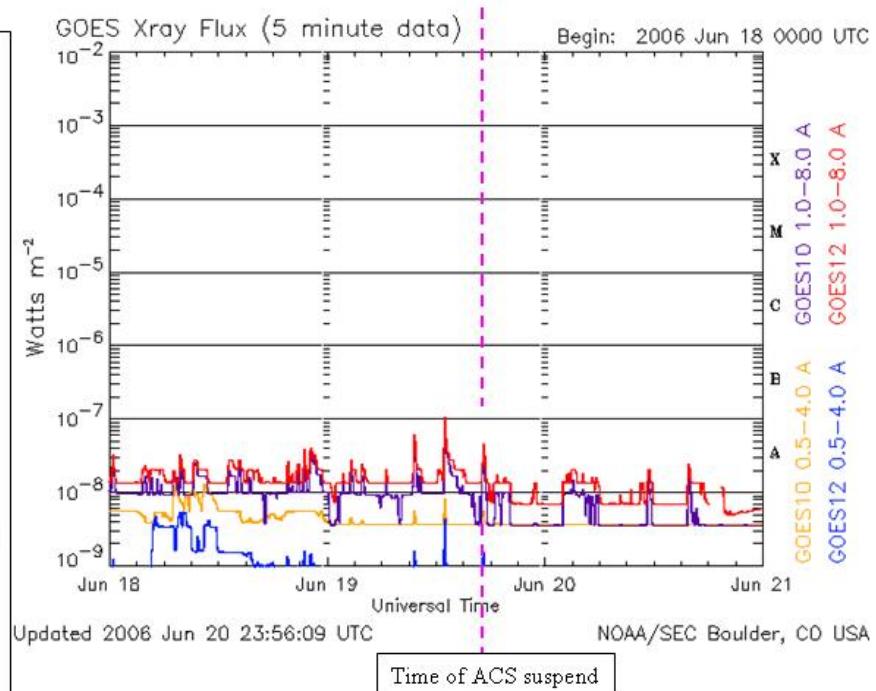


Time of ACS suspend

## X-rays and Flares

### Comments:

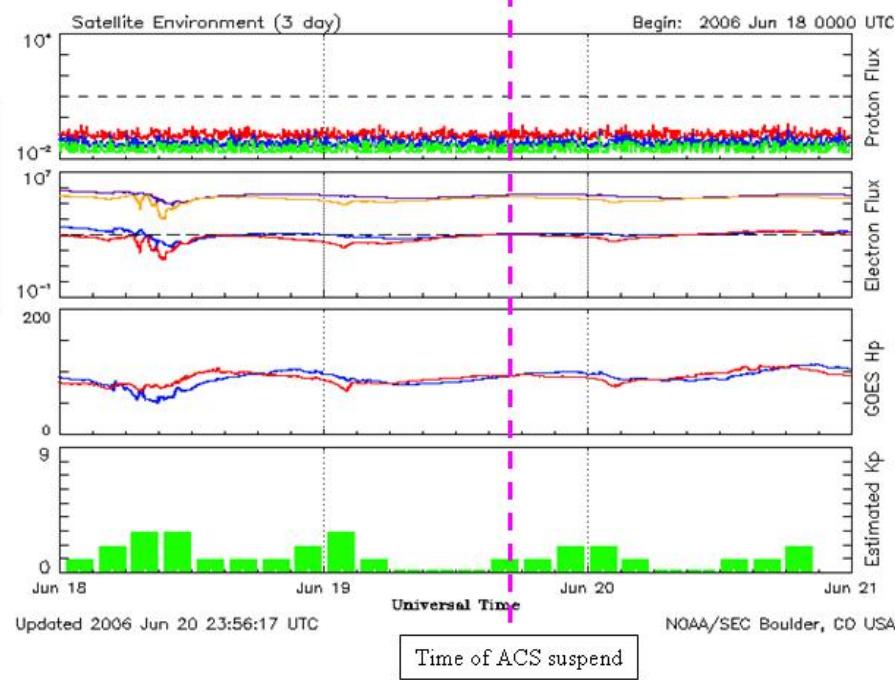
- the X-ray sun was not very dynamic on June 19
- there were two reported “events” for June 19, one several hours before the suspend (a very weak B-class flare), and an even weaker A-class flare more or less coincident with the ACS suspend
- it is well-established that the magnetospheric response to flares is already extremely weak by the time class C is reached (cf. right ordinate); A & B flares are orders of magnitude weaker yet



## Energetic protons, electrons, magnetospheric field strength and variability

### Comment:

- nothing stands out as significant near June 19.72 timeframe



# Conclusion

- No case to be made that interplanetary and/or magnetospheric conditions were possible contributors to the ACS suspend event on June 19.72 UT





## **Appendix B:**

*Anomaly Review Board (ARB) Final Report, Advanced Camera for Surveys Side  
2, June 1 2007*

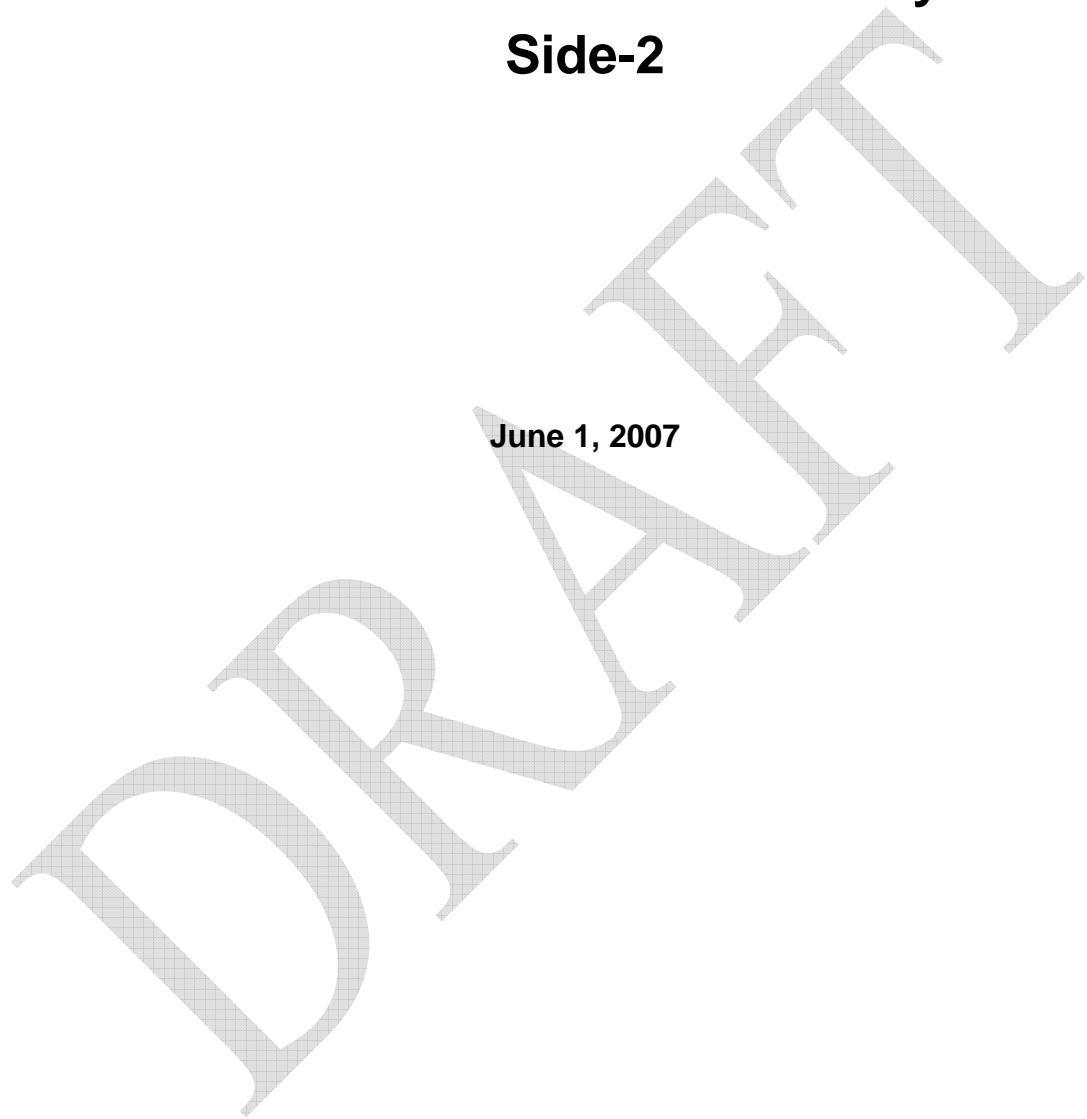
# **Anomaly Review Board (ARB)**

## **Final Report**

### **Advanced Camera for Surveys**

#### **Side-2**

**June 1, 2007**



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LM IS&S/Code 441  
HTSI/Code 441  
Code 441  
J&T/Code 442  
LMTO/Code 442  
Code 546  
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Code 581/441  
Code 303/442  
Code 667/440  
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Code 563  
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BATC  
Vantage Systems/Code 442  
BATC  
LMTO/Code 442  
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LMTO/Code 442  
BATC  
LMSS  
LMTO/Code 442  
QSS  
Code 303/442  
RSTX/Code 442  
BATC  
SSI/Code 442  
LMTO/Code 442



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DRAFT

## Acronyms

ACR	Autonomous Command Response
ACS	Advanced Camera for Surveys
CEB	CCD Electronics Box
CS	Control Section
DMS	Data Management System
EMI	Electromagnetic Interference
ESB	Executive Status Buffer
ESM	Electronics Support Module
FGS	Fine Guidance Sensor
FHST	Fixed Head Star Tracker
FPS	Focal Plane Structure
GPEFP	General Purpose Event Flag Processor
GS	Guide Star
HRC	High Resolution Camera
HST	Hubble Space Telescope
HV	High Voltage
HWSP	Hardware Sunpoint
I&C	Instrumentation & Communications
LVPS	Low Voltage Power Supply Board
MEB	Main Electronics Box
MSR	Mission Support Room
MSS	Magnetic Sensing System
NCC	NICMOS Cryo-Cooler
NCS	NICMOS Cooling System
NICMOS	Near Infrared Camera & Multi-Object Spectrometer
NSSC-1	NASA Standard Spacecraft Computer - 1
OTA	Optical Telescope Assembly
PCS	Pointing Control Subsystem
PDU	Power Distribution Unit
RIU	Remote Interface Unit
RSU	Rate Sensing Unit
RTCS	Relative Time Command Sequence
SAA	South Atlantic Anomaly
SBC	Solar Blind Channel
SDF	Science Data Formatter
SES	Secondary Electronics Section
SI	Science Instrument
SOC	State of Charge
SPA	Solar Panel Assembly
STIS	Space Telescope Imaging Spectrograph
STScI	Space Telescope Science Institute
STOCC	Space Telescope Operations Control Center
TEC	Thermo-Electric Cooler
TPS	Total Pressure Sensor
VEST	Vechicle Electrical Systems Test (facility)
VSTIF	VEST Software Test and Integration Facility
WFC	Wide Field Camera
WFC3	Wide Field Camera 3
WFPC-2	Wide Field Planetary Camera-2



## 1 Event Summary

On January 27, 2007 at 7:34:38 a.m. EST, the Hubble Space Telescope (HST) entered Inertial Hold Safe Mode. The first indication of trouble came at 07:34:17 EST in the form of a brief, transitory (~2 second) increase in load and structure current. Engineering data then show the spacecraft structure current rising from zero to a peak above 15A as the HST load current simultaneously rose by roughly 37A between 07:34:21 and 07:34:28 EST. The Advanced Camera for Surveys (ACS) experienced a loss of power from the Power Distribution Unit supporting ACS Side-2. As the structure and load currents began rising, the Total Pressure Sensor (TPS) installed with the Near Infrared Camera & Multi-Object Spectrometer (NICMOS) Cryo-Cooler (NCC) began sensing and reporting an anomalous increase in pressure inside the HST Aft Shroud. The pressure briefly increased about 700-fold to more than 0.0001 torr, causing multiple TPS limit violations. In response, payload and spacecraft commands were issued to safe the NCC and place HST into Inertial Hold.

## 2 ARB Charter

1. Assess the risks, if any, of operating the ACS Solar Blind Channel on Side 1.
2. To the extent practicable, determine the condition of ACS Side-2 and the Power Distribution Unit fuse that provides input power to ACS Side-2.
3. Assess the risks and benefits of diagnostic flight testing of ACS.
4. If possible, identify the reason for the January 27, 2007 anomaly.
5. Assess whether the anomaly stressed any of the remaining ACS components (Side 1, Side-2, and common).
6. Assess whether the anomaly was a significant source of contamination to ACS, the other science instruments, or to the HST Optical Telescope Assembly.
7. If identified, assess whether the cause of the ACS anomaly is a failure mode that is present in any of the other HST instruments, especially COS and WFC3.

## 3 Executive Summary of ARB Findings

On January 27, 2007, the Hubble Space Telescope (HST) entered Inertial Hold Safe Mode. The entry was caused by an increase in pressure detected by the TPS in the NICMOS Cooling System (NCS). The TPS was designed to detect a Neon leak in the NCS; however it will measure any pressure increase in its vicinity within the HST aft shroud.

Subsequent analysis of the safing event showed that the source of the anomaly was not in the NCS, but in the Advanced Camera for Surveys (ACS). The ACS experienced a failure while operating on its Side-2. This failure drew sufficient current to clear the PDU2 fuse as well as produce significant outgassing that was detectible in the aft shroud by the TPS in the NCS. The details of the anomaly timeline and recovery of HST from the safing event are detailed in Section 4 on page 18.

Since the anomaly produced measurable outgassing, the ARB assessed the risk of contamination to the HST observatory as well as the ACS instrument. A contamination model was created to

predict the amount of contaminants released during the anomaly. The model correlated the pressure curve measured by the NCS TPS, the current draw seen during the anomaly, and the venting characteristics of the ACS Main Electronics Box (MEB), ACS, the Aft Shroud, and HST. Contamination analysis suggested that a sizeable portion of a circuit board could have been heated, resulting in the decomposition of the circuit board, conformal coating, epoxy, and component cases. Most contaminants that would have affected other HST optics would have condensed on surfaces within the ACS MEB cavity or on the Aft Shroud walls. Contamination analysis predicted little affect on HST optics. This was later confirmed with ultraviolet (UV) images taken with the Wide Field Planetary Camera 2 (WFPC2). When ACS operations were resumed on Side-1 with the Solar Blind Channel (SBC) detector, additional SBC images also confirmed no measurable contamination. For additional details on the contamination analysis refer to Section 5 on page 22.

The ARB electrical analysis focused on the various signatures of the fault:

- An initial glitch of current to HST structure
- A rising fault current at a rate of 5 amps per second
- A noisy fault current at about 15 amps peak-to-peak
- A sustained fault current of about 37 amps prior to the PDU fuse clearing
- Sufficient gas released to raise pressure to the milliTorr range
- Fault current bridges primary power, return, and chassis
- Fault occurred about 5000 hours after switching ACS operations to Side-2.

An analysis of the various electrical components showed that the most likely candidates for a component failure were wet tantalum capacitors, EMI filters, or Interpoint power converters. These components were used on all three Low Voltage Power Supply (LVPS) boards and in the Auxiliary Power Box (APB), which powers the Anneal heaters. Since the current draw was 37A and current was seen by the HST structure current sensor, the ARB concluded that the electrical fault would be on the primary side of either the Hold converter or the Operate converter. Additional analysis of secondary voltages prior to the fuse clearing confirmed the conclusion that the fault was on the primary side of the Hold or Operate converter. The ARB identified a total of 47 suspect electrical devices: 29 on the Hold bus and 18 on the Operate bus. For additional details of the electrical analysis, see Section 6 on page 27.

The ARB assessed the risk of returning to SBC-only operations on ACS Side-1. Of particular concern was the fact that the LVPS Side-2 electronics resided in the same physical box as the Control Section (CS) Side-1 electronics. Likewise, for the APB, both the Side-1 and Side-2 electronics reside in the same physical box. Was it possible for a failure on Side-2 to adversely affect Side-1 (e.g., could sputtered material from Side-2 cause a short on Side-1)? The ARB determined that both the MEB and APB boxes contain partitions that completely separate the Side-1 and Side-2 components. In the MEB the only path for sputtered material would be out of the MEB vent holes from the LVPS Side-2 section and into the MEB vent holes of the CS Side-1 section. This highly circuitous path of sputtered material was deemed to be highly unlikely. As shown by previous contamination analysis, most material would likely be deposited on the walls of the LVPS Side-2 cavity.

A similar analysis was done for the APB. Unlike the MEB, the APB has no vent holes. The only path from Side-2 to Side-1 would be through the connectors, which was highly unlikely. Thus, the ARB determined it was safe to resume SBC-only operations on Side-1.

ACS was switched back to Side-1 SBC-only operations on February 16, 2007. Stored commanding of ACS resumed with the SMS beginning February 19. ACS SBC images taken February 20 successfully supported the New Horizons flyby mission. For additional details on the switch back to Side-1 see Section 7 on page 37.

The ARB assessed the risks and benefits of running a Bus C diagnostic test on ACS Side-2. Typically, all HST electrical loads are powered from the A/B power bus. Bus C is used only during Hardware Sunpoint safing, although it can be energized manually. The PDU bus A/B fuse cleared for ACS Side-2, but the Bus C fuse remained intact. Therefore, it was possible to power ACS Side-2 for diagnostic testing using Bus C. A similar Bus C test was run to help troubleshoot the STIS Side-1 failure. The Bus C fuse was deemed expendable, so the risk of clearing the Bus C fuse during the test was considered acceptable.

The benefits of Bus C testing would be to isolate the anomaly to either the Hold bus or Operate bus. If the Side-2 Hold bus was still functional, then additional redundant devices would be available to ACS if the fuse were to be replaced during an upcoming Servicing Mission.

Running the Bus C test was not without risks. When Bus C is energized, all HST electrical loads are effectively double-fused. Thus, if a non-ACS anomaly occurred while Bus C was energized, then twice the current could be drawn than what would have otherwise been seen. The ARB determined that this risk was acceptable since it is akin to a “double fault” scenario. In addition, the time that Bus C was energized would be kept to a minimum during the test.

Contamination is another risk of the Bus C test since the same electrical short that produced outgassing before could be re-energized during the test. The ARB determined that contamination was an acceptable risk since the possible short would be energized for a maximum of 50 msec. With such a short duration, the estimated outgassing would be only 1.2% of the original anomaly. In addition, all high voltage devices in HST would be powered off during the Bus C test.

The Bus C test was performed on March 27, 2007. The results indicated the anomaly was on the ACS Side-2 Hold bus. The Bus C fuse for ACS Side-2 was cleared during the test. For additional details of the Bus C test, see Section 8 on page 47.

During the course of ARB investigations, the Jet Propulsion Lab (JPL) alerted the ARB of the potential for hardware damage caused by resonances that could arise between Interpoint DC/DC converters and their associated Interpoint EMI filters. Early Spice model simulations indicated the high rail of the 28V converter input could spike up potentially to almost 40 volts. It was also stated that the voltage spike could be closer to 100V on a 1V line step change. In order to investigate this concern fully, the ARB agreed that a course of ground tests was required. In addition to these ground test efforts, a Science Instrument Independent Review Team (SI-IERT) was commissioned by HST Code 442 to aid in this investigation. Full-up, flight-like testing of the ACS hardware led the team to conclude that the risk of hardware damage induced by system resonance effects was very low. JPL representatives agreed that although the addition of added internal filtering to the power supply designs would be helpful, it was not absolutely necessary in light of the ground test results obtained. For more details on ground-based testing, see Section 9

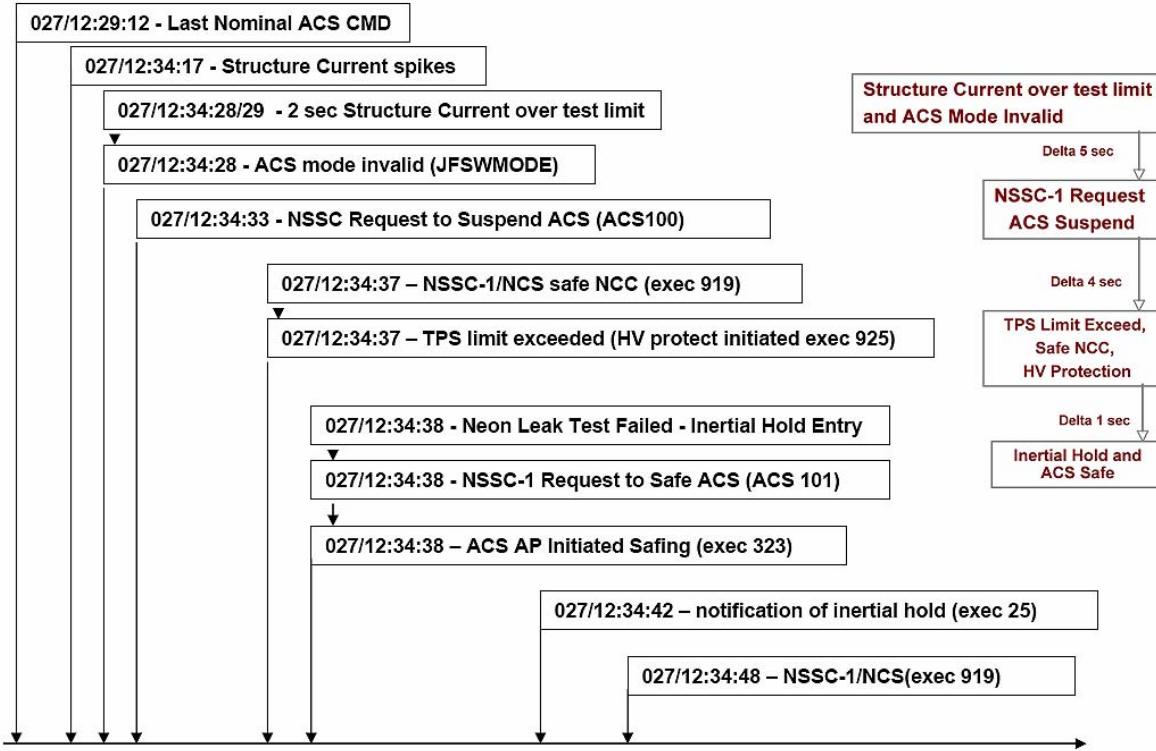
on page 57. For detailed tests and results, see Appendix 1 through Appendix 6 beginning on page 65.

## 4 Detailed Chronology of Event

### 4.1 Sequence of Anomalous Activities

On January 27, 2007 at 12:34:38 GMT (7:34:38 a.m. EST), the ACS entered Suspend Mode, and the HST then entered Inertial Hold Safe Mode. Figure 1 shows a schematic timeline of the events leading up to and throughout the event, along with the reaction of the FSW and the ultimate instrument Safing and Spacecraft Inertial Safe Mode actions. At the time of the Suspend event the ACS was in nominal Operate mode on Side-2 and initiating Proposal 10905. Specifically, the ACS was executing a Wide Field Camera (WFC) full frame exposure with the shutter closed.

Three seconds prior to the main anomalous event data showed a brief, transitory (~2 second) increase in structure current, up to 6 Amps. Engineering data then show the spacecraft structure current rising from zero to a peak above 15A, which exceeded the Structure Current Safing Test limit, as the HST load current simultaneously rose by roughly 37A between 12:34:21 and 12:34:28. This invalid mode lasted for 5 seconds, and subsequently prompted the NASA Standard Spacecraft Computer (NSSC-1) to request the ACS to suspend at 12:34:33. Four seconds later the TPS exceeded its limit for three samples. The increase in pressure inside the HST Aft Shroud resulted in the initiation of its High Voltage (HV) protection and the Safing of the NCC. One second after this action (12:34:38), the Neon Leak Test failed. In response, the ACS entered Safe mode and the HST entered Inertial Hold mode. Other activities related to the Inertial Hold consisted of autonomous commanding to power off the FHSTs and Fine Guidance Sensor (FGS) HV, to stop the High Gain Antenna (HGA) tracking, and to stop the Science Mission Specification (SMS). As a preventative measure, the HST Project decided to Safe NICMOS

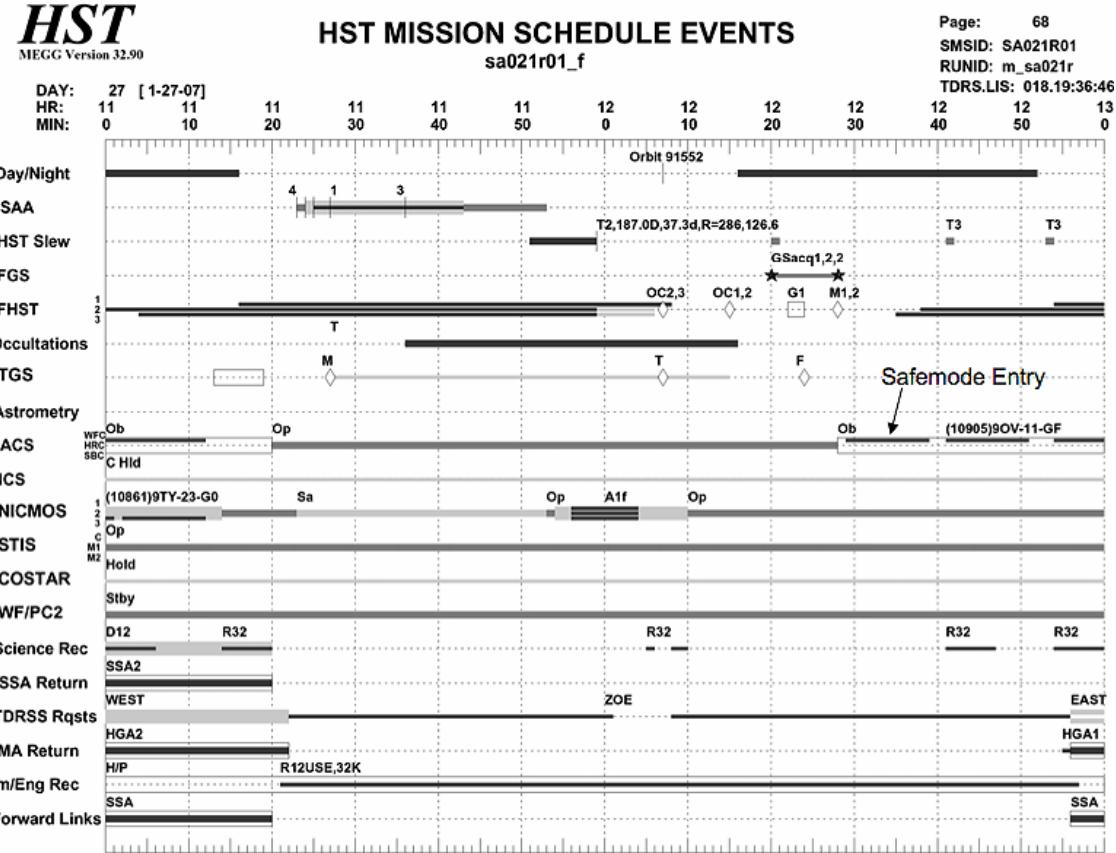


**Figure 1. Timeline of Anomalous Events**

Figure 2 shows the spacecraft activities surrounding the anomalous event. The HST was in orbit Night and outside of the South Atlantic Anomaly (SAA). The other instruments were characterized as follows:

- NICMOS in Operate mode, but not actively exposing
- WFPC2 in Standby Operate mode
- STIS in Hold mode.

The FGS had failed a routine Guide Star (GS) acquisition (due to a double star) just prior to the anomalous event, but is considered to have no association with the onset of the structure and load current increases.

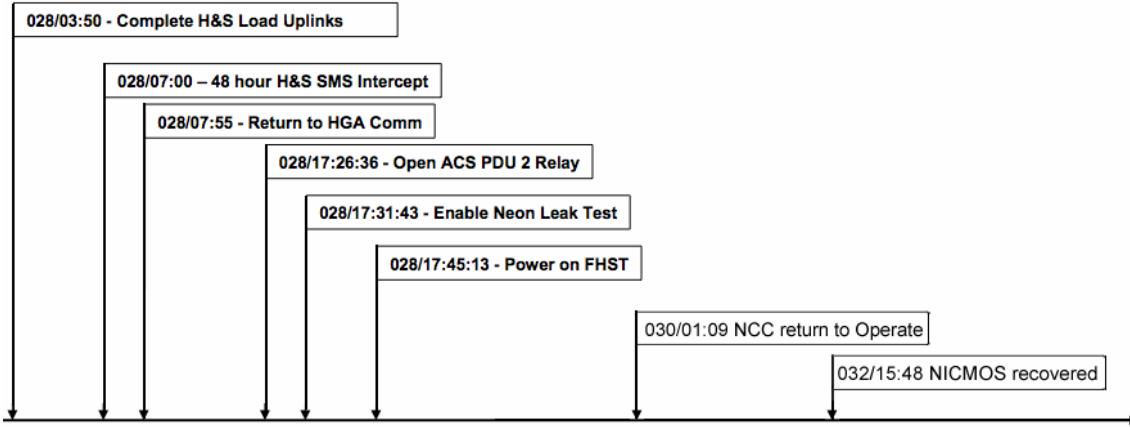


**Figure 2. SMS Surrounding Anomalous Events**

## 4.2 Recovery

The HST was recovered from Inertial Hold Safe mode on January 28, 2007. Figure 3 depicts the sequence of events involved, along with the time of each action. This included the following, in chronological order:

- Upload the Health and Safety SMS intercept
- Restore HGA communications
- Open the ACS Power Distribution Unit -2 (PDU2) relay (isolates Side-2 from potential Bus C power on)
- Enable the Neon Leak Safe mode Test
- Power on the Fixed Head Star Trackers (FHSTs) and FGSSs
- Return NCC to its operate configuration
- Recover NICMOS to SAA Operate



**Figure 3. Recovery Timeline**

Battery performance was nominal and the system State of Charge (SOC) increased by 3-5 A-H. The TPS reported nominal pressures. WFPC2 resumed nominal science operations shortly after NICMOS was recovered.

### 4.3 ACS Status after Recovery

ACS remained in Safe mode and the ARB team was formed. The team confirmed that the Side-2 Power failed and only the Side-1 Zone A heaters were on, operating nominally, and maintaining safe thermal conditions. The HST Project decided to enable the Zone B heaters to further protect the ACS thermal environment. ACS Side-2 HOLD power and Zone B heater relays remain closed with no power applied (PDU-2 fuse open). All other ACS Side-2 relays (e.g. Thermo-Electric Cooler (TEC), Control Electronics Box (CEB), Operate, Anneal, Mechanism, and Calibration lamps) were commanded open during the instrument safing. See Figure 4 for a schematic of the ACS configuration after the initial spacecraft recovery.

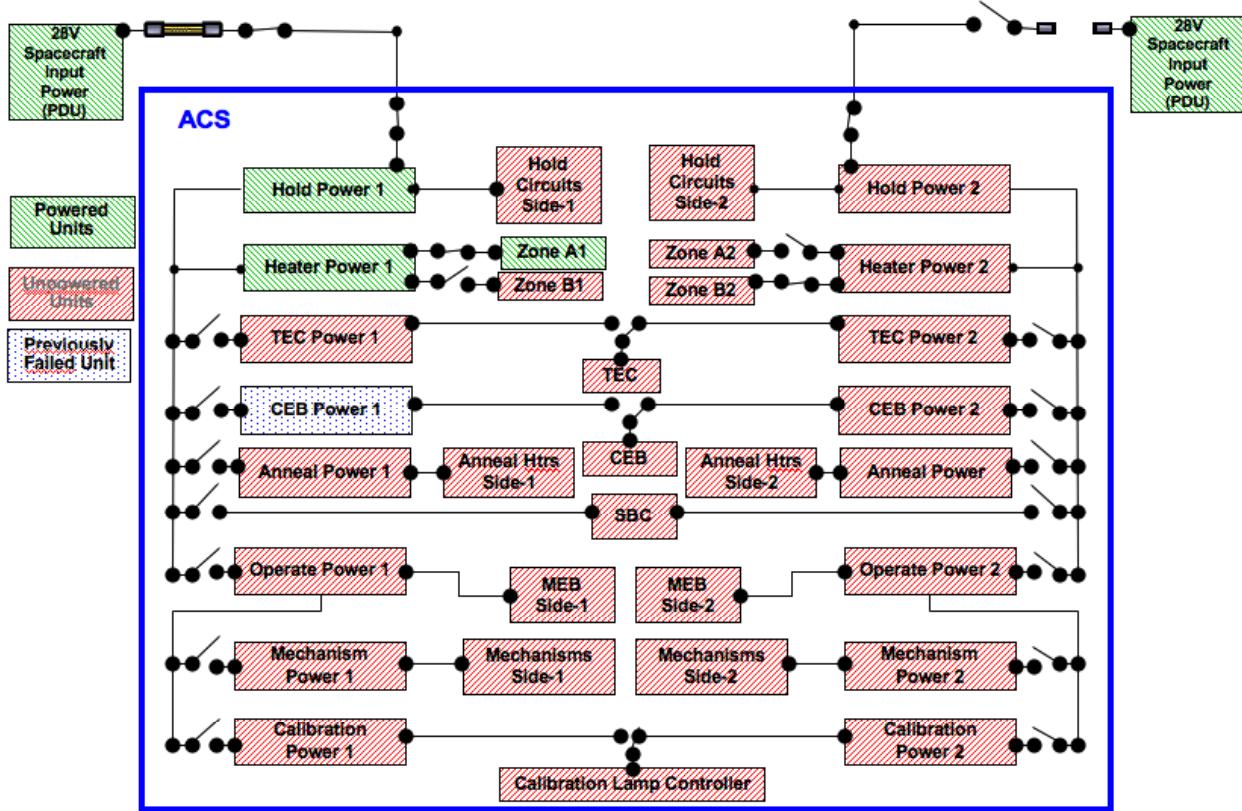


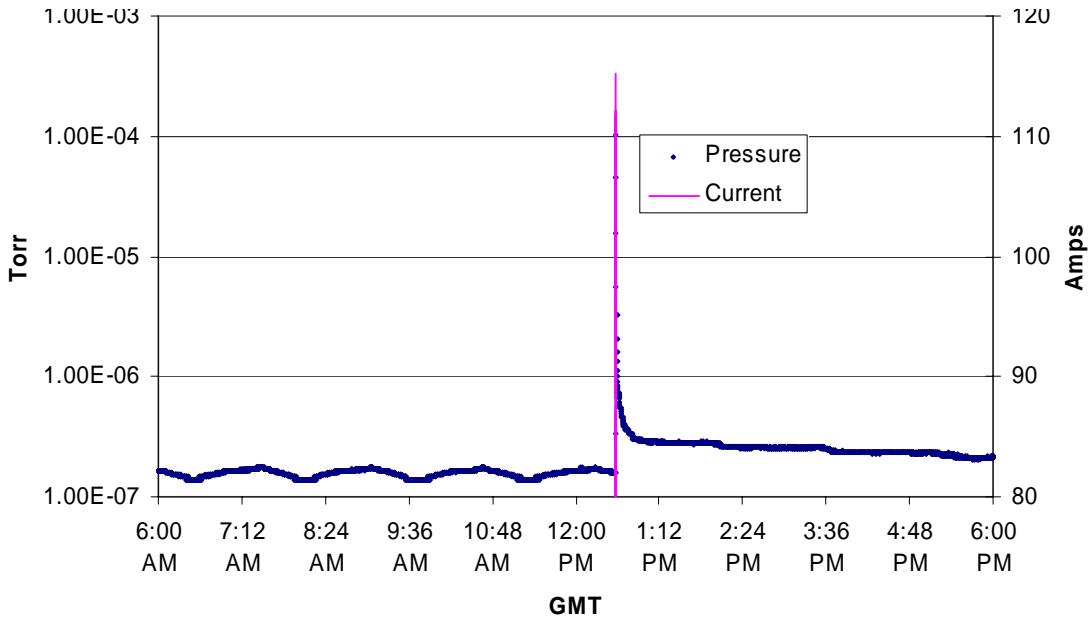
Figure 4. ACS Configuration After Initial Recovery

## 5 Contamination Analysis – Main Event

HST does not have on-board contamination monitoring devices. Instead, proxies such as pressure and optical throughput must be used to evaluate the cleanliness of the telescope. The ACS anomaly was immediately interesting (from a contamination perspective) because of the sharp rise in Aft Shroud pressure. Whenever an anomaly creates a measurable pressure rise in the Aft Shroud, concern is raised over the potential for condensable gasses to contaminate the HST and instrument optics. To quantify the probability and severity of contamination associated with the ACS anomaly, the quantity and type of contaminants released must be assessed. Determining the quantity requires a model of the HST vent paths, and determining the type requires knowledge of the materials involved, which are discussed in the upcoming subsections.

### 5.1 Anomaly Pressure Measurement

The pressure inside the Aft Shroud is monitored by the TPS on the NICMOS Cooling System (NCS) Electronics Support Module (ESM). The pressure is reported every 10 seconds. The plot of pressure during and after the anomaly is shown in Figure 5.



**Figure 5. NCS Total Pressure Sensor during Anomaly**

Features of the pressure plot worth noting are the cyclic behavior due to orbital variation in external pressure, the peak pressure of  $1\text{-}4$  Torr, and the long tail period where the pressure has not yet returned to the baseline level.

## 5.2 Venting Model

HST venting has been analyzed in the past: for ground thermal vacuum testing<sup>1</sup>, for deployment<sup>2</sup>, and for the installations of COSTAR<sup>3</sup> and the NCS<sup>4</sup>. The vent models are network analyses, where the nodes represent volumes and the connections between nodes are gas conductance paths. The equation of state for a node is:

$$V_i \frac{dP_i}{dt} = \sum_j F_{ij} (P_j - P_i) + G_i$$

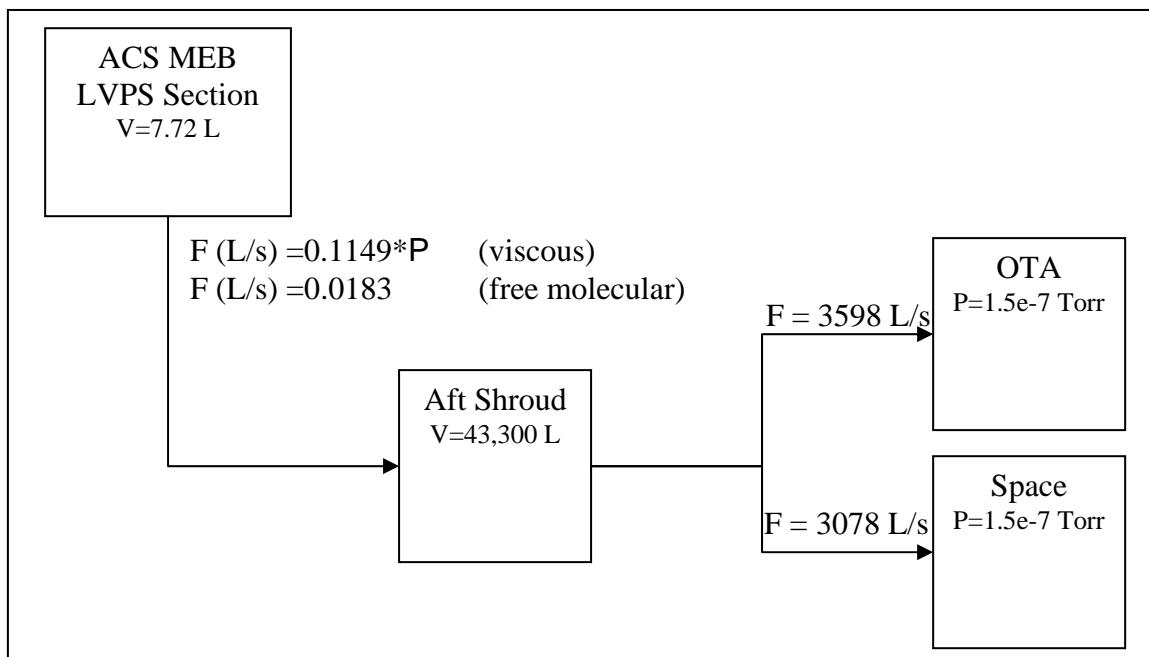
where  $V$  is the volume of node  $i$ ,  $P$  is the pressure,  $F_{ij}$  is the conductance from node  $i$  to node  $j$ , and  $G$  is the gas generation term in node  $i$ . The network configuration for this analysis is shown in Figure 6.

<sup>1</sup> S&M 341, Space Telescope – Aft Shroud Pressure Decay, 7/8/1982

<sup>2</sup> TSS 314, Summary HST Low Pressure Venting, 3/19/1987

<sup>3</sup> COSTAR-SYS-061, Graphite/Epoxy Desorption Effects on Aft Shroud Pressure, 12/20/1991

<sup>4</sup> SAI-2113-140/MSW-1, Quick Look at FGS Pressure Due to NCS Neon Leak, 2/25/2002

**Figure 6. Venting Model Configuration**

The conductance term is a function of the pressure differential in the viscous flow regime, but only of geometry for free molecular flow. The distinction in flow regimes is due to the low frequency of intermolecular collisions when the mean free path of a molecule is large compared with the dimensions of the container. For the MEB vent holes, which are 0.8 mm in diameter, the transition occurs between 2e-2 and 2 Torr (Knudsen number between 1 and 0.01). The conductance in the transition region was calculated as a linear interpolation between the free molecular and viscous conductances.

The parameters used to calculate the Network volumes and conductances are listed in Table 1.

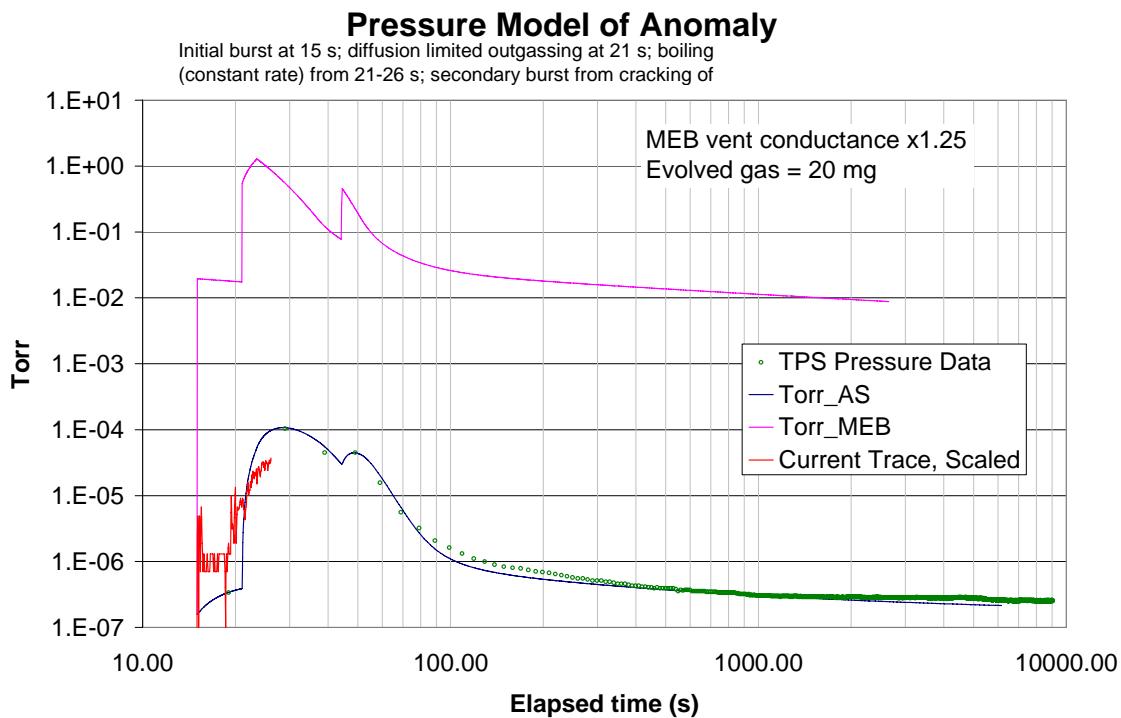
**Table 1. Contamination Model Parameters**

<b>Dimensions</b>			
	MEB vent (3 holes)	0.032	in, diam
		0.15	in, length
	LVPS section (80% free space)	9.5	in, deep
		15.5	in, wide
		4	in, long
	AS volume	43300	1
<b>Temperature</b>			
	MEB box	273	K
<b>Vapor</b>			
	Molecular weight	18	g/mol
	Molecular diameter	1.00E-09	m

### 5.3 Anomaly Model Correlation

The gas generation term in the MEB node of the model was set in a variety of ways. The best fit to the measured pressure data uses an initial large gas release coincident with 1) the start of the anomaly; 2) a period of constant rate of release during the anomaly; 3) a second, smaller gas release occurring after the current has been stopped by the fuse; and 4) a long term source that decreases proportionally to the square root of time. Physically, this could correspond to a burst or sudden vaporization, a release due to cracking of melted material that contained gas bubbles, and outgassing from the warm material surrounding the anomaly location.

A plot of the model predictions superimposed on the measured data is shown in Figure 7.



**Figure 7. Overlay of Pressure Model and Anomaly Measurements**

The current trace is arbitrarily scaled current (CLDBUSCP), and shows the progression of the electrical anomaly relative to the pressure response. The top curve is the MEB internal pressure, for which no measurement data exists. Because the pressure of space was fixed in the model, the cyclic variation of approximately  $1\text{e-}7$  Torr is not reproduced in the Aft Shroud pressure model (solid line), but is visible in the measured data (points).

As noted in the figure, a correction factor has been applied to the MEB vent conductance. The 25% higher conductance required to achieve the fit to the data may be due to additional vent paths through connectors in the mother board or due to errors in the assumed molecular weight, fill factor for the LVPS section, and other factors in Table 1 on page 24.

The gas generation terms used are:

- Initial burst of 450 Pa-L at 15 seconds (0.16 mg)

- Constant generation of 450 Pa-L/s from 21 to 23.5 seconds (3.8 mg)
- Generation of 1000 Ps-L/s from 44 to 44.5 seconds (13.64 mg)
- Outgassing of  $4t^{-0.5}$  Pa-L/s beginning at 21 seconds (2.4 mg)

where the summation of these terms gives a total gas evolution of 19.7 mg.

One of the proposed failure locations is inside an Interpoint converter. Looking at the initial burst, 0.16 mg of material, vaporized at a temperature of 30 °C, would produce a pressure of 14 atmospheres inside an Interpoint device. This is less than half the pressure required to cause the device to burst under normal conditions. Unfortunately, because of buffering and the way the data is reported, there is some uncertainty in the exact timing of the pressure data relative to the current data, so the possibility of an Interpoint failure cannot be ruled out on this evidence.

## **5.4 Anomaly Impact Assessment**

The duration of the anomaly and the high amount of power consumed suggest that a sizeable portion of a circuit board could have been heated, resulting in the decomposition of the circuit board, conformal coating, epoxy, and component cases. Some of these species may be condensable at Aft Shroud temperatures. Species that could condense on surfaces at -10 °C or warmer could affect the telescope and instrument optics; those species, however, would be collected inside the ACS electronics cavity and on the Aft Shroud walls, leaving very little to reach the optical surfaces. Species that condense only at colder temperatures, such as at -88 °C, would pose a risk to the WFPC2 CCD window, which is the only exposed cold optical surface.

The nodal model could be updated to determine the pressure response inside WFPC2, but it is conservative to assume that the WFPC2 pressure follows the Aft Shroud pressure. In this case the pressure may be converted to a flux of atoms using:

$$\Phi = P(2\pi \cdot mk_b T)^{-0.5}$$

Where  $\Phi$  is the flux in atoms/m<sup>2</sup>/s,  $m$  is the weight of a molecule,  $T$  is the gas temperature in Kelvin, and  $k_b$  is Boltzman's constant.

Applying this formula to the measured data and integrating over the event yields a flux of 0.5055 g/m<sup>2</sup>, roughly 5000 Angstroms if all of the mass is deposited. Even if only a small percentage of this mass was deposited on the WFPC2 detector window, the optical effect could be significant. Assuming the high temperature decomposition products are not condensable, deposition of the outgassing products (19% of the total) could produce up to 979 Angstroms.

In addition to vaporizing hydrocarbons, metal may have been evaporated. The metal would deposit on the first surface encountered and is not a contamination threat outside the electronics box. Vaporized metal would also not be measured by the Aft Shroud pressure sensor.

Measurement of the contamination effects was performed using optical measurements by WFPC2 and the ACS Solar Blind Channel. In both cases, the throughput was nominal within the measurement accuracy (a few percent). In the far UV spectrum, the rule of thumb is that 3 angstroms causes a 1% degradation; to be consistent with a maximum WFPC2 degradation of 6%, therefore, fewer than 20 angstroms were deposited. This implies that most of the evolved gas was non-condensable.

## 6 Electrical Analysis

The analysis for the root cause of the anomaly occurred along the following steps:

- What kind of event was this? By looking at the sampling times and telemetry data such as voltage, current and pressure sensor data, we obtain a characterization of the anomalous event.
- What kind of component was this? The events are then compared to known failure modes of components that exist in the system to see what kind of component could have failed.
- Where is this kind of component? Using the schematics, board and harness drawings, and photographs, we then search for where this particular part could be located.
- What else could have been affected? This analyzes any collateral damage, and any other parts that can be salvaged.

Each of these major points will be discussed in the subsections below.

### **6.1 *What kind of event was this?***

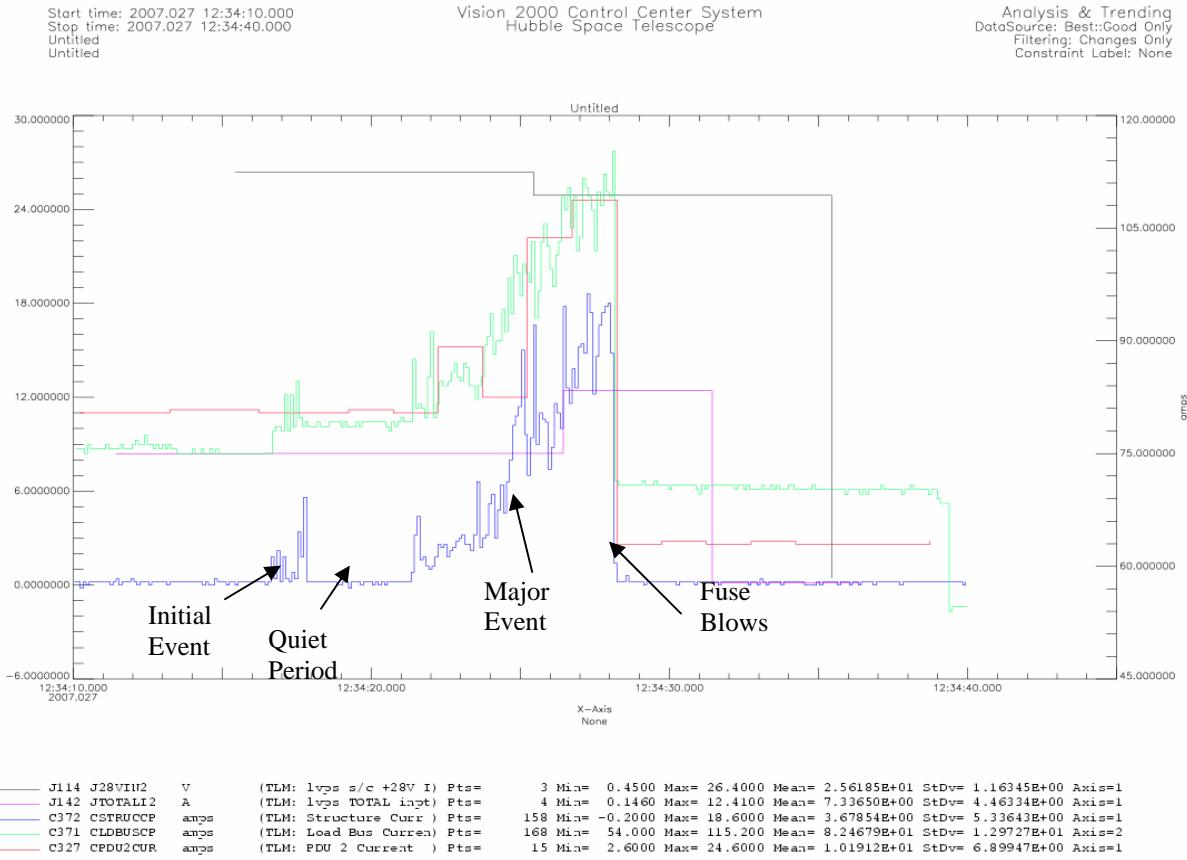
Figure 8 shows the important telemetry points during the anomaly. The locations of each of the telemetry monitors in the electrical system are shown in the simplified block diagram in Figure 9 on page 29. The first measurable anomalous current occurs at about 12:34:16, when the blue line (structure current – CSTRUCCP) shows glitches that are about 2-3 Amps in magnitude. Shortly thereafter, the green line (load bus current – CLDBUSCP) shows an upward step of about 2-3 Amps. This upward step is most likely not associated with this anomaly. As will be shown later, this current is associated with a different PDU feed, most likely due to an OTA heater that switches on due to the electrical noise caused by the structure current. After the initial burst of current on the structure and load bus, there is a quiet period of about 3 seconds before the anomalous current really takes off.

Very soon after the initial spike in current, but before the second major event, the TPS shows a spike in pressure. This indicates that the energy expended in that initial burst of current caused enough of a temperature rise to vaporize material, and further corroborates that the significance of the initial event. This correlation is shown in Figure 10 on page 29.

The second major event consists of a very noisy and gradually increasing current in the structure and load bus. This builds until 12:34:28, when the Main Bus A/B fuse finally blows, shutting off the anomalous current. The noise of the fault current appears on all the telemetry items, and is the explanation for the apparent drop of current in the red (CPDU2CUR) line at 12:34:24. We do not feel that the current actually drops for the entire duration of the sample, but is a result of noise during the sample.

Note that steady state input current of ACS prior to the anomaly is about 8 Amps (JTOTALI2 - purple line). We can see that the decrease in the load bus current (green line) from 12:34:20 (during the ‘quiet’ period) to 12:34:30 (fuse has blown) is about 8 Amps. The fact that the load bus current (green line) does not drop 8 Amps from the pre-anomaly level shows that the initial step, referred to above, is fed via a different PDU fuse. In other words, if that initial step were

going into ACS, the current level after the fuse blows would be 8 Amps below the pre-anomaly level.



**Figure 8. Plots of important telemetry during the anomaly with significant events**

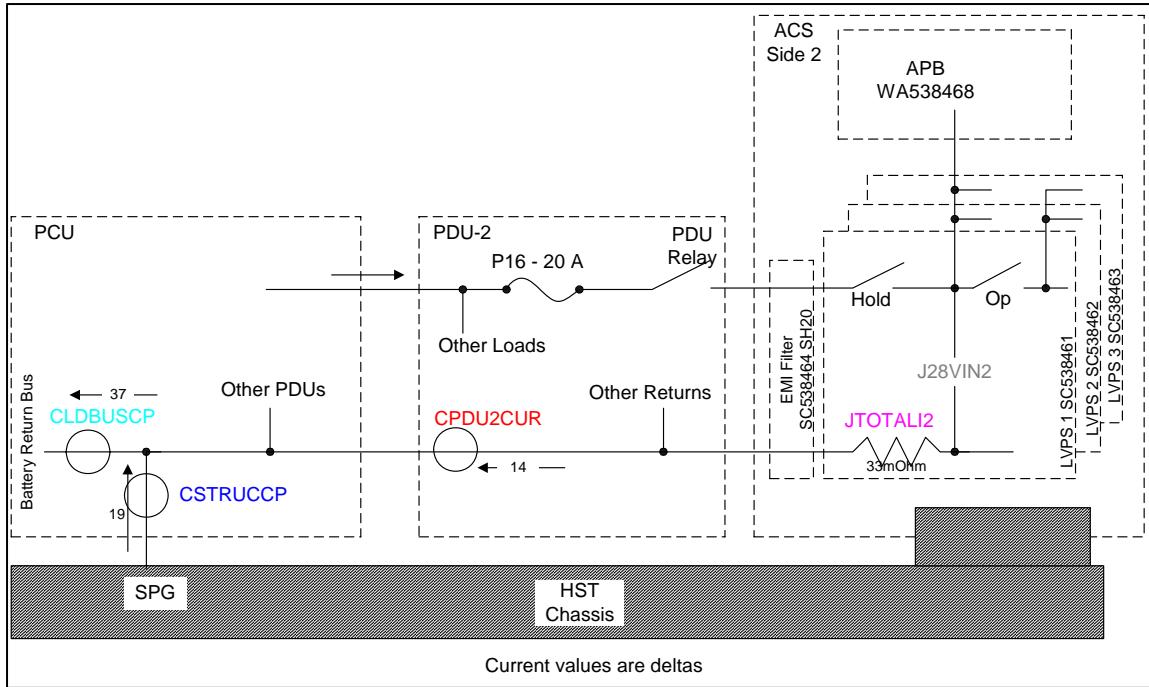


Figure 9. Simplified diagram with location of telemetry monitors.

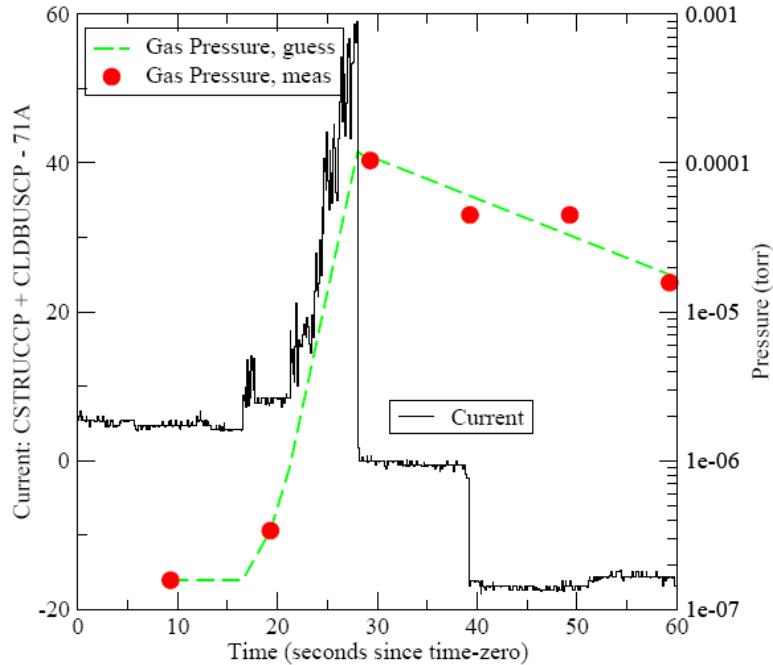


Figure 10. Pressure Sensor Data (red dots) aligned with Load Bus Current.

To summarize, we see the following characteristics of the fault:

- There is an initial glitch of current to structure. Perhaps also to return, but the sampling rate is too slow to see this.
- The fault current rises at a very slow 5 Amps/second.
- This current is very noisy, about 15 Amps peak-peak.
- The fault sustains tens of Amps of current, about 37 Amps.
- Enough gas is released to raise the pressure to the milliTorr range.
- The fault current bridges primary power, return and chassis.
- This anomaly occurred about 5khrs after the switch to Side-2.

In the next section, we analyze what kind of component could match this signature.

## **6.2 *What kind of component was this?***

The identification of what kind of component this could be was performed by comparing known faults and the characteristics extracted in the previous section. The information is matrixed into a table, and then a point system assigned to each of these matches. Finally, a tally of the total point value ranks the failure candidates.

**Table 2. Comparison of possible failure modes.**

<b>Symptom → Candidate ↓</b>	<b>Initial current glitch</b>	<b>Slowly rising current</b>	<b>Very noisy current</b>	<b>Can sustain tens of amps</b>	<b>Sufficient release of matter.</b>	<b>Can bridge high, return, chassis</b>	<b>Delay of 5k hrs before anomaly</b>	<b>Points</b>
On secondary side	Possible	Possible	Possible	No	Yes	No	Possible	16
Tin whisker	No	No	Yes	Yes	Yes	No	Yes	16
Exploding/ Burning Tantalum Cap	Possible	Possible	Yes	Yes	Yes	Yes	Possible	25
Conductive FOD	No	No	No	Possible	No	No	Not likely	5
Cold Flow of insulation/ Harness Short	Highly unlikely	No	No	Yes	Yes	Highly Unlikely	Possible	13
Transformer fault (Dog House + Intp)	Not likely	Not likely	Not likely	Yes	Yes	Yes	Yes	22
Reversed cap	Yes	Not likely	Yes	Yes	Yes	Yes	Not likely	24

The possibility of each fault was ranked in the following manner:

- No – This signature does not match the characteristic (0 points)
- Highly Unlikely – Although possible, it is highly unlikely to match the signature (1 point)
- Not Likely – This is unlikely to match the signature (2 points)
- Possible – This could quite possibly match the signature (3 points)
- Yes – This is a very good match (4 points).

The final point value was obtained by adding all the points in a row. The process of assigning possibilities, the point system, and the method of combining the points is subjective. For example, we could have used a multiplicative system instead of addition. However, we felt that some candidates had multiple ‘No’ assignments and that would not have been reflected in multiplicative system. The matrix and its point ranking attempts to express in quantitative form the collective opinion, experience, and wisdom of the ARB members with the goal of converting the failure signatures into the identification a type of failure. Although this can be subjective, we felt this was the best way to capture the collective knowledge of the board.

The point tally shows that a failed/reversed tantalum capacitor best matches our failure characteristics. There were no ‘No’ assignments of possibility, and the tantalum mass offers a

good way to short multiple nodes while releasing matter. The second most likely candidate was a transformer fault in an Interpoint Electromagnetic Interference (EMI) filter or converter. In our next section, we try to find where this component could be located.

### **6.3 Where was this component?**

Using the current telemetry and the simplified block diagram, Figure 9 on page 29, we can tell that the short occurred inside ACS, and to the right of the internal current sensor. This is because this sensor measured a large increase during the anomaly, and most likely exonerates hardware outside of ACS and the associated MEB mother board circuitry such as the EMI ‘doghouse’. We briefly considered the possibility of a failure occurring outside of the current sensor, but still inside the MEB, that would have bridged past the current sensor, but thought this to be unlikely.

At a particular instance during the short, the 28V telemetry dropped by 1.5V. The fault current at that time was  $21 \pm 5$  Amps. This allows us to calculate the approximate effective series impedance that supplied the short at that time:  $1.5/21=70\text{m}\Omega$ . The above impedance includes the following components that fed the short:

- 33 mOhm sense resistor in ACS
- Round trip wiring to battery
- Relays, fuse, connectors, etc
- Battery output impedance.

The calculated impedance does not assist us in further narrowing down the location of the anomaly. There are enough components involved that no clear candidate for exoneration exists. Since the traces on the board account for only a few mOhm, the location of the a fault can be anywhere on the board.

Each of the Interpoint converters have their individual current limit. This limit is in the range of 65 Watts. At the peak of the event, we had the following conditions:

- ~40 W dissipated in HST wiring
- ~925W dissipated in ACS
- 37 Amps fault current
- Short inside ACS was at 0.6 Ohms.

The high amount of power dissipated compared to the current/power limit of the converters suggests that the fault could not have occurred in the output of a converter. In addition, a fault on the output (secondary side) of the converter would not have caused a current in HST’s structure current sensor. It is however still possible that the fault occurred on the secondary domain inside the converter and then ejected enough material to cause a short on the primary side.

With the information presented thus far, the resulting fault tree is shown in Figure 11. To summarize, the fault is located on the primary side of the power supply and to the ‘right’ of ACS’ current sensor (see Figure 9 on page 29). The most likely culprit is a failed/reversed tantalum capacitor or transformer in an EMI filter or converter.

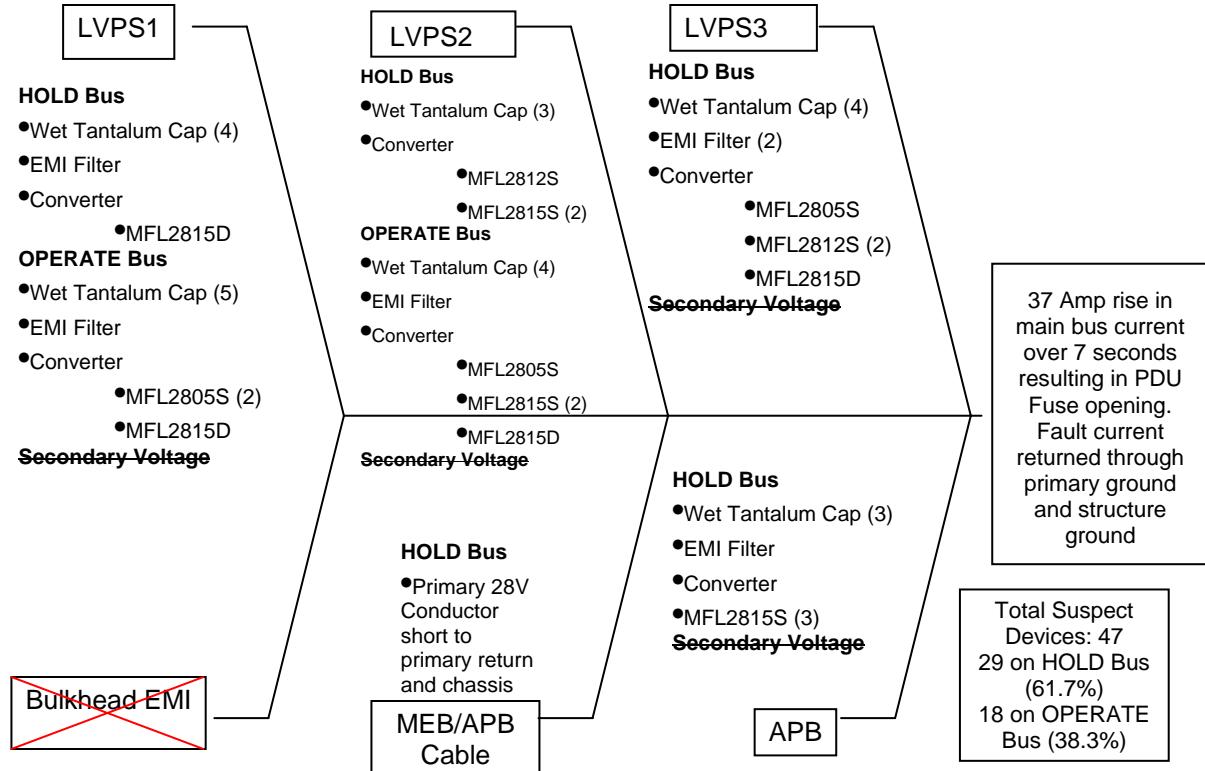


Figure 11. ACS Side-2 Fault Tree.

#### 6.4 A closer look at the Secondary Side

An issue relevant to the ACS repair effort is the integrity of the secondary (output) side of the converters feeding the CEB. As was explained above, the anomaly could not have occurred on the output of the converters, but it could have originated inside the Converters themselves. This would impact the feasibility of ‘backpowering’ the downstream circuits with a new supply. To best determine the status of the secondary side, we looked at the last telemetry data points gathered from them, along with their time-stamps. This is then compared to the load bus and structure current at the time to understand how likely it is that the anomaly resulted from a problem with that converter. Specifically, if that converter had data showing it was operating normally (normal output voltage) while the anomaly was ongoing, it suggests that the fault is not caused by that converter. Since the anomaly current was continuously increasing, the later the telemetry sample was taken, the higher the confidence we have that the converter was operating correctly.

This voltage telemetry data is shown in Figure 12 and Figure 13, and summarized in Table 3. As we can see in this table, we can exonerate with the greatest confidence the CEB +5V and the Secondary Hold power circuits. These have a valid sample that is within expected values that occurred when the anomaly was about 30 Amps and 780 Watts. It is highly unlikely that these converters would have had a short of this magnitude on its secondary side, and still maintained proper output. The table then lists the other converters in decreasing confidence, with the last one being the CEB analog voltage converters. Their output was verified within expected values

when the anomaly was just getting started at a level of 4 Amps and 100 Watts. As a result, the evidence that Side-2's CEB supplies can be backpowered is mixed. The digital supply is most likely fine, with the analog supply being somewhat inconclusive.

A short description of each of the mnemonics listed in Figure 12 and Figure 13 is given below:

JHTECI2	Hrc TEC input I s2
JWECI2	Wfc TEC input I s2
JSHTECI2	wfc SHield TEC I s2
JHS1CHI	Hrc Serial 1 C HIgh
JHS1CLO	Hrc Serial 1 C LOw
JHS2CDLO	Hrc Serial 2 CD LOw
JHS2CDHI	Hrc Serial 2 CD HIgh
JWTG1P5	Wfc ceb Tim Gen1 +5v
JWTG2P5	Wfc ceb Tim Gen2 +5v
JZON1AP2	thrm ctrl ZONE 1A P2
JZON1BP2	thrm ctrl ZONE 1B P2
JZON2AP2	thrm ctrl ZONE 2A P2
JZON2BP2	thrm ctrl ZONE 2B P2
JZON3AP2	thrm ctrl ZONE 3A P2
JZON3BP2	thrm ctrl ZONE 3B P2
J5VHOLD +5V	Hold mode conv
J15VHLD +15V	Hold mode conv
JM15VCB2	M15 V CeB out lvps 2
J35VCEB2	35 V CEB out lvps 2

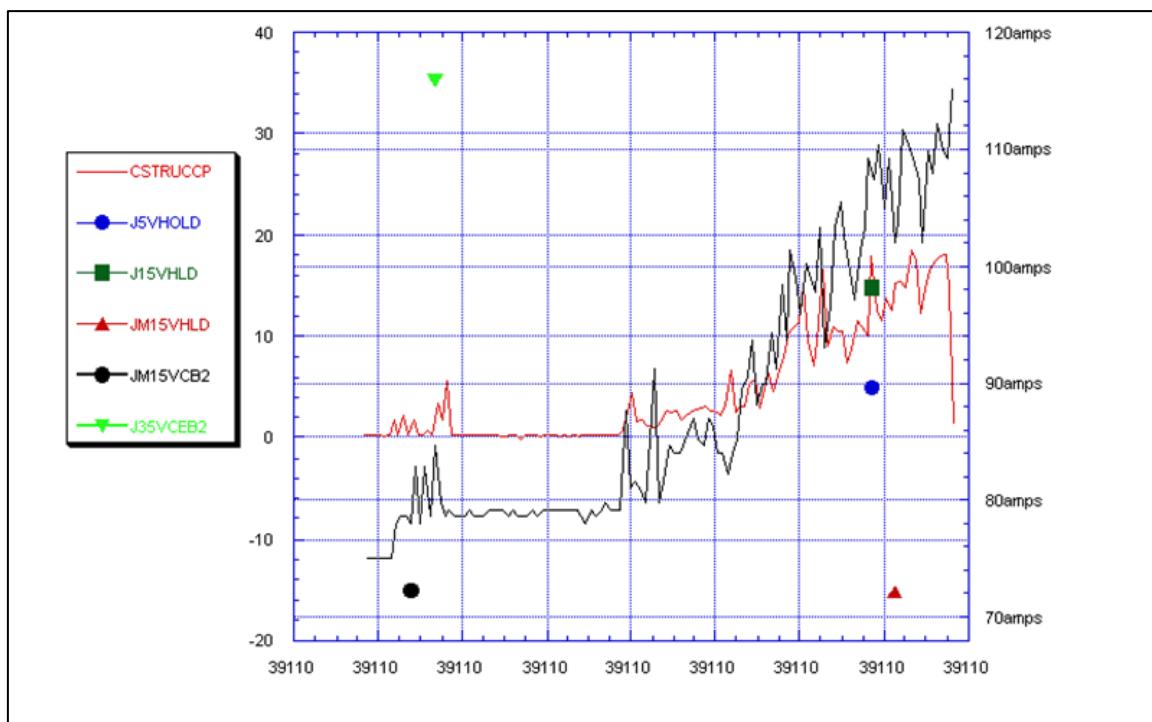
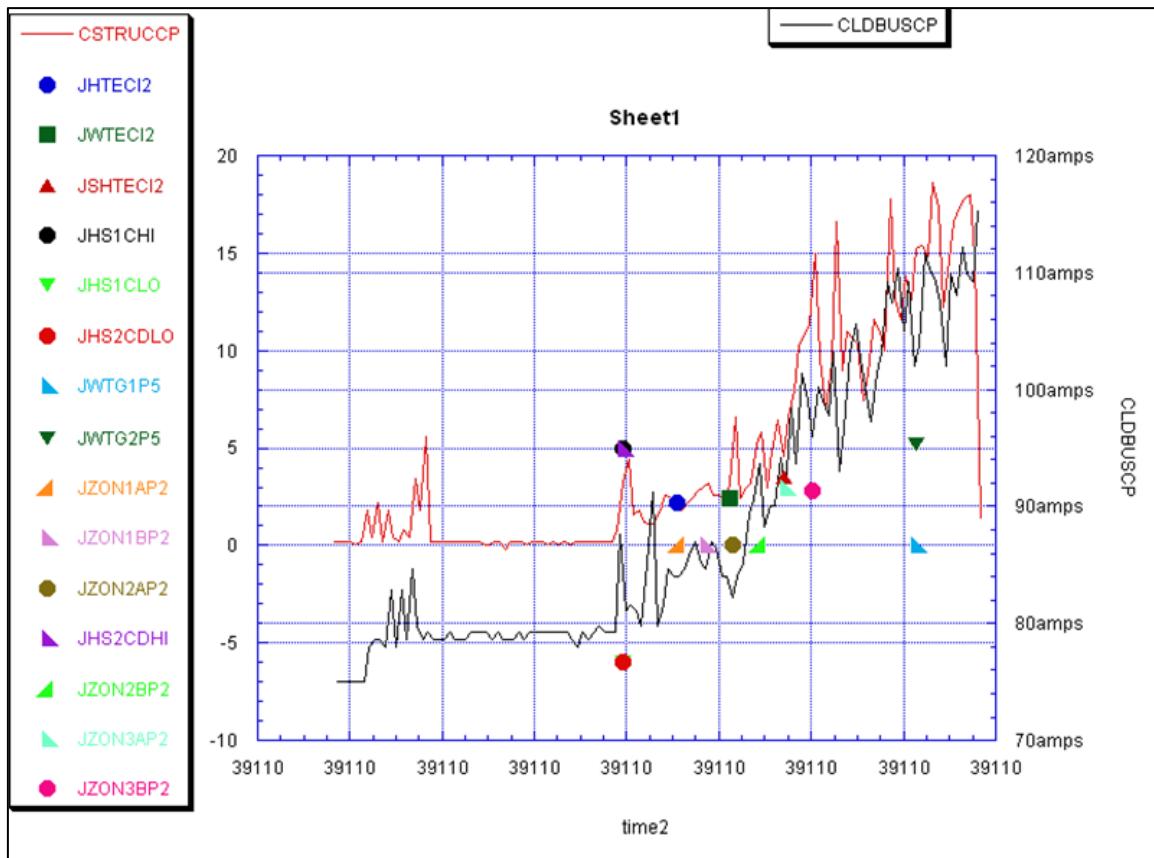


Figure 12. Secondary output telemetry compared to anomaly current.



**Figure 13.** Secondary Output Telemetry compared to anomaly current.

**Table 3.** Listing of Secondary circuits verified valid during anomaly.

Description	Anomaly level (Amps/Watts)
CEB +5V	30/780
Hold +5/+15/-15V	28/730
Shield TEC	15/390
WFC TEC	8/210
HRC TEC	6/160
Heater A & B	6-16/160-420
CEB +15/-15	4/100

## 7 Return to ACS SBC Science Operations on Side-1 following ACS Side-2 Failure

This section documents the studies and steps taken to insure that the “return to SBC science” on ACS Side-1 was safe for ACS and the HST. SBC Operations on Side-1 was contingent on the condition and functionality of the ACS Side-1 after the June 2006 Side-1 Anomaly and potential ramifications of Side-2 collateral damage. A brief chronology of the related events is illustrated in Figure 14.

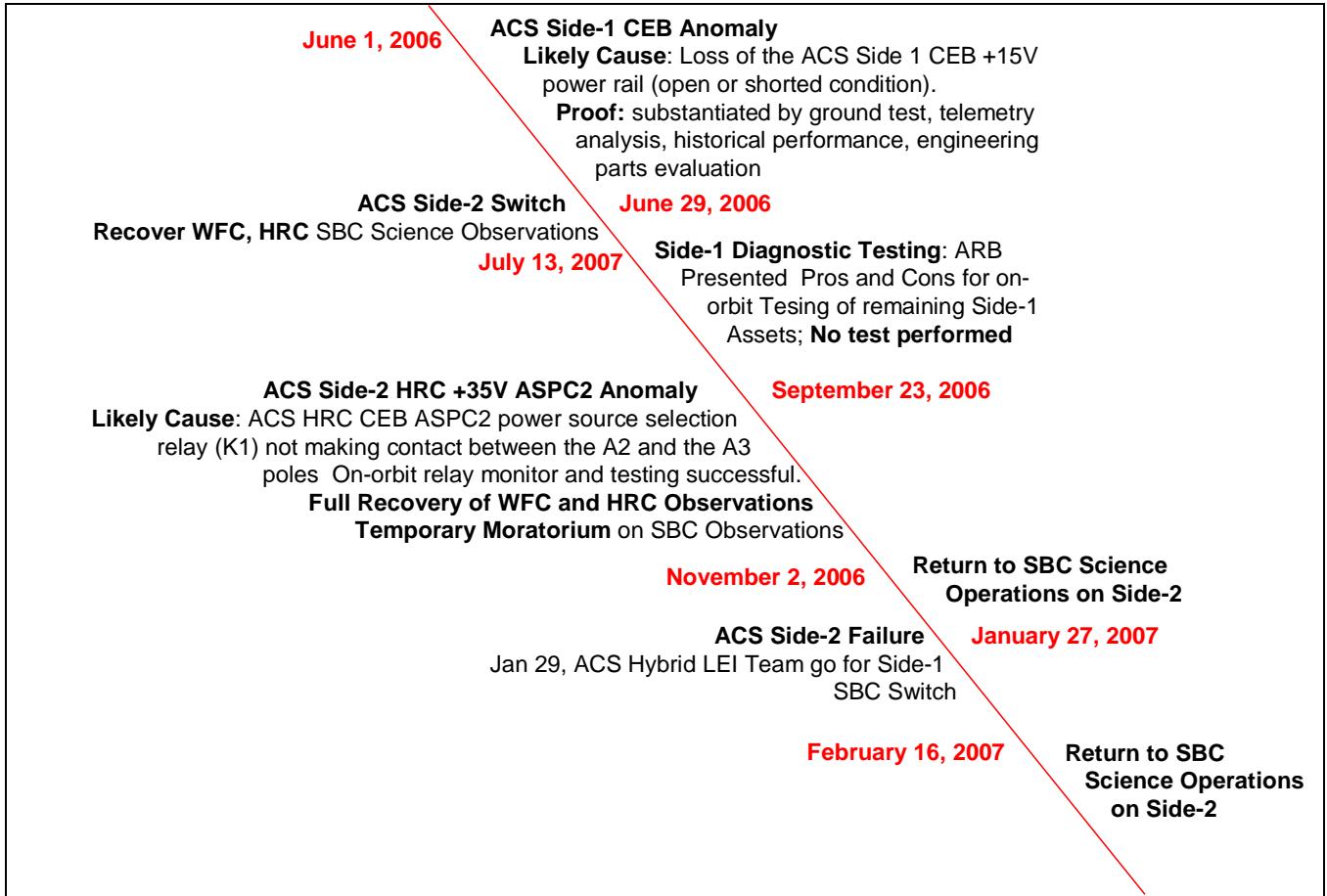


Figure 14. Chronology of Recent ACS Events

### 7.1 ACS Side-1 CEB Anomaly – June 2006: Summary and ARB Findings

The foundation for recovering ACS SBC operations on Side-1 was established by the investigative work on the remaining viable assets of Side-1 by the June 2006 ARB and the ACS Hybrid LEI team.

This section includes a brief review of the Side-1 CEB fault and addresses associated concerns with respect to Side-1 SBC operation. For a detailed report by the ARB on the June 2006 anomaly, the reader is referred to [ACS Side-1 ARB Final Report - LMSS/C060410](#) (ARB Chair

R. Chiei 442, August 24, 2006) and related documentation at <http://edocs.hst.nasa.gov/hstsystman/ACSCEBARB/default.aspx>.

### **7.1.1 Side-1 CEB Anomaly Event**

The ACS entered suspend mode on June 19, 2006 because of several out of limits parameters. Telemetry later showed that all 158 telemetry parameters sampled by the WFC and High Resolution Camera (HRC) CEBs began reporting 12-bit hexadecimal FFF values (twelve 1s) in the same sampling cycle. This data failed limit checking three consecutive times, which caused the Suspend.

At the time of the fault, ACS current telemetry decreased by 1.2 to 1.8 amps within a 100 msec interval. Current data indicated that the anomaly lasted ~7 seconds prior to the suspend. During the fault and through the 7 seconds, there was no indication of current spikes and the current remained constant after the event. There was no indication of a thermal rise, or anomalous secondary voltages. The Bus voltage and all other parameters were nominal.

### **7.1.2 ARB Investigation – Origin of the Side-1 CEB Fault**

As documented in the Side-1 CEB ARB final report, concluded that *the most likely cause of the ACS Side 1 on-orbit anomaly was a result of the loss of the ACS Side 1 CEB +15V power rail in either an open or shorted condition.* This theory was based on the knowledge that 1) the power rail was common to both WFC and HRC CEBs, 2) CEB A/D converters required +/-15V rails to operate, and 3) NED software operating in the Secondary Electronics Section (SES) section of MEB was evaluated and found to be very robust, with numerous FIFO checks being conducted as part of the process, substantiating that the root cause of the anomaly was not located in the SES. *The most likely cause of the ACS failure resided within LVPS Board #3, component U2-7, the MFL2815D Interpoint DC-DC converter.* The next most likely cause is a short to ground in the transformer T6 on the same LVPS board.

Based on the signatures of the fault, the ARB ruled out the following fault sources: CEB A/D Converters and associated serial interface, CEB 8kHz clock, CEB Interface inverter, FIFO Read Control, CEB Optocoupler. Since LVPS #3 contains all of the active components that produce and/or interface with the suspected +15V CEB power rail the ARB deemed the board as the most likely location. However, other possible but less likely locations were also identified: MEB Backplane (+15V trace to ground fault), MEB to CEB harnessing (+15V wire short to ground fault) and a short on +15V Input to a CEB prior to power switching relay.

### **7.1.3 Switching to ACS to Side-2 Operations**

As a result of the investigation, and the Side-1 CEB ARB's unanimous recommendation to proceed, the switch to Side-2 was executed on June 29, 2006. Procedures were based on the Life Extension Initiative completed in the previous year. Key recommendations to note are:

- The ARB determined that switching to ACS Side-2 is safe regardless of an open or shorted condition on the +15V CEB power rail
- The ARB cautioned that, although deemed safe, switching to ACS Side-2 will not restore ACS CEB operation in all fault scenarios

- The ARB initially precluded SBC activities with either CEB powered until further study. The issue at the time addressed the fact that the +5V input power onto the CEB timing board was allowed even though the CEBs were configured with all +/-15V and +35V input relays open resulting in a type of “hybrid power mode.” The CEB timing board power-on Reset maintains a safe configuration until the MEB is commanded by the CEB. As a result and with the addition of two CARD item proposals (prevent commanding of the ‘off’ CEB and prevent hot switching of the CEB power configuration relays), the ARB concluded that SBC operations on Side-2 presented no safety issues.

## **7.2 Risk Assessment for a Switch to Side-1 SBC Operations following the January 2007 ACS Side-2 Failure**

As a result of the Side-1 CEB failure investigation, that the SBC operations on Side-1 were still a viable configuration. The Side-1 CEB ARB concluded that the following Side-1 capabilities were deemed accessible:

- Power the SBC
- Power and control both TECs and the WFC shield TEC
- Power thermal shelf heaters
- Power window and interface plate heaters

The analysis after the Side-2 failure focused on potential collateral damage to ACS (Side 1 or Side-2 components) and to the rest of the HST by the ACS Side-2 anomaly or as a result of an unforeseen or spurious Side-1 fault when re-enabling SBC operations on Side-1.

A two-fold approach was used to comprehend and attempt mitigation of potential risks of re-enabling the SBC on Side-1. The Subsystem analysis targeted understanding the implications of 3 static scenarios defined by combinations of STIS and ACS failure modes. The results (for a nominal 6-battery case) as described in this section revealed only one thermal concern to ACS and STIS where they may fall below their survival limits and suffer (unknown) damage. This was deemed to be a *very low risk* associated with attempting a Side-1 recovery to SBC-only mode of operation. The second approach was a study of potential collateral damage, also described in more detail in the subsequent section.

### **7.2.1 Subsystem Risk Assessment - Summary**

All HST subsystem impacts were carefully analyzed for 3 cases, each compromising a combination of ACS and STIS states. The relevancy of STIS (currently in Safemode) in this context is in the implications on power load and thermal impacts of two Science Instruments (SIs) in a compromised or failed condition. The 3 scenarios are listed in Table 4 and the Subsystem conclusions are summarized in this subsection.

**Table 4.** Three status ACS/STIS scenarios and their implications on HST subsystems.

	<b>ACS</b>	<b>STIS</b>
<b>Case 1</b>	Side 1-SBC Operational	Safed
<b>Case 2</b>	Failed	Safed
<b>Case 3</b>	Failed	Failed

***Data Management System (DMS) and Instrumentation & Communications (I&C):***

No ramifications to the DMS and I&C subsystems were identified other than serendipitous reduction of SSR usage and SSAT cycling due to lower science data volume.

***Safing:***

An over-voltage condition could occur during a Hardware Sunpoint (HWSP) if a Solar Panel Assembly (SPA) was connected to the bus.

***Pointing Control Subsystem (PCS):***

A positive thermal impact (of varying degrees depending on the case) to the Rate Sensing Units (RSUs) thermal control system will occur because of the decrease in temperature due to a compromised or failed SI. The cooler the RSUs, the higher the RSU heater duty cycle; this is a scenario that provides better thermal control. Note that the Magnetic Sensing System (MSS) calibration would have to be redone due to the reduced PDU load.

***Optical Telescope Assembly (OTA):***

For Case 1, FGS 1R may periodically go out of thermal control in hot attitudes. For Case 2 and 3, FGS1R will be colder, which encourages better thermal control by its heaters. Also for Cases 2 and 3, the Focal Plane Structure (FPS) heater duty cycle will increase and 1 out of 54 heaters may saturate. However in the case of the FPS, which is designed as a zero coefficient-of-expansion structure, the temperature change is predicted to be a benign 3 degrees.

***Thermal Control System (TCS):***

For Case 2, the ACS will exceed its cold constraint limits (worst case -30C). For Case 3, both ACS and STIS will exceed their cold constraint limits (-30C and -40C respectively).

***Electrical Power Subsystem (EPS):***

In all cases, there are no impact to EPS with a 6- battery PSEA. However, a 5-battery PSEA requires additional contingency loads.

**SI:**

The SI subsystem impacts have both ACS and NICMOS implications as well as reduced science capability for HST.

Case 1 – Due to the reduced temperature of a compromised ACS, the NICMOS buffer box temperatures will require management in two ways (i.e., turning on the warmer buffer boxes first). Also SI recovery times might require modification.

Case 2 and 3 – NICMOS buffer boxes may approach survival limits in safemode (-25C) and would thus require the shell heater to be left on (this configuration would mandate Safing Sequence Changes). ACS will also exceed its cold constraint limits.

## **7.2.2 Contamination and Collateral Damage Risk Assessment**

The collateral damage assessment study showed the following (see Section 5 on page 22 for details):

- No high probability/high risk scenarios were found to preclude initiating Side-1 SBC turn-on.
- No evidence was found supporting an increased risk for a potential Side-1 failure, that either duplicated the Side-2 fault or may be an unrelated inherent weakness

Conclusions were based on: 1) board, wire, and electronics housing construction; 2) on telemetry, on fuse plug and PDU wire design; 3) on the potential for a Side-1 failure; and 4) accounting for Side-1 parts that were still operational. The arguments and conclusions for each of these concerns are summarized below.

### **7.2.2.1 Possible Locations for the Side-2 Fault for Collateral Damage Assessment**

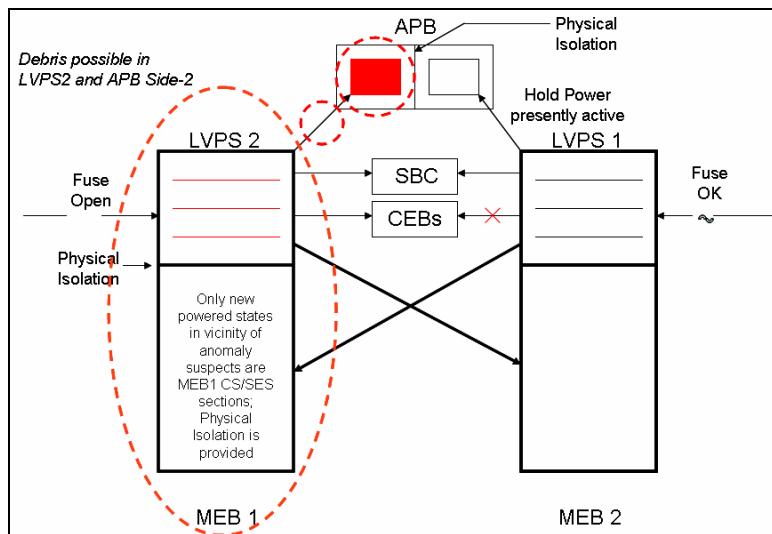
The possible origins of the Side-2 fault are illustrated in

Figure 15. The suspects include: the 1) LVPS-2 board; 2) Auxiliary Power Box (APB); and 3) harness between Side-2 LVPS and the APB. Details on each source are discussed further below.

- LVPS-2 (physically located in MEB1) - Analysis by the ARB demonstrated that the energy required to breach the barrier separating the Side-2 LVPS section from the ACS Side-1 electronics would have to be much larger than the derived energy from the Side-2 fault. The total electrical energy of the main event was about 4300 joules. Ballistics analysis showed that to generate a high energy projectile, the scenario must include a funneling mechanism, higher energies, faster propagation, and a constraining of the solid angle of the ejecta. A component disintegration would be contained within the LVPS-2 box. Only the external sides of the MEB contain 3 tiny (paper clip-sized) vent holes.
- APB - A barrier physically separates the Side-1 and Side-2 sides of the APB. The barrier and APB box have no physical vent holes. Preliminary thermal modeling suggests that either the fault did not occur in the APB or the thermistor did not register the event due to its relative location on the board (additional modeling in work & board design under investigation). The anneal relays were open at the time of the Side-2 fault. In addition, the

+28V Hold Power is present on the input side of the Side-1 APB. Both these observables suggest that the APB may not be the source of the fault.

- Harnesses between Side-2 LVPS and APB - The double signature of the failure suggests that the harness is not the source of the fault. The scenario invoked to explain the double power spike would require wires in cable bundles to short together, separate some how and short again to coincide with dual-current peak . Also, the wire insulation of the type in HST will not participate in the short. The ARB also addressed potential collateral damage to the harness from the event. The harness between LVPS1 and APB was not damaged because the HOLD power is present at the input of the APB. The harness between LVPS1 and Side-1 Heaters was not damaged because Zone A and Zone B (the latter since Feb 9) heaters are operating on Side-1. (The status of the harnesses between LVPS1 and Side-1 Electronics in MEB-2 and between LVPS1 and SBC would not be known until entry into Operate).



**Figure 15. Schematic of the Side-2 Fault locations are Circled**

### 7.2.3 PDU Fuse Box and PDU Wiring Concerns

The potential for collateral damage to the Side-1 PDU fuse, located within the same fuse box as the “blown” Side-2 PDU fuse was investigated as a potential risk. The ARB concluded that the design of the fuse plugs (i.e., isolated from each other), together with relevant ground based experimentation results by H. Leidecker ([Experimental and Theoretical Studies of FM08 Electrical Fuses](#), 1996), proved that the potential for collateral damage to the other fuses was negligible. As far as the potential for blowing the Side-1 PDU1 20 Amp fuse as a result of the Side-1 CEB fault was assessed to be very low based on the current signature during and after the event (i.e., the current decreased and then remained constant with no evidence of spiking).

#### 7.2.3.1 Systemic Problems Associated with the Multiple Interpoint Converters off a Single EMI Filter

The premise that systemic problems associated with Multiple Interpoint converters hanging off a given Interpoint EMI filter as a potential fault source was addressed at a high level (at this point

in the investigation – see Section 9 on page 57 for details). The ARB concluded that if the problem exists, it is systemic to ACS. The risk associated with the occurrence is unquantifiable, but 4 years of operations on Side-1 and preliminary lab results indicated to the ARB that this risk was low. The low risk for a potential Side-1 failure mitigated concerns of additional contamination to the vehicle.

### **7.2.3.2 Contamination from a “Repeat” event on Side-1**

The ARB and Bus C teams addressed the consequences of a “repeat” event with the same large energy matter release as the Side-2 anomaly – but occurring at the Side-1 power up. First, the ARB concluded that this scenario was exceedingly remote since no evidence was found that exposed a Side-1 inherent weakness. No new species would be introduced, therefore the photon absorption cross section of the contamination will be the same per milligram of gas produced as the original event.

The species and amount of material released by the Side-2 event was such that initial WFPC2 Visible Light observations of Omega Cen showed no contamination nor evidence of widespread “grey” soot being present or a threat. [*Note that the more sensitive WFPC2 UV observations were obtained prior to taking data with the SBC but after the initial Side-1 SBC turn-on hence were not available for this risk assessment. These showed upper bound degradation from the original fault of -6% with a 5% 2-sigma error bar*]. Contamination models show that the failure of some parts can produce the amount of estimated vented material seen in the sensor data pressure (instantaneous mass < 20 milligrams). Molecular deposition on the warm primary HST optics was considered very remote because of the labyrinth of “cold traps” in the geometry between ACS and OTA optics that would draw contaminants. The Aft shroud ranges from 0 to -10C.

## **7.3 On-Orbit Switch to Side-1 SBC Operations**

The ACS Hybrid LEI Team was given the “go” from Project to prepare for a switch to Side-1 SBC Operations while the ARB continued investigating the Side-2 failure and assessing risks associated with the side switch. The plans to switch back to ACS Side-1 were a combination of two separate HST Life Extension Initiative (LEI) activities:

- ACS Side-2 LEI Presentation given on 4/15/05 - The presentation served as a “roadmap” for returning to Side-1 (ref: [http://edocs.hst.nasa.gov/MOP/Shared%20Documents/LEIAssess/ACS\\_Side2\\_Assessment\\_FRR.ppt](http://edocs.hst.nasa.gov/MOP/Shared%20Documents/LEIAssess/ACS_Side2_Assessment_FRR.ppt))
- ACS Hybrid LEI – The Phase 1 task identified SBC-only operations as a viable hybrid mode in terms of power, electrical, thermal, and science considerations. The Phase 2 task, in work when the Side-2 Anomaly occurred, identified specific changes required to implement SBC-only operations.

The Switch to ACS Side-1 incorporated lessons learned from previous STIS and ACS failures, which included:

- Side-2 adapter plugs for ACS Test Benches can be removed to restore benches to Side-1 configuration
- Transition CCLs and Instructions designed to operate from either ACS side

- Transitions are modified to reflect SBC-only operations
- Some transitions are no longer valid; e.g., anneal
- FSW Image to be loaded is identical to Side-2 (except for MEB select byte)
- Side-1 load requires difference load from the time ACS switched to Side-2
- Difference load includes all on-orbit Side-2 changes
- Both Side-1 and Side-2 difference loads built with each ACS FSW release
- EEPROM has been managed from before launch

### 7.3.1 Side-Switch Methodology

The following is an overview of the steps for the switch to Side-1 SBC Operations as extracted from the Side Switch FRR (on February 15, 2007).

1. Initial Conditions
  - All ACS commanding has been removed from SMS timeline
  - ACS is in Safe (heater zones on Side 1) with power removed from Side-2
2. ACS reconfiguration
  - ACS to Side-1 Safe Mode
    - Remote Interface Unit (RIU), Science Data Formatter (SDF), and Side-2 Hold relay reconfiguration
    - NSSC-1 limit table selection patches
    - Safing Sequence Patches
3. Load the new SMAC20 to support ACS Side-1
  - *Wait for STScI analysis of WFPC2 UV images before proceeding – the WFPC2 images would be used to assess level of contamination from the Side-2 Anomaly.*
4. Transition ACS to Side-1 Boot and collect a baseline memory dump
  - Will not transition to Operate because of potential incompatibilities between the FSW and current database
  - Baseline Side-1 image with checksum and memory dump
5. Load Side-1 image changes into EEPROM via real time commanding
  - Verify load with checksum and memory dump
6. Activate new FSW via realtime commanding
  - Initial Jump to Operate
  - Verify transition commanding for Side-1 SBC-only operations through SBC Low-voltage mode
7. Safe ACS for SMS intercept

Seven DM-05 defined ACS transition changes were made in order to enable Side-1 SBC operations. The transition commanding modifications are listed here and illustrated in Figure 16 (from the FRR charts): Off to Safe, Launch to Safe, Safe to Hold, Boot to WFHROper, WFHROper to Boot, Hold to Safe, Safing Sequence.

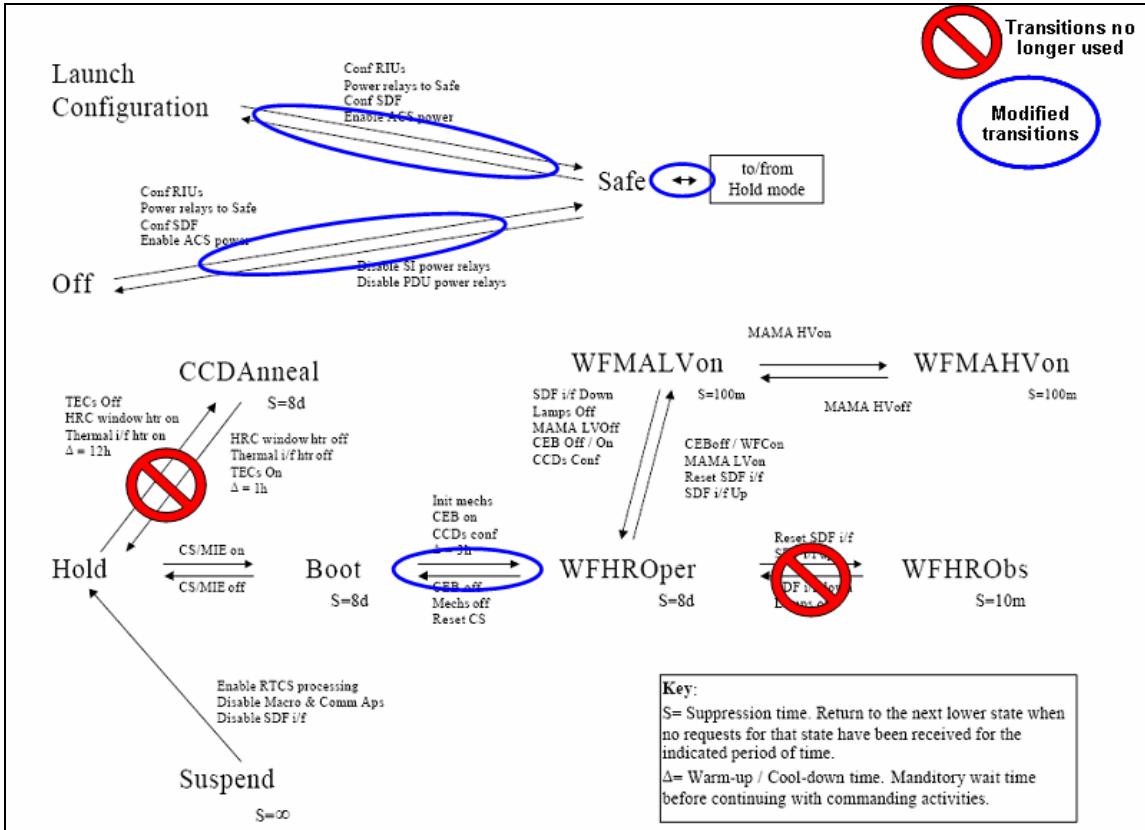


Figure 16. ACS Transition Changes for a Switch to Side-1 SBC-only Operations

Figure 17 illustrates the configuration after the full switch to Side-1 SBC Operate mode.

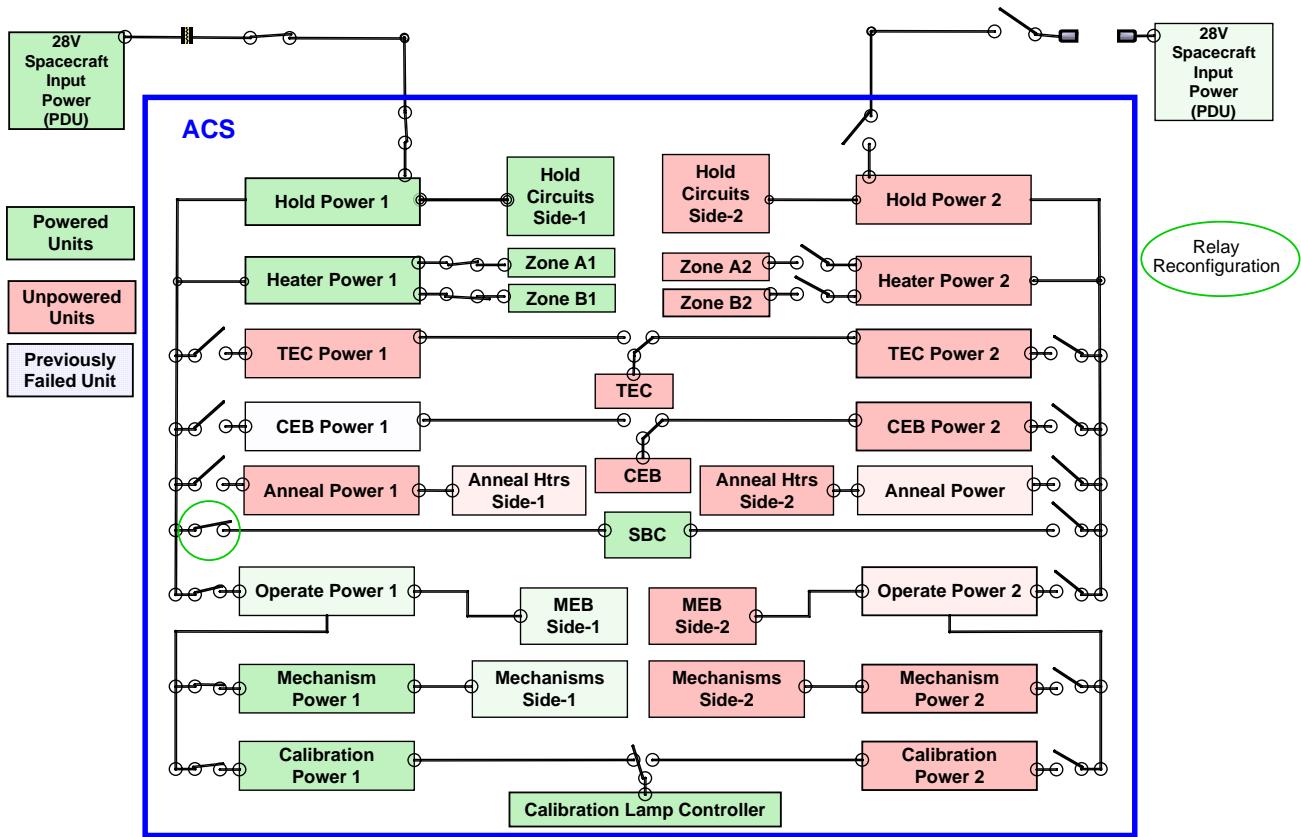
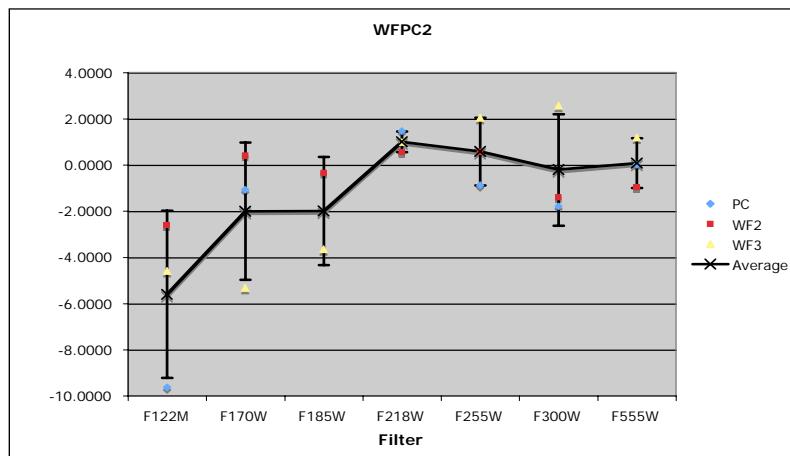


Figure 17. Final ACS state following the switch to ACS Side-1 SBC-only Operations

## 7.4 Conclusions from Science Observations

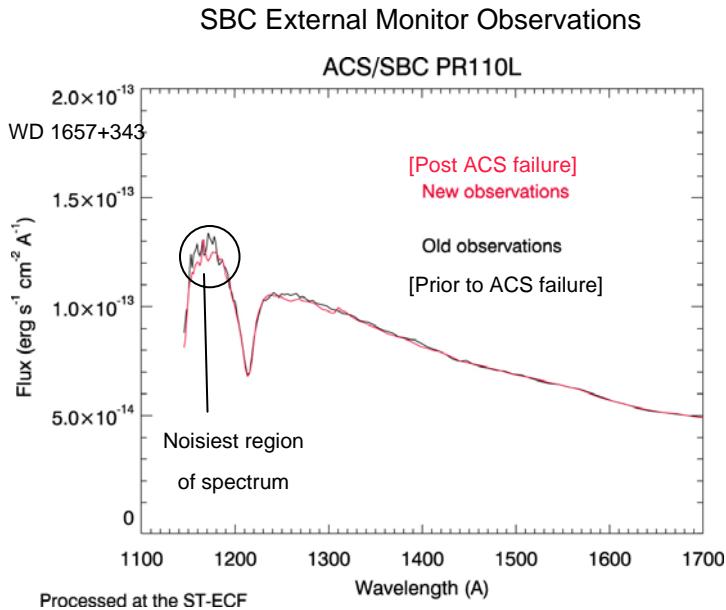
On Feb 16, 2007, analysis of UV images taken by WFPC2 was completed. These showed a degradation from the original fault of 5-6% with a 5% 2-sigma error bar]. The value represents an upper limit of a decrease in sensitivity. The analyses are show in Figure 18. The “go” was then given to proceed with the SBC commissioning and resumption of science data acquisition.

Figure 18. Percent Variation in WFPC2 Throughput: Before and After the ACS Side-2 Failure  
(courtesy ST ScI)

The SBC was successfully enabled on Side-1 on February 16, 2007. Calibration lamp flat field images obtained by the SBC showed a slight decrease in throughput (~0.5%) in the intermediate wavelength Long Pass Filters (F115LP, F125LP, F165LP) and a possible 8-10% +/- 4% decrease in throughput in the least used and shortest wavelength SBC filter F122M. Also, the last measurements through this filter were in October 2005 hence caution must be used in the interpretation that any measured decrease is due solely to the Side-2 event. Prism observations of a white dwarf standard star did not corroborate the potential loss in throughput through F122M. No decrease in counts was seen between August 2005 and March 2007.

Observations of a standard star cluster (NGC6681) in F125LP actually showed a potential increase in throughput although the error bars were comparable in size to the increase (2-4% +/- 2%). No reduction was seen. The conclusion at this time was that if a change in SBC throughput >1% did occur, it was restricted to the shortest wavelengths and was not severe. SBC UV throughput measurements are shown in Figure 19.

Science observations obtained with the SBC on Side-1 were and have been nominal and as expected.



**Figure 19. External SBC Standard Target Observations after the ACS Side-2 Fault**

## 8 Bus-C Test

### 8.1 Overview

The purpose of the Bus C on-orbit test was to isolate the fault. The test was split into 3 phases to accommodate the goals of ARB fault analysis.

Phase 1 was designed to test the Side-2 Hold relay and converter. This test would determine if ACS Side-2 can support Hybrid operations (i.e., operate on Side-1 but use the CEB function on Side-2; the Side-2 fault was have to be on the Operate bus for this scenario to be viable).

Phase 2 was designed to determine if Side-1 can support Hybrid Mode science if Hybrid Mode operations produced excessive readout noise (there is a high probability of noise because of the lack of power supply synchronization).

Phase 3 was designed to determine the available assets on the Side-2 Hold bus. Particularly to confirm the functionality of the remaining Hold bus relays and converters on Side-2 and the functionality of the Side-2 Operate relay and converter.

The concept for ACS Side-2 Phase 1 testing was approved on March 5, 2007. The objective of the phase 1 test was to isolate the Side-2 fault to the Hold or Operate domain and to determine if a short exists in the Side-2 electronics. In order to observe the fault current of the short, development of a high data rate telemetry format (T-Prime), Autonomous Command Response (ACR), and FSW Macros were required.

## **8.2 Bus-C Test Contamination Risk Assessment**

Prior to execution of the Bus-C test, an assessment of the contamination risk was performed. Even though a contamination source has not been identified, certain physical constraints apply: conversion of matter from solid or liquid to vapor state requires energy, and the quantity converted is proportional to the energy input. Because of the long duration of the initial anomaly, it is assumed that many materials were affected, and no new species are expected to be introduced. At low depositions, the throughput loss is proportional to the mass of contaminant deposited, thus the relative effect of the Bus-C test can be found by taking the ratio of the energy used by the Bus-C test to the energy used during the ACS Anomaly.

The total energy consumed during the anomaly event was approximately 4200 Joules. Bus-C powering of the short at 26V, 40A will consume 1040 J/s. The two likely durations for the Bus-C test were believed to be 50 ms (time until first relay open command takes effect) and 300 ms (time until second relay open command takes effect). The power consumptions for these durations are 52 J, 1.2% of the anomaly event, and 312 J, 7.4% of the anomaly event.

The degradation from the Bus-C test was expected to be an order of magnitude less than that of the initial event – which represented minimal risk to the Telescope.

## **8.3 Telemetry Modification to Support the Test**

An existing telemetry format, T-format, was modified to sample specific telemetry parameters at a high data rate for diagnostic purposes as well as “safe to continue” decision points. The modified format, T-Prime, monitored the following specified telemetry: load bus current at 1KHZ, structure and PDU current at 500 Hz, ACS redundant power status at 1 Hz , and main bus (A, B, and C) at 1/3 Hz. The vehicle time, relay state, several SI mnemonics and other hardware telemetry was available in this format. The T-Prime format was used during the macro commanding of main bus C, PDU Side-2, and Hold relay. Each SSM486 macro in Phase 1 commands included the transition to T-Prime format before hardware commanding, and automatically restored back to H-format (nominal format) at the completion of the macro. The

T-Prime data was displayed on a specified ops string in the Space Telescope Operations Control Center (STOCC) and Mission Support Room (MSR).

Additionally, high data rate telemetry and NSSC-1 format changes were needed for bus-C test. Since the STIS MEBs are off in safemode, the 7 bytes of STIS internally subcommutated telemetry was replaced with ACS telemetry. The STIS telemetry slots were temporarily replaced by the following ACS mnemonics:

- ACS Total Input Current (Side-2)
- ACS 28V Input Voltage (Side-2)
- ESM TPS Pressure
- ACS 5V Operate Voltage(Side-2)
- ACS Hold Relay State (side-2)
- ACS Hold Relay State(Side-2)
- ACS Operate Relay State(Side-2)
- ACS Htr Cntl Pwr Zone A Relay State(Side-2)
- ACS Htr Cntl Pwr Zone A Relay State(Side-2)
- ESM TPS Pressure.

A test database, Ops 69 PRD, was built and deployed to the VEST Operation Control Center (VOCC). This PRD allowed the special ACS data to be decommutated on the ground. A specific CCL was generated to facilitate monitoring, patching, and restoration of unused the STIS slots.

## **8.4 Autonomous Command Routine**

An ACR was developed to provide added protection during the test. The ACR would monitor the PDU2 current during specific periods of the on-orbit test. If the current exceeded 14.0 amps for 2 consecutive samples the ACR would issue commands to open the ACS Side-2 Hold relay.

## **8.5 Macro Commanding**

Critical hardware commanding was implemented via macros to ensure the timing with respect to the T-Prime high rate data and the command separation for the relay toggle test. Four macros were developed for the Phase 1 testing. The contents of each macro contained the commands to transition to T-Prime format, then wait 150 seconds to verify the format switch and telemetry. Each macro then issues the hardware command, waits 30 seconds, and then commands the transition back to H-format (the format switch occurs at next major frame boundary). Macro 1 closes the Primary Main Bus B relay, Macro 2 closes the ACS redundant power relay, Macro 3 toggles the ACS Side-2 Hold relay (RIU A) with a 50 msec wait. Macro 3 then waits 250 msec and disables the ASC Side-2 Hold relay, and Macro 4 enables ACS Side-2 Hold relay. ACS Side-2 Hold command would be issued via ground command.

## **8.6 Safety Precautions**

Many safety precautions were exercised for the test. To protect against contamination, all high voltage equipment was powered off. The Neon Leak Safemode Test was disabled, the FHSTs were off, and the FGSSs were commanded to default. Safemode Macro (SMAC00) was modified to switch back to H-format in the event a vehicle safemode entry occurs during the test. Without this change, the vehicle would remain in T-Prime format until a ground command is sent to switch formats or until SMAC05 executes and commands to A-format. All SPC stored commands and ACS hardware commands would be halted immediately upon a safemode entry. Additionally, an ACR was used to monitor PDU2 current for over-current protection during the Bus C test.

Modifications were made to the NSSC-1 response to a TPS pressure limit violation. To prevent an unnecessary safing of the NCC due to a pressure rise from the potential ACS short, the NSSC-1 response was changed from safing the NCC to posting an Executive Status Buffer (ESB) for the TPS limit violation. An actual loss of pressure integrity within the NCC would result in safing due to limit violations on any number of other independent telemetry monitors within the system (e.g., loop pressures, system temperatures, compressor slip command parameters (voltage, current m frequency) etc). This change was a permanent change for normal operations following the test. NSSC-1 General Purpose Event Flag Processor (GPEFP) slot 15 was configured to monitor the TPS pressure telemetry and set ACS event flag 15 if a violation over  $2 \times 10^{-5}$  torr was detected. The NSSC-1 RTCS monitoring the status of ACS event flag 15 would result in opening the ACS Side-2 Hold relay (2x) and posting an ESB message if the flag is observed to be set. The RTCS was loaded and inhibited via the SMS and was expired following the test. The GPEFP 15 slot was restored following the test.

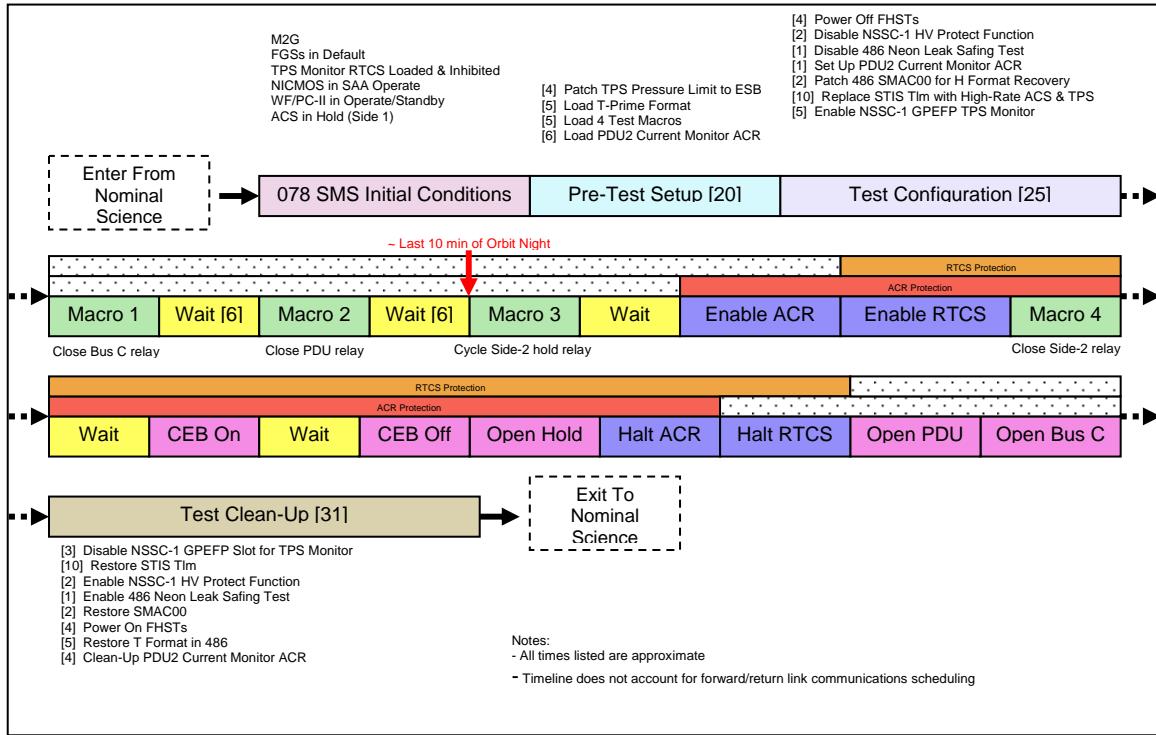
## **8.7 Bus C On-orbit Test**

HST Project approval was given on March 22, 2007 to proceed with the on-orbit test. To support the on-orbit test, IP-129 was developed for the installation and execution of the Special Processor Macros, Format T-Prime, and ACR for PDU over current protection. This procedure provided the operational commanding necessary to support the ACS Side-2 and Main Bus C on-orbit testing. The procedure:

- loaded the T-Prime test format, the macros and ACR
- modified SMAC00 for safemode protection
- disabled/enabled Neon Leak Safemode test
- enabled/disabled the ACR macro
- restored flight version of T-format
- provided commanding for Special Processor Macros usage.

The Bus C test was executed on March 27, 2007. The command window began on 086/10:05 UTC with five orbits of dedicated time were allocated for the test by the Space Telescope Science Institute (STScI). During the entire the test window, the vehicle was in M2G mode. The FGSSs were in default mode and the TPS monitor RTCS was loaded and inhibited. NICMOS was in SAA Operate, WFPC-2 was in Operate/Standy, and ACS was in Hold mode

on Side 1 at the beginning of the test. The on-orbit test activities were broken into four parts as shown in Figure 20.



**Figure 20. On-Orbit Test Timeline**

### **Part 1: pre-test setup**

This section patched the NSSC-I TPS pressure limit action and installs T-Prime format, Bus C SSPC macros and ACR support macros

### **Part 2: final configuration to support the test**

To protect against possible contamination the FHSTs (3) were powered off. The Neon Leak safing test was disabled. The ACR SSPC macros were activated and SMAC00 was modified. The NSSC-I HV Protection was deactivated and the NSSC-I GPEFP for TPS monitoring was enabled. The commanding to replace STIS telemetry with ACS was executed. Finally the ACS event flag 2 was set to prevent any HV commanding to the SBC for the duration of the test

### **Part 3: execute Macros 1, 2 and 3 as specified in the test timeline.**

Macro 1 was commanded 10 seconds before the major frame to close Main Bus C as shown in Figure 21.

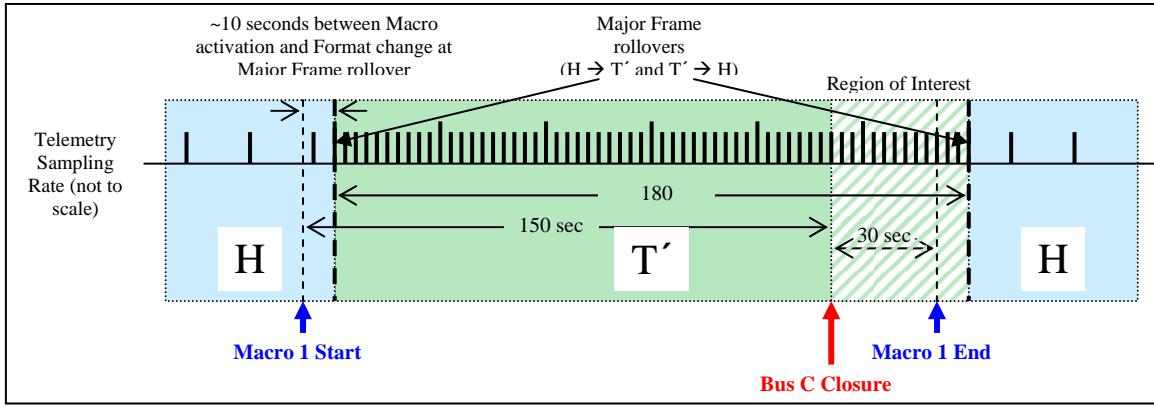


Figure 21. Macro 1 Execution Timing

Macro 2 was commanded 10 seconds before the major frame to close the PDU2 relay (ACS Side-2) as shown in Figure 22. The ACR 3 was enabled for current monitoring.

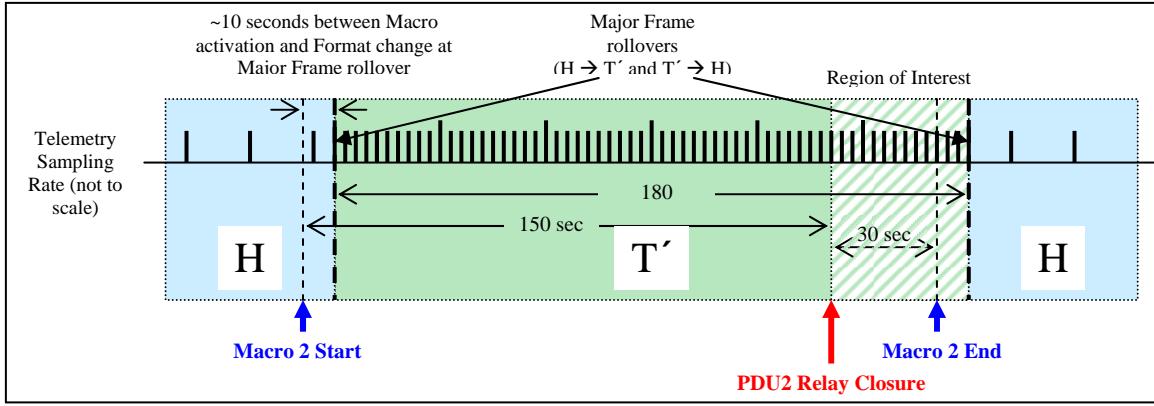


Figure 22. Macro 2 Execution Timing

Macro 3 was commanded 10 seconds before the major frame to cycle ACS Hold relay (closed for 50 msec) as shown in Figure 23. To mitigate against vehicle safing during the 50 msec window in Macro 3, a ground command was issued to open the ACS Side-2 PDU relay after 166 sec from start of macro 3 activation. Finally, Main Bus C was powered off.

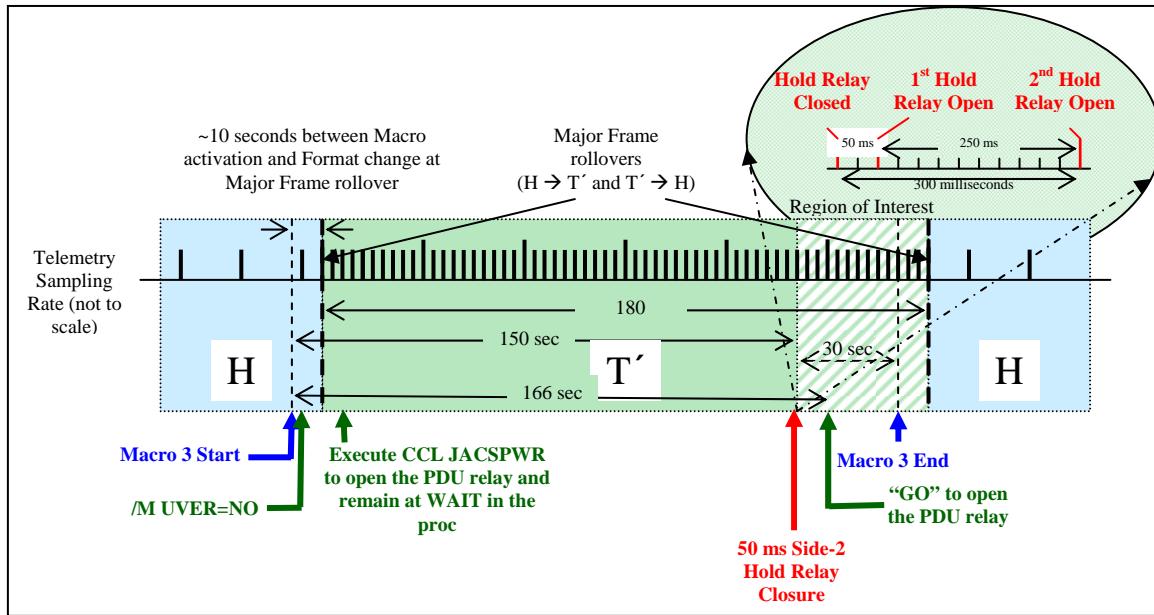


Figure 23. Macro 3 Execution Timing

#### **Part 4: Configure the vehicle for nominal operations.**

The STIS telemetry was restored. The NSSC-I HV protection table for TPS pressure and cyrovalve temperatures was enabled. The ACS Event Flag 2 was cleared to all HV commanding in the SBC and the Neon Leak Safemode test was enabled. The FHSTs were powered on and SMAC00 and T-format were restored to nominal configuration.

### **8.8 Bus C Test Results/Conclusions**

Phase I of the ACS Main Bus C testing was completed via execution of Operations Requests 18024 through 18027 on 27 March 2007 (DOY 086). Following the execution of the Side-2 Hold relay closure portion of the test through Macro 3, analysis of the high-rate T-prime format telemetry data revealed a substantial increase in the ACS load current of almost 60 Amp for about 130 ms (see Figure 24 and Figure 25). Elevated PDU2 current was also observed near 30 A, while vehicle structure current was seen to jump to 15 Amp and steadily rise to approximately 24 Amp. Additionally, the HST486 current monitor Automated Command Response (ACR), which was set in place as an added safety measure tripped following 2 consecutive out-of-limit samples above 14 A.

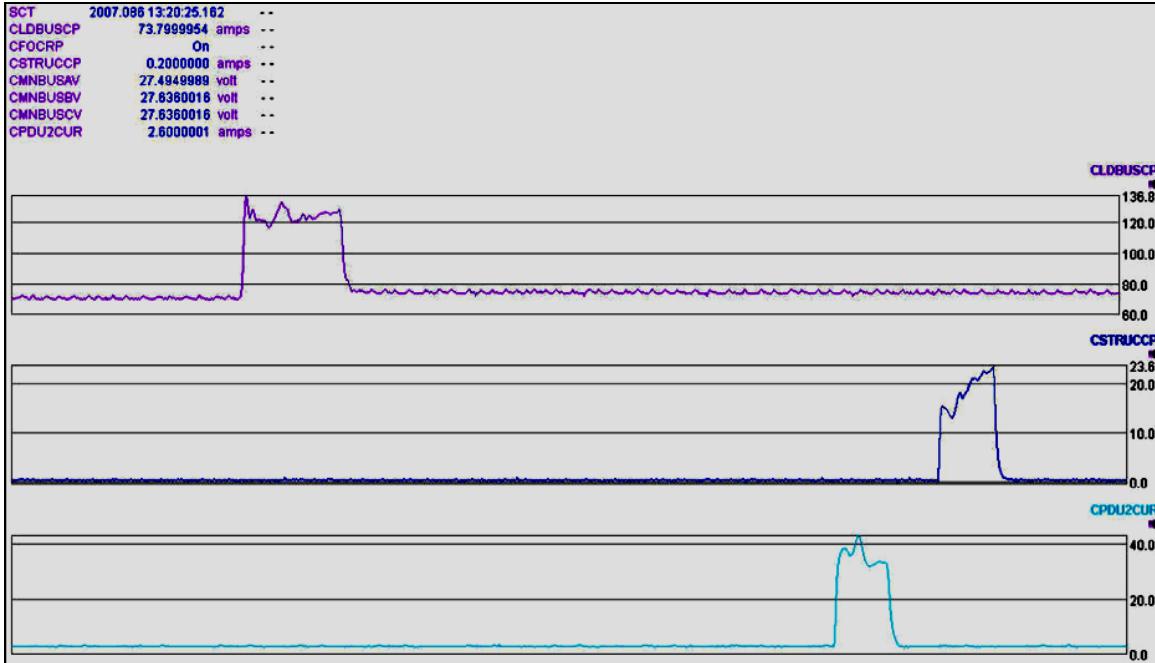


Figure 24. Realtime Data Collected via High Rate Data Format

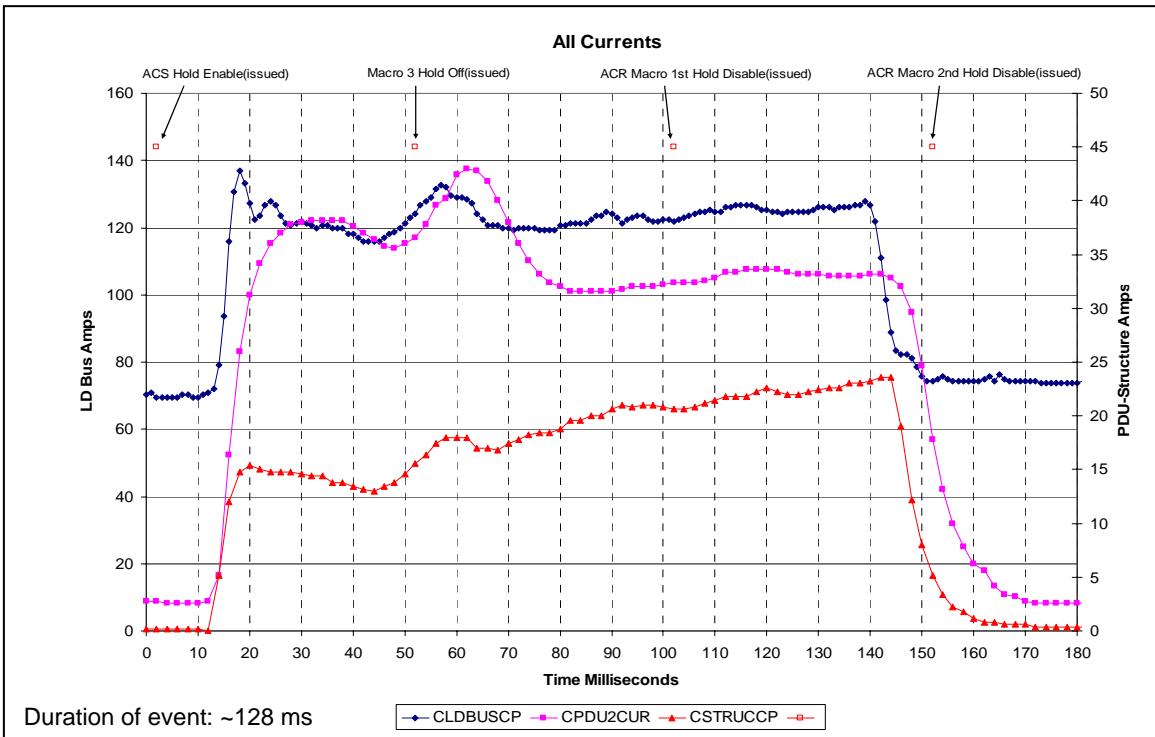


Figure 25. Actual Data Collected

During the test, the ESM TPS reported a pressure increase to just over  $1 \times 10^{-6}$  torr, roughly two orders of magnitude lower than the 27 January event and about 20 times shorter in duration (see Figure 28). This corresponds to significantly less gas generation than the original failure, by

approximately 2 orders of magnitude. All indications are that the Bus C fuse “blew”. Figure 26 represents the configuration after the test, which is the current configuration as of the writing of this report. Following the completion of the test, the spacecraft was returned to its nominal configuration, including powering on the FHSTs, the restoration of the High Voltage Protect sequence, and the deactivation of Main Bus C.

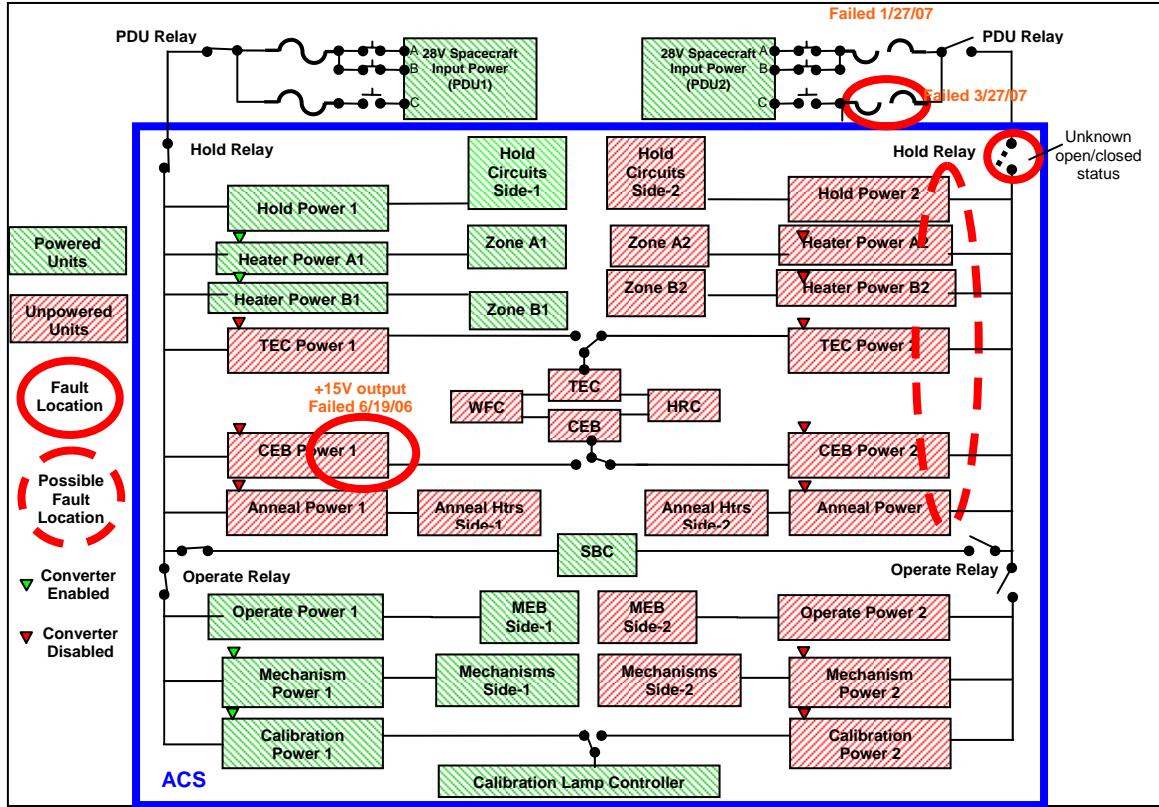


Figure 26. Failure Path Overview

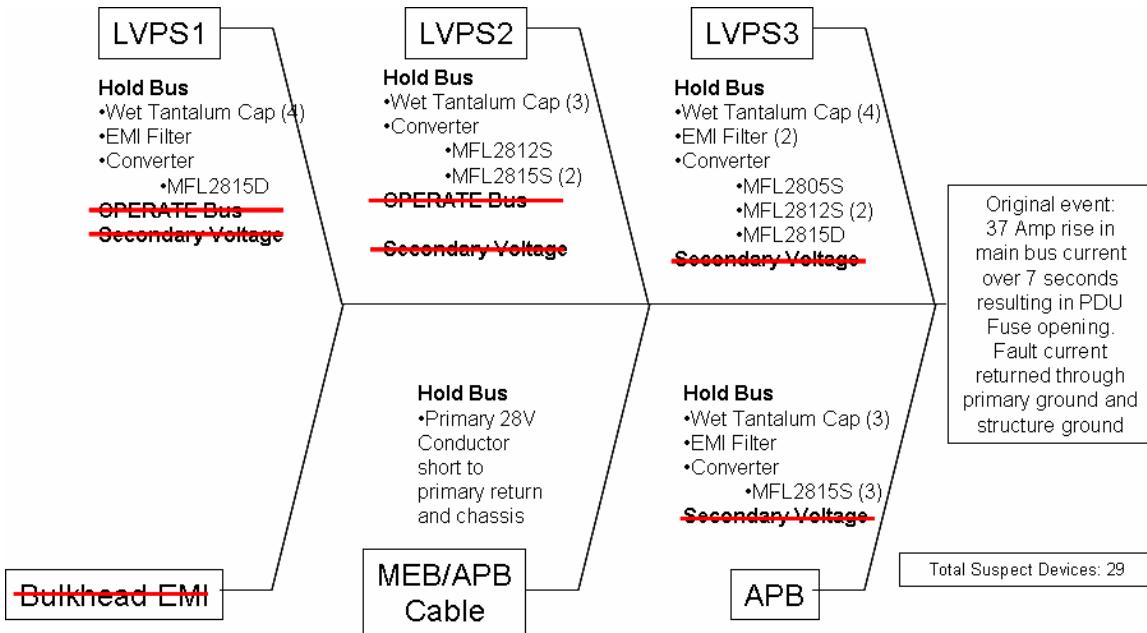
Follow-on analysis of the test results was able to quantify the Main Bus C short as  $0.54 \Omega$ , or 27.6 V at 51 A, compared to 0.6 W for the 27 January failure. The total energy of the Main Bus C event was calculated to be 170 J as compared to the energy of the original event on Main Bus A/B of 4300 J. Using the numerical integration of the sum of the PDU2 and structure currents (less the contribution of the SIC&DH on the same PDU), the total fuse stress for the test was determined to be  $315 \text{ A}^2\text{s}$ .

Completion of Phase 1 of the ACS Main Bus C Test allowed the following conclusions to be drawn:

- The ACS failure occurred on the primary service side of the Side-2 Hold Bus (see Figure 27 for the resulting (and final) version of the fault tree), despite the fact that the ~55 A draw through the PDU2 fuse is within the operational tolerance of the relay according to Leach data sheet specifications.
- The failure in and of itself cannot be considered a ‘dead’ short, and must be downstream (i.e. toward the instrument) of the EMI bulkhead filter circuitry in ACS.

- As the current path appears to have persisted between the 27 January failure and the 27 March Bus C Test, theories involving transient phenomena such as plasma arcs or tin whiskers may be discounted.

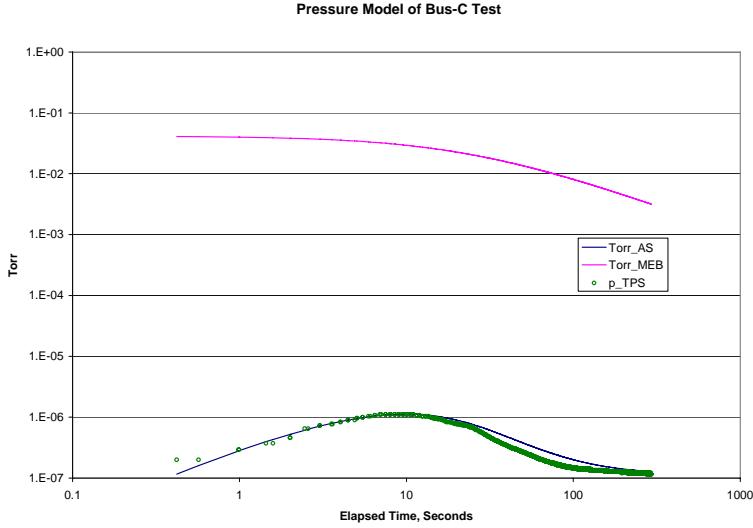
Since only Phase 1 of the testing could be completed, no additional information on the condition of the Side 1 CEB could be discerned.



**Figure 27: Final ACS Fault Tree including Bus C Test Results**

## 8.9 Bus-C Test Contamination Model Correlation

The actual Bus-C test energy consumption was 4% of the original anomaly event and lasted 170 ms. Using the venting model, the generation term that best fit the TPS data was an initial burst of 100 Pa-L. The predicted MEB and Aft Shroud pressures are shown in Figure 28. Note that the rate of TPS telemetry was increased for this test.



**Figure 28. Bus C Test: Predicted and Measured Pressures**

Comparing the mass of evolved gas in the Bus-C test to the mass evolved in the anomaly event gives a ratio of 1.67%. It is reasonable that the power ratio of 4% is greater than the mass ratio of 1.67% because much of the energy was expended in heating the material to the vaporization point, as well as in Joule heating of other electrical components. The expected degradation from this event is less than 0.06%, which is not detectable by the HST instruments.

## 9 Ground Based Testing

During the course of the ACS Side-2 ARB, a few of the ARB members were alerted to concerns raised by JPL coworkers regarding the potential for hardware damage caused by resonances that could arise between Interpoint DC/DC converters and their associated Interpoint EMI filters. The resonance behavior is directly related to the inherent negative input impedance characteristic of the DC/DC converters.

Early Spice model simulations indicated that resonances around 8-12 KHz and additional resonances around 80-100 KHz would be present. This early analysis was conducted simulating a worst-case, no-load condition, which is not realistic when compared with HST on-orbit hardware and operations. In addition, the initial modeling did not account for inherent system level parasitics nor did it account for the Science Instrument front end ‘Dog House’ input filter. Be that as it may, the early simulations did indicate that a potential for an 88dB gain at 8 kHz was possible. Using a conservative analysis with the equation  $V_{db} = 20 \log (V / V_0)$ , this indicated that the high rail of the 28V converter input could spike up potentially to almost 40 volts. It was also stated that the voltage spike could be closer to 100V on a 1V line step change.

The potential for such high voltage resonances based on initial Spice modeling was reviewed by the ARB. In order to investigate this concern fully, the ARB agreed that a course of ground tests was required. Three major ground test efforts were executed in the following order:

1. ACS VEST Software Test and Integration Facility (VSTIF) Bench LVPS engineering signal evaluation
2. Bench Level Testing with just Interpoint Converters and Interpoint EMI filters

### 3. ACS VSTIF Bench LVPS resonance testing (Conducted Susceptibility Testing)

In addition to these ground test efforts, a Science Instrument Independent Review Team (SI-IERT) was commissioned by HST Code 442 to aid in this investigation. The SI-IERT visited the engineering team at Interpoint and then proceeded to generate Spice models of the HST Interpoint Converter system, inclusive of real world parasitics and all HST SI components, including the ‘SI Dog House Filter’ circuitry. This refined model indicated that the resonances that could occur would only be in the 10dB to 15dB range. In other words, the peak amplitude of the resonance would never exceed 55V, where all of the components are rated to 100V. This finding was drastically different from the previous initial assessment of resonances on the order of 88dB. Therefore, real world hardware testing was required to validate the accuracy of the modeling.

#### **9.1 *Ground Test 1: ACS VSTIF Bench LVPS engineering signal evaluation***

The ACS VSTIF Test Bench contains an ACS flight like MEB. This MEB contains a full set of three engineering LVPS boards and a dog house input power EMI filter section. Each LVPS board contains the suspect Interpoint EMI filters (FME28-461 /883) and DC/DC Converters (various MFL28\*\*\* /883 types).

For the purposes of this evaluation, the ACS power system was divided into manageable segments based on EMI input filters. Each segment was then evaluated as follows:

- Attached differential scope probe to output of EMI filter
- Baseline measurement @ 28V one converter enabled at a time (to extent possible) at nominal VSTIF load value
- Manually swept voltage range from 24V up to 32V
- Where possible, altered VSTIF load values and repeat steps 2 and 3 above
- Enabled all converters and swept voltage range from 24V up to 32V
- Performed additional transient switching tests as deemed necessary (enabling and disabling converters at varying loads, as well as transient dynamic load change response to extent possible)

The goal of the test was to identify any unanticipated voltage transients in the system and then further characterize them in order to determine their source.

Detailed test results and waveforms are provided in Appendix 1 on page 65 of this report. A summary of the findings follows:

- No resonances detected on primary power bus between Interpoint EMI filter and Interpoint Converters. However, it is also noted that this test was not configured to inject noise in an attempt to elicit resonance behavior.
- No load condition on Thermal Converters resulted in cycle skipping behavior of the output secondary voltage (sawtooth type waveform). This no load condition is purely a result of the ground test hardware not containing heater loads like the flight article. On-orbit thermal loads of just under 10 Watts are present in the flight instrument. Therefore, this phenomenon was noted during this test, with the intent of adding variable realistic on-orbit max/min loading in a later test (ACS VSTIF Bench LVPS resonance testing) and evaluating the response.

- No load condition on Thermal Electric Cooler (TEC) Converters (MFL2812S converters externally configured as constant current mode devices) resulted in the primary input bus being dragged down to approximately 10V for 5ms, presumably by the converter's input FETs turning on hard, as a function of the TEC Converter being disabled. This phenomenon was not expected at the time. However, this testing did note that under a nominal orbital TEC load scenario of 1.5 ohms, the system responded nominally. Therefore, this no load TEC disable scenario is considered to be not operationally possible (since a TEC load of 1.5 ohms is always present on-orbit) and should therefore be treated as an outlier condition that can not be realized on-orbit. Subsequent investigation into this MFL2812S response by the SI-IRT with Interpoint and the Wide Field Camera-3 (WFC3) team revealed that this phenomenon had been previously seen by the WFC3 team in a slightly different circuit application and was reported to Interpoint. Interpoint was aware of this issue with the older /883 devices and indicated that this issue had since been corrected by a design change that added a bleed down diode between the converters input FET and Power Input section. Thus, this issue was corrected on the newer SMFL devices. WFC3 has since verified that to be true; the new SMFL devices no longer exhibit the primary bus shorting disturbance during power disable operations.

The results of this testing concluded that no load conditions would result in effects such as cycle skipping and, in the case of the TEC Converters, disruption of the primary bus input during converter disable operations. However, these conditions are considered outliers since they are not achievable with the on-orbit flight hardware. Additional testing of these conditions was conducted during the ACS VSTIF Bench LVPS resonance testing.

## **9.2 Ground Test 2: Bench Level Testing with just Interpoint Converters and Interpoint EMI filters**

Bench level testing was conducted to see the effects of adding converters to the output of an Interpoint filter. The Bench level testing did not incorporate all electrical components present in the flight design or thermal heat sinks, however, this testing was invoked to provide a first look sanity check to determine if full up flight like circuit testing was necessary. Refer to Appendix 2 on page 89 for the full test writeup.

The first days testing ended when a converter suffered a catastrophic failure. The feedback loop stability testing showed little to no margin in its stability, and also seen were resonance point between the EMI Filter and the converters with and without external capacitance. Also examined was the efficiency of one converter under very low loads, and it was found that with the light loading there is approximately 2 watt dissipated in the converter.

## **9.3 Ground Test 3: ACS VSTIF Bench LVPS resonance testing (Conducted Susceptibility Testing)**

A test plan was generated to further investigate the ACS LVPS power system's hardware sensitivity/potential for resonance issues and to verify correlation of the refined HST SI power system SPICE model to actual HST hardware designs.

Due to the large number of hardware configuration permutations possible, the ARB/Code 442 decided to limit the scope of this testing. Prior to the execution of this test, on-orbit ACS Bus C

Testing confirmed that the ACS Side-2 shorting anomaly was physically located on the ACS Side-2 Hold bus. Therefore, this test concentrated on converters that are located on the Hold bus only.

The VSTIF ACS test bench was configured to provide enough variability to effectively characterize the system's hardware design sensitivity/potential for resonance. The following 'variables' were set/adjusted as follows:

- Bus Voltage: The ACS Test Bench Sorenson Supply was initially set to 26.5V; this matched the ACS internal voltage measured just prior to the ACS on-orbit anomaly. Testing was also conducted at max and min bus voltages, 32V and 24V respectively.

Nominal Bus V = 26.5V

High Bus V = 32V

Low Bus V = 24V

- Loads: VSTIF ACS Test Bench secondary loads were set using variable power loads (resistive load boxes), where possible, to closely match loading conditions experienced just prior to the on-orbit anomaly.
- Thermal Control Loads: Based on on-orbit experience, Thermal Control Loads were tested at the following max/min behavior per +15V converter:
  - Typical = 10W
  - Min = 5W
  - Max = 25W
- TECs: Based on on-orbit experience, the HRC and WFC TECS were tested at the following max/min secondary current draw behavior per converter:

Typical = 2.3 to 2.4 Amps (-76.5C setpoint)

Min = 1 Amp (-66.7C setpoint)

Max = 4.2 Amps (-90.0C setpoint)

The test was designed to evaluate the system response to injected primary power line ripple. A copy of the detailed test plan is provided as Appendix 3 on page 103 of this report.

Using an Impedance Analyzer (HP 4194A) and injecting AC frequencies from 100 Hz up to 1 MHz onto the input power bus, the overall system impedance response was measured. All test results were plotted and are contained in Appendix 4 on page 115 of this report.

A review of the data indicated that the SI system had two distinct responses to injected power line ripple. One was Differential Mode, and the other was Common Mode. The Differential Mode measurements, made between the Primary Power output of the Interpoint EMI filter and the associated Primary Power return, showed excellent attenuation (-40 dB at approximately 10 KHz). The system response did not change drastically as a function of changing variables, such as bus voltage and loads.

The Common Mode measurements, made between the Primary Power output of the Interpoint EMI filter and the chassis ground of the system did show some attenuation. A maximum of 18

dB of Common Mode attenuation was measured at approximately 23 KHz. Using the equation  $V_{db} = 20 \log (V / V_0)$ , 18 dB of gain for a 1V peak to peak noise signal translates to an amplified voltage of only 8V peak to peak. Thus, a 32V DC bus input with a 1V AC noise signal riding on it would be amplified to maximum of 36V. The piece part devices are rated for 100V, and thus are not affected by this modest gain. If one were to assume a 2V peak to peak noise signal, the amplified voltage would only be 16V. Thus, a 32V DC bus input with a 2V AC noise signal riding on it would be amplified to a maximum of 40V, thus still remaining well under the 100V rating of the devices.

Due to the difference in Differential Mode versus Common Mode response, the ACS VSTIF test bench was checked to ensure grounding was flight like. A review found that the Primary Power return did not connect back to the Common structure ground at any point. On orbit, this single point ground is achieved back at the PCU. Therefore, the team decided to add a Primary Return to Chassis ground interconnection very close to the ACS VSTIF power supply to ensure grounding was like that of HST on orbit. Appendix 5 on page 137 contains the ACS VSTIF Bench LVPS resonance testing (Conducted Susceptibility Testing) results with and without the added connection between Chassis ground and Primary Return near the power supply source. A review of the data indicated that the Differential Mode and Common Mode responses were nearly identical to those previously measured without this added grounding.

As a final check of the system's robustness, a sinusoidal noise sweep was conducted and frequencies that produced audible sounds were noted. The test team then allowed the test system to dwell at those frequencies that produced the audible sounds for approximately five to ten minutes. In each and every case, the system continued to function without any noticeable change in secondary output voltages or performance. The system continued to function without any anomalies.

In addition to the resonance testing, the ACS VSTIF Bench Sync signal waveforms were evaluated at the input to the converters with respect to their Primary Ground pin. Refer to Appendix 6 on page 147 of this report for the detailed waveforms. The Sync signals were found to be 0V to 5V, approximately 50% duty cycle signals. All Sync signal edges were clean; there were no double transitions noted on either the rising or falling edges. All of the Sync waveforms appear to be nominal; no concerns were noted.

## **9.4 Conclusion**

The modest Common Mode gain of only 18 dB measured on the full up flight like SI ACS hardware, tested in a flight like condition with Sync and Inhibit signals present and used as designed in orbit, led the team to conclude that the risk of hardware damage induced by system resonance effects was very low. JPL representatives agreed that although the addition of added internal filtering to the power supply designs would be helpful, it was not absolutely necessary in light of the ground test results obtained.

## 10 Recommendations

### **10.1 On-orbit Testing of Assets for Side-1 WFC/HRC Science Operations**

The upcoming ACS-Repair (during SM4) is intended to restore operability to the Side-1 WFC (and possibly the HRC). However, relevant WFC (and HRC) Side-1 hardware has not been used since the Side-1 CEB failure in June 2006. The ARB believes that it is important for the HST Operations Project to demonstrate the ability to power hardware that is required to support ACS Side-1 Science operations post-SM4. This test should be performed prior to the installation of the new CEB. The assets include:

- WFC & HRC CCDs and CEB electronics
- Optical paths
- WFC & HRC Thermoelectric Coolers (TECs)
- Shield TEC
- Anneal components (interface plate heaters, window heaters, APB)
- Filter wheels
- WFC & HRC shutters

The ARB recognizes that there are associated risks to performing such a functional test. These risks include, but are not limited to:

- Unforeseen or a repeat of a Side-2 like failure on Side-1, which could lead to a high current draw on the main bus and result in a blown Side-1 PDU 20 Amp fuse. The result would be the inability to perform Side-1 SBC science, which is the only science mode currently available on either side.
- Side-2-like failure on Side-1 will subject the HST to contamination and the potential for collateral damage.
- If the Side-2 fault occurred in the APB, collateral damage to the Side-1 APB may be present since both sides are housed in the same box
- If a fault occurs on Side-1 during an on-orbit test, and the ACS fails, other subsystems may be impacted

The HST Operations Project will further address the risks and mitigations associated with such an on-orbit test, and ultimately decide on a course of action.

### **10.2 On-orbit Testing of Assets for Side-1 Contingency Loads**

Contingency loads are required 1) in the event of a hardware failure that would disable the full complement of the identified assets for load shedding *and* 2) a battery failure or during the execution of a Battery Capacity Test. In the past, ACS components were included to support load shedding activities. Although Side-2 assets are no longer available, the HST Operations Project is currently considering using the following *Side-1* ACS components as contingency loads:

- Interface plate heater
- Window heater
- APB

Due to possible collateral damage sustained from this latest anomaly, however, these assets are in an unknown state of operability. The ARB thus suggests testing each of the above items to confirm their availability if the Project decides to include them as contingency loads.

### **10.3 Replacement of the PDU2 Fuse Plug**

The ARB recommends replacing the fuse plug unless higher priority mission objectives are present and competing for EVA time. The benefit will be the possible use of the full instrument (i.e., both sides) if the plug is ever replaced.

### **10.4 Leach Relay**

The ARB reviewed in detail the possibility that one of the ACS Leach relays (PDU2 relay, Side-2 Hold relay, Side-2 Operate relay), welded closed during the anomalous event (refer to “ACS Bus C Test Design Review” presentation for details). All three relays are 3-pole double throw on a common rocker. Welding any one of the contacts would immobilize all three poles. The team concluded that all relays experienced currents below the design ratings; thus, there should be no impact to the contact or reliability due to the initial anomaly. Part specification requirements state no contact sticking and weld free operations for up to 50 cycles at currents of 50 and 60 Amps per contact.

During the Bus C test, currents reached 55 Amps through the Hold relay, but since the contact was only exercised once before the part was still in spec. However, indications imply that there could have indeed been a welding event. The ARB recommends further investigation of a possible welding event of the relay. The GSFC Parts Branch has been in contact with the manufacturer and is pursuing the issue.

### **10.5 Multiple Converters Hanging off an under-dampened EMI Filter – Possible Resonances**

With respect to the resonance issue raised by JPL (see Section 9), the ARB believes that the ground test data has shown no resonance present that is of any concern to the current and future complement of instruments. The SI-IRT, who is delving into the issue, agrees with the ARB. Although the risk is considered low, some members of the ARB believe that additional filtering should be considered. At the very least, the ARB recommends additional testing related to phase and gain margin, which has begun with the continued support of the SI-IRT.



**Appendix 1: ACS VSTIF Test Bench Evaluation, Date:  
2/23/07**



ACS Side-2 ARB #2  
 ACS VSTIF Test Bench Evaluation  
 Date: 2/23/07

Introduction:

The ACS Side-2 ARB #2 was informed of concerns raised by JPL colleagues that the HST ACS anomaly may have been caused by a voltage/current ringing phenomenon that can occur between Interpoint EMI Filters and Interpoint DC/DC Converters. JPL has generated Spice models that corroborate the potential for excessive ringing between these components that could lead to destruction of certain components both internal and external to the Interpoint devices in question. The Spice modeling indicates that there is a higher risk of being impacted by this phenomenon as the following system variables occur:

1. Multiple DC/DC Converters feeding from a single EMI Filter. The larger the number, the greater the risk.
2. Lightly loaded DC/DC Converters. The lighter the load, the greater the risk.
3. High bus voltage. The higher the bus voltage, the more likely the occurrence of oscillations.

The ACS design meets all of the risk criteria variables defined above, namely:

1. Up to four DC/DC Converters are feed from a single EMI Filter
2. The Interpoint MFL28\*\* Converters are rated for 65 Watts. In ACS operations at the time of the anomaly, a number of the Interpoint converters were operating at less than 10 Watts (<15% of rated).
3. HST Bus Voltage can range from 24V up to 32V due to normal day/night charge/discharge cycles. The ACS internal voltage was at approximately 26.5V at the time of the anomaly.

In light of ACS being compliant with the established risk factors as determined by the JPL analysis, the ACS ARB authorized an evaluation of ACS ground assets to determine if evidence of ringing could be located in the ACS system hardware as designed.

ACS Engineering Hardware:

The ACS VSTIF Test Bench contains an ACS flight like MEB. This MEB contains a full set of three engineering LVPS boards. Each board contains the suspect Interpoint EMI filters and DC/DC Converters (Note that this is unlike the ACS ESTIF unit, which does not contain all of the flight like circuitry). The boards are not conformally coated.

The construction of the three LVPS boards is such that current probes could not be used without modification to the boards (i.e. would require adding wire loops). Therefore, the team agreed that the prudent means of investigation would rely on evaluating voltage waveforms between the

EMI Filters and their associated DC/DC Converters to the extent possible. Variables such as input voltage were manually adjusted to determine the effect. However, the test bench does not readily allow for changes to secondary loads. Where possible, secondary loads were adjusted/changed and the impact evaluated.

For the purposes of this evaluation, the ACS power system was divided into manageable segments based on EMI input filters. Each segment was then evaluated as follows:

1. Attach differential scope probe to output of EMI filter
2. Baseline measurement @ 28V one converter enabled at a time (to extent possible) at nominal VSTIF load value
3. Manually sweep voltage range from 24V up to 32V
4. If possible, alter VSTIF load value and repeat steps 2 and 3 above
5. Enable all converters and sweep voltage range from 24V up to 32V
6. Perform additional transient switching tests as deemed necessary (enabling and disabling converters at varying loads, as well as transient dynamic load change response to extent possible)

The goal of the test is to identify any unanticipated voltage transients in the system and then further characterize them in order to determine their source.

Testing was conducted using the following test equipment:

Oscilloscope: Tektronix TDS 754A S/N B0011563, Cal due date = 10/4/07

Oscilloscope Probes: Tektronix P5205 100 MHz High V Differential probes S/N B016462, Cal due date = 4/5/07

Additional test equipment was used to look at the primary bus voltage in the frequency domain:

Spectrum Analyzer:

It should be noted that at the initiation of testing, it was determined that the act of connecting a scope probe to LVPS2 U9 pin 1 (WFC Shield TEC DC/DC Converter +28V input pin) resulted in the ACS telemetry system reporting the +28V hold bus voltage was at 0V. The scope verified that this was not the case, and that the bus voltage was truly +28V. Debug determined that the bench primary power rail in relation to the secondary power rails are floating with respect to each other at this time (i.e. not reference to each other at a star ground point within the GSE), thus resulting in the primary bus sampling circuit drifting out of range relative to the primary rail. As this issue is not expected to interfere with Primary power rail oscillation measurements with respect to Primary return, the testing was allowed to commence and this issue will be correct at a later date.

Test Team:

Testing was conducted by Roger Chiei, Jack Shue, John Kolasinski, Ed Cheung, Steve Arslanian, and Bill Kantonki

### ACS Test Segments:

Below is a summary of findings obtained from testing each segment. Detailed waveforms are shown in section following this one.

#### Hold Converter

DC/DC Converter	Function	Orbit Load @ Anomaly	VSTIF Load	Comment	Board	Bus
MFL2815D	Hold Converter	20W	14W	No findings	LVPS1	Hold
MFL2812S	WFC Shield TEC	10W	0W	Approx 400mv drop in V @ 43 Hz . Did not collapse as voltage was raised.	LVPS2	
			16.8W	No findings		
MFL2815S	Thermal Controller A	<10W	1.4W	When enabled at low V, approx 100mv drop in V @ 200 Hz. Effect disappears when V raised >25.3V. Did not return when V lowered again down to 24V. Restart at V<25V required to see voltage dips again.		
MFL2815S	Thermal Controller B	<10W	1.4W	When enabled at low V, approx 100mv drop in V @ 200 Hz. Effect disappears when V raised >24.8V. Did not return when V lowered again down to 24V. Restart at V<24.8V required to see voltage dips again.		

#### Thermal Electric Coolers (TECs)

DC/DC Converter	Function	Orbit Load @ Anomaly	VSTIF Load	Comment	Board	Bus
MFL2812S	HRC TEC	6W	0W	Substantial voltage drop detected during converter turn off	LVPS3	Hold

MFL2812S	WFC TEC	10W	0W	Substantial voltage drop detected during converter turn off		

### CEB Converters

DC/DC Converter	Function	Orbit Load @ Anomaly	VSTIF Load	Comment	Board	Bus
MFL2805S	CEB	50W			LVPS3	Hold
MFL2815D	CEB					

### APB Converters

APB converters are not present on the VSTIF test bench and therefore could not be evaluated.

DC/DC Converter	Function	Orbit Load @ Anomaly	VSTIF Load	Comment	Board	Bus
MFL2815S	Window Heater	0W	N/A	Not enabled at time of anomaly; only used during anneal operations	APB	Hold
MFL2815S	Interface Heater A	0W				
MFL2815S	Interface Heater B	0W				

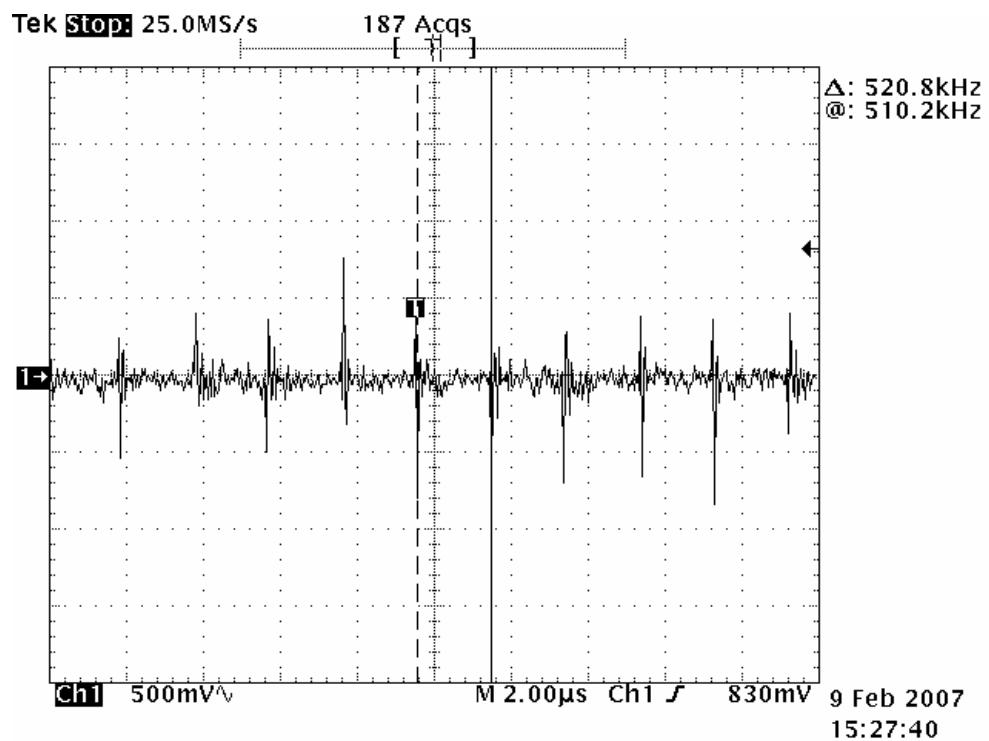
### Operate Converters

DC/DC Converter	Function	Orbit Load @ Anomaly	VSTIF Load	Comment	Board	Bus
MFL2805S	Operate Converters	60W			LVPS1	Oper
MFL2815D						
MFL2805S	Cal Lamp -5V		2.8W (partly here and partly in 2815D in Mech converter section)			

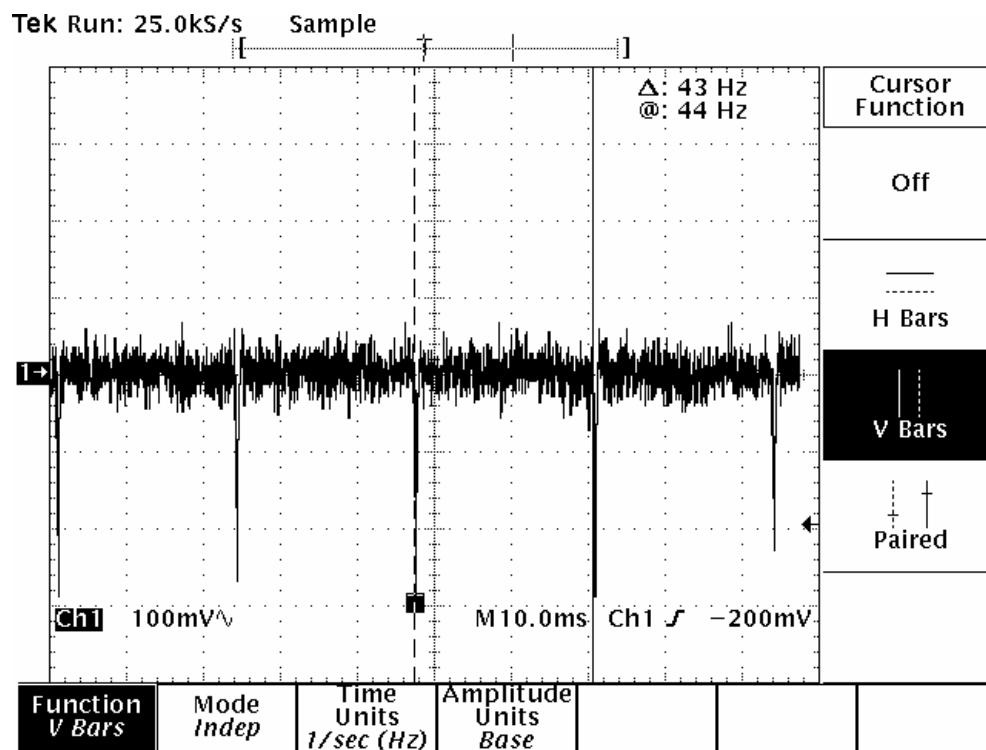
## Mechanism Converters

DC/DC Converter	Function	Orbit Load @ Anomaly	VSTIF Load	Comment	Board	Bus
MFL2815D	Cal Lamp	5W	2.8W (partly here and partly in 2805S in Operate converter section)	No findings [Dual +/-15V stacked to produce +30V supply]	LVPS2	Oper
MFL2805S MFL2815S MFL2815S	Mech Converters	15W	14.1W	200 Hz beat detected at low V start in range of 24V to 25.3V. Effect disappears when V raised >25.3V. Did not return when V lowered again down to 24V. Restart at V<25V required to see voltage dips again. [+5V,+15V,+30V using two +15V]		

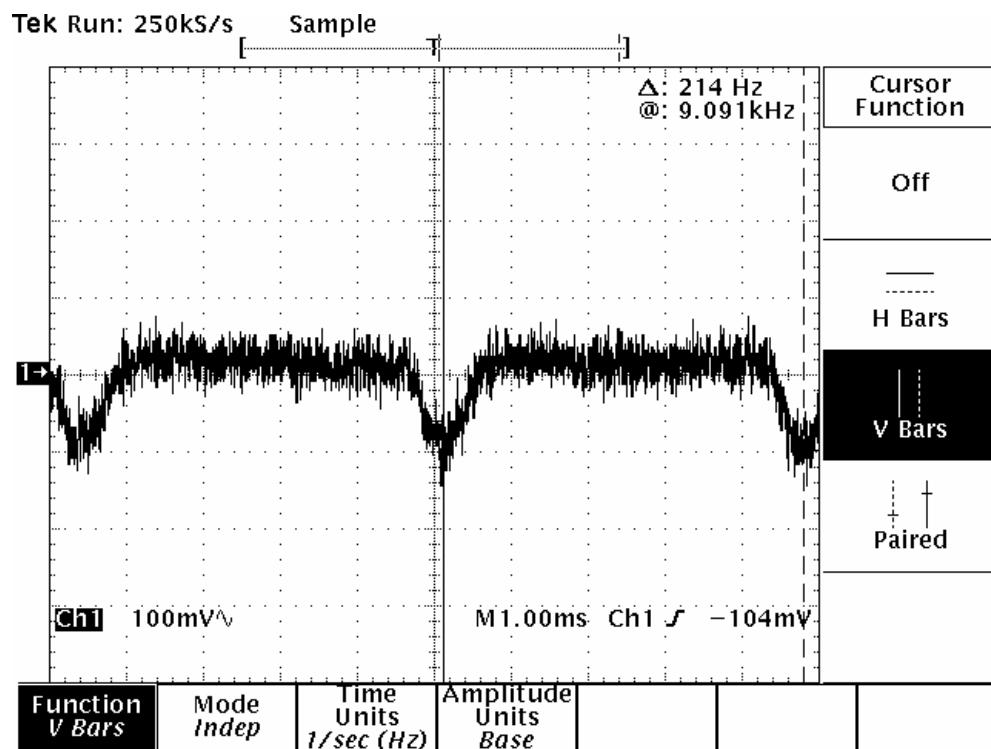
The following pages contain test waveforms captured during the investigation.



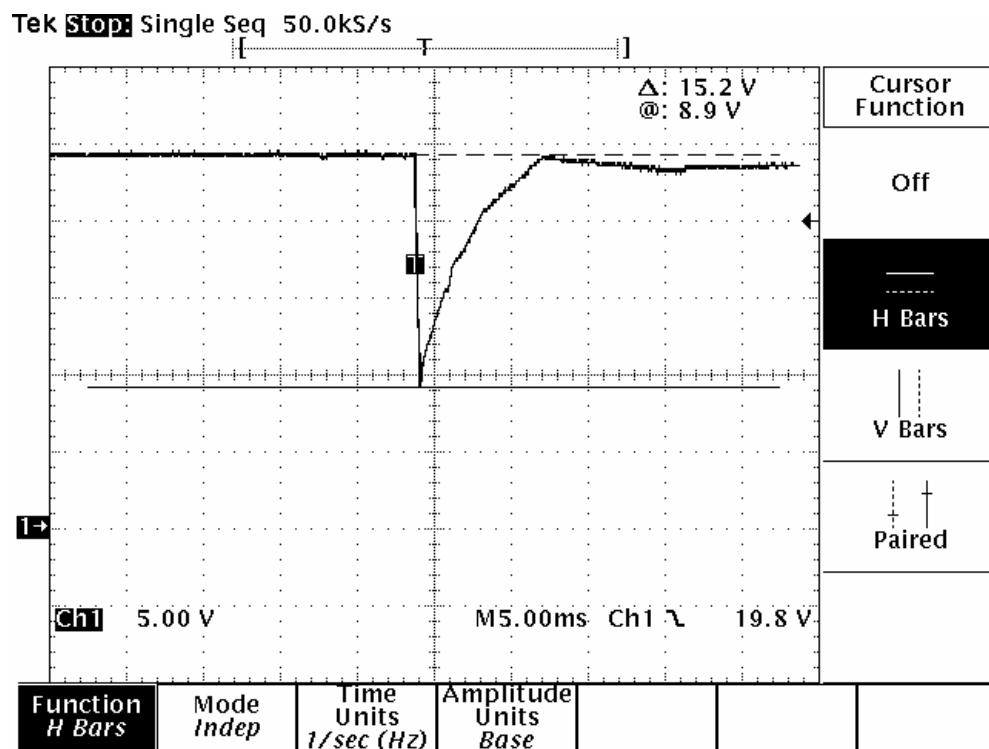
Switching Frequencies seen at input to Cal Lamp converter (part of Mech EMI filter section)  
Frequency on the order of 500KHz Interpoint switching.



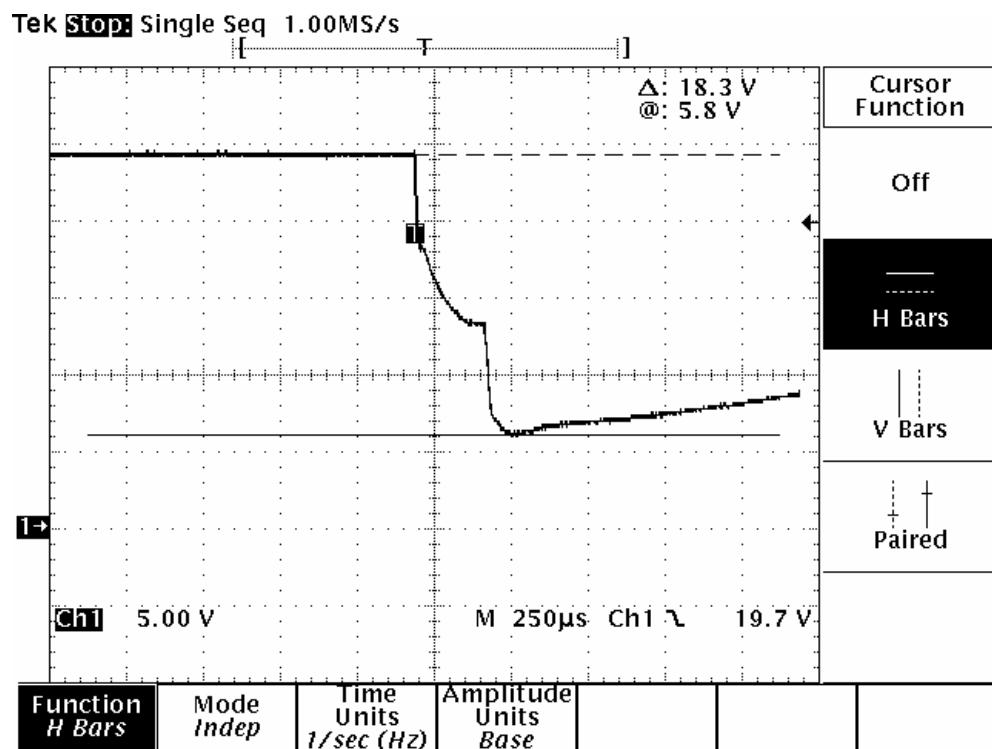
WFC Shield TEC Converter enabled at 24V. Approximately 40 Hz noise detected and remained as Bus V raised up in voltage to 28V. Waveform did not collapse.



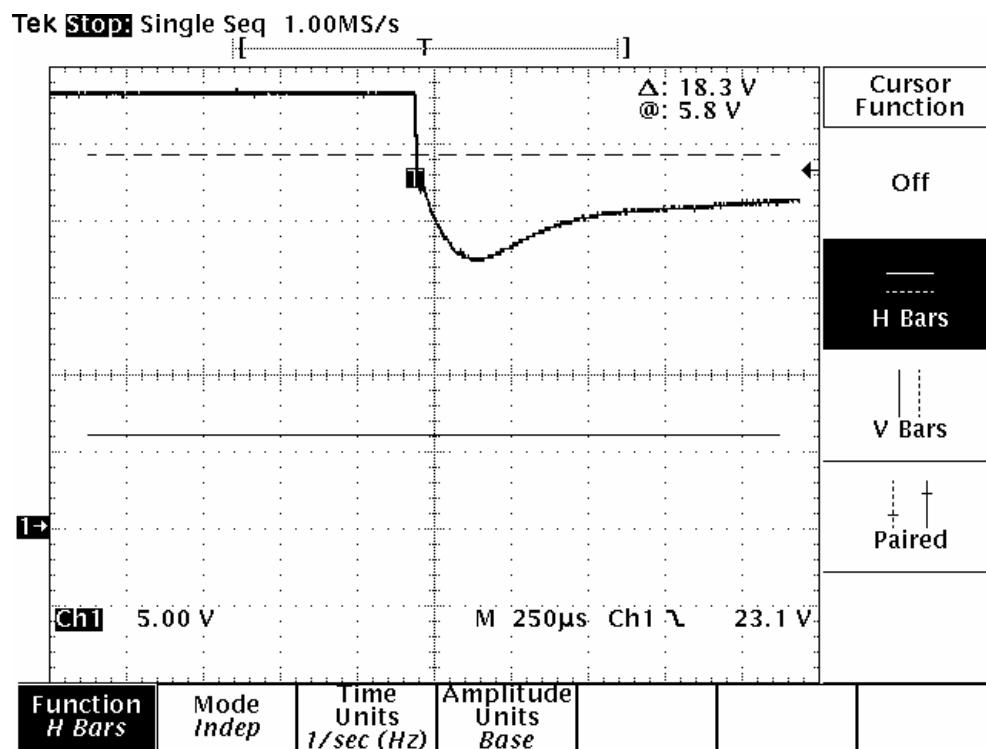
Mech Converter (with Cal Converter disabled) enabled at 24V. 200 Hz noise detected and remained as Bus V raised up to 25.3V. Ripple disappears above 25.3V, and does not re-appear if bus V decreased to 24V again. The Mech Converter must be disabled and re-enabled below 25V in order to obtain the ripple seen above.



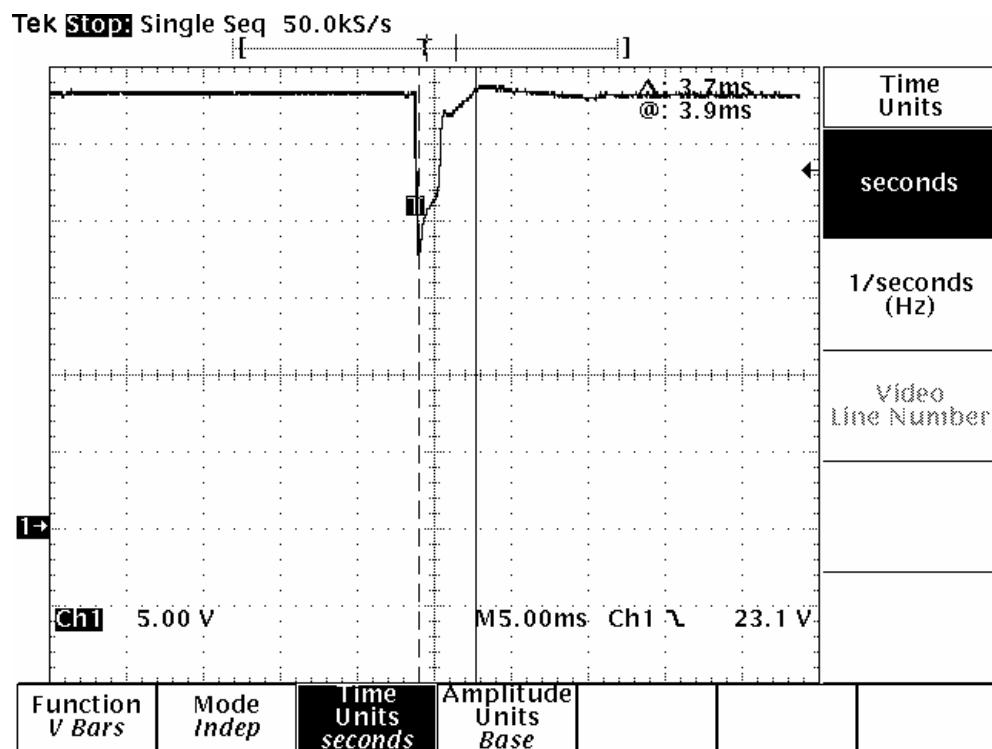
Converter Disable Testing: Initial condition = Hold bus, both Heater converters and the Shield TEC at no load were enabled and operating at 24V Primary Bus. The Shield TEC converter was commanded off. A 15.2 V drop in the Primary Voltage for approximately 5 ms is detected.



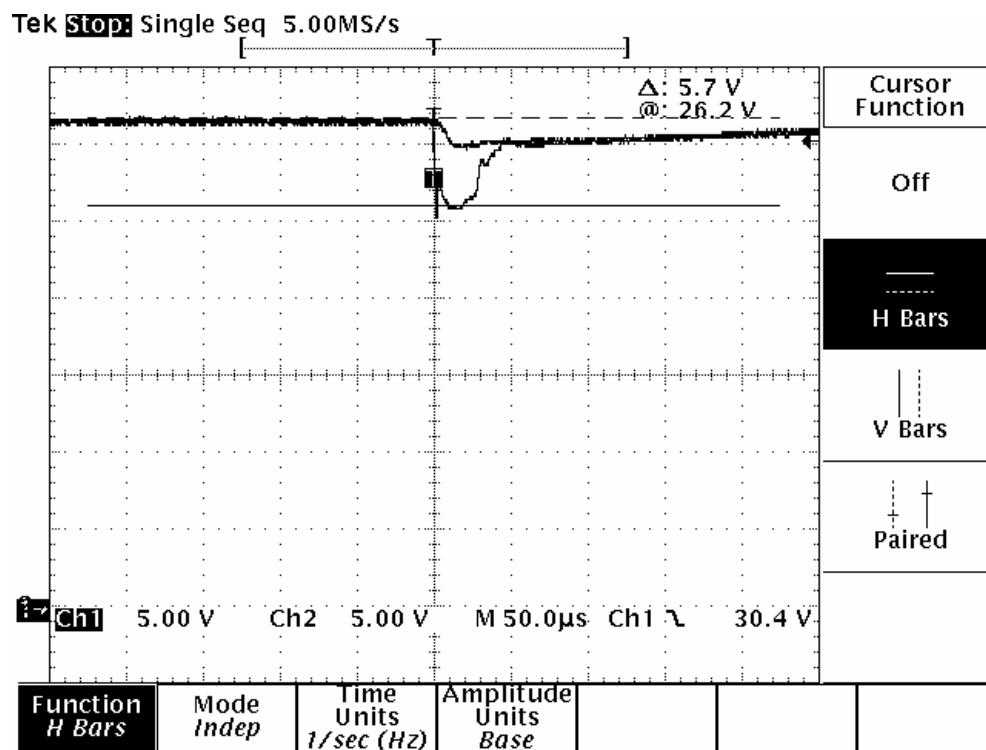
This image was taken using the same criteria as the previous image (24V Primary Bus), except zoomed in on the leading edge of negative going Voltage transient



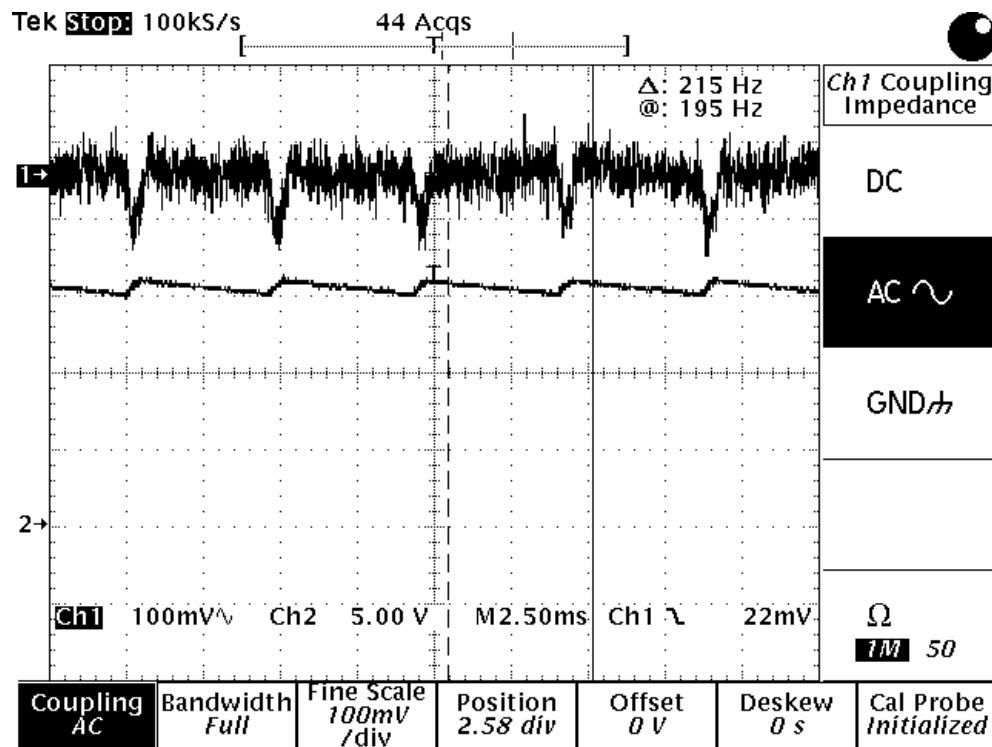
This image was taken using the same criteria as the previous two images except that it was executed using a 28V Primary Bus. The bus voltage drops by approximately 10V in this case, less than the drop detected at lower bus voltages.



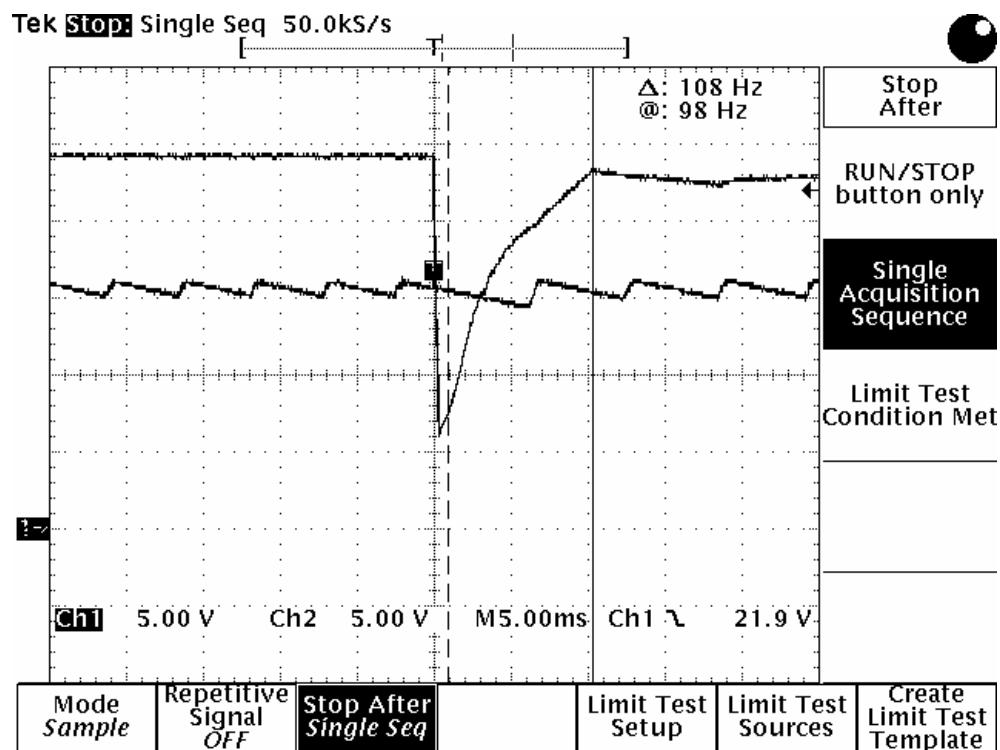
This image was taken using the same criteria as the previous image at a 28V Primary Bus. The bus voltage drops by approximately 10V.



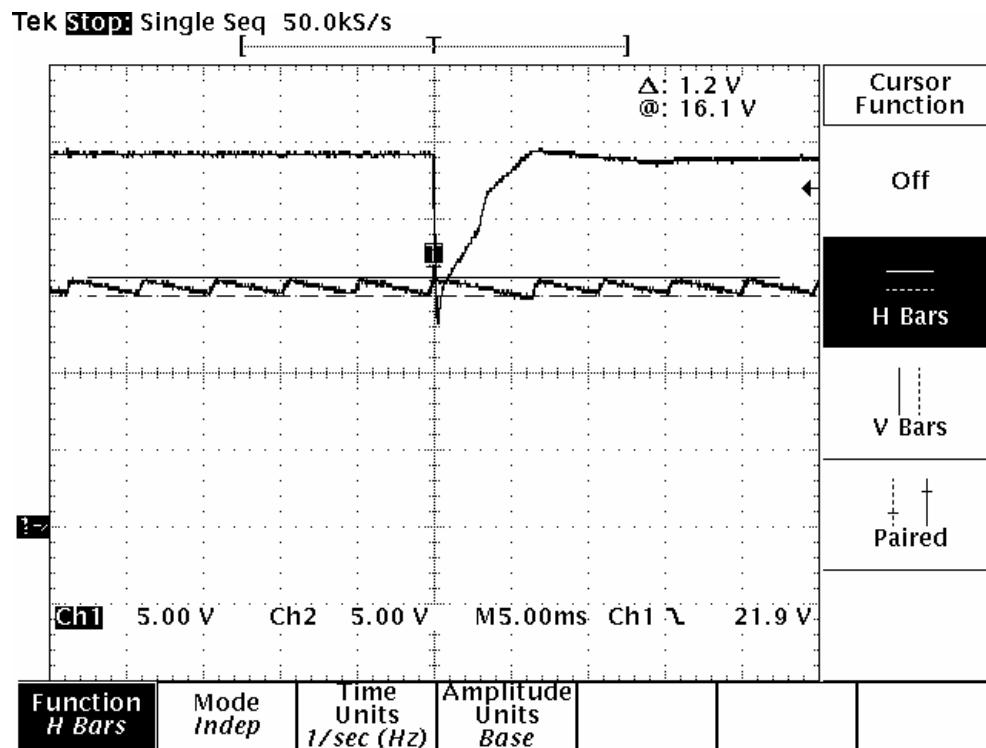
At a 32 V Primary Bus, the impact of turning off the unloaded Shield TEC converter is a drop in bus voltage of 5.7V.

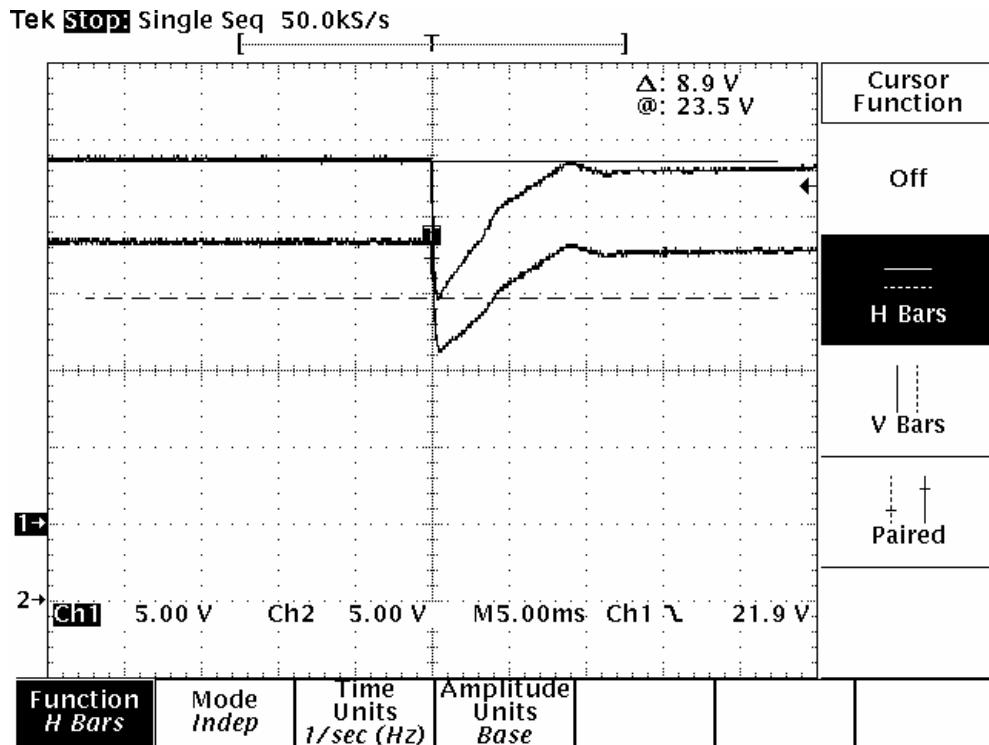


Heater B secondary +15V output was monitored. Note that the Primary Voltage bus chop corresponds with an output +15V regulation problem (i.e. the saw tooth waveform). This effect is due to cycle skipping, caused by the no load condition present in the VSTIF ACS test bench (i.e. unlike on-orbit, there are no heater loads in the VSTIF bench).

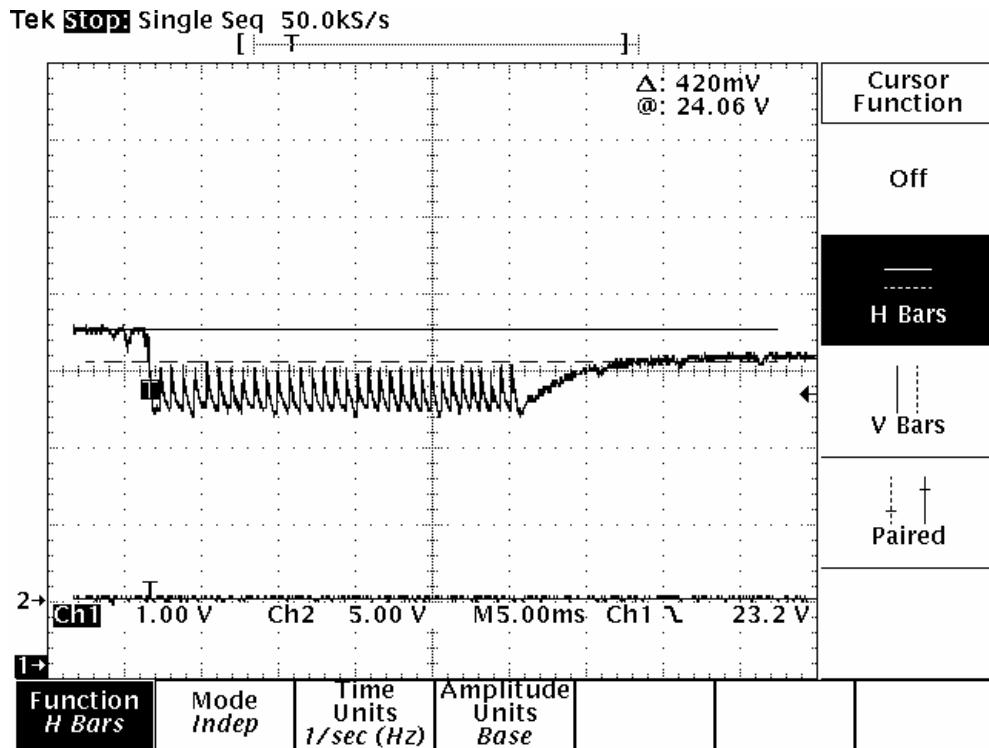


Heater B secondary +15V output was monitored at a 24V Primary Bus input. The Shield TEC with no load was commanded off. Chan 2 shows the Heater B secondary voltage response to the bus transient generated by turning off the Shield TEC converter.



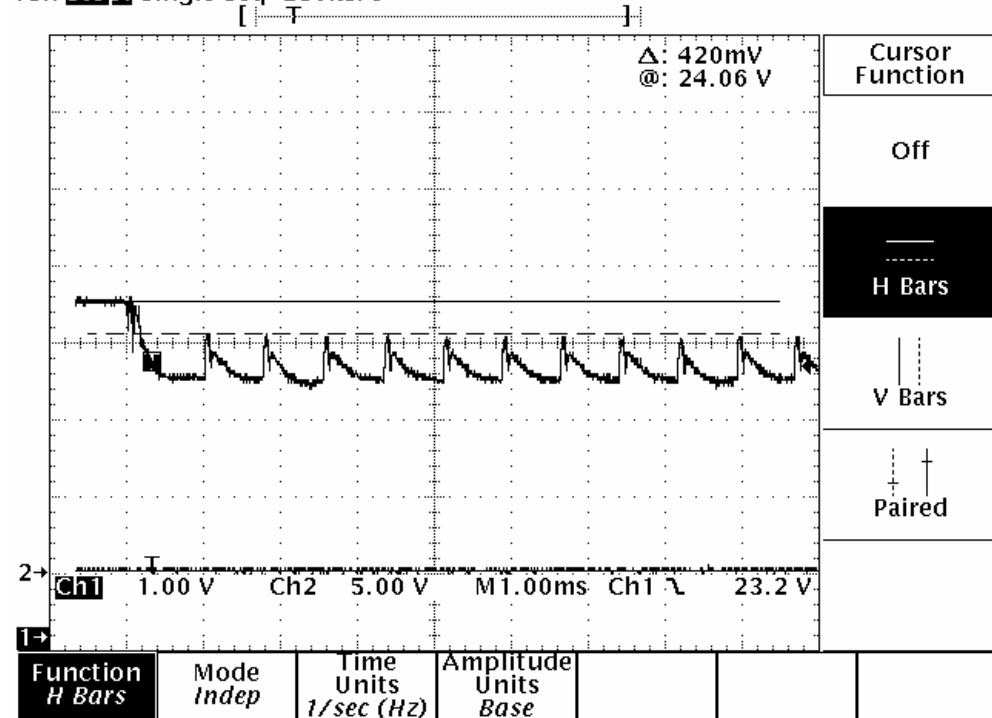


The Primary Bus voltage was monitored at the outputs of the HOLD EMI filter (Chan 1) as well as the outputs of the MECH EMI filter (Chan 2, located on the Operate bus). This test was conducted at 24V. The Shield TEC converter with no load was commanded off. Both scope channels detected the bus voltage transient.

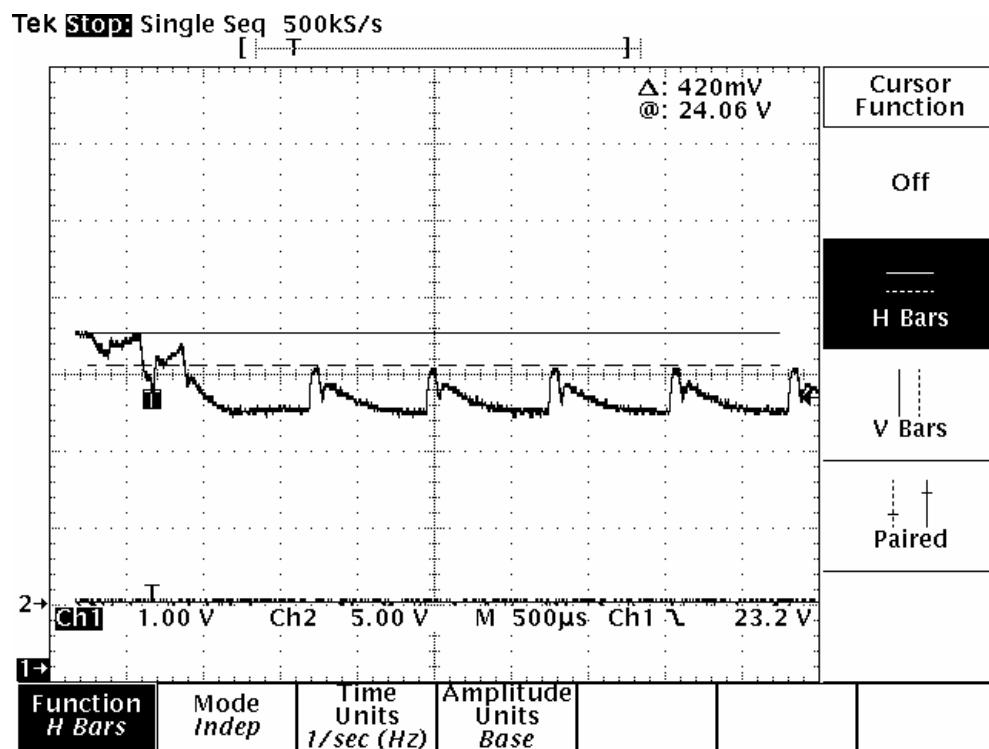


Dynamic Load Transient Test: Transient load testing was performed at a 24V Primary Bus with the Shield TEC converter. The Shield TEC converter output was subjected to a no load to full VSTIF load transient and the Primary Bus V was monitored. Dynamically switching in the load caused the bus to drop down 1V until recovery.

Tek Stop: Single Seq 250kS/s



Same test as previous image.



Same test as previous image.

A Spectrum Analyzer was connected on EMI Filter outputs while the two heater zone converters were enabled and the Shield TEC with its load was enabled. The Spectrum Analyzer detected a 517 KHz switching frequency from the Interpoints. It also detected a 39 KHz switching frequency from an unknown source. Converters were disabled one at a time, but 39 KHz component remained. Ultimately, the HOLD bus was switched off, which resulted in a decrease in amplitude of the 39KHz component, but not elimination. Thus, the 39 KHz is being introduced into the system by some other mechanism in the test system other than through the power bus of power bus components themselves. Removal of probes from unit under test was required to eliminate presence of 39 KHz frequency.

## **Appendix 2: Bench Level Testing with just Interpoint Converters and Interpoint EMI filters**



## **Events Leading Up to the Failure of an Interpoint Converter**

Jack Shue Code 563 301-286-5752 3/22/07

### **Abstract**

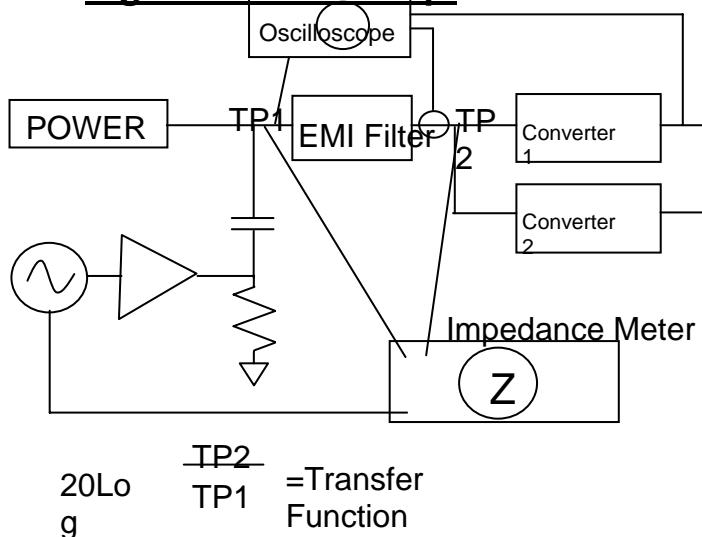
Bench testing started on Monday February 26 2007 to see the effects of adding converters to the output of an Interpoint filter. The first days testing ended when a converter suffered a catastrophic failure. The feedback loop stability testing showed little to no margin in its stability, and also seen were resonance point between the EMI Filter and the converters with and without external capacitance. Also examined was the efficiency of one converter under very low loads, and it was found that with the light loading there is approximately 2 watt dissipated in the converter.

### **Test Plan**

The plan was to look at the transfer function from the input of the Interpoint EMI filter to its output at DC – DC converters input as converters and capacitors were added. The EMI filter, DC-DC converters and capacitors were chosen to duplicate those being used in flight. The filter and DC-DC converters were from residual stock and were of the same date code. To inject the noise at the front, the standard Mil-Spec 461 CS02 test set up was used. The frequencies in question were high enough that the capacitor injection method was used. One deviation of note was the amplitude of the signal was not modulated to keep the signal at a given level, instead the signal varied in amplitude, and was limited to a maximum of less than 100 milli-volts (or 0.5 amperes). The order of testing was to start with just the EMI filter, then to add one converter, and then a second converter, and finally a third converter (the third converter was never added). At each step different loading was to be used. The loading was to be stepped from 0.1A to 4A.

After the catastrophic failure of one of the pair of converters, testing was done to determine the feedback loop stability on the surviving converter and then the external capacitors were added to see their effect on the resonance point of the EMI Filter. Thermal imaging was also preformed to see if there were any hot spots appearing due to the loading of the converter. Imaging was done both at low loads and at higher loading. Thermal testing did not show any unusual heating patterns at low loads.

Power consumption and converter efficiency measurements were made at low load to determine how much power remains inside the converter when it is under light loads.

**Figure 1 Test Set Up.**

## Results and Observations

**Table 1. The resonance frequency, and magnitude of the first resonance point that was observed under different filter and converter conditions.**

Load	Resonance Frequency	Gain dB
Filter No Load	68kHz	34 dB
Filter 0.1A Load	32kHz	12 dB
Filter 4 A Load	35kHz	11.8dB
Filter one converter 0.1 A Load	19.8kHz	10dB
Filter one converter 4 A Load	20.8kHz	11.5dB
Filter two converters 0.1 A ea.	~15kHz*	~10dB*

\* Failure occurred before data was saved.

\*\* dB = 20 Log (V2/V1)

During all testing an oscilloscope was looking at: 1. The EMI filter input voltage, 2. The EMI filter output current, and 3. The DC – DC Converter output voltage. In all but the two-converter case, the peak current (measurement as seen on the scope) was made at a resonance point. In the case of the 2 converters being on the filter the peak current was at a lower frequency than what was appearing on the transfer function.

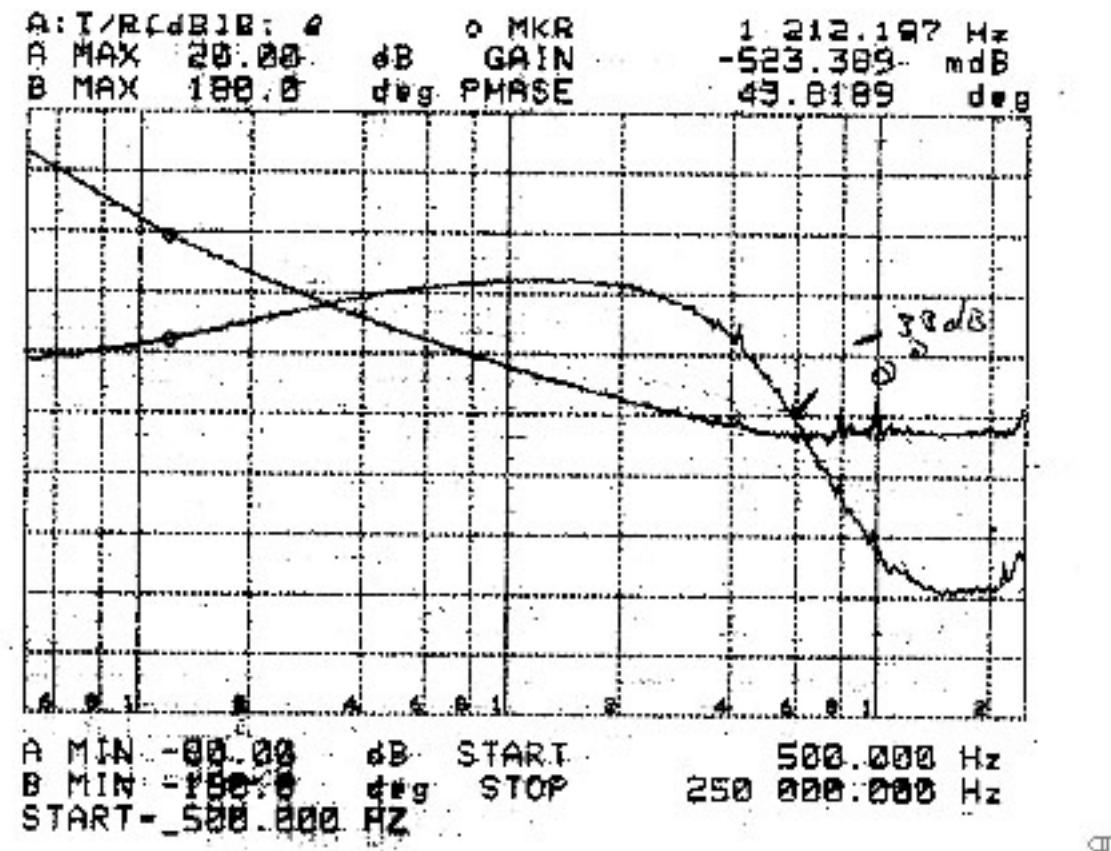
An audible chirping was heard when the two converters were up and running and the power op-amp was modulating the input voltage. In order to locate the chirping to the filter or one of the pair of converters the sweep was changed to a manual sweep rate and was set to the point where the noise was loudest. After roughly 10 seconds a bang was heard coming from the test set up. The first converter was still up and running, but the second converter had its output showing about 1 volt, and the top of this converter was very warm. During this time, nothing of note was seen on the oscilloscope. (See figure 1 for oscilloscope probe positions.) Voltages and currents appeared as before. The DPA revealed that an output capacitor had failed and had turned black from the heat.

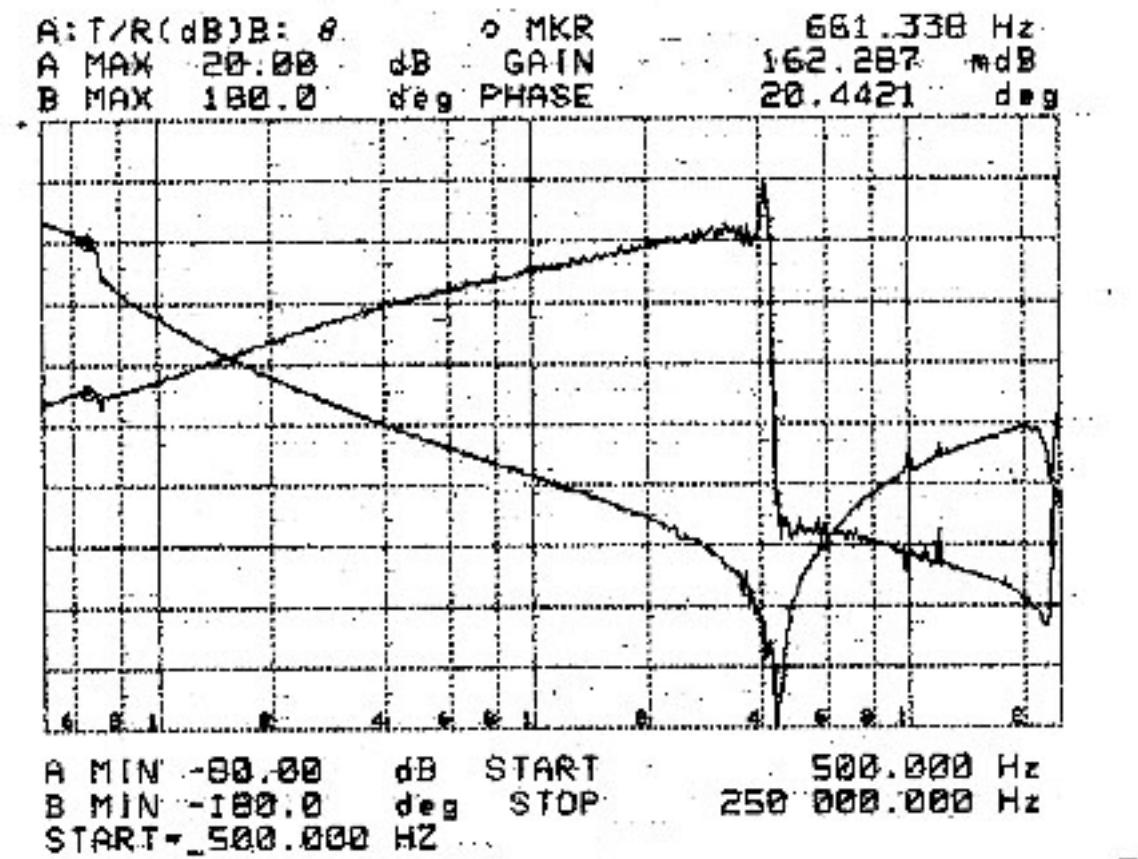
The feedback loop was checked with the one converter. The crossover point as expected changes as the load changes (see table 2). Appendix A is a brief discussion on the practices used in determining when a converter is stable.

**Table 2 Feedback Loop Stability as a Function of Load.**

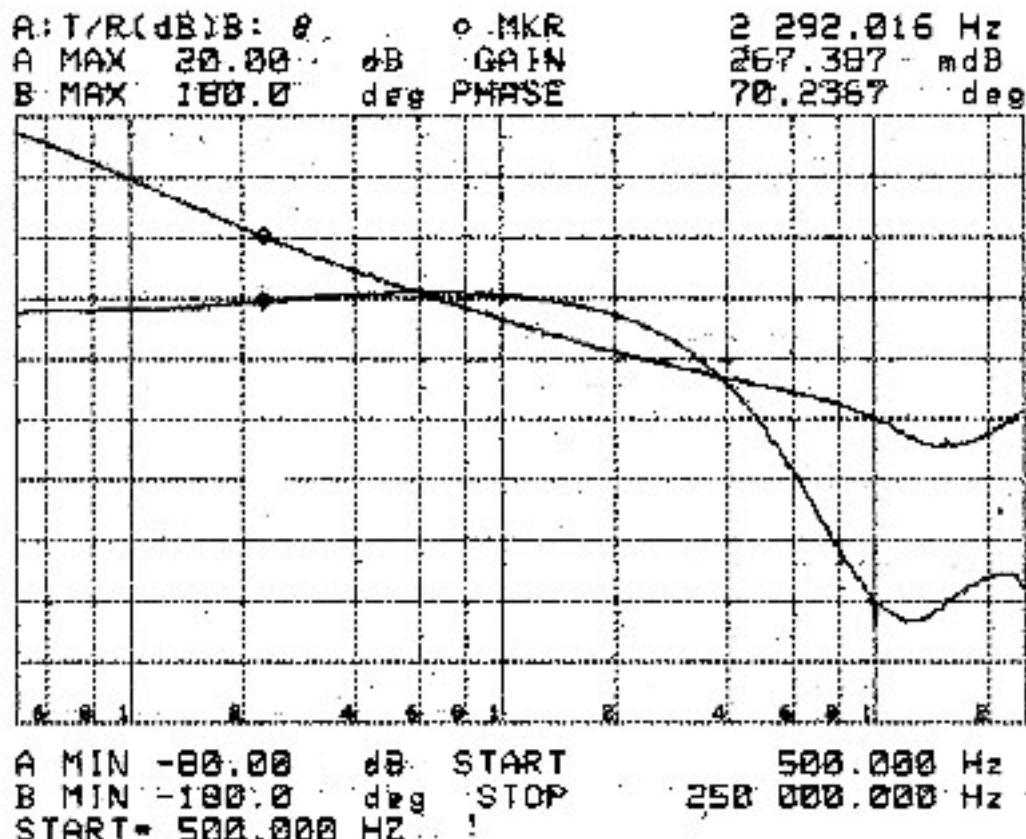
Load	Frequency at Crossover	Phase Margin	Output Power	Percent of Max Power (65W)
0.1A*	1.2kHz	43°	1.2W	1.8%
0.28A*	661Hz	20°	3.4W	5.2%
0.3A*	682Hz	27°	3.6W	5.5%
0.35A	1.4kHz	55°	4.2W	6.5%
1A	2.2kHz	70°	12W	18.5W
4A	6.7kHz	73°	48W	73.8W

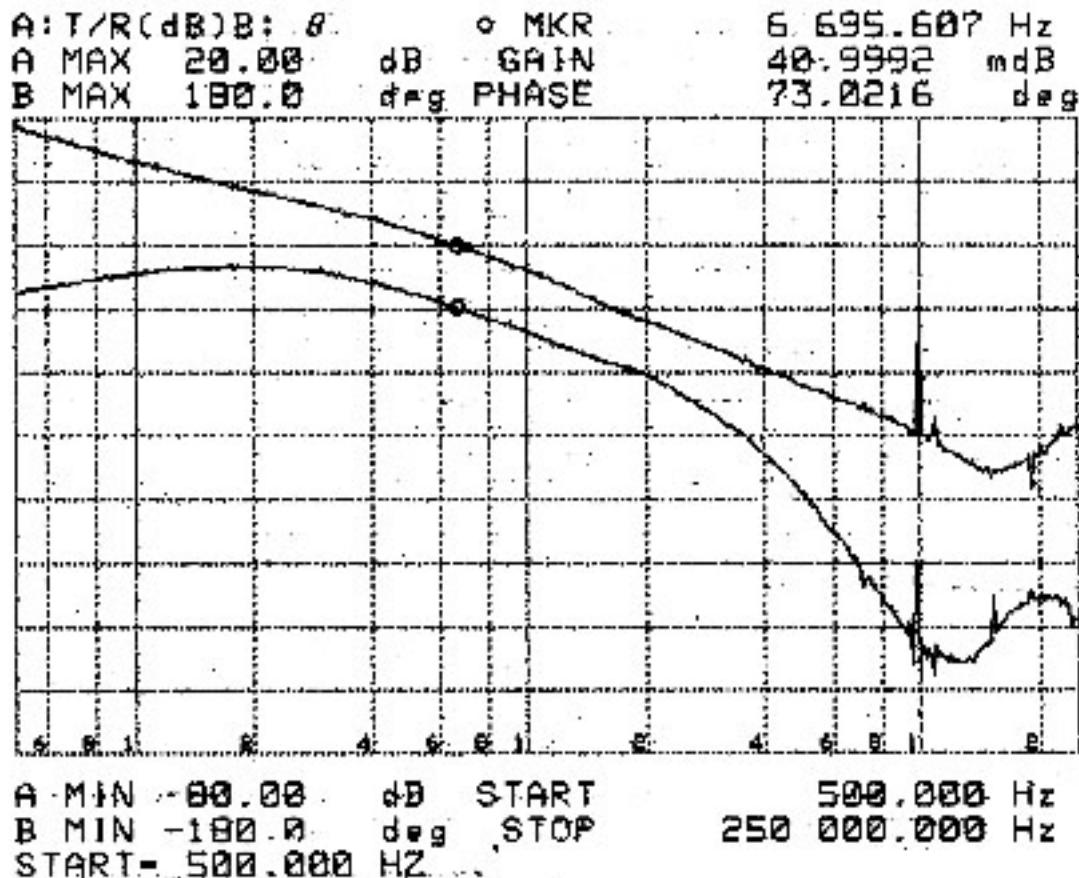
\* Does not meet Stability Margin Practice

**Figure 2:** Feedback Loop Bode Plot at 0.1a load (1.2w)<sup>¶</sup>

**Figure 3:** Feedback Loop Bode Plot at 0.28a (3.4w)<sup>¶</sup>

¶

**Figure 4:** Feedback Loop at 1a (12w)<sup>¶</sup>

**Figure 5:** Feedback Loop at 4a (48w)<sup>¶</sup>

The final data set taken was to look again at the transfer function, but instead of changing the number of converters, the external capacitance were added. There are 3 sets of capacitors being added, all between the EMI filter and the converter. The first set was two 1500pF capacitors, one to the return to chassis, and the second from the power line to chassis. The second set was two 0.01uF capacitors at the same locations. The third capacitor was 33uF and it was placed between the power and return lines. The gains at the first resonance point are given in table 3 below. The resonant frequency did not change as the capacitors were added.

**Table 3 Effect of External Capacitors Between Filter and Converter**

Capacitors in Use	Gain (dB) at First Resonance	Gain (dB) @ Secondary Resonance
No Cap	10dB	5dB
1500pF Cap	-29dB	-35dB
0.010uF Cap	11dB	23dB
33uF Cap	4.7dB	14dB

As capacitors were added, the higher frequency resonances became dominant, and the response amplitude exceeded the primary resonance. It was also noted that the response amplitude at resonance changed as a function of temperature. It was seen that the gain increased as the 33uF capacitor was heated. An estimated temperature change of 10 °C resulted in a 6 dB gain of the system.

**Figure 6 No Capacitor Between Filter and Converter**

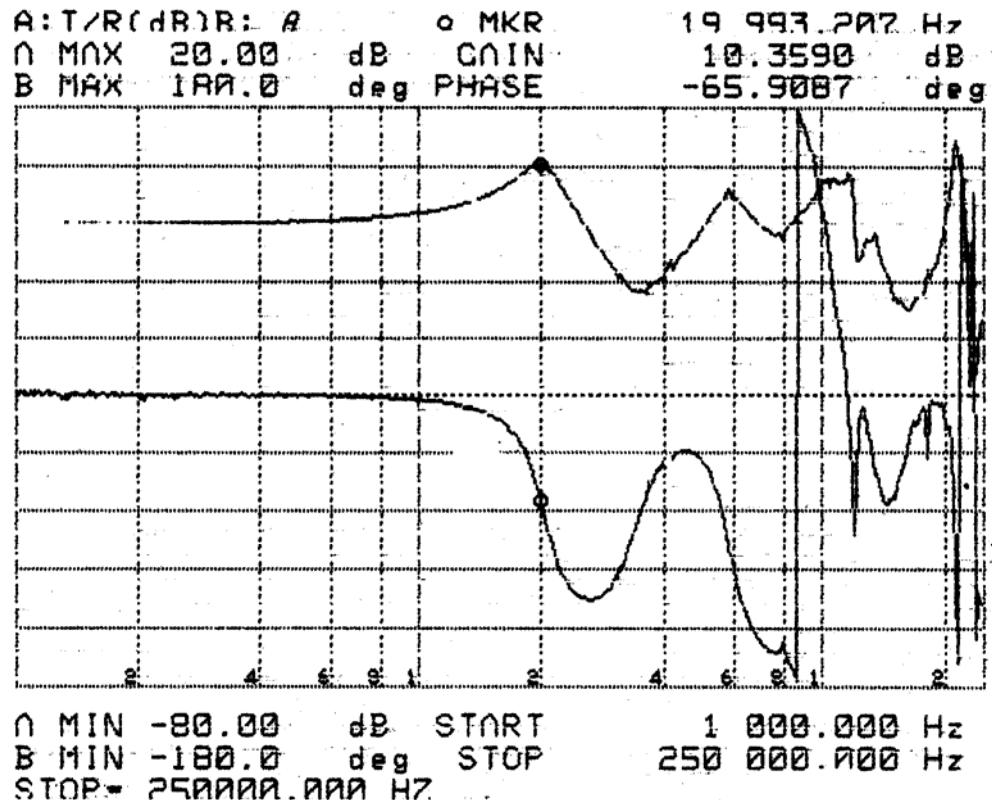
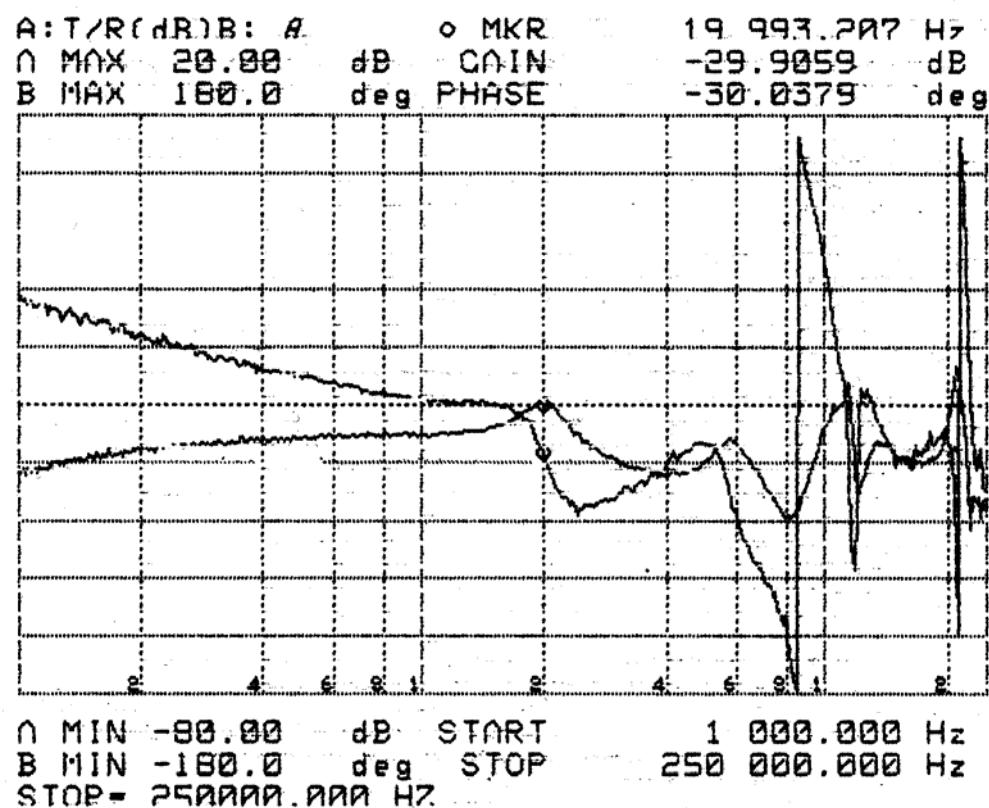
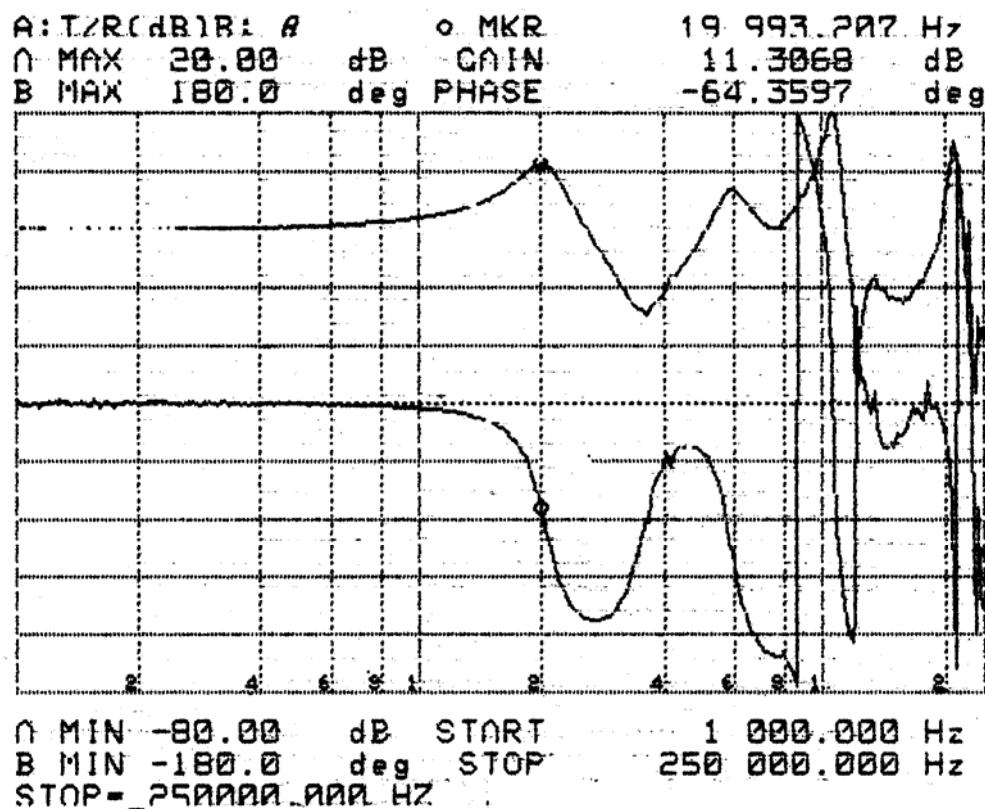


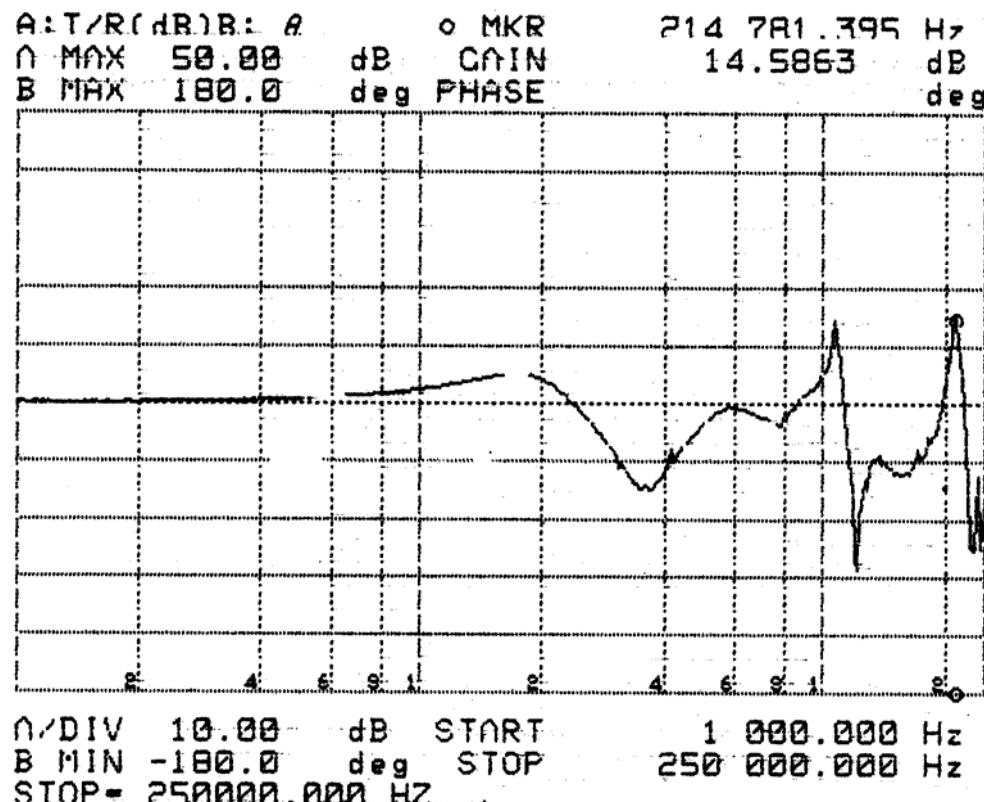
Figure 7 Set of 1500pf Capacitors Between Filter and Converter



**Figure 8 1500pf Capacitor and 0.01uf Capacitor Between Filter and Converter**



**Figure 9 1500pf Capacitor, 0.01uf Capacitor, and 33uf Capacitor Between Filter and Converter**



### Converter Efficiency

Table 4 shows the efficiency of the converter when it is under light loads, and the amount of power in the converter when it is under no load.

**Table 4 Low Loading Efficiency and Internal Power Consumption**

Output Current	Input Power	Output Power	Efficiency	Internal Power
0 A	1.44 W	0.00 W	0.00%	1.44 W
0.102 A	3.33 W	1.23 W	36.97%	2.10 W
0.152 A	4.07 W	1.83 W	45.08%	2.23 W
0.202 A	4.64 W	2.44 W	52.48%	2.21 W
0.252 A	5.12 W	3.04 W	59.34%	2.08 W
0.302 A	5.86 W	3.64 W	62.16%	2.22 W
0.352 A	6.65 W	4.24 W	63.79%	2.41 W

### Conclusions From Testing

The testing has revealed that the converters when lightly loaded are either unstable or at the edge of being unstable (Actually oscillating or only failing). Adding more than one DC to DC

converters to the output of the EMI filter lowers the frequency at which the EMI filters resonance occurs, but at the low loading the filter rolls off at a frequency much higher than the bandwidth of the feedback loop. The filter should roll off before the feedback loop does and as a result there is a potential for oscillation. The capacitors added to the filter design have not been damped other than through their Effective Series Resistance (ESR), and have added new resonance points. The data also shows that if one capacitor was lost, a higher Q can be formed which could lead to secondary failures, it was also noted that the temperature of the capacitors effect the amplitude of the resonances, and is not unexpected are the temperature of the capacitors will effect the ESR of the capacitors.

## **Appendix A**

Due to the inherent non-linearity of a switching converter the accepted practice is to have 54 degrees of phase margin when the Bode plots have the gain of the feedback loop is at 0dB. The margin is set to allow for effects such as aging, thermal, transient loading and others. As can be seen in table 2 the crossover point is also non-linear when it is a function of load. At lower loads the output inductor is in its discontinuous mode of operation. With the converter being used the convert becomes stable when there is a 0.35 A load. This translates to 4.2 W on a single converter. Using 4 converters of the same type would require at least 16.8 W to have all converters stable. At the time of the ACS failure the converters with the maximum load on them was 10 watts, not 16.8 watts.

## **Equipment List**

Converter #1 Interpoint MFL2812S 6962-9316201HXC SN 0205 DC 9848

EMI Filter Interpoint FME28-461 9500401HXC SN 1301 DC 9812

Impedance Analyzer HP 4194A ECN 2035377

Power Op-Amp Venable ECN G43151

Oscilloscope Agilent 54832B ECN 3039482

Electronic Load Bank Agilent N3300A M151579

Capacitor 2000mfd Mallory

## **Appendix 3: ACS VSTIF Bench LVPS resonance testing (Conducted Susceptibility Testing) Test Plan**



**ACS Side-2 ARB/ HST Code 442**  
**VSTIF ACS Bench Test Plan**  
**Version: 4/30/07**

**Description:**

Additional ground testing as it relates to the ACS Side-2 on-orbit anomaly is required. The ACS Side-2 ARB and HST Code 442 would like to better characterize the ACS LVPS power system's hardware design sensitivity/potential for resonance. The VSTIF ACS test bench is the closest hardware facsimile to the ACS hardware in orbit that HST has in its possession. A similar ACS test bench exists in ESTIF, but does not possess the fidelity of the VSTIF hardware. Therefore, all testing will be conducted on the VSTIF ACS test bench.

**Initial Configuration:**

Due to the large number of hardware configuration permutations possible, the ARB/Code 442 has decided to limit the scope of this testing. On-orbit ACS Bus C Testing has confirmed that the ACS Side-2 shorting anomaly is physically located on the ACS Side-2 HOLD bus.

Therefore, this test will concentrate on converters that are located on the HOLD bus only. If this present VSTIF test identifies any issues or concerns that may indicate that additional testing is required on the ACS Operate Bus, then ACS Operate side testing will be considered at that time and hardware configuration changes to accommodate that level of testing will be accommodated at that time.

The VSTIF ACS test bench will be configured during testing to provide investigators with enough variability to effectively characterize the system's hardware design sensitivity/potential for resonance. Thus, the following 'variables' will be set/adjusted as follows:

1. Bus Voltage: The ACS Test Bench Sorenson Supply will be initially set to 26.5V; this matches the ACS internal voltage measured just prior to the ACS on-orbit anomaly. Testing will also be conducted at max and min bus voltages, 32V and 24V respectively.
  - Nominal Bus V = 26.5V
  - High Bus V = 32V
  - Low Bus V = 24V
2. Loads: VSTIF ACS Test Bench secondary loads will be set using variable power loads, where possible, to closely match loading conditions experienced just prior to the on-orbit anomaly. Loading will be verified by measuring the delta current draw of the instrument when a secondary is switched on/off. Note that this 'load' value, in watts, will therefore include the inefficiencies of the converter. Loads will be adjusted higher and lower, where possible, to characterize the effect on the system's hardware design.

Thermal Control Loads: Based on on-orbit experience, Thermal Control Loads have the following max/min behavior per +15V converter:

Typical = 10W

Min = 5W

Max = 25W

TECs: Based on on-orbit experience, the HRC and WFC TECS have the following max/min secondary current draw behavior per converter:

Typical = 2.3 to 2.4 Amps (-76.5C setpoint)

Min = 1 Amp (-66.7C setpoint)

Max = 4.2 Amps (-90.0C setpoint)

Note: The Shield TEC is configured as a fixed current driven load. When enabled, the Shield TEC converter will source 3.5A. There is no Shield TEC setpoint control. Therefore, testing will the Shield TEC will be fixed at the designed 3.5A current load.

Bus	Board	EMI Filter	Converter(s)	Orbital Load (W)	Present VSTIF Load (W)	Proposed VSTIF Load (W)	Comment	Test Group	
HOLD	LVPS1	FL1	Hold	20	14	--	Add Current Monitor Loop on FL1	1	
			WFC Shield TEC (on LVPS2)	(10W in TEC)	3.5A fixed (1.5 Ohm)	--	Fixed Constant Current		
			Thermal Control Conv A (on LVPS2)	<10 (at heaters )	1.4	Add variable load	No heater loads in VSTIF		
			Thermal Control Conv B (on LVPS2)	<10 (at heaters )	1.4	Add variable load	No heater loads in VSTIF		
	LVPS3	FL1	CEB +5	50	<b>TBD</b>	--		2	
			CEB +/-15						
		FL2	HRC TEC	(6W in TEC)	Variab le (1.5 Ohm)	--	Cmd TEC Setpoint	3	
			WFC TEC	(10W in TEC)	Variab le (1.5 Ohm)	--	Cmd TEC Setpoint		
	APB			OFF	--	--	No APB in ACS test rack	--	
OPERATE	LVPS1	FL2	Operate +5	60	<b>TBD</b>	--		--	
			Operate +/- 15						
			Cal Lamp - 5V	5	2.8	--	Power split unknown		
	LVPS2	FL1	Cal Lamp +30V				--		
			Mech +5V	15	14.1	--		Power split unknown.	
			Mech +15V						
			Mech +15V						



### **VSTIF Hardware Pre-Test Modifications:**

In order to perform this test, modifications to the existing VSTIF ACS LVPS boards are required. This includes adding tacked on jumper wires to identified points and adding external variable loads where possible.

All jumper wires defined below will use 20 AWG wire.

#### **TEST GROUP 1:**

LVPS1:

Remove LVPS1

Desolder wire from FL1-10 and isolate wire with kapton tape

Desolder wire from FL1-11 and isolate wire with kapton tape

Add jumper wire extension (for current loop; extend above top of bd) at FL1-12

Add 2' jumper wire to FL1-11 (HOLD Filter)

Add 2' jumper wire to U1-7 (+15V HOLD output)

Replace LVPS1

LVPS2:

Remove LVPS2

Add 2' jumper wire to U1-7 (+15V Therm A output)

Add 2' jumper wire to U1-8 (Thermal RTN A & B)

Add 2' jumper wire to U7-7 (+15V Therm B output)

Add 2' jumper wire to U9-7 (Shield TEC output)

Replace LVPS2

#### **TEST GROUP 2:**

LVPS3:

Remove LVPS3

Add 2' jumper wire to FL1-12 (CEB Filter)

Add 2' jumper wire to U1-7 (+5V CEB output)

Add 2' jumper wire to U2-7 (+15V CEB output)

#### **TEST GROUP 3:**

(still on LVPS3)

Add 2' jumper wire to FL2-12 (TEC Filter)

Add 2' jumper wire to U6-7 (HRC TEC output)

Add 2' jumper wire to U14-7 (WFC TEC output)

Replace LVPS3

Connect all jumper wires to terminal blocks associated with each test group. Add labels as appropriate.

Set and verify all Variable Load Banks are initially configured for 25 Ohms.

### **TEST GROUP 1:**

Connect variable load bank resistor across terminal block, Shield TEC Load

Connect variable load bank resistor across terminal block, LVPS2 U1-7 (+15V Therm A output) to U1-8 (Thermal RTN A & B)

Connect variable load bank resistor across terminal block, LVPS2 U7-7 (+15V Therm B output) to U1-8 (Thermal RTN A & B)

### **TEST GROUP 2:**

n/a

### **TEST GROUP 3:**

n/a

#### **Test Equipment List:**

Impedance Analyzer HP 4194A ECN 2035377

Power Op-Amp Venable ECN G43151

Capacitor 2000mfd, 450V rated Mallory

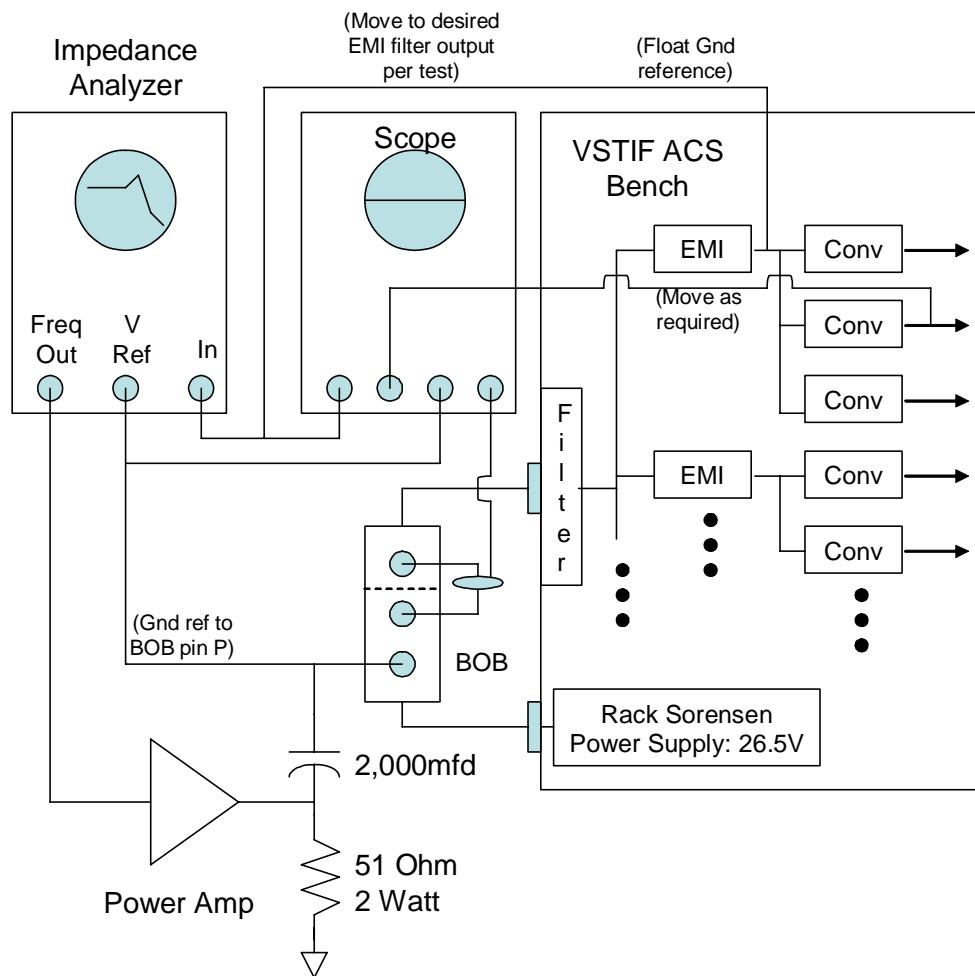
Resistor 51 Ohm, 2 Watt

Break out Box

Scope: 4 Channel

1 Current Probe

2 Power Decade Boxes or equivalent variable power potentiometers



## Test Configuration

BOB: +V power is on pins R, T, V, X  
Primary Return is on pins P, S, U W

## **Test Sequence:**

Impedance Analyzer:

Set nominal sweep frequency range = 1KHz to 1 MHz (excursions down to 100Hz shall be allowed as warranted by the Test Team)

Amplifier:

Dial down to 0V

Power down ACS VSTIF Bench

Test EMI Filters Bank by Bank (in Test Groups 1, 2, and 3) as identified below. Dial down Amplifier injected voltage to 0V prior to changing test configurations. Once a configuration is established, raise the Amplifier injection voltage up until a 100mV maximum peak to peak amplitude is measured via the scope. Store sweep response Frequency and Amplitude data obtained with the Impedance Analyzer:

### TEST GROUP 1:

1. HOLD Converter
  - a. HOLD Converter only
    1. Sweep at nominal bus V
    2. Sweep at high bus V
    3. Sweep at low bus V
  - b. HOLD Converter with Thermal Controller A On
    1. Sweep at nominal bus V
      1. thermal A load 25 ohms (0.6 Amps; 9 Watts)
      2. thermal A load 10 ohms (1.5 Amps; 22.5 Watts)
      3. thermal A load 50 ohms (0.3 Amps; 4.5 Watts)
    2. Sweep at high bus V
      1. thermal A load 25 ohms
      2. thermal A load 10 ohms
      3. thermal A load 50 ohms
    3. Sweep at low bus V
      1. thermal A load 25 ohms
      2. thermal A load 10 ohms
      3. thermal A load 50 ohms
  - c. HOLD Converter with Thermal Controller B On
    1. Sweep at nominal bus V
      1. thermal B load 25 ohms
      2. thermal B load 10 ohms
      3. thermal B load 50 ohms
    2. Sweep at high bus V
      1. thermal B load 25 ohms
      2. thermal B load 10 ohms

- 3. thermal B load 50 ohms
- 3. Sweep at low bus V
  - 1. thermal B load 25 ohms
  - 2. thermal B load 10 ohms
  - 3. thermal B load 50 ohms
- d. HOLD Converter with Shield TEC On
  - 1. Sweep at nominal bus V
  - 2. Sweep at high bus V
  - 3. Sweep at low bus V
- e. HOLD Converter with Thermal Controller A and B On
  - 1. Use worst combination identified in sections a-c above
- f. HOLD Converter with Thermal Controllers A & B and Shield TEC On
  - 1. Use worst combination identified in sections a-d above

**TEST GROUP 2:**

- 2. CEB Converter
  - a. CEB Converters on
    - 1. Sweep at nominal bus V
    - 2. Sweep at high bus V
    - 3. Sweep at low bus V

**TEST GROUP 3:**

- 3. TEC Converters
  - a. HRC TEC Converter on only
    - 1. Sweep at nominal bus V
      - 1. HRC TEC 2.3 Amp load (-76.5C setpoint)
      - 2. HRC TEC 4.2 Amp load (-90.0C setpoint)
      - 3. HRC TEC 1.0 Amp load (-66.7C setpoint)
    - 2. Sweep at high bus V
      - 1. HRC TEC 2.3 Amp load (-76.5C setpoint)
      - 2. HRC TEC 4.2 Amp load (-90.0C setpoint)
      - 3. HRC TEC 1.0 Amp load (-66.7C setpoint)
    - 3. Sweep at low bus V
      - 1. HRC TEC 2.3 Amp load (-76.5C setpoint)
      - 2. HRC TEC 4.2 Amp load (-90.0C setpoint)
      - 3. HRC TEC 1.0 Amp load (-66.7C setpoint)
  - b. WFC TEC Converter on only
    - 1. Sweep at nominal bus V
      - 1. WFC TEC 2.3 Amp load (-76.5C setpoint)
      - 2. WFC TEC 4.2 Amp load (-90.0C setpoint)
      - 3. WFC TEC 1.0 Amp load (-66.7C setpoint)

2. Sweep at high bus V
    1. WFC TEC 2.3 Amp load (-76.5C setpoint)
    2. WFC TEC 4.2 Amp load (-90.0C setpoint)
    3. WFC TEC 1.0 Amp load (-66.7C setpoint)
  3. Sweep at low bus V
    1. WFC TEC 2.3 Amp load (-76.5C setpoint)
    2. WFC TEC 4.2 Amp load (-90.0C setpoint)
    3. WFC TEC 1.0 Amp load (-66.7C setpoint)
- c. HRC TEC and HRC TEC Converters on
1. Use worst combination identified in sections a-b above

Test EMI Filters with all HOLD converters on. Use worst combination of variables identified in subsequent testing.

Test EMI Filters with all HOLD and Operate converters on. Use worst combination of variables identified in subsequent testing.

## **Appendix 4: ACS VSTIF Bench LVPS resonance testing (Conducted Susceptibility Testing) results**



VSTIF

5/3/07 W

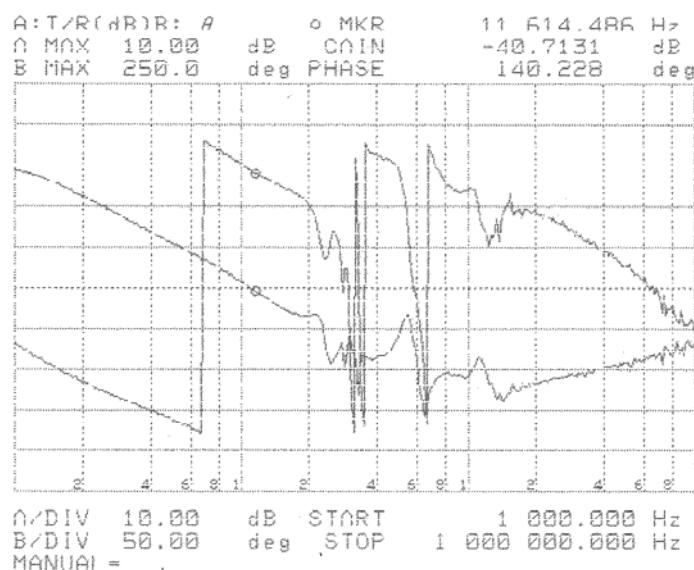
Vbus = 26.5 V

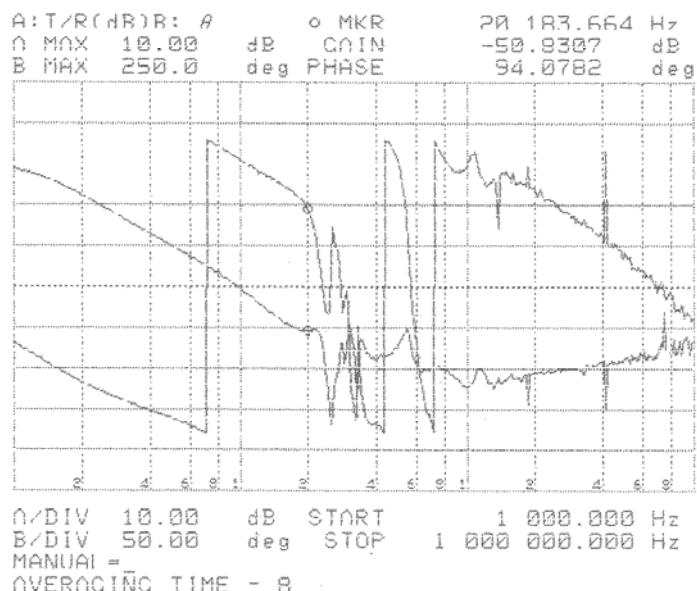
No diode - w/33μf cap

Pin = 8W

Hold Conv. only

Sec. 1. a: 1.



$V_{bus} = 32V$ VSTIF5/3/07 W  
Sec. 1.a.2.

$V_{bus} = 24V$

$P_{in} = 8W$

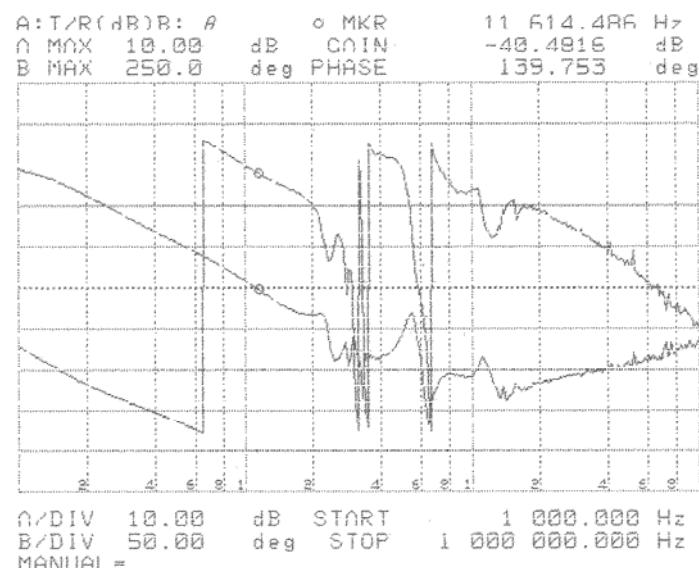
No Diode - w/ 33uf cap

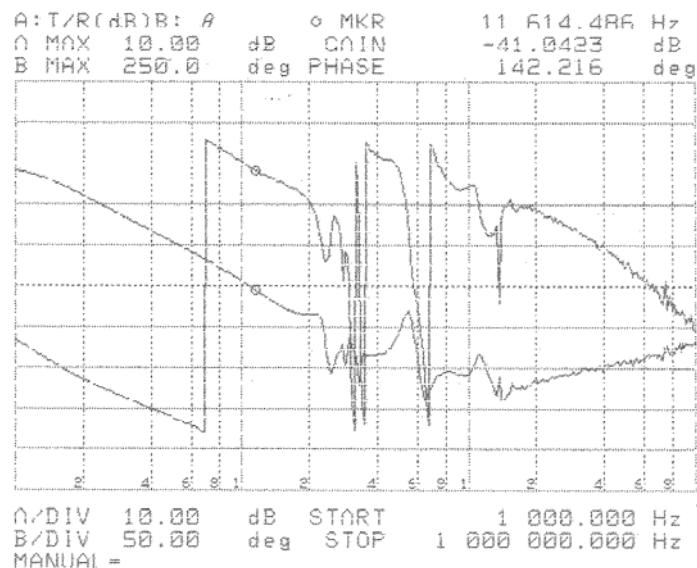
Hold Conv. only

VSTIF

5/3/07 H.

Sec. 1.a.3.



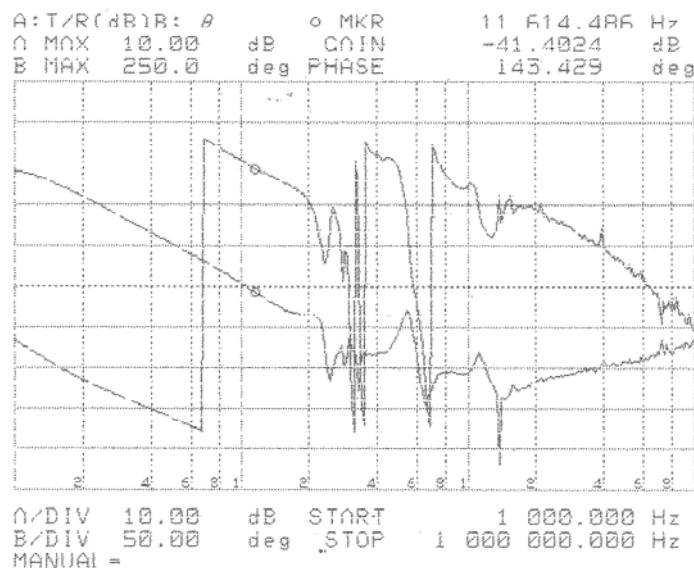
VSTIF5/3/07 *W*  
Sec. 1, b, 1.1

VSTIF

5/3/07 11P.

 $V_{bus} = 26.5V$ 

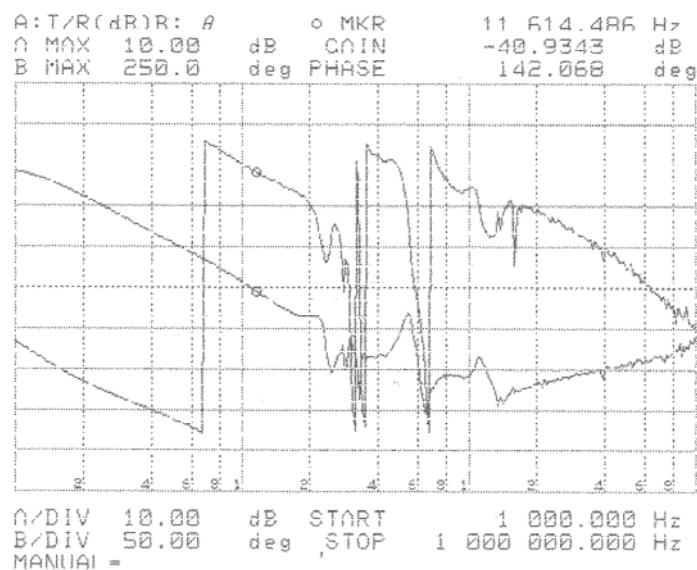
See. 1, b, 1, 2



VSTIF

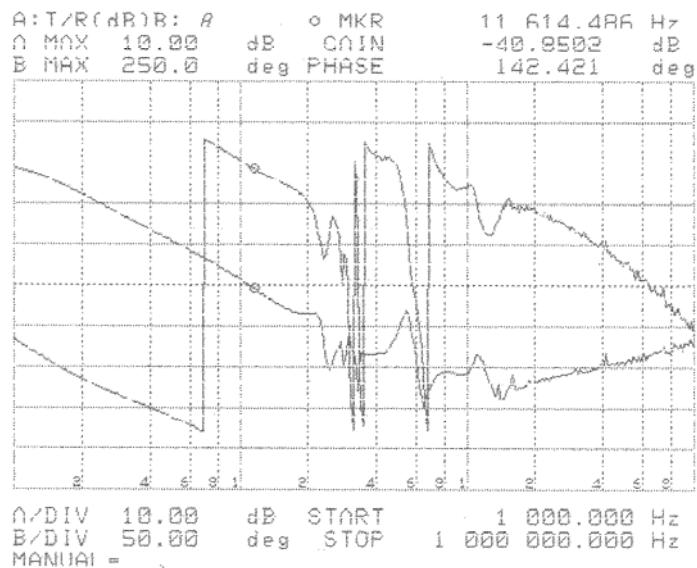
5/3/07 H.

### Sec 1.b.1.3.



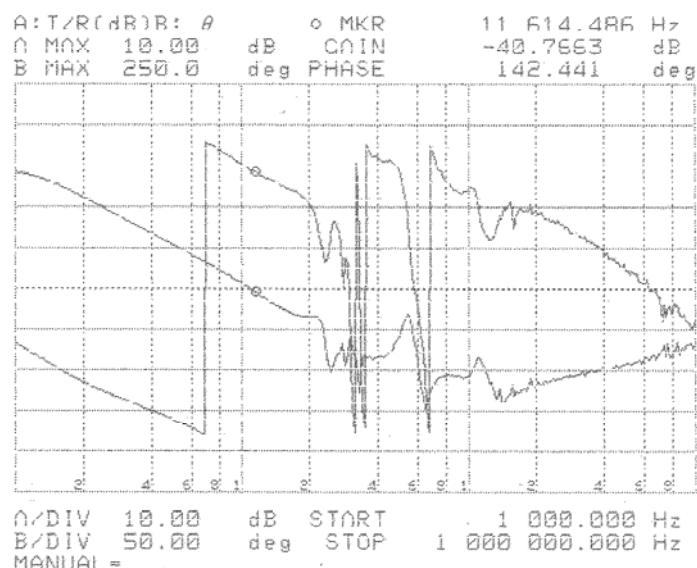
VSTIF

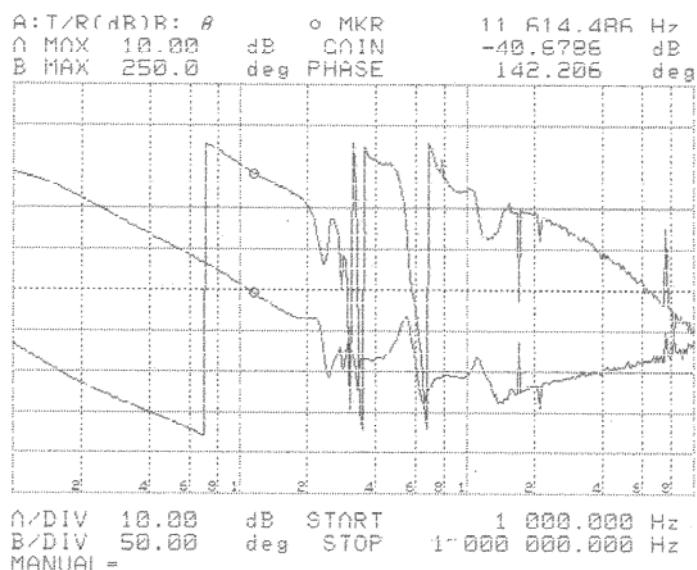
5/3/07 W.  
Sec 1.b.1. (60<sub>2</sub><sup>Load</sup>)  
(4.)

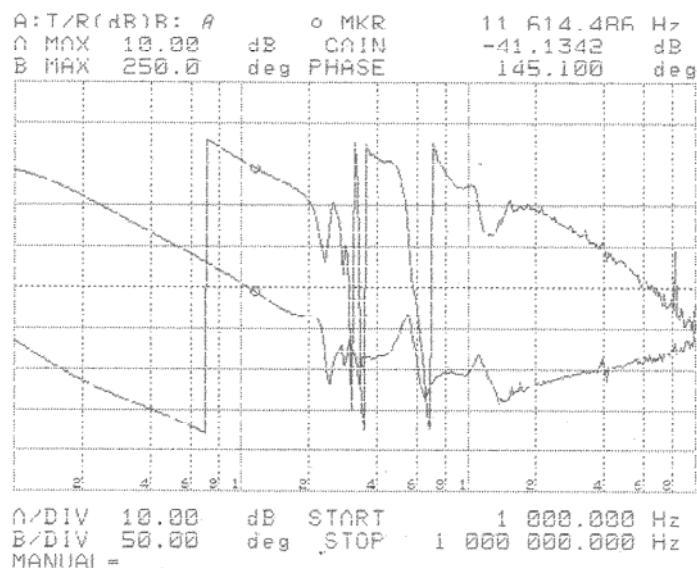


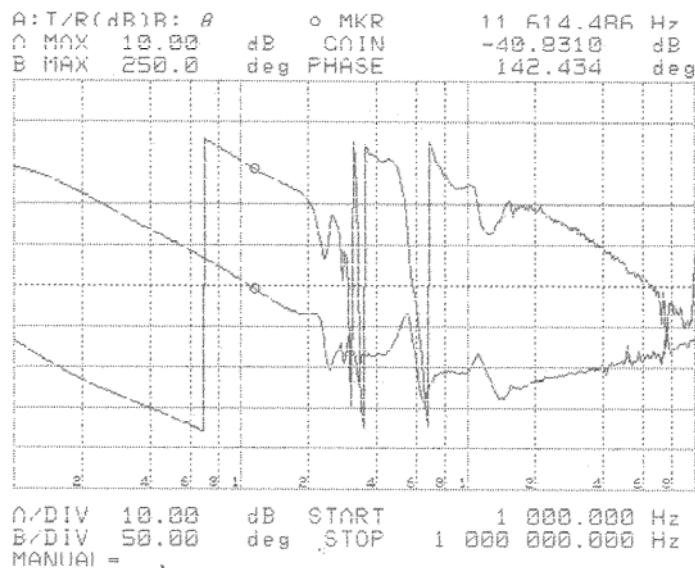
VSTIF

5/3/07 1P  
 Sec 1.b.1. 5  
 $\downarrow$   
 $75\Omega$



VSTIF5/3/07 MP  
Sec. 1b,2,1.

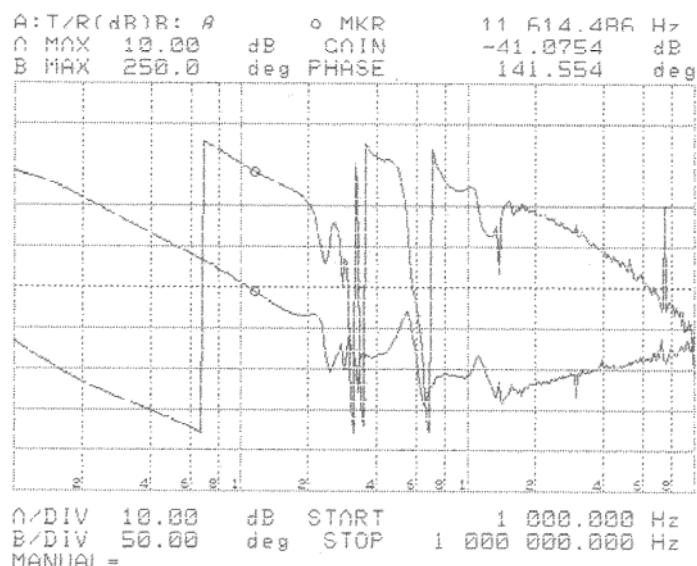
VSTIF5/3/07 *RP*  
Sec. 1.b.2.2.

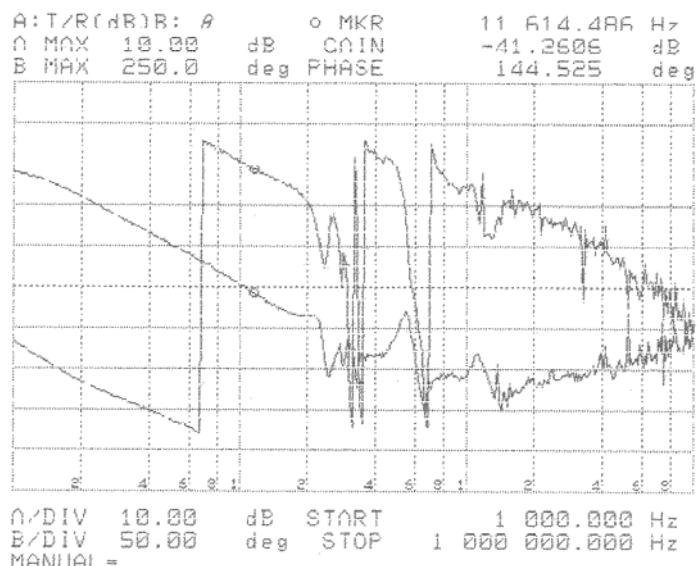
VSTIF5/3/07 HF  
Sec 1.b.2,3

VSTIF

5/3/07 H.

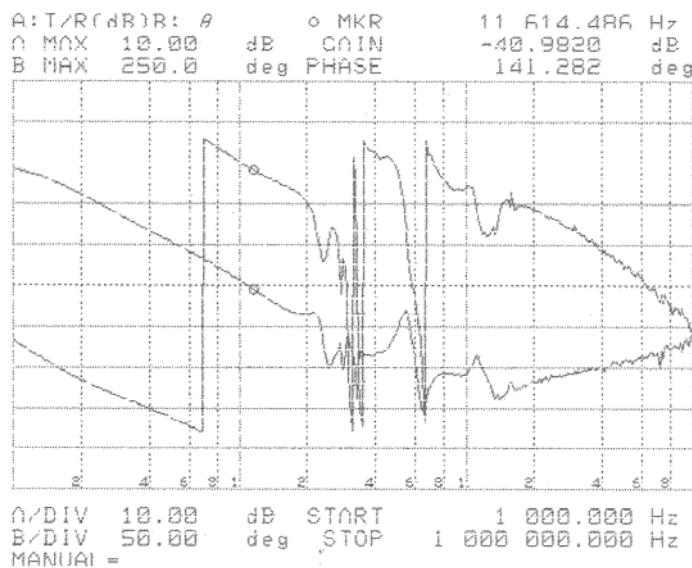
Sec. 1.b.3.1.

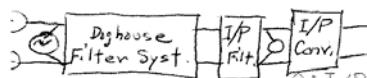


V STIF5/3/07 H.  
Sec. 1.b.3.2.

## VSTIF

5/3/07 HW  
Sec 1.b, 3.3c

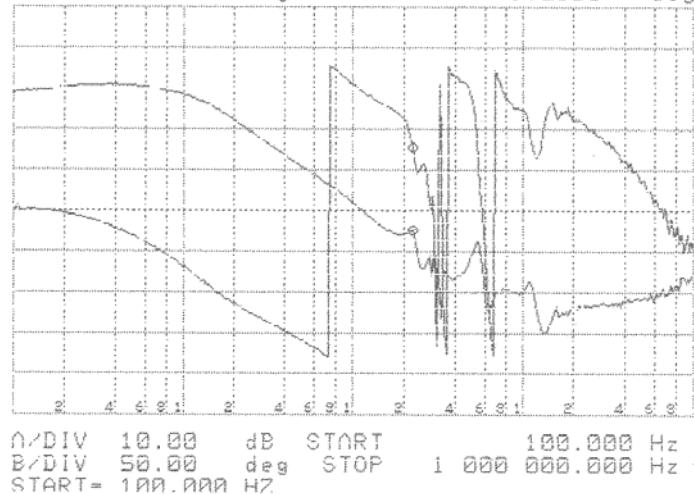


VSTIF5/4/07 11:  
①

A:T/R(FIRB)B: A      o MKR      22 387.211 Hz  
 A MAX 10.00 dB      GAIN -44.9870 dB  
 B MAX 250.0 deg      PHASE 78.2886 deg

Full system Filter Differential Mode  
 $V_{bus} = 26.5$

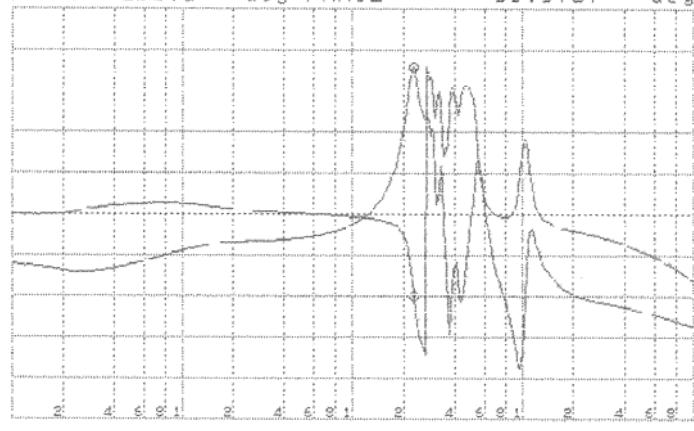
(A)



A:T/R(FIRB)B: A      o MKR      22 908.677 Hz  
 A MAX 25.00 dB      GAIN 17.9123 dB  
 B MAX 250.0 deg      PHASE -99.9767 deg

Ground Leg  
 $V_{bus} = 26.5V$

(B)

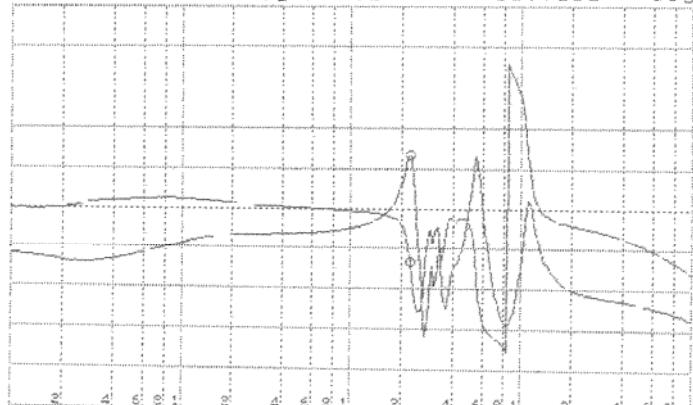


V311F

2/4/01 11:

(2)

A:T/R(fdB)B: A      o MKR      22 387.211 Hz  
 □ MAX 25.00 dB GAIN 6.66776 dB  
 B MAX 250.0 deg PHASE -66.7010 deg

Partial GND Leg

(C)

 $V_{bus} = 26.5V$ 

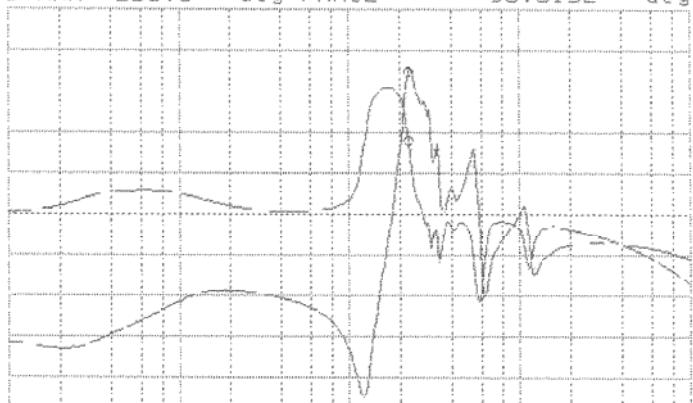
A/DIV 5.000 dB START 100.000 Hz  
 B/DIV 50.00 deg STOP 1 000 000.000 Hz  
 START= 100.000 Hz

A:T/R(fdB)B: A      o MKR      22 387.211 Hz  
 □ MAX 25.00 dB GAIN 17.4609 dB  
 B MAX 250.0 deg PHASE 90.3152 deg

A:T/R(fdB)B: A      o MKR      22 387.211 Hz  
 □ MAX 25.00 dB GAIN 17.4609 dB  
 B MAX 250.0 deg PHASE 90.3152 deg

Positive Leg

(D)

 $V_{bus} = 26.5V$ 

A/DIV 5.000 dB START 100.000 Hz  
 B/DIV 50.00 deg STOP 1 000 000.000 Hz  
 START= 100.000 Hz

V511F

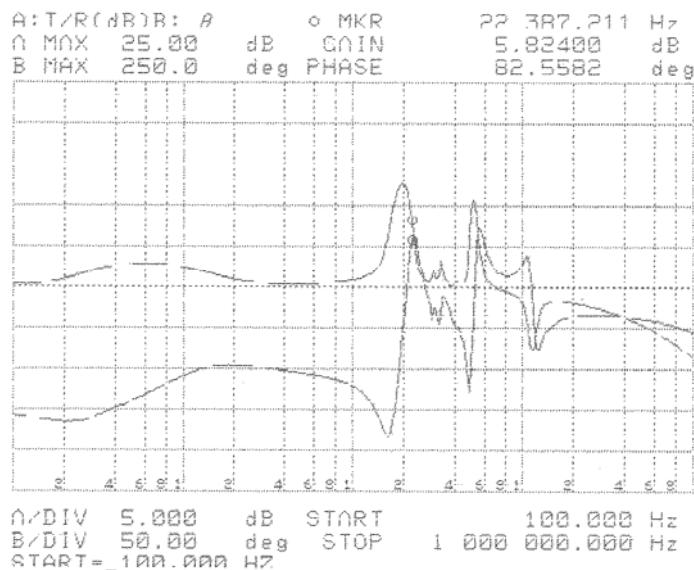
5/4/07 7-

(3)

Partial Pos. Leg

(E)

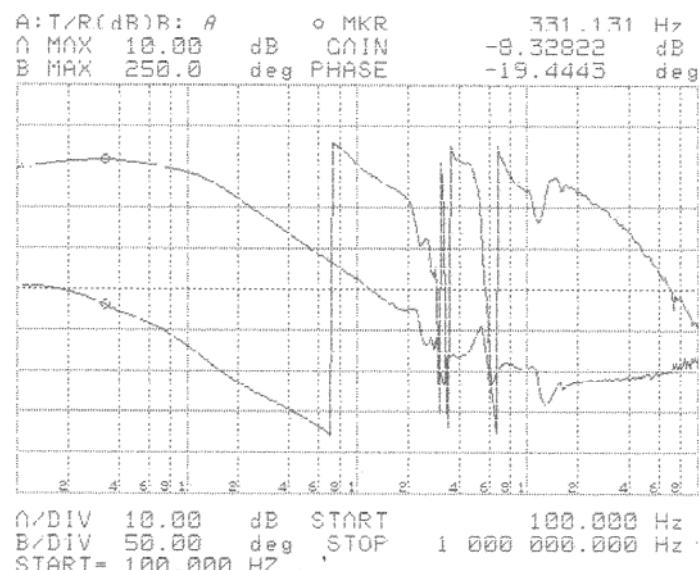
Vbus = 26.5V



Recheck @

Vbus = 26.5V

(A)



VSTIF

5/4/07

H.

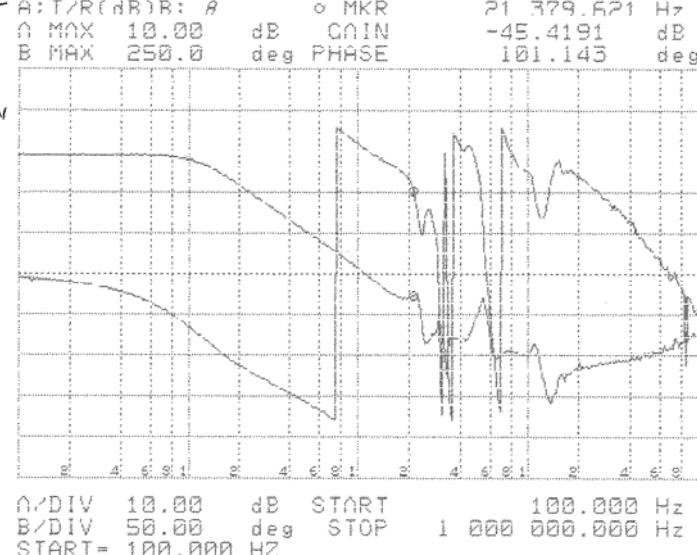
(4)

Differential Mode  
 (Next 4 plots)

Vbus = 26.5V

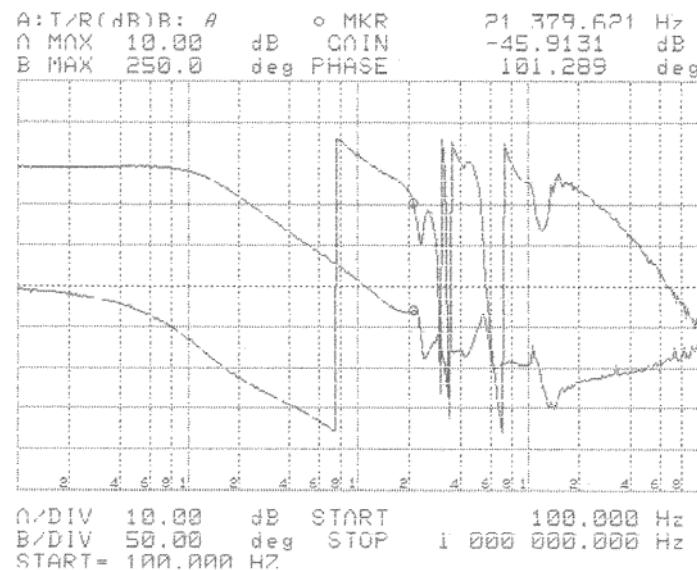
INIECTEC CONV. ON  
HOLD CONV. ON

Sec. 1. d.1



Vbus = 32V  
 INIECTEC CONV. ON  
 HOLD CONV. ON

Sec 1.d.2



VSTIF

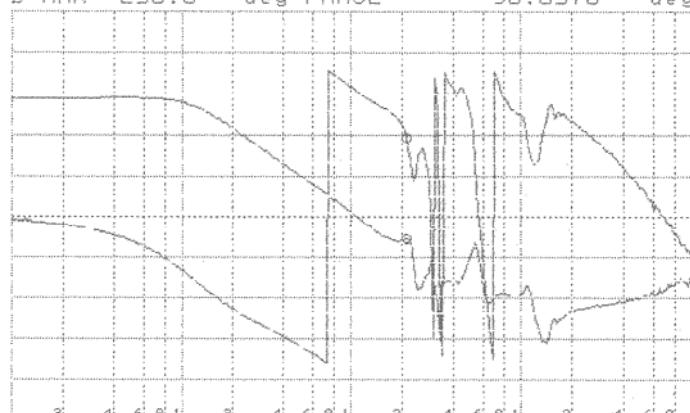
1/3

Vbus = 24 V.

SWING TEC CONV, ON  
HOLD CONV ON

Sec. 1.d.3

A:T/R(dB)R: A o MKR  
 A MAX 10.00 dB GAIN P1 379.621 Hz  
 B MAX 250.0 deg PHASE -45.4669 dB  
 96.8570 deg



A/DIV 10.00 dB START 100.000 Hz  
 B/DIV 50.00 deg STOP 1 000 000.000 Hz  
 START = 100.000 Hz

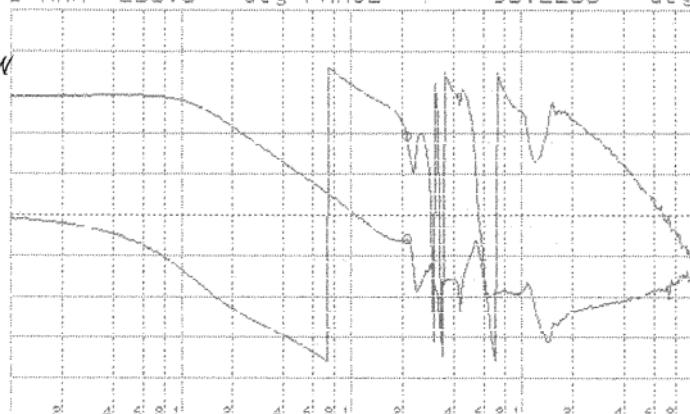
Vbus = 24 V

All 4 IEC CONV, ON

HOLD CONV  
 SWING TEC CONV  
 THER CONV A  
 THER CONV B

Sec. 1.f.1

A:T/R(dB)R: A o MKR  
 A MAX 10.00 dB GAIN P1 379.621 Hz  
 B MAX 250.0 deg PHASE -45.0098 dB  
 96.2206 deg



A/DIV 10.00 dB START 100.000 Hz  
 B/DIV 50.00 deg STOP 1 000 000.000 Hz  
 START = 100.000 Hz

VSTIF5/4/07 HR  
⑥

$V_{bus} = 26.5V$   
All 4 IEC's on

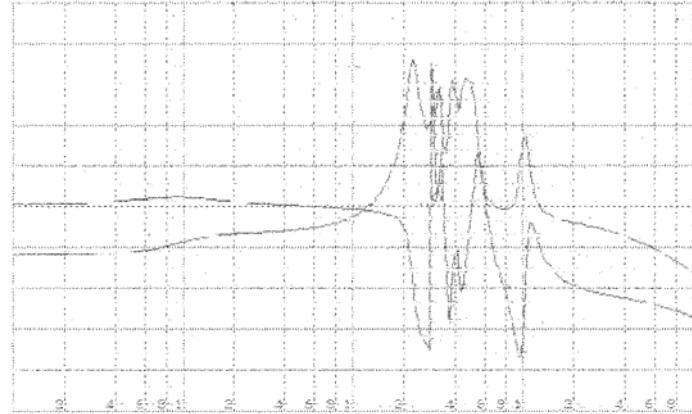
(B)

(RTN Leg)

See Gain vs. Freq.  
Tabulated  
Data sheet  
(6a)

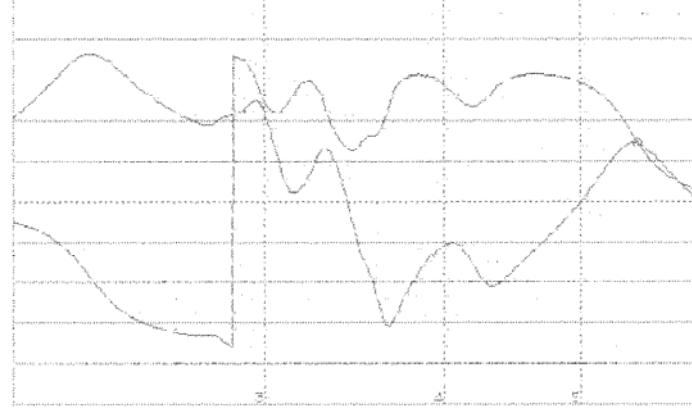
Sec. 1.F.1

A:T/R(dB)R: A o MKR 51 622.777 Hz  
 A MAX 25.00 dB GAIN 1.10216 dB  
 B MAX 250.0 deg PHASE 134.564 deg



A/DIV 5.000 dB START 100.000 Hz  
 B/DIV 50.00 deg STOP 1'000 000.000 Hz  
 START= 100.000 Hz

A:T/R(dB)R: A o MKR 54 801.033 Hz  
 A MAX 25.00 dB GAIN 7.19164 dB  
 B MAX 250.0 deg PHASE 72.8853 deg

Expanded Sweep  
of that above.

A/DIV 5.000 dB START 30 000.000 Hz  
 B/DIV 50.00 deg STOP 60 000.000 Hz  
 STOP= 60000.000 Hz

**Appendix 5: ACS VSTIF Bench LVPS resonance testing  
(Conducted Susceptibility Testing) results with and without  
added Bench connection between Chassis ground and  
Primary Return near the power supply source.**



5/9107 ①

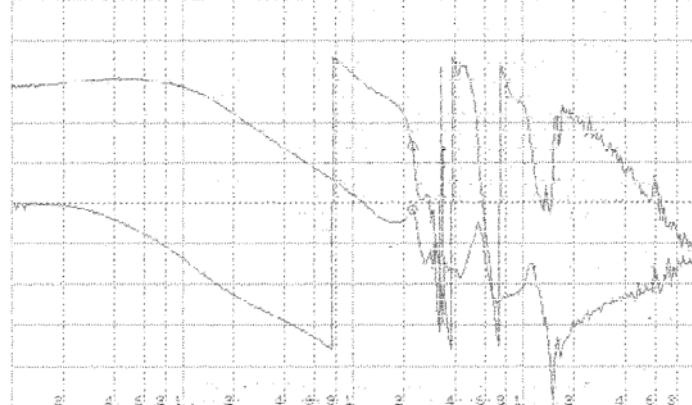
 $V_{bus} = 26.5V$ 

Holo conv. only

DIFF. MODE

BASELINE

A:T/R(fdB)R: A	o_MKR	22 387.211 Hz
A MAX 10.00	dB GAIN	-41.8072 dB
B MAX 250.0	deg PHASE	70.5090 deg

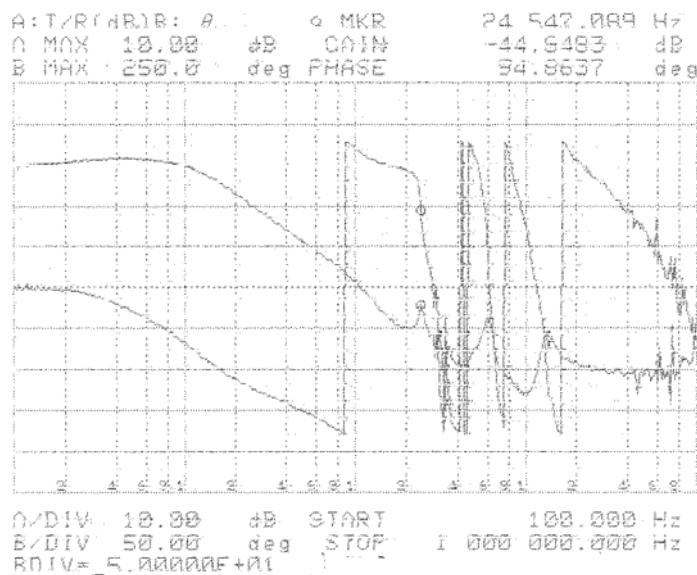


A/DIV 10.00 - dB START . 100.000 Hz  
 B/DIV 50.00 - deg STOP . 1000 000.000 Hz  
 RDIV= 5.00000E+01  
 AVERAGING TIME = 9

$V_{bus} = 26.5\text{V}$   
HOLD CONV. ONLY

57/9/07 ②

DIFF MODE  
ADDED JUMPER  
FROM PRIMARY  
RETURN TO CHAN#  
GROUND AT BOB.



5/5/07 (3)

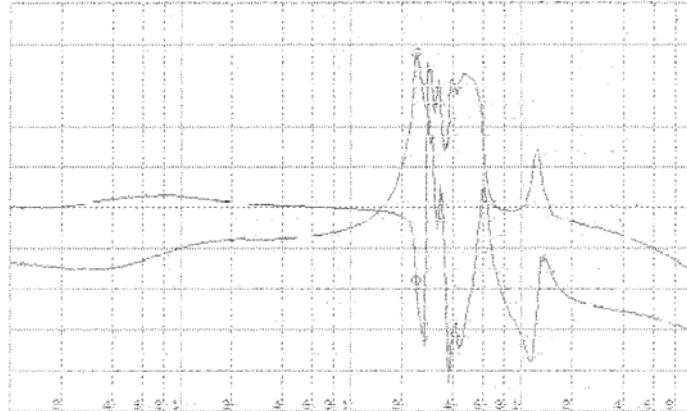
 $V_{bus} = 26.5V$ 

No load conn. only

~~4462~~  
GROUND LEG

WITH PRIMARY  
RETURN TO CHASSIS  
GROUND JUMPER

A:T/RdBR(B: A) MKR P4 547.000 Hz  
 A MAX 25.00 dB GAIN 19.0462 dB  
 B MAX 250.0 deg PHASE -89.1733 deg



A/DIV 5.000 dB START 100.000 Hz  
 B/DIV 50.00 deg STOP 1 000 000.000 Hz  
 ADIV= 5.00000E+00

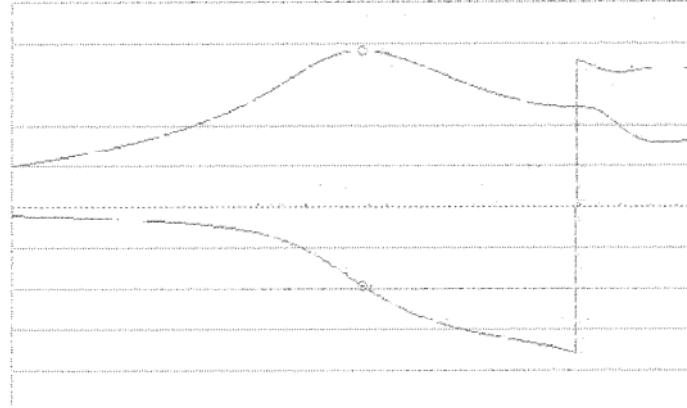
$V_{bus} = 26.5 V$   
HOLD conv. ONLY

5/9/07 ④

~~PARTIAL GND LEG~~  
(EXPANDED)

WITH PRIMARY  
RETURN TO CHASSIS  
GROUND JUMPER

A:T/R(HB)B: A      o MKR      24 644.329 Hz  
 A MAX 25.00 dB      GAIN 19.1520 dB  
 B MAX 250.0 deg PHASE -95.8960 deg



A/DIV 5.000 dB START 20 020.000 Hz  
 B/DIV 50.00 deg STOP 30 000.000 Hz  
 STOP=30000.000 Hz

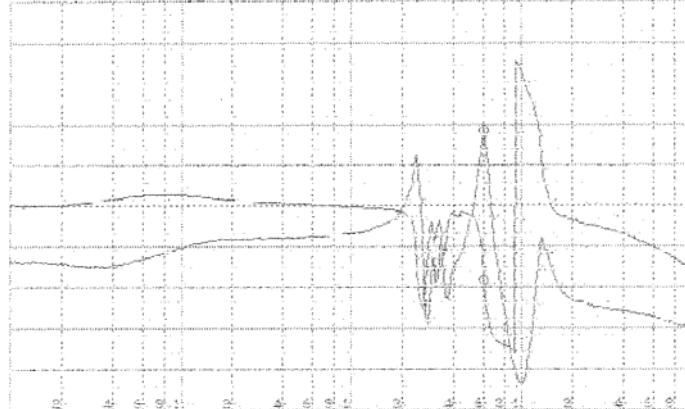
$V_{SW} = 26.5V$   
HALO CONV. ONLY

579/07 ⑤

PARTIAL AND LEG

WITH PRIMARY  
RETURN TO CHASSIS  
GND JUMPER

A: T/R(FB1B): A      o. MKR      f. 255.959 Hz  
 A MAX: 25.00 dB      GAIN: 9.26283 dB  
 B MAX: 250.0 deg PHASE: -31.6275 deg



A/DIV 5.000 dB START 100.000 Hz  
 B/DIV 50.00 deg STOP 1 000 000.000 Hz  
 STOP = 1000000.000 Hz

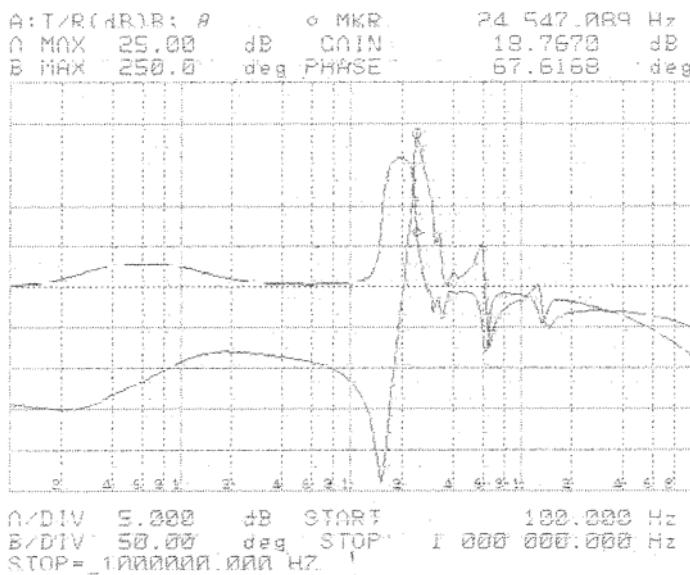
$$V_{300} = 26.5 \text{ V}$$

(No CO<sub>2</sub> convolution)

5/9/07 ⑥

### Positive Leg

WITH PRIMARY  
RETURN TO CHASSIS  
GROUND JUMPER

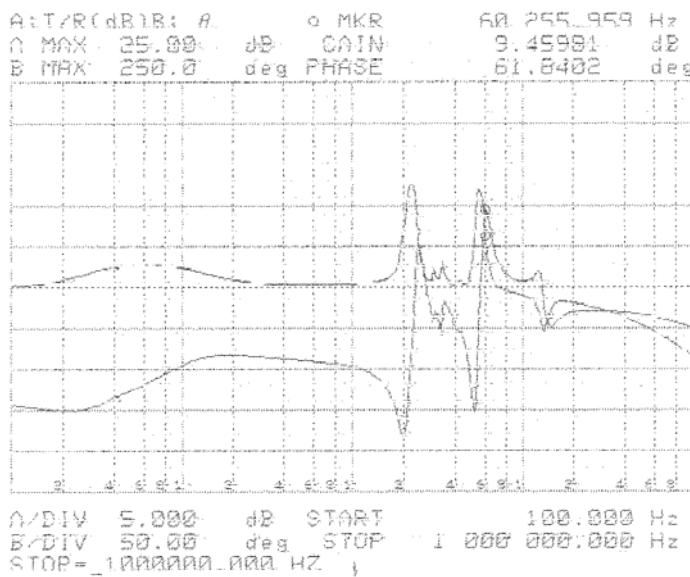


$V_{SUS} = 26.5V$   
HALO CAVV ONLY

5/9/07 ⑦

PARTIAL POS. L66

WITH PRIMARY  
RETURN TO CHANNEL  
GROUND JUMPER





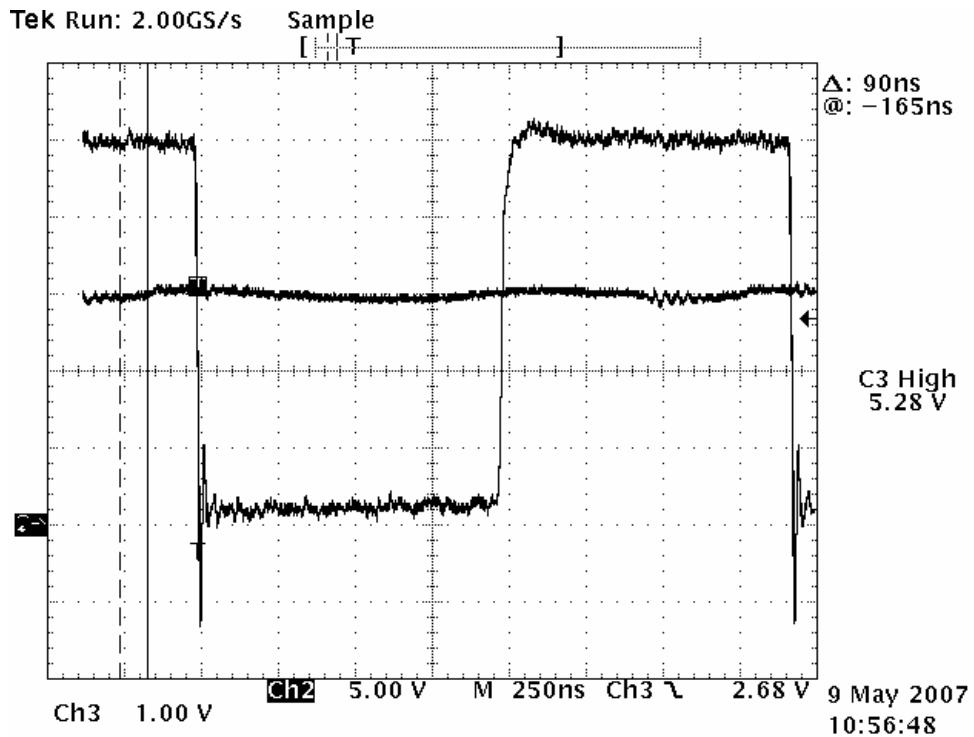
## Appendix 6: ACS VSTIF Bench Sync signal waveforms



Attached are Sync Signal waveforms collected on the VSTIF ACS Bench on 5/9/07.

Each waveform has been annotated to describe the test configuration at the time the waveform was taken.

All waveforms appear to be nominal; no concerns noted.

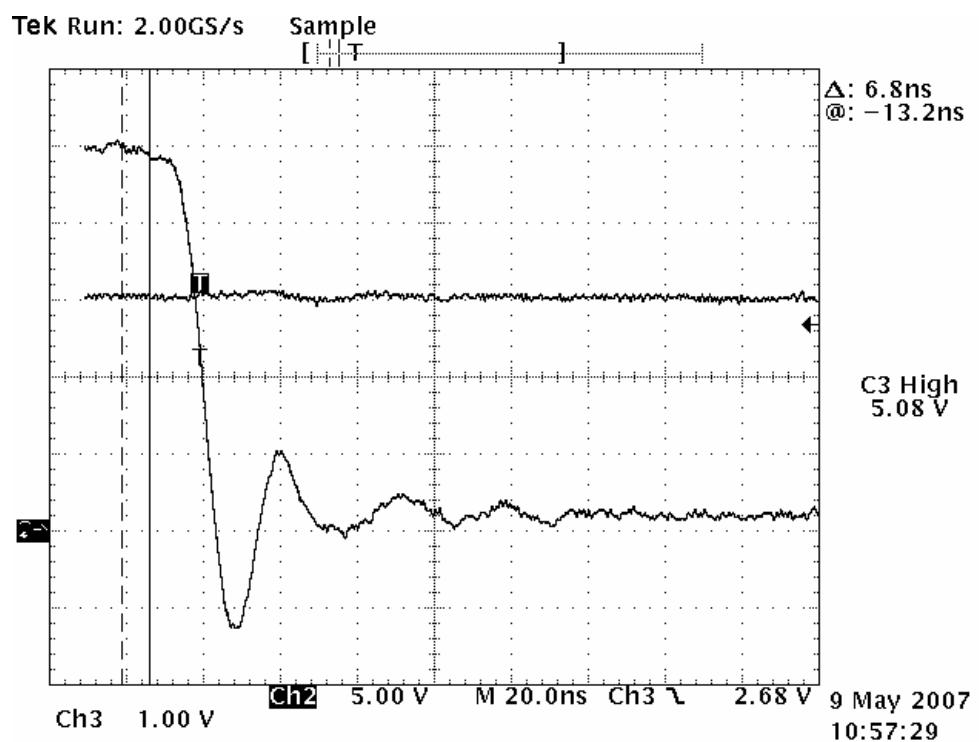


Scope waveforms taken with only the VSTIF ACS HOLD Converter enabled. Thus, the three remaining converters on the common Interpoint EMI filter (Shield TEC, Thermal Conv A, and Thermal Conv B) were Inhibited.

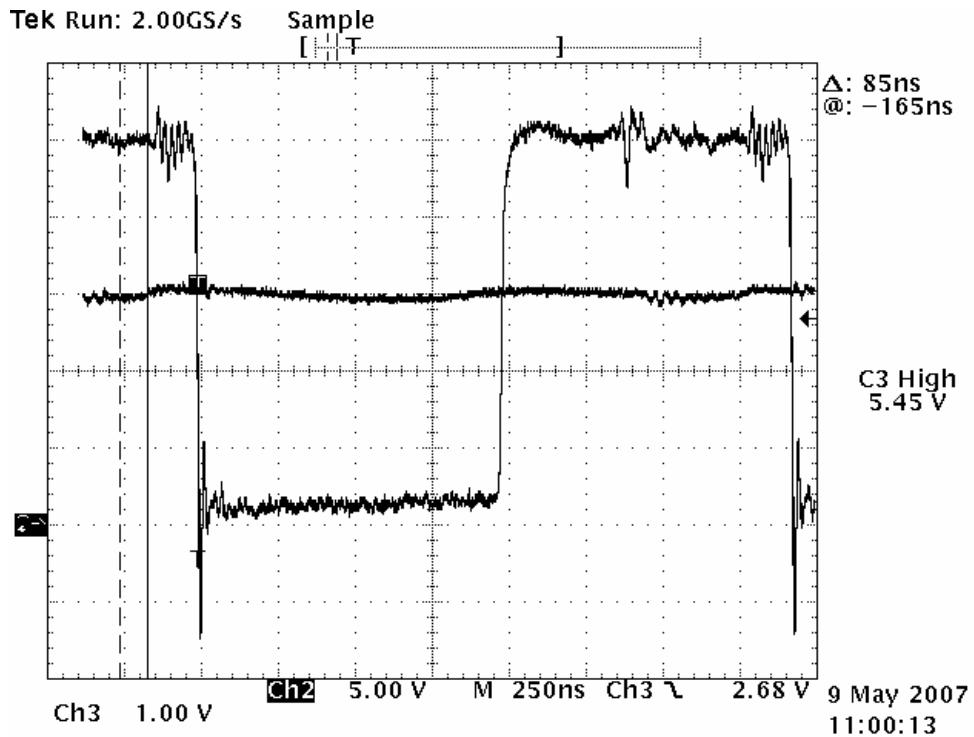
Sync input waveform (scope Channel 3) at VSTIF ACS Shield TEC Converter located on LVPS2 board, device U9. The Shield TEC Converter is an MFL2812S converter that is configured as a 3.5 Amp constant current supply, driving a fixed 1.5 ohm load. Differential pod used, with black lead connected to U9-2 (In Common) and red lead connected to U9-3 (Sync In).

HOLD Converter Secondary Voltage waveform shown on scope Channel 2. HOLD Converter is an MFL2815D. Differential pod used, with black lead connected to Chassis.

Sync High voltage shown to be between 4.8V and 5.3V. Sync duty cycle approximately 50%. Falling edge of sync noted to drop about 1.25V below ground level momentarily and then recover (see next waveform for expanded time scale).



Identical test set up as previous scope image, however, expanded time scale looking at falling edge of sync waveform. Falling edge of Sync waveform drops 1.25V below ground for less than 10ns. This extremely short duration is not believed to be of concern.



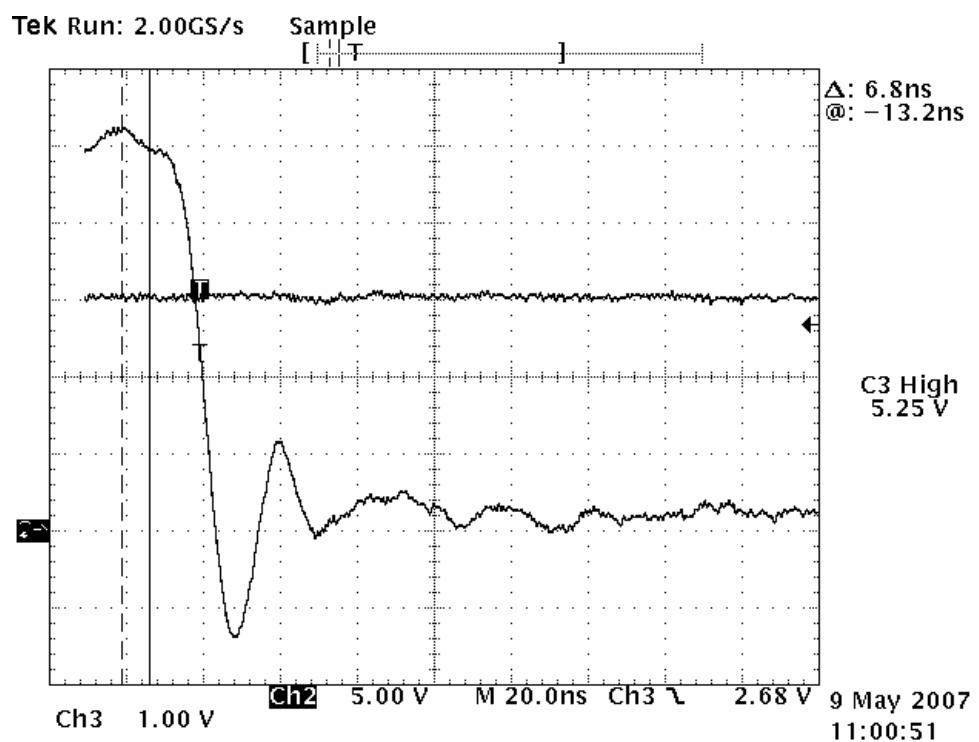
Scope waveforms taken with the VSTIF ACS HOLD Converter enabled as well as the Shield TEC converter enabled.

Sync input waveform (scope Channel 3) at VSTIF ACS Shield TEC Converter located on LVPS2 board, device U9 (same as in previous scope images). The Shield TEC Converter is an MFL2812S converter that is configured as a 3.5 Amp constant current supply. Differential pod used, with black lead connected to U9-2 (In Common) and red lead connected to U9-3 (Sync In).

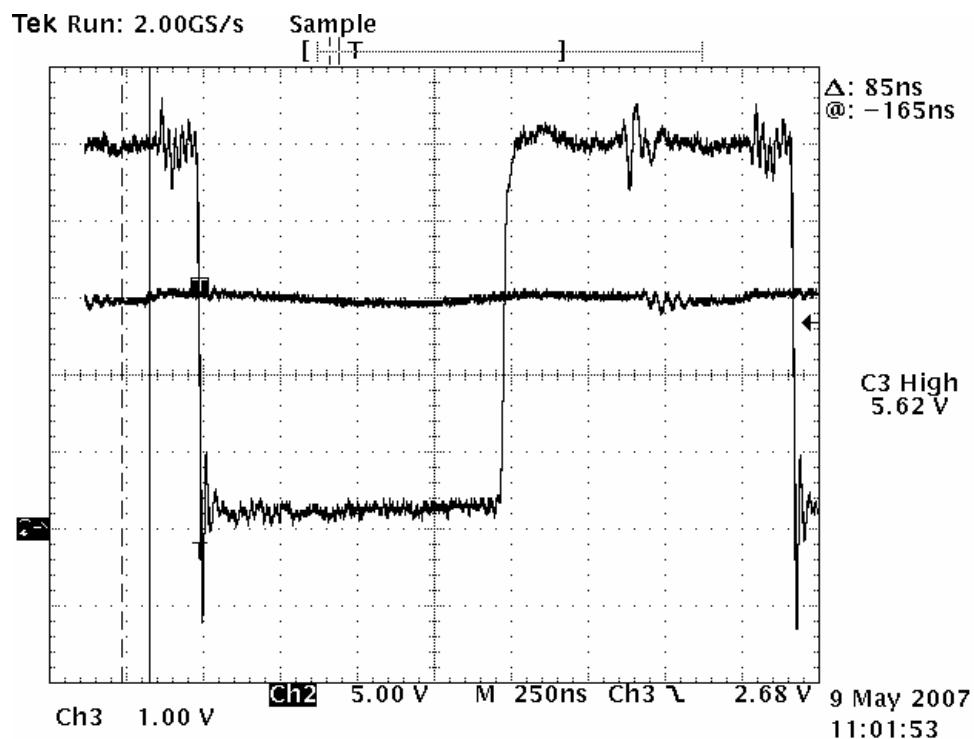
HOLD Converter Secondary Voltage waveform shown on scope Channel 2. HOLD Converter is an MFL2815D. Differential pod used, with black lead connected to Chassis.

Sync High voltage shown to be between 4.4V and 5.5V. Sync duty cycle approximately 50%. Falling edge of sync noted to drop about 1.4V below ground level momentarily and then recover (see next waveform for expanded time scale).

Converter switching noise is now noted on the high level of the Sync waveform in what appears to be two bursts.

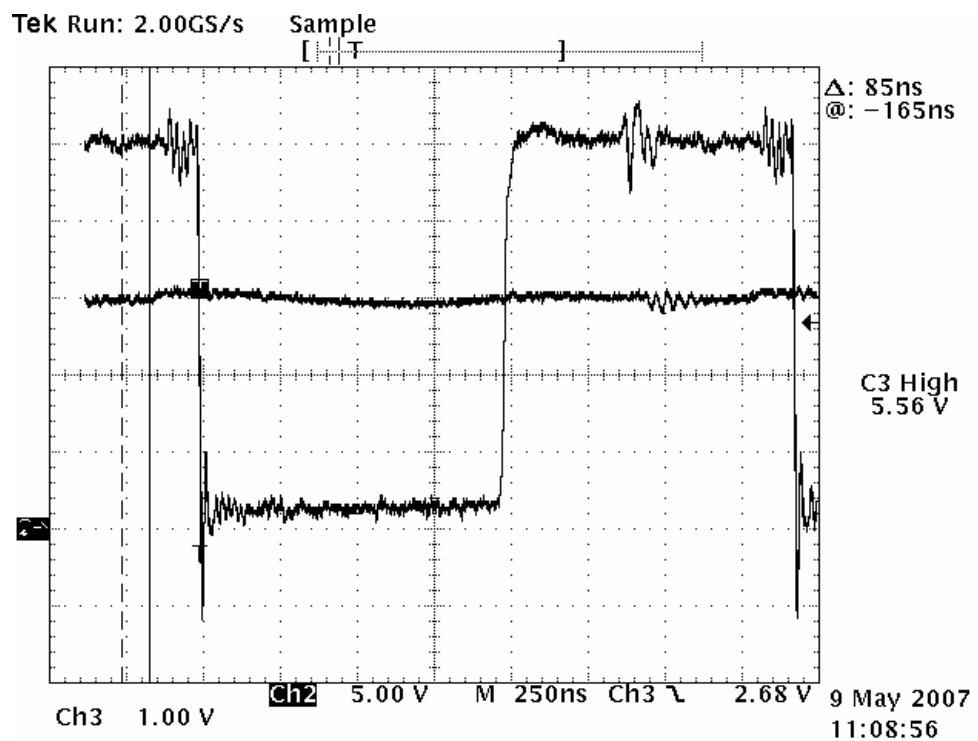


Identical test set up as previous scope image, however, expanded time scale looking at falling edge of sync waveform. Falling edge of Sync waveform drops 1.4V below ground for less than 10ns. This extremely short duration is not believed to be of concern.



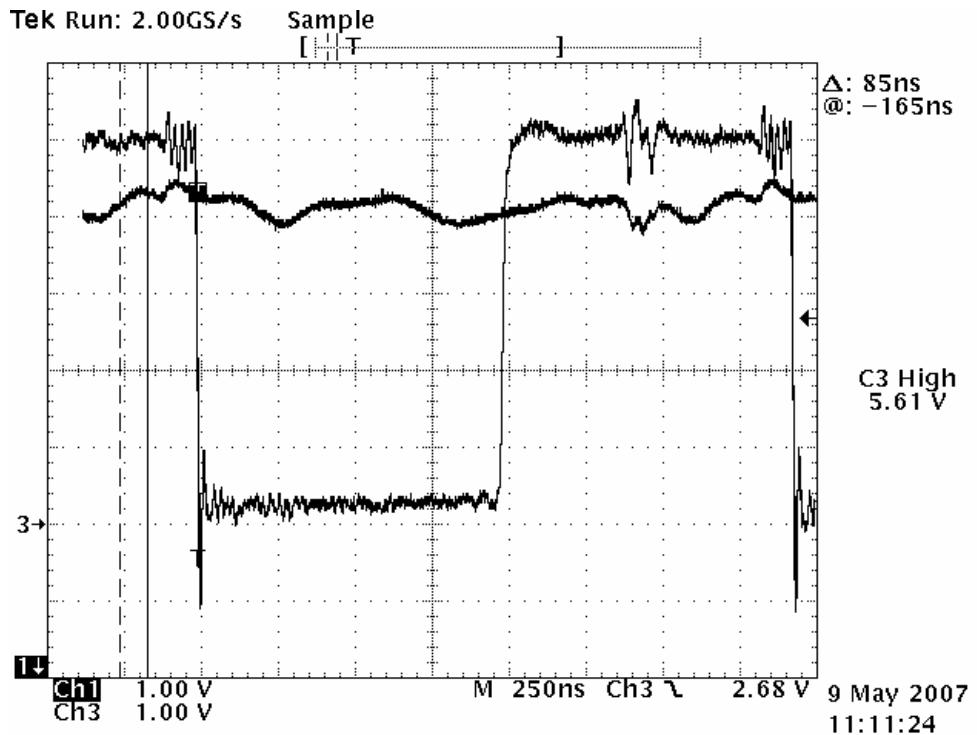
Scope waveforms taken with the VSTIF ACS HOLD Converter enabled as well as the Shield TEC converter enabled and the two Thermal Converters (MFS2815S) enabled. Thermal Converter loads were set to 25 Ohms each.

No perceptible difference noted between this waveform taken with the Thermal Converters enabled and the previous waveform taken with just the HOLD and Shield TEC converters enabled.



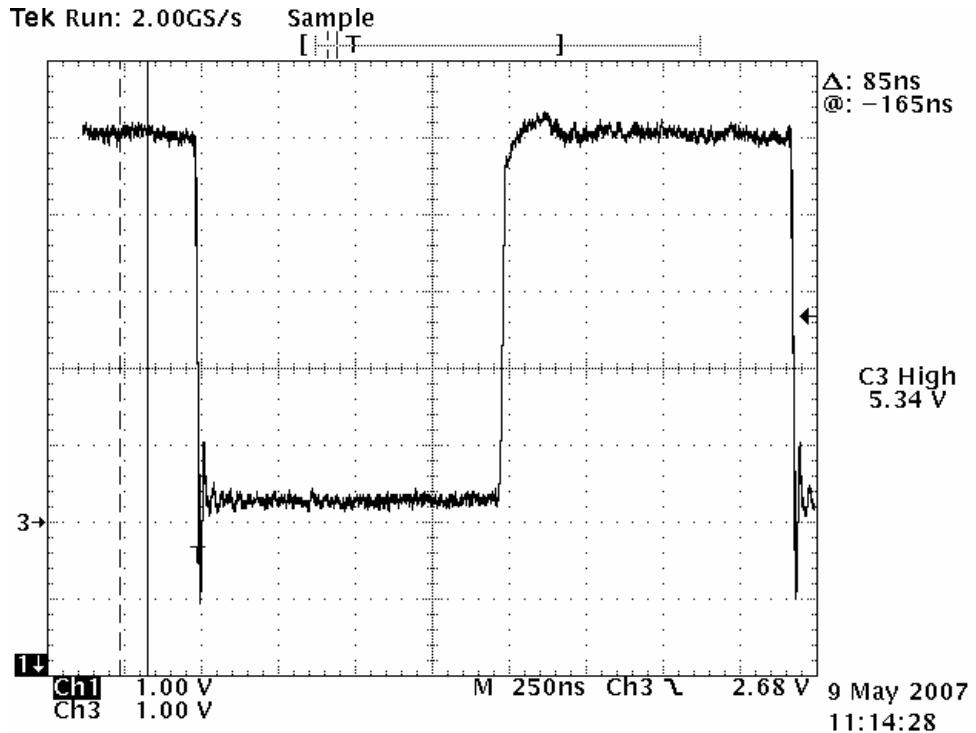
Scope waveforms taken with the VSTIF ACS system up in Operate Mode. All converters enabled across entire system in flight like configuration.

No perceptible difference noted between Operate Mode configuration and the previous waveform taken with just the HOLD and Shield TEC converters enabled.



Scope waveforms taken with the VSTIF ACS system up in Operate Mode. All converters enabled across entire system in flight like configuration.

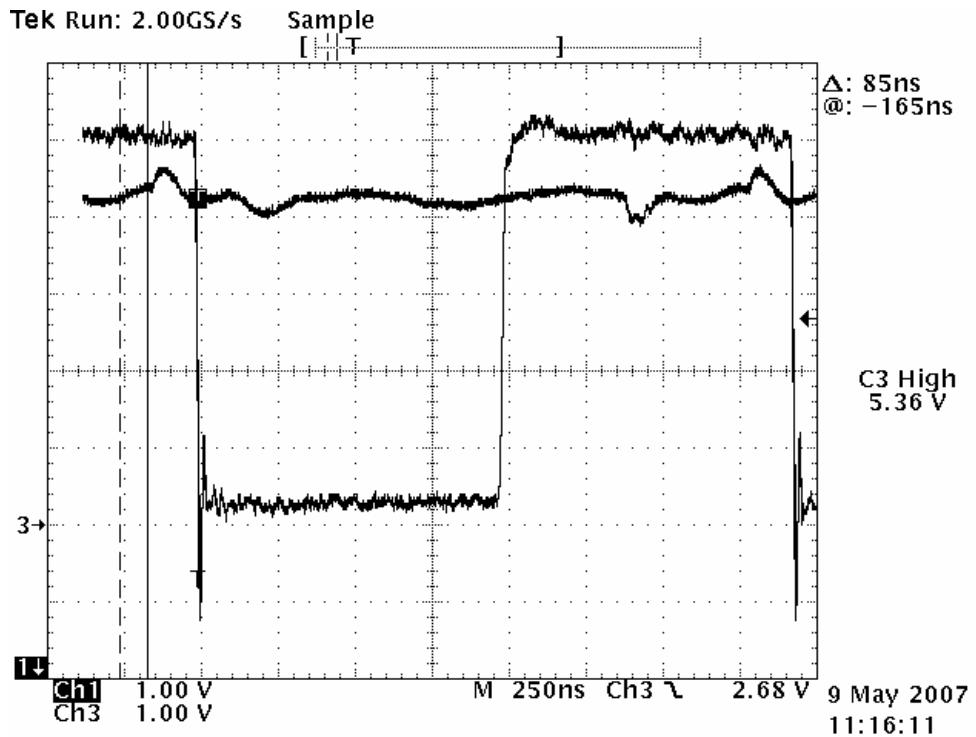
Scope channel 1 added to show Shield TEC secondary voltage output. Vertical scale set to 1V per division in an attempt to better understand nature of the two switching noise bursts seen on the high Sync waveform.



Scope waveforms taken with only the VSTIF ACS HOLD Converter enabled. Thus, the three remaining converters on the common Interpoint EMI filter (Shield TEC, Thermal Conv A, and Thermal Conv B) were Inhibited.

Sync input waveform (scope Channel 3) was MOVED to VSTIF ACS Thermal Converter B located on LVPS2 board, device U7. The Thermal Converter is an MFL2815S converter connected to a 25 ohm load. Differential pod used, with black lead connected to U7-2 (In Common) and red lead connected to U7-3 (Sync In).

The Sync waveform shown above with just the HOLD converter enabled is identical to the Sync waveform taken at the Shield TEC Converter when just the HOLD converter was enabled.

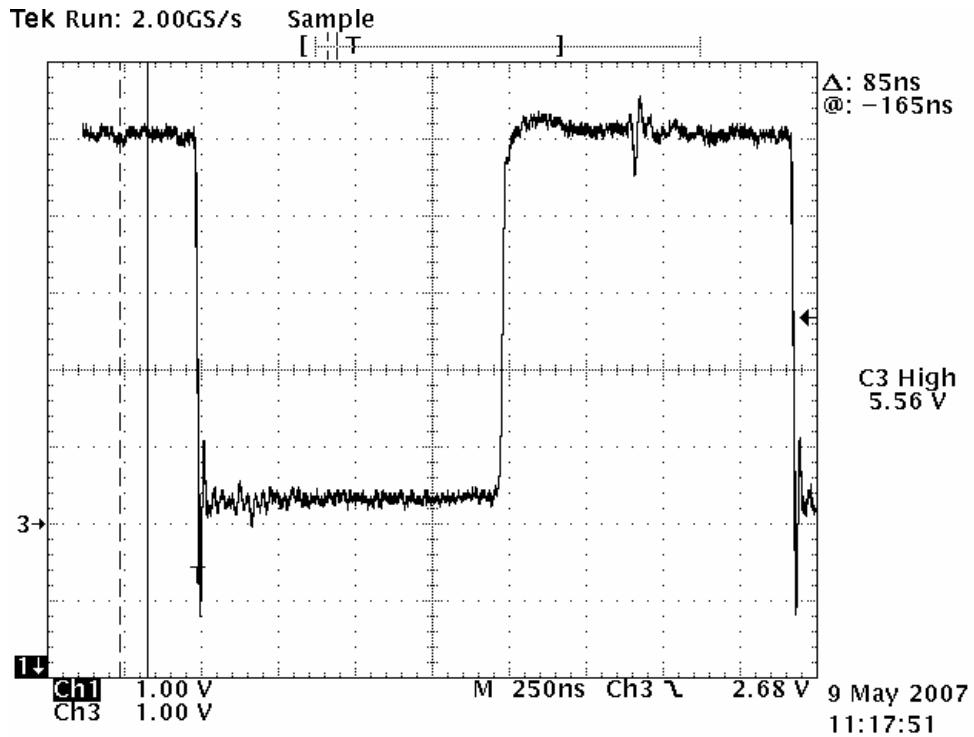


Scope waveforms taken with the VSTIF ACS HOLD Converter enabled and the Shield TEC Converter enabled.

Sync input waveform (scope Channel 3) still connected to VSTIF ACS Thermal Converter B located on LVPS2 board, device U7. The Thermal Converter is an MFL2815S converter connected to a 25 ohm load. Differential pod used, with black lead connected to U7-2 (In Common) and red lead connected to U7-3 (Sync In).

Scope channel 1 added to show Shield TEC secondary voltage output.

The Sync waveform shown above with the HOLD converter enabled and the Shield TEC converter enabled is identical to the Sync waveform taken with just the HOLD converter was enabled. Thus the switching noise noted on the Shield TEC Converter sync input when the Shield TEC Converter is enabled is not seen at the Thermal Converter Sync input.



Scope waveforms taken with the VSTIF ACS HOLD Converter enabled and the Thermal Converters enabled. The Shield TEC Converter has been disabled.

Sync input waveform (scope Channel 3) still connected to VSTIF ACS Thermal Converter B located on LVPS2 board, device U7. The Thermal Converter is an MFL2815S converter connected to a 25 ohm load. Differential pod used, with black lead connected to U7-2 (In Common) and red lead connected to U7-3 (Sync In).

The Sync waveform shown above with the HOLD converter enabled and the Thermal Converters enabled (driving a 25 ohm load each) shows the presence of a single burst of converter switching noise. Thus the second burst of switching noise noted near the end of the sync high waveform measured at the Shield TEC Converter sync input when the Shield TEC Converter is enabled is not seen at the Thermal Converter Sync input.

## **Appendix C:**

*MFL Single and Dual DC/DC Converters*, Crane Aerospace & Electronics Power Solutions (Created Feb 09, 2007)

## MFL Single and Dual DC/DC Converters

### 28 VOLT INPUT – 65 WATT

#### FEATURES

- $-55^{\circ}$  to  $+125^{\circ}\text{C}$  operation
- 16 to 40 VDC input
- Fully Isolated
- Magnetic feedback
- Fixed frequency, 600 kHz typical
- Topology – Single Ended Forward
- 50 V for up to 120 ms transient protection
- Inhibit (input & output side)
- Sync function (in and out)
- Output trim on single output models
- Indefinite short circuit protection
- Remote sense on single output models
- Up to 87% efficiency / 43 W/in<sup>3</sup>
- Parallelable up to 148 watts



#### DESCRIPTION

The MFL Series™ 28-volt DC/DC converters are rated up to 65 watts of output power over a  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  temperature range with a 28 VDC nominal input. On dual output models up to 70% of the rated output power can be drawn from either the positive or negative output. Current sharing allows the units to be paralleled for total power of up to 148 watts. The welded, hermetically sealed package is only 3.005 x 1.505 x 0.400 inches, giving the series an overall power density of up to 43 watts per cubic inch.

#### DESIGN FEATURES

The MFL Series converters are switching regulators that use a quasi-square wave, single ended forward converter design with a constant switching frequency of 600 kHz.

Isolation between input and output circuits is provided with a transformer in the forward path and a wide bandwidth magnetic coupling in the feedback control loop. The MFL uses a unique dual loop feedback technique that controls output current with an inner feedback loop and an output voltage with a cascaded voltage mode feedback loop.

The additional secondary current mode feedback loop improves transient response in a manner similar to primary current mode control and allows for ease of paralleling, but without the cost and complexity.

The constant frequency, pulse-width modulated converters use a quasi-square wave single-ended forward design. Tight load regulation is achieved through a wide-bandwidth magnetic feedback circuit. The output on single MFL models can be trimmed (see Figure 1 for voltage changes with different resistor values).

MODELS	
VDC OUTPUT	
SINGLE	DUAL
3.3	$\pm 5$
5	$\pm 12$
12	$\pm 15$
15	
28	

Other output voltages available upon request, including 2 V, 8 V and 54 V single.

#### INHIBIT

The MFL Series converters have two TTL compatible inhibit terminals (INH1 and INH2) that can be used to disable power conversion, resulting in a very low quiescent input current and no generation of switching noise. An open collector TTL compatible low (<0.8 volts) is required to inhibit the converter between INH1 (pin 4) and Input Common (pin 2). An open collector TTL compatible low (<0.5 volts) is required to inhibit the converter between INH2 (pin 12) and Output Common (pin 8). The application of intermediate voltages to these pins (1.5 to 10.5 volts) should be avoided.

#### SYNC

Converters may be synced to an external clock (525 to 675 kHz) or to one another by using the sync in or out pins. The nominal free-run switching frequency is 600 kHz.

#### CURRENT AND PARALLEL OPERATION

Multiple MFL converters may be used in parallel to drive a common load (see Figure 2). In this mode of operation the load current is shared by two or three MFL converters. In current sharing mode, one MFL converter is designated as a master. The SLAVE pin (pin 11) of the master is left unconnected and the MSTR/INH2 pin (pin 12) of the master is connected to the SLAVE pin (pin 11) of the slave units. The units designated as slaves have the MSTR/INH2 pin (pin 12) connected to the SNS RTN pin (pin 9). Figure 2 shows the typical setup for two or three units in parallel. Note that synchronizing the units together (though shown in the figure) is not required for current sharing operation. A second slave unit may be placed in parallel with a master and slave; this requires the TRI pin (pin 3) of the master unit to be connected to the SNS RTN pin (pin 9).

When paralleled, 76% of the total combined power ratings of the MFL converters are available at the load. Overload and short circuit performance are not adversely affected during parallel operation.

# MFL Single and Dual DC/DC Converters

## 28 VOLT INPUT – 65 WATT

### OPERATING CONDITIONS AND CHARACTERISTICS

#### **Input Voltage Range**

- 16 to 40 VDC continuous
- 50 V for 120 msec transient

#### **Output Power**

- 50 to 65 watts depending on model

#### **Lead Soldering Temperature (10 sec per lead)**

- 300°C

#### **Storage Temperature Range (Case)**

- -65°C to +150°C

#### **Power Dissipation (Pd)**

- 14 watts (16 watts MFL2805S, MFL2805D)

#### **Case Operating Temperature (Tc)**

- -55°C to +125°C full power
- -55°C to +135°C absolute

#### **Derate Output Power/Current**

- Linearly from 100% at 125°C to 0% at 135°C
- MFL283R3S: linearly from 100% at 100°C to 80% at 125°C and to 0% at 135°C

#### **Output Voltage Temperature Coefficient**

- 100 ppm/°C typical

#### **Input to Output Capacitance**

- 150 pF, typical

#### **Current Limit**

- 125% of full load typical

#### **Isolation**

- 100 megohm minimum at 500 V

#### **Audio Rejection**

- 50 dB typical

#### **Conversion Frequency (-55°C to 125°C)**

- Free run mode 600 kHz typical
- 525 kHz min, 675 kHz max

#### **Inhibit Pin Voltage (unit enabled)**

- INH1 = 9 to 12 V, INH2 = 6 to 9 V

### **SYNC AND INHIBIT (INH1, INH2)**

#### **Sync In (525 to 675 kHz)**

- Duty cycle 40% min, 60% max
- Logic low 0.8 V max
- Logic high 4.5 V min, 5 V max
- Referenced to input common

#### **Sync Out**

- Referenced to input common

#### **Inhibit (INH1, INH2) TTL Open Collector**

- Logic low (output disabled)  
INH1 referenced to input common  
Logic low 0.8 V max  
Inhibit pin current 10 mA max
- Logic low (output enabled)  
INH2 referenced to output common  
Logic low 0.5 V max  
Inhibit pin current 5 mA max
- Logic high (output enabled)  
Open collector

### MECHANICAL AND ENVIRONMENTAL

#### **Size (maximum)**

3.005 x 1.505 x 0.400 inches (76.33 x 38.23 x 10.16 mm)

See case U for dimensions.

Case options V, W, Y and Z are available by special order.

#### **Weight (maximum)**

86 grams

#### **Screening**

Standard, ES, or /883 (Class H, QML). See "883, Class H, QML Products – Element Evaluation" and "883, Class H, QML Products – Environmental Screening" for more information.

# MFL Single and Dual DC/DC Converters

## 28 VOLT INPUT – 65 WATT

PIN OUT				PINS NOT IN USE	
Pin	Single Output	MFL2828S	Dual Output	TR1	
1	Positive Input	Positive Input	Positive Input	Master	Leave unconnected
2	Input Common	Input Common	Input Common	Slave	Leave unconnected
3	Triple (TRI)	Triple (TRI)	Triple (TRI)	Sync in	Connect to input common
4	Inhibit 1 (INH1)	Inhibit 1 (INH1)	Inhibit 1 (INH1)	Inhibit (INH1)	Leave unconnected
5	Sync Out	Sync Out	Sync Out	Inhibit (INH2)	Leave unconnected
6	Sync In	Sync In	Sync In	Sync Out	Leave unconnected
7	Positive Output	Positive Output	Positive Output	Sense Lines	Must be connected to appropriate outputs
8	Output Common	No connection	Output Common		
9	Sense Return	Output Common	Negative Output		
10	Positive Sense	No connection	No connection		
11	Slave	Slave	Slave		
12	Master/ Inhibit 2	Master/ Inhibit 2	Master / Inhibit 2		

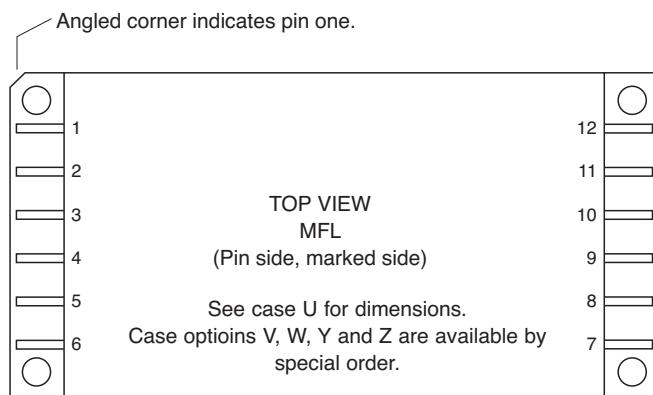


FIGURE 1: PIN OUT

## MFL Single and Dual DC/DC Converters

### 28 VOLT INPUT – 65 WATT

#### SINGLE OUTPUT MODELS CONNECTION DIAGRAMS - SENSE AND PARALLEL

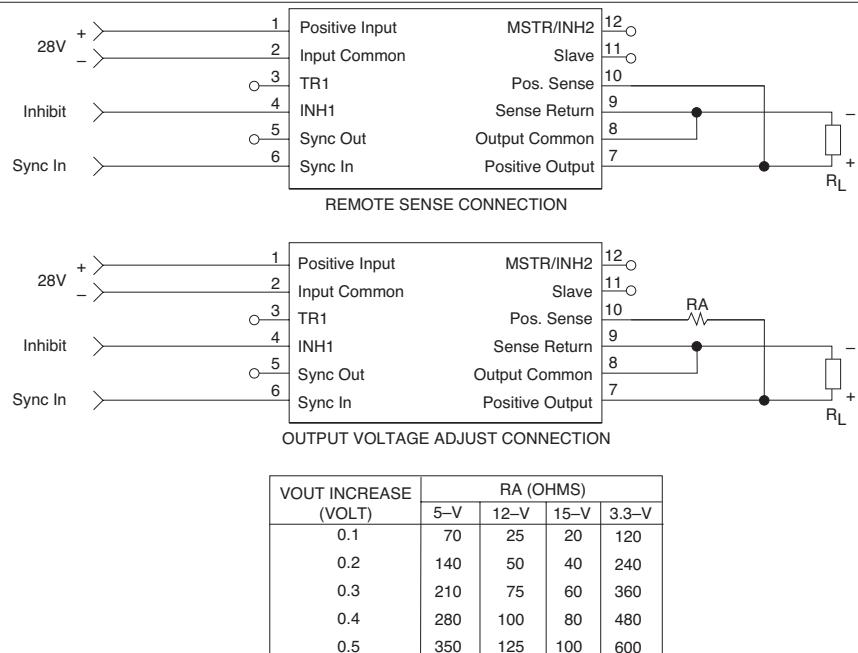


FIGURE 2: SENSE CONNECTIONS AND TRIM TABLE

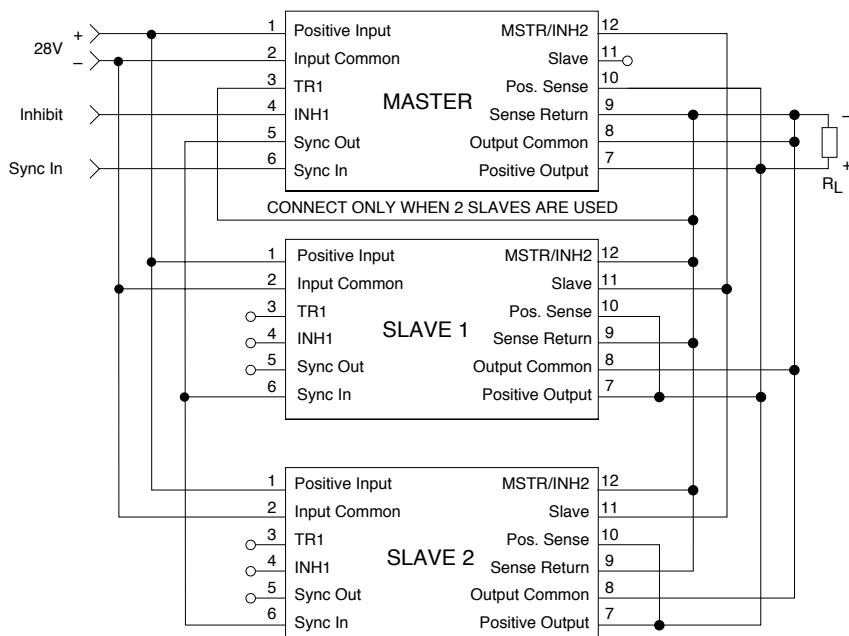
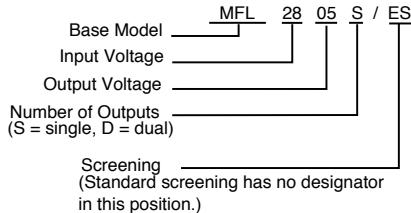


FIGURE 3: PARALLEL CONNECTIONS

## MFL Single and Dual DC/DC Converters

### 28 VOLT INPUT – 65 WATT

#### MODEL NUMBERING KEY



#### SMD NUMBERS

STANDARD MICROCIRCUIT DRAWING (SMD)	MFL SERIES SIMILAR PART
IN PROCESS	MFL283R3S
5962-9316301HXC	MFL2805S/883
5962-9316201HXC	MFL2812S/883
5962-9316101HXC	MFL2815S/883
IN PROCESS	MFL2828S/883
5962-9319101HXC	MFL2805D/883
5962-9319201HXC	MFL2812D/883
5962-9319301HXC	MFL2815D/883

For exact specifications for an SMD product, refer to the SMD drawing. SMDs can be downloaded from:  
<http://www.dscc.dla.mil/programs/smcr>

#### Model Selection

##### MFL28

Base model      Vout value      number of outputs      screening

Choose one from each of the following rows

<b>Vout value</b>	for singles: 3R3, 5, 12, 15, 28	for duals: 5, 12, 15
<i>"R" = decimal point, 3R3 = 3.3VDC</i>		
<b>Number of outputs</b>	S (single) or D (dual)	
<b>Screening</b>	standard screening, leave blank	/ES (ES screening), /883 (Class H, QML)

## MFL Single and Dual DC/DC Converters

### 28 VOLT INPUT – 65 WATT

**Electrical Characteristics: -55°C to +125° C Tc, 28 VDC Vin, 100% load, free run, unless otherwise specified.**

SINGLE OUTPUT MODELS		MFL283R3S			MFL2805S			MFL2812S			UNITS
PARAMETER	CONDITION	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
OUTPUT VOLTAGE	Tc = 25°C	3.26	3.3	3.34	4.95	5.00	5.05	11.88	12.00	12.12	VDC
OUTPUT CURRENT	V <sub>IN</sub> = 16 TO 40 VDC	0	—	12.12 <sup>2</sup>	0	—	10	0	—	5	A
OUTPUT POWER	V <sub>IN</sub> = 16 TO 40 VDC	0	—	40 <sup>2</sup>	0	—	50	0	—	60	W
OUTPUT RIPPLE	Tc = 25°C	—	10	35	—	15	35	—	30	75	mV p-p
VOLTAGE 10 k - 2 MHz	Tc = -55°C to +125°C	—	10	50	—	30	50	—	45	100	
LINE REGULATION	V <sub>IN</sub> = 16 to 40 VDC	—	0	20	—	0	20	—	0	20	mV
LOAD REGULATION	NO LOAD TO FULL	—	—	40	—	—	20	—	—	20	mV
INPUT VOLTAGE	CONTINUOUS	16	28	40	16	28	40	16	28	40	VDC
NO LOAD TO FULL	TRANSIENT <sup>1, 3</sup> 50 ms	—	—	50	—	—	50	—	—	50	V
INPUT CURRENT	NO LOAD	—	70	100	—	70	120	—	50	100	mA
	INHIBITED - INH1	—	9	14	—	9	14	—	9	14	mA
	INHIBITED - INH2	—	35	70	—	35	70	—	35	70	
INPUT RIPPLE											
CURRENT	10 kHz - 10 MHz	—	15	50	—	15	50	—	15	50	mA pp
EFFICIENCY	Tc = 25°C	73	—	—	77	80	—	83	86	—	%
LOAD FAULT	POWER DISSIPATION										
	SHORT CIRCUIT										
	Tc = 25°C	—	12.5	20	—	12.5	16	—	10	14	W
STEP LOAD RESP.	RECOVERY <sup>1</sup>	—	1.5	4	—	1.5	4	—	1.5	4	ms
	50% – 100% – 50%										
	TRANSIENT	—	200	400	—	250	350	—	450	600	mV pk
STEP LINE RESP.	RECOVERY <sup>1, 4</sup>	—	1.5	3.0	—	1.5	3.0	—	1.5	3.0	ms
	16 – 40 – 16 VDC										
	TRANSIENT <sup>1, 5</sup>	—	250	300	—	250	300	—	250	400	mV pk
START-UP <sup>6</sup>	RECOVERY <sup>1, 4</sup>	—	200	600	—	200	300	—	200	300	μs
	DELAY	—	3.5	6	—	3.5	6	—	3.5	6	ms
	OVERSHOOT <sup>1</sup>	—	0	25	—	0	25	—	0	50	mV pk
C <sub>OUT</sub>	Tc=25°C <sup>1, 7</sup>	—	—	1000	—	—	1000	—	—	1000	μF

#### Notes

1. Guaranteed by design, not tested.
2. MFL283R3S current and power maximum are at 25°C only.
3. Unit will shut down above approximately 45V but will be undamaged and will restart when voltage drops into normal range.
4. Recovery time is measured from application of the transient to point at which Vout is within 1% of final value.
5. Transition time ≥ 10 μs.
6. Tested on release from inhibit.
7. Shall not compromise DC performance

## MFL Single and Dual DC/DC Converters

### 28 VOLT INPUT – 65 WATT

**Electrical Characteristics:**  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{ C}$   $T_c$ , 28 VDC  $V_{in}$ , 100% load, free run, unless otherwise specified.

SINGLE OUTPUT MODELS		MFL2815S			MFL2828S <sup>2</sup>			UNITS
PARAMETER	CONDITION	MIN	TYP	MAX	MIN	TYP	MAX <sup>2</sup>	
OUTPUT VOLTAGE	$T_c = 25^{\circ}\text{C}$	14.85	15.00	15.15	27.72	28.00	28.28	VDC
OUTPUT CURRENT	$V_{IN} = 16$ TO 40 VDC	0	—	4.33	0	—	2.32	A
OUTPUT POWER	$V_{IN} = 16$ TO 40 VDC	0	—	65	0	—	65	W
OUTPUT RIPPLE VOLTAGE 10 k - 2 MHz	$T_c = 25^{\circ}\text{C}$ $T_c = -55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	—	30	85	—	100	200	mV p-p
LINE REGULATION	$V_{IN} = 16$ to 40 VDC	—	0	20	—	20	60	mV
LOAD REGULATION	NO LOAD TO FULL	—	0	20	—	20	75	mV
INPUT VOLTAGE NO LOAD TO FULL	CONTINUOUS	16	28	40	16	28	40	VDC
	TRANSIENT <sup>1, 3</sup> 50 ms	—	—	50	—	—	50	V
INPUT CURRENT	NO LOAD	—	50	100	—	60	100	mA
	INHIBITED - INH1	—	9	14	—	9	14	mA
	INHIBITED - INH2	—	35	70	—	35	70	mA
INPUT RIPPLE CURRENT	10 kHz - 10 MHz	—	15	50	—	20	50	mA pp
EFFICIENCY	$T_c = 25^{\circ}\text{C}$	84	87	—	83	86	—	%
LOAD FAULT	POWER DISSIPATION SHORT CIRCUIT $T_c = 25^{\circ}\text{C}$	—	10	14	—	7	14	W
	RECOVERY <sup>1</sup>	—	1.5	4	—	1.0	4	ms
STEP LOAD RESP.	50% – 100% – 50% TRANSIENT	—	500	600	—	800	1400	mV pk
	RECOVERY <sup>1, 4</sup>	—	1.5	3.0	—	1.5	3.0	ms
STEP LINE RESP.	16 – 40 – 16 VDC TRANSIENT <sup>1, 5</sup>	—	250	400	—	250	800	mV pk
	RECOVERY <sup>1, 4</sup>	—	200	300	—	200	400	$\mu\text{s}$
START-UP <sup>6</sup>	DELAY	—	3.5	6	—	3.5	6	ms
	OVERSHOOT <sup>1,</sup>	—	0	50	—	0	100	mV pk
$C_{OUT}$	$T_c=25^{\circ}\text{C}$ <sup>1, 7</sup>	—	—	1000	—	—	1000	$\mu\text{F}$

Notes

1. Guaranteed by design, not tested.
2. MFL2828S specifications are at  $25^{\circ}\text{C}$ .
3. Unit will shut down above approximately 45V but will be undamaged and will restart when voltage drops into normal range.
4. Recovery time is measured from application of the transient to point at which  $V_{out}$  is within 1% of final value.
5. Transition time  $\geq 10 \mu\text{s}$ .
6. Tested on release from inhibit.
7. Shall not compromise DC performance

## MFL Single and Dual DC/DC Converters

### 28 VOLT INPUT – 65 WATT

**Electrical Characteristics:**  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$   $T_c$ , 28 VDC  $V_{IN}$ , 100% load, free run, unless otherwise specified.

DUAL OUTPUT MODELS		MFL2805D			MFL2812D			MFL2815D			UNITS
PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
OUTPUT VOLTAGE	$T_c = 25^{\circ}\text{C}$ $\pm V_{OUT}$	4.95	5.00	5.05	11.88	12.00	12.12	14.85	15.00	15.15	VDC
	$V_{IN} = 16$ TO 40 VDC	4.92	5.00	5.08	11.82	12.00	12.18	14.77	15.00	15.23	
OUTPUT CURRENT <sup>2</sup>	EACH OUTPUT	0	—	7	0	—	3.5	0	—	3.03	A
	TOTAL OUTPUT	0	—	10	0	—	5	0	—	4.34	
OUTPUT POWER <sup>2</sup>	$V_{IN} = 16$ TO 40 VDC	0	—	50	0	—	60	0	—	65	W
OUTPUT RIPPLE											
VOLTAGE $\pm V_{OUT}$	10 kHz - 2 MHz	—	50	100	—	50	120	—	50	150	mV p-p
LINE REGULATION	$+V_{OUT}$	—	0	50	—	0	50	—	0	50	mV
	$-V_{OUT}$	—	25	100	—	25	100	—	25	100	
LOAD REGULATION	$+V_{OUT}$	—	0	50	—	10	50	—	10	50	mV
NO LOAD TO FULL	$-V_{OUT}$	—	25	100	—	50	120	—	50	150	
CROSS REGULATION	SEE NOTE 3	—	5	8	—	2	4	—	2	4	%
	SEE NOTE 4	—	3	6	—	2	4	—	2	4	
INPUT VOLTAGE	CONTINUOUS	16	28	40	16	28	40	16	28	40	VDC
NO LOAD TO FULL	TRANSIENT <sup>1, 5</sup> 50 ms.	0	—	50	0	—	50	0	—	50	V
INPUT CURRENT	NO LOAD	—	50	120	—	50	100	—	50	100	mA
	INHIBITED - INH1	—	9	14	—	9	14	—	9	14	
	INHIBITED - INH2	—	35	70	—	35	70	—	35	70	
INPUT RIPPLE											
CURRENT	10 kHz - 10 MHz	—	15	50	—	15	50	—	15	50	mA p-p
EFFICIENCY $25^{\circ}\text{C} T_c$	BALANCED LOAD	77	80	—	83	86	—	84	87	—	%
LOAD FAULT	POWER DISSIPATION										
	SHORT CIRCUIT										
	$T_c = 25^{\circ}\text{C}$	—	12.5	16	—	10	14	—	10	14	W
	RECOVERY <sup>1</sup>	—	1.5	4.0	—	1.5	4.0	—	1.5	4.0	ms
STEP LOAD RESP. $\pm V_{OUT}$	50 %–100%– 50% LOAD										
	TRANSIENT	—	250	350	—	450	600	—	500	600	mV pk
	RECOVERY <sup>1, 6</sup>	—	1.5	3.0	—	1.5	3.0	—	1.5	3.0	ms
STEP LINE RESP. $\pm V_{OUT}$	16 – 40 – 16 $V_{IN}$										
	TRANSIENT <sup>1, 7</sup>	—	250	300	—	250	400	—	250	400	mV pk
	RECOVERY <sup>1, 6</sup>	—	200	300	—	200	300	—	200	300	$\mu\text{s}$
START-UP <sup>8</sup>	DELAY	—	3.5	6	—	3.5	6	—	3.5	6	ms
	OVERSHOOT <sup>1</sup>	—	0	25	—	0	50	—	0	50	mV p
$C_{OUT}$	$T_c=25^{\circ}\text{C} 1,9$	—	—	500	—	—	500	—	—	500	$\mu\text{F}$

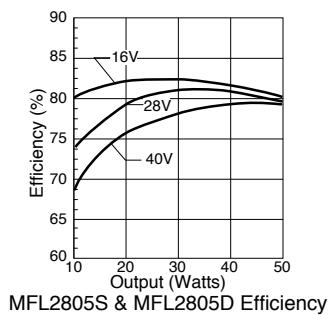
#### Notes

1. **Guaranteed by design, not tested.**
2. Up to 70% of the total output power is available from either output providing the opposite output is simultaneously carrying 30% of the total power.
3. Effect on negative  $V_{OUT}$  from 50%/50% loads to 70%/30% or 30%/70% loads.
4. Effect on negative  $V_{OUT}$  from 50%/50% loads to +Pout=50%, -Pout=10%.
5. Unit will shut down above approximately 45V but will be undamaged and will restart when voltage drops into normal range.
6. Recovery time is measured from application of the transient to point at which  $V_{OUT}$  is within 1% of final value.
7. Transition time  $\geq 10 \mu\text{s}$ .
8. Tested on release from inhibit.
9. Shall not compromise DC performance

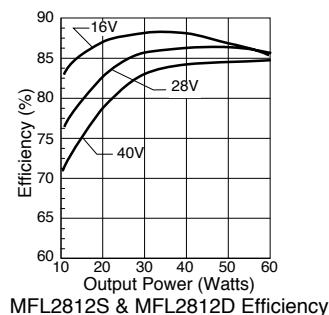
## MFL Single and Dual DC/DC Converters

### 28 VOLT INPUT – 65 WATT

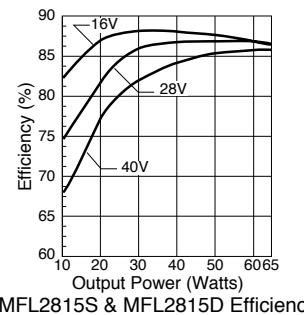
**Typical Performance Curves: 25°C Tc , 28 VDC Vin, 100% load, free run, unless otherwise specified.**



MFL2805S & MFL2805D Efficiency



MFL2812S & MFL2812D Efficiency



MFL2815S & MFL2815D Efficiency

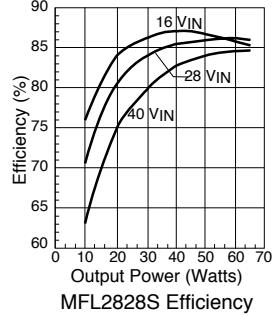


FIGURE 7

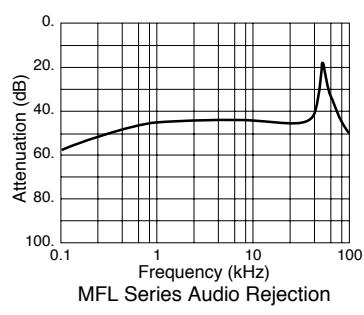


FIGURE 8

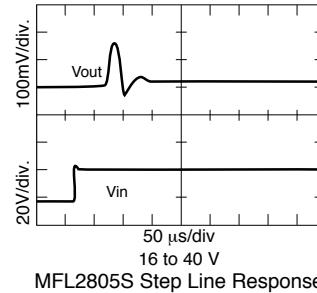
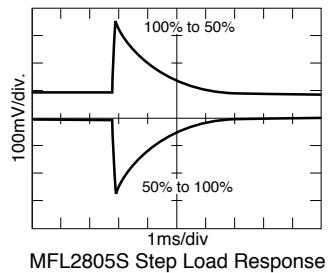
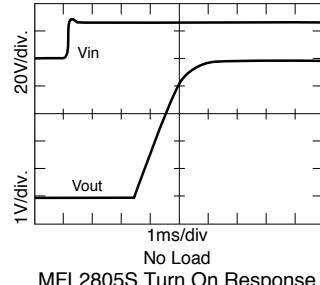


FIGURE 9



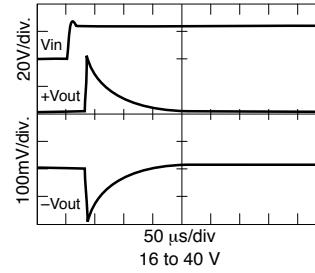
MFL2805S Step Load Response

FIGURE 10



MFL2805S Turn On Response

FIGURE 11



MFL2815D Step Line Response

FIGURE 12

## MFL Single and Dual DC/DC Converters

### 28 VOLT INPUT – 65 WATT

**Typical Performance Curves: 25°C Tc , 28 VDC Vin, 100% load, free run, unless otherwise specified.**

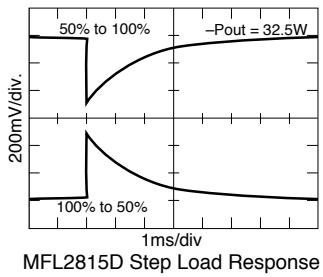


FIGURE 13

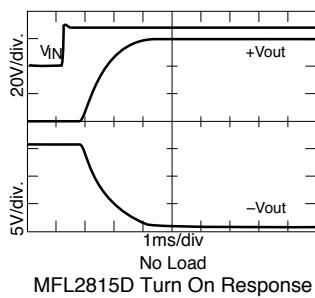


FIGURE 14

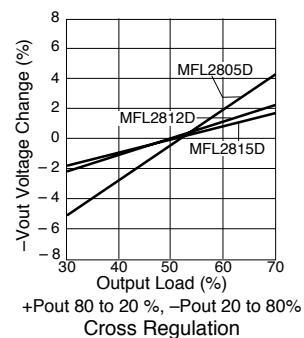


FIGURE 15

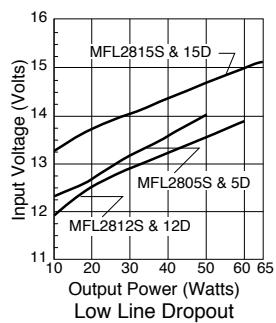


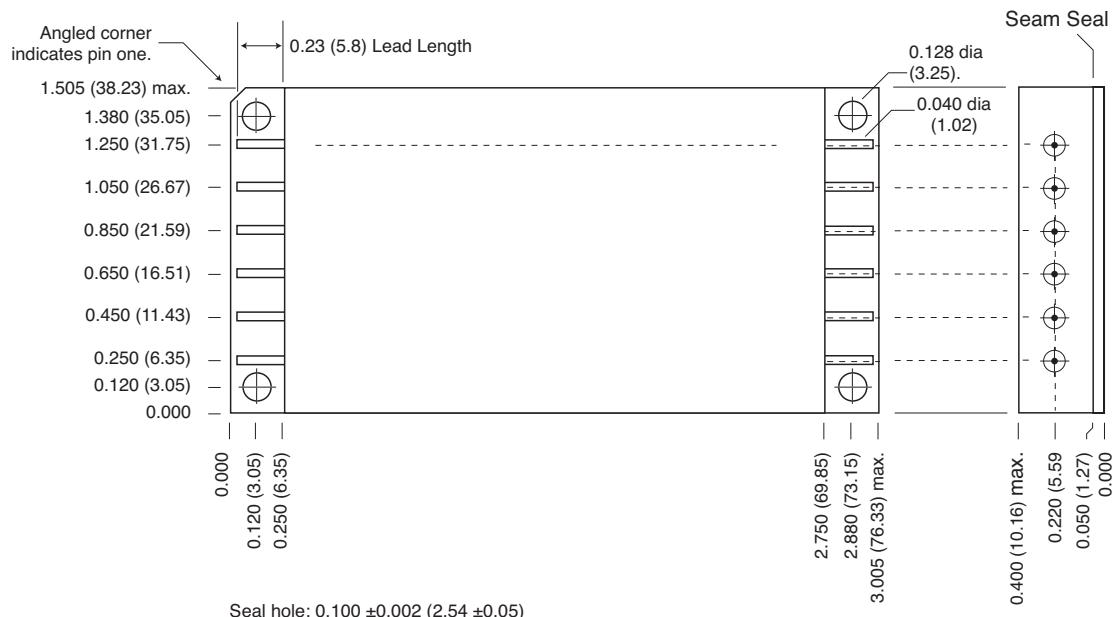
FIGURE 16

## MFL Single and Dual DC/DC Converter Cases

### 28 VOLT INPUT – 65 WATT

#### TOP VIEW CASE U Flanged case, short-leaded

\*Does not require designator in Case Option position of model number.



#### Case dimensions in inches (mm)

Tolerance  $\pm 0.005$  (0.13) for three decimal places  
 $\pm 0.01$  (0.3) for two decimal places  
unless otherwise specified

#### CAUTION

Heat from reflow or wave soldering may damage the device.  
Solder pins individually with heat application not exceeding 300°C for 10 seconds per pin

#### Materials

Header Cold Rolled Steel/Nickel/Gold  
Cover Kovar/Nickel  
Pins #52 alloy/Gold; compression glass seal

Case U, Rev C, 20060302

Please refer to the numerical dimensions for accuracy. All information is believed to be accurate, but no responsibility is assumed for errors or omissions. Interpoint reserves the right to make changes in products or specifications without notice.

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**FIGURE 17: CASE U**

## MFL Single and Dual DC/DC Converters

**28 VOLT INPUT – 65 WATT**

### 883, CLASS H, QML PRODUCTS – ELEMENT EVALUATION

<b>ELEMENT EVALUATION</b> <b>TEST PERFORMED (COMPONENT LEVEL)</b>	<b>STANDARD (NON-QML)<sup>1</sup></b>		<b>CLASS H, QML</b>	
	<b>M/S<sup>2</sup></b>	<b>P<sup>3</sup></b>	<b>M/S<sup>2</sup></b>	<b>P<sup>3</sup></b>
Element Electrical (probe)	yes	no	yes	yes
Element Visual	no	no	yes	yes
Internal Visual	no	no	yes	no
Final Electrical	no	no	yes	yes
Wire Bond Evaluation <sup>4</sup>	no	no	yes	yes
SLAM™/C-SAM: Input Capacitors only (Add'l test, not req. by H or K)	no	no	no	yes

#### Definitions:

Element Evaluation: Component testing/screening per MIL-STD-883 as determined by MIL-PRF-38534

SLAM™: Scanning Laser Acoustic Microscopy

C-SAM: C - Mode Scanning Acoustic Microscopy

#### Notes:

1. Non-QML products do no meet all of the requirements of MIL-PRF-38534
2. M/S = Active components (Microcircuit and Semiconductor Die)
3. P = Passive components
4. Not applicable to EMI filters that have no wire bonds

## MFL Single and Dual DC/DC Converters

**28 VOLT INPUT – 65 WATT**

### 883, CLASS H, QML PRODUCTS – ENVIRONMENTAL SCREENING

TEST	125°C STANDARD non-QML	125°C /ES non-QML	Class H /883 QML
Pre-cap Inspection Method 2017, 2032	yes	yes	yes
Temperature Cycle (10 times) Method 1010, Cond. C, -65°C to 150°C, ambient Method 1010, Cond. B, -55°C to 125°C, ambient	no no	no yes	yes no
Constant Acceleration Method 2001, 3000 g Method 2001, 500g	no no	no yes	yes no
Burn-In Method 1015, 160 hours at 125°C case, typical 96 hours at 125°C case, typical	no no	no yes	yes no
Final Electrical Test MIL-PRF-38534, Group A Subgroups 1 through 6: -55°C, +25°C, +125°C case Subgroups 1 and 4: +25°C case	no yes	no yes	yes no
Hermeticity Test Fine Leak, Method 1014, Cond. A Gross Leak, Method 1014, Cond. C Gross Leak, Dip ( $1 \times 10^{-3}$ )	no no yes	yes yes no	yes yes no
Final Visual Inspection Method 2009	yes	yes	yes

Test methods are referenced to MIL-STD-883 as determined by MIL-PRF-38534.

## **Appendix D:**

*MTR Single, Dual and Triple DC/DC Converters*, Crane Aerospace & Electronics  
Power Solutions (Created Sep 18, 2006)

## MTR Single, Dual and Triple DC/DC Converters

### 28 VOLT INPUT – 30 WATT

#### FEATURES

- -55° to +125°C operation
- 16 to 40 VDC input
- Fully isolated
- Magnetic feedback
- Fixed frequency 600 kHz typical
- Topology – Single Ended Forward
- 50 V for up to 50 ms transient protection
- Inhibit and synchronization functions
- Indefinite short circuit protection
- Up to 30 watts output power
- Trim and remote sense on single output models
- Up to 84% efficiency



MODELS		
VDC OUTPUT		
SINGLE	DUAL	TRIPLE
3.3	±5	+5 & ±12
5	±12	+5 & ±15
12	±15	
15		
18		

#### DESCRIPTION

The MTR Series™ of DC/DC converters offers up to 30 watts of output power from single, dual, or triple output configurations. They operate over the full military temperature range with up to 84% efficiency. MTR converters are packaged in hermetically sealed metal cases, making them ideal for use in military, aerospace and other high reliability applications.

#### CONVERTER DESIGN

The MTR converters are constant frequency, pulse-width modulated switching regulators which use a quasi-square wave, single ended, forward converter design. Tight load regulation is maintained via wide bandwidth magnetic feedback and, on single output models, through use of remote sense. On dual output models, the positive output is independently regulated and the negative output is cross regulated through the use of tightly coupled magnetics and shunt regulators. The MTR Series triple output DC/DC converter's design includes individual regulators on the auxiliary outputs which provide for no cross regulation error when a minimum 500 mA load is maintained on the main (+5) output.

Indefinite short circuit protection and overload protection are provided by a constant current-limit feature. This protective system senses current in the converter's secondary stage and limits it to approximately 115% of the maximum rated output current.

MTR converters are provided with internal filtering capacitors that help reduce the need for external components in normal operation. For systems that require compliance with MIL-STD-461C's CE03 standard, Interpoint offers filter/transient suppression modules (including the FMC-461, FMD-461 and FM-704A series filters) which will result in compliance. Contact your Interpoint representative for further details.

#### SYNCHRONIZATION

Synchronizing the converter with the system clock allows the designer to confine switching noise to clock transitions, minimizing interference and reducing the need for filtering. In sync mode, the converter will run at any frequency between 500 kHz and 675 kHz. The sync control operates with a quasi-TTL signal at any duty cycle between 40% and 60%. The sync pin must be connected to input common pin when not in use.

## MTR Single, Dual and Triple DC/DC Converters

### 28 VOLT INPUT – 30 WATT

#### OPERATING CONDITIONS AND CHARACTERISTICS

##### Input Voltage

- 16 to 40 VDC continuous
- 50 V for 50 msec transient

##### Output Power

- 25 to 30 watts depending on model

##### Lead Soldering Temperature (10 sec per pin)

- 300°C

##### Storage Temperature Range (Case)

- -65°C to +135°C

##### Case Operating Temperature (Tc)

- -55°C to +125°C full power
- -55°C to +135°C absolute

##### Derating Output Power/Current

- Linearly from 100% at 125°C to 0% at 135°C

##### Output Voltage Temperature Coefficient

- 100 ppm/°C typical single and dual outputs
- 200 ppm/°C main typical, 300 ppm/°C aux triple output typical

##### Input to Output Capacitance

- 50 pF typ (100 pF typical triple outputs)

##### Current Limit

- 115% of full load typical

##### Isolation

- 100 megohm minimum at 500 V

##### Audio Rejection

- 40 dB typ (50 dB typical triple output)

##### Conversion Frequency

- Free run 550 min, 600 typical, 650 max kHz duals and singles
- Free run 525 min, 600 typical, 650 max kHz triples
- External sync 500 to 675 kHz singles and duals
- External sync 500 to 700 kHz triples

#### SYNC AND INHIBIT

##### Sync (500 to 675 kHz)

- Duty cycle 40% min, 60% max
- Logic low 0.8 V max
- Logic high 4.5 V min, 5 V max
- Referenced to input common
- If not used, connect to input common

##### Inhibit TTL Open Collector (referenced to input common)

- Logic low (output disabled), ≤0.8 V  
Inhibit pin current  
8.0 mA max for singles & duals,  
6.0 mA for triples
- Logic high (output enabled)  
Input pin voltage, unit enabled, 9 to 11 V

#### MECHANICAL AND ENVIRONMENTAL

##### Size (maximum)

###### Non-flanged

Single and dual output 2.125 x 1.125 x 0.400 inches (53.98 x 28.58 x 10.16 mm) See case H2 for dimensions.  
MTR Dual with standard or ES screening, ht. 0.417", (10.59 mm) See Case H4 for dimensions.

Triple output 1.950 x 1.350 x 0.405 inches (49.53 x 34.29 x 10.29 mm) See case F1 for dimensions.

###### Flanged

Single and dual output 2.910 x 1.125 x 0.400 inches (73.91 x 28.58 x 10.16 mm) See case K3 for dimensions.  
MTR Dual with standard or ES screening, ht. 0.417", (10.59 mm) See case K5 for dimensions.

Triple output 2.720 x 1.350 x 0.405 inches (69.09 x 34.29 x 10.29 mm) See case J1 for dimensions.

##### Weight (maximum)

Single and dual non-flanged 50 grams, flanged 52 grams

Triple non-flanged 58 grams, flanged 62 grams

##### Screening

Standard, ES, or /883 (Class H, QML). See "883, Class H, QML Products – Element Evaluation" and "883, Class H, QML Products – Environmental Screening" for more information.

## MTR Single, Dual and Triple DC/DC Converters

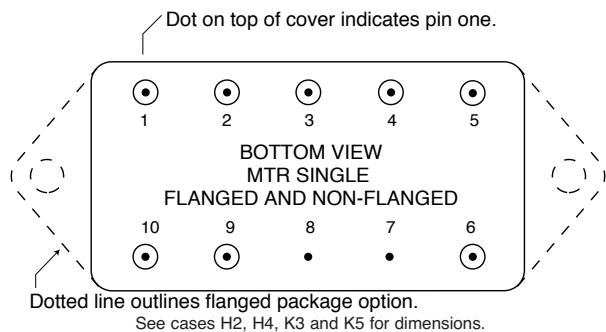
**28 VOLT INPUT – 30 WATT**

### PIN OUT

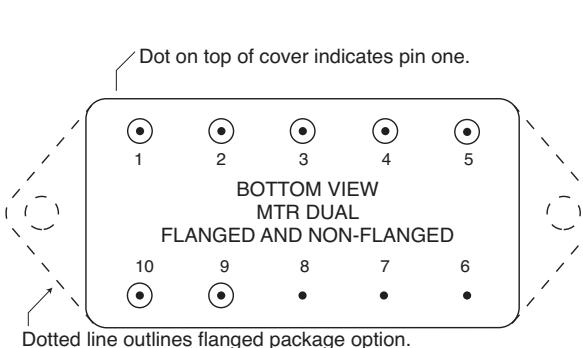
Pin	Single Output	Dual Output	Triple Output
1	Positive Input	Positive Input	Positive Input
2	Inhibit	Inhibit	Main (+5) Output
3	Sense Return	Positive Output	Output Common
4	Output Common	Output Common	Neg. Aux. Output
5	Positive Output	Negative Output	Pos. Aux. Output
6	Positive Sense	Case Ground	Case Ground
7	Case Ground	Case Ground	Case Ground
8	Case Ground	Case Ground	Inhibit
9	Sync	Sync	Sync
10	Input Common	Input Common	Input Common

### PINS NOT IN USE

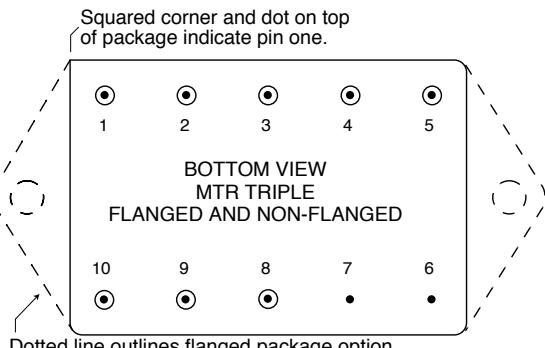
Inhibit	Leave unconnected
Sync In	Connect to input common
Sense Lines	Must be connected to appropriate outputs



**FIGURE 1: PIN OUT SINGLE OUTPUT MODELS**



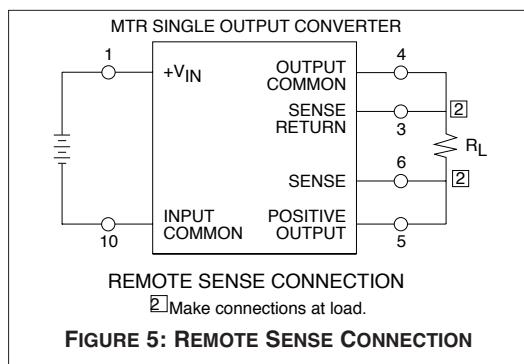
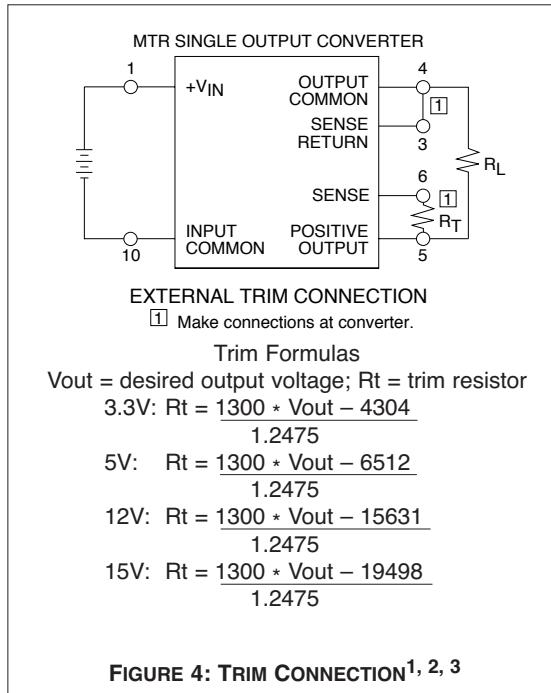
**FIGURE 2: PIN OUT DUAL OUTPUT MODELS**



**FIGURE 3: PIN OUT TRIPLE OUTPUT MODELS**

## MTR Single, Dual and Triple DC/DC Converters

### 28 VOLT INPUT – 30 WATT

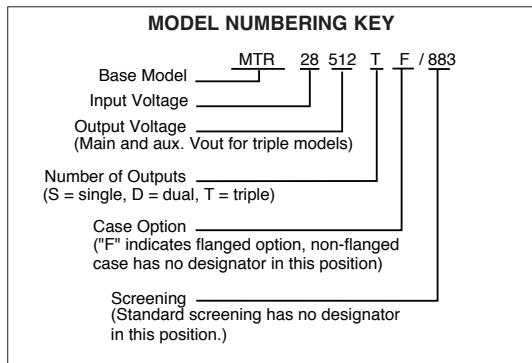


#### Notes for Remote Sense and Trim

1. When trimming output voltage and/or remote sensing, the total output voltage increase must be less than 0.6 volts at the converters pins to maintain specified performance.
2. If neither voltage trim nor remote sense will be used, connect pin 3 to pin 4 and pin 5 to pin 6 or the output voltage will increase by 1.2 volts.
3. CAUTION: The converter will be permanently damaged if the positive remote sense (pin 6) is shorted to ground. Damage may also result if the output common or positive output is disconnected from the load with the remote sense leads connected to the load.

## MTR Single, Dual and Triple DC/DC Converters

### 28 VOLT INPUT – 30 WATT



<b>SMD NUMBERS</b>	
<b>STANDARD MICROCIRCUIT DRAWING (SMD)</b>	<b>MTR SERIES SIMILAR PART</b>
5962-0150101HXC	MTR283R3S/883
5962-9306801HXC	MTR2805S/883
5962-9306901HXC	MTR2812S/883
5962-9307001HXC	MTR2815S/883
5962-9320201HXC	MTR2818S/883
5962-9320501HXC	MTR2805D/883
5962-9307101HXC	MTR2812D/883
5962-9307201HXC	MTR2815D/883
5962-9307301HXC	MTR28512T/883
5962-9307401HXC	MTR28515T/883

To indicate the flanged case option change the "X" to "Z" in the SMD number. The SMD number shown is for Class H screening, non-flanged. For exact specifications for an SMD product, refer to the SMD drawing. SMDs can be downloaded from:  
<http://www.dsccl.dla.mil/programs/smcr>

### Model Selection

#### MTR28

Base model    Vout value    number of outputs    case option    screening

Choose one from each of the following rows

<b>Vout value</b>	for singles or duals: 5, 12, or 15	for triples*: 512 or 515
-------------------	------------------------------------	--------------------------

<b>Number of outputs</b>	S (single)	D (dual)	or T (triple)
--------------------------	------------	----------	---------------

<b>Case option</b>	non-flanged case option, leave blank	F (flanged case option)
--------------------	--------------------------------------	-------------------------

<b>Screening</b>	standard screening, leave blank	/ES (ES screening), /883 (Class H, QML)
------------------	---------------------------------	---

\* for triple output models "5" indicates the main voltage, "12" or "15" indicate the ± auxiliary voltages.

## MTR Single, Dual and Triple DC/DC Converters

### 28 VOLT INPUT – 30 WATT

**Electrical Characteristics: 25°C Tc, 28 VDC Vin, 100% load, free run, unless otherwise specified.**

SINGLE OUTPUT MODELS		MTR283R3S			MTR2805S			MTR2812S			MTR2815S			MTR2818S			UNITS
PARAMETER	CONDITION	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
OUTPUT VOLTAGE		3.27	3.30	3.34	4.95	5.00	5.05	11.88	12.00	12.12	14.85	15.00	15.15	17.82	18.00	18.18	VDC
OUTPUT CURRENT <sup>2</sup>	V <sub>IN</sub> = 16 to 40 VDC	0	—	6.06	0	—	5.0	0	—	2.5	0	—	2.0	0	—	1.67	A
OUTPUT POWER <sup>2</sup>	V <sub>IN</sub> = 16 to 40 VDC	0	—	20	0	—	25	0	—	30	0	—	30	0	—	30	W
OUTPUT RIPPLE VOLTAGE	10 kHz – 2 MHz	—	15	40	—	35	50	—	25	40	—	25	40	—	—	40	mV p-p
VOLTAGE	Tc = -55°C TO +125°C	—	—	50	—	50	90	—	40	90	—	40	90	—	—	90	
LINE REGULATION <sup>3</sup>	Vin = 16 to 40 VDC	—	5	10	—	10	50	—	10	50	—	10	50	—	—	50	mV
	Tc = -55°C TO +125°C	—	—	10	—	15	50	—	15	50	—	15	50	—	—	50	
LOAD REGULATION	NO LOAD TO FULL	—	2	10	—	5	50	—	5	50	—	5	50	—	—	50	mV
	Tc = -55°C TO +125°C	—	—	10	—	15	50	—	15	50	—	15	50	—	—	50	
INPUT VOLTAGE <sup>2</sup>	CONTINUOUS	16	28	40	16	28	40	16	28	40	16	28	40	16	28	40	VDC
NO LOAD TO FULL	TRANSIENT 50 ms	—	—	50	—	—	50	—	—	50	—	—	50	—	—	50	V
INPUT CURRENT <sup>2</sup>	NO LOAD	—	30	75	—	35	75	—	35	75	—	35	75	—	—	75	mA
	INHIBITED	—	7	8	—	3	8	—	3	8	—	3	8	—	—	8	mA
INPUT RIPPLE CURRENT	10 kHz – 10 MHz	—	25	50	—	20	50	—	20	50	—	20	50	—	—	50	mA p-p
EFFICIENCY		74	76	—	76	78	—	80	83	—	81	84	—	81	84	—	%
LOAD FAULT <sup>4</sup>	SHORT CIRCUIT POWER DISSIPATION	—	10	—	—	10	—	—	10	—	—	10	—	—	10	W	
	RECOVERY <sup>1, 2, 5</sup>	—	1.4	6	—	1.4	5	—	1.4	5	—	1.4	5	—	1.4	5	ms
STEP LOAD RESP.	50% – 100% – 50% TRANSIENT	—	±125	±250	—	±200	±300	—	±250	±400	—	±350	±500	—	—	±600	mV pk
	RECOVERY <sup>1, 4</sup>	—	—	200	—	60	200	—	60	200	—	60	200	—	60	—	μs
STEP LINE RESP. <sup>1</sup>	16 – 40 – 16 VDC TRANSIENT <sup>6</sup>	—	—	±300	—	±200	±300	—	±400	±500	—	±500	±600	—	±500	—	mV pk
	RECOVERY <sup>5</sup>	—	—	300	—	—	300	—	—	300	—	—	300	—	300	—	μs
START-UP <sup>2, 7</sup>	DELAY	—	1.4	5	—	1.4	5	—	1.4	5	—	1.4	5	—	—	5	ms
	OVERSHOOT	—	0	50	—	0	50	—	0	120	—	0	150	—	0	—	mV pk
	FULL LOAD <sup>1</sup>	—	33	150	—	50	250	—	120	600	—	150	750	—	—	—	
CAPACITIVE LOAD <sup>1</sup>	NO EFFECT ON DC PERFORMANCE	—	—	300	—	—	300	—	—	3000	—	—	3000	—	—	2000	μF

#### Notes

1. Guaranteed, not tested.

2. Tc = -55°C to +125°C

3. Operation is limited below 16V (see Figure 22).

4. Indefinite short circuit protection not guaranteed above 125°C case.

5. Recovery time is measured from application of the transient to point at which Vout is within 1% of final value.

6. Transition time ≥10 μs.

7. Tested on release from inhibit.

## MTR Single, Dual and Triple DC/DC Converters

### 28 VOLT INPUT – 30 WATT

**Electrical Characteristics: 25°C Tc, 28 VDC Vin, 100% load, free run, unless otherwise specified.**

DUAL OUTPUT MODELS		MTR2805D			MTR2812D			MTR2815D			UNITS
PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
OUTPUT VOLTAGE	+V <sub>OUT</sub>	4.95	5.00	5.05	11.88	12.00	12.12	14.85	15.00	15.15	VDC
	-V <sub>OUT</sub>	4.92	5.00	5.08	11.82	12.00	12.18	14.77	15.00	15.23	
OUTPUT CURRENT <sup>2, 3</sup>	V <sub>IN</sub> = 16 TO 40 VDC	0	2.5	4.5	0	1.25	2.25	0	1.0	1.8	A
OUTPUT POWER <sup>2, 3</sup>	V <sub>IN</sub> = 16 TO 40 VDC	0	—	25	0	—	30	0	—	30	W
OUTPUT RIPPLE	10 kHz - 2 MHz	—	20	40	—	30	80	—	25	80	mV p-p
VOLTAGE +/- V <sub>OUT</sub>	Tc = -55°C TO +125°C	—	40	90	—	40	120	—	40	120	mV p-p
LINE REGULATION <sup>4</sup> V <sub>IN</sub> = 16 TO 40 VDC	+V <sub>OUT</sub>	—	10	50	—	10	50	—	10	50	mV
	-V <sub>OUT</sub>	—	50	100	—	50	150	—	50	180	
	Tc = -55°C	+V <sub>OUT</sub>	—	10	50	—	10	50	—	10	50
	TO +125°C	-V <sub>OUT</sub>	—	50	100	—	50	150	—	50	180
LOAD REGULATION NO LOAD TO FULL	+V <sub>OUT</sub>	—	5	50	—	15	50	—	15	50	mV
	-V <sub>OUT</sub>	—	25	100	—	30	150	—	30	180	
	Tc = -55°C	+V <sub>OUT</sub>	—	5	50	—	15	50	—	15	50
	TO +125°C	-V <sub>OUT</sub>	—	25	100	—	30	150	—	30	180
CROSS REGULATION <sup>1</sup>	SEE NOTE 5	—	7	12	—	4	8.3	—	3	8	%
EFFECT ON -V <sub>OUT</sub>	SEE NOTE 6	—	4	6	—	4	6	—	4	6	
INPUT VOLTAGE <sup>2</sup> NO LOAD TO FULL	CONTINUOUS	16	28	40	16	28	40	16	28	40	VDC
	TRANSIENT 50 ms	0	—	50	0	—	50	0	—	50	V
INPUT CURRENT	NO LOAD	—	35	75	—	50	75	—	50	75	mA
	INHIBITED	—	3	8	—	3	8	—	3	8	mA
INPUT RIPPLE CURRENT <sup>2</sup>	10 kHz - 10 MHz	—	15	50	—	20	50	—	20	50	mA p-p
EFFICIENCY		76	78	—	78	81	—	80	83	—	%
LOAD FAULT <sup>7</sup>	POWER DISSIPATION	—	10	—	—	10	—	—	10	—	W
	SHORT CIRCUIT <sup>2</sup>	—	1.4	5.0	—	1.4	5.0	—	1.4	5.0	ms
STEP LOAD RESPONSE ± V <sub>OUT</sub>	50 – 100 – 50% BALANCED TRANSIENT	—	±200	±300	—	±150	±300	—	±200	±400	mV pk
	RECOVERY <sup>1, 8</sup>	—	100	200	—	100	200	—	100	200	μs
STEP LINE <sup>1</sup> RESPONSE ± V <sub>OUT</sub>	16 – 40 – 16 V <sub>IN</sub> TRANSIENT <sup>9</sup>	—	±200	±400	—	±200	±400	—	±400	±500	mV pk
	RECOVERY <sup>8</sup>	—	—	300	—	—	300	—	—	300	μs
START-UP <sup>2, 10</sup>	DELAY	—	1.4	5	—	1.4	5	—	1.4	5	ms
	OVERSHOOT	—	0	50	—	0	120	—	0	150	mV pk
CAPACITIVE LOAD <sup>1</sup>	FULL LOAD <sup>1</sup>	—	—	500	—	—	500	—	—	500	
	NO LOAD <sup>1</sup>	—	50	250	—	120	600	—	150	750	μF
NO EFFECT ON DC PERFORMANCE		—	—	500	—	—	500	—	—	500	μF

Notes

1. Guaranteed, not tested.
2. Tc = -55°C to +125°C.
3. Up to 90% of the total output current/power is available from either output providing the positive output is carrying at least 10% of the total output power.
4. Operation is limited below 16 V (see Figure 22).
5. Effect on negative Vout from 50%/50% loads to 80%/20% or 20%/80% loads.
6. Effect on negative Vout from 50%/50% loads to 90%/10% or 10%/90% loads.
7. Indefinite short circuit protection not guaranteed above 125°C case.
8. Recovery time is measured from application of the transient to point at which Vout is within 1% of final value.
9. Transition time ≥ 10 μs.
10. Tested on release from inhibit.

## MTR Single, Dual and Triple DC/DC Converters

### 28 VOLT INPUT – 30 WATT

**Electrical Characteristics: 25°C Tc, 28 VDC Vin, 100% load, free run, unless otherwise specified.**

TRIPLE OUTPUT MODELS		MTR28512T			MTR28515T			UNITS
PARAMETER	CONDITION	MIN	TYP	MAX	MIN	TYP	MAX	
OUTPUT VOLTAGE	MAIN	4.95	5.0	5.05	4.95	5.0	5.05	VDC
	+ AUXILIARY	11.82	12.0	12.18	14.77	15.0	15.23	
	- AUXILIARY	11.82	12.0	12.18	14.77	15.0	15.23	
OUTPUT CURRENT <sup>2</sup> V <sub>IN</sub> = 16 TO 40	MAIN	0.3	—	4.0	0.3	—	4.0	A
	+ AUXILIARY	—	0.416	0.750	—	0.333	0.600	
	- AUXILIARY	—	0.416	0.750	—	0.333	0.600	
OUTPUT POWER <sup>2</sup> V <sub>IN</sub> = 16 TO 40	MAIN	—	20	20	—	20	20	W
	+ AUXILIARY	—	5	9	—	5	9	
	- AUXILIARY	—	5	9	—	5	9	
	TOTAL	—	—	30	—	—	30	
OUTPUT RIPPLE VOLTAGE	10 kHz to 2 MHz	MAIN	—	50	125	—	50	125
	± AUXILIARY	—	20	60	—	20	60	mV p-p
LINE REGULATION V <sub>IN</sub> = 16 TO 40	MAIN	—	10	20	—	10	20	mV
	± AUXILIARY	—	25	75	—	30	75	
LOAD REGULATION <sup>3, 4</sup>	MAIN	—	10	50	—	10	50	mV
	± AUXILIARY	—	30	75	—	30	75	
INPUT VOLTAGE	CONTINUOUS	16	28	40	16	28	40	VDC
	TRANSIENT 50 ms	—	—	50	—	—	50	
INPUT CURRENT	NO LOAD	—	70	100	—	70	120	mA
	INHIBITED	—	3.0	6	—	3.0	6	
INPUT RIPPLE CURRENT	10 kHz TO 10 MHz	—	20	45	—	20	45	mA p-p
EFFICIENCY		72	75	—	73	75	—	%
LOAD FAULT <sup>5</sup>	POWER DISSIPATION SHORT CIRCUIT							
	ALL OUTPUTS SHORTED TOTAL	—	14	—	—	14	—	W
STEP LOAD RESPONSE	RECOVERY EACH OUTPUT <sup>1</sup>	—	4	6.0	—	4	6.0	ms
	TRANSIENT <sup>6</sup>	MAIN	—	150	250	—	150	250
		± AUXILIARY	—	500	800	—	500	800
	RECOVERY <sup>7</sup>	MAIN	—	0.05	0.10	—	0.05	0.10
		± AUXILIARY	—	3	4	—	2	4
STEP LINE RESPONSE <sup>1</sup> V <sub>IN</sub> = 16 TO 40	TRANSIENT	MAIN	—	150	250	—	150	250
		± AUXILIARY	—	100	250	—	100	250
START-UP <sup>8</sup>	DELAY	—	4	6.0	—	4	6.0	ms
	OVERSHOOT	MAIN <sup>1</sup>	—	0	500	—	0	500
	± AUXILIARY <sup>1</sup>	—	0	1500	—	0	1500	mV

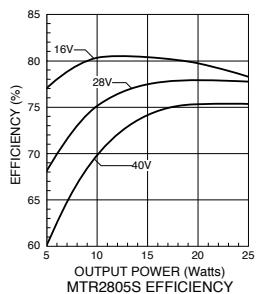
#### Notes

- Guaranteed, not tested.**
- The sum of the two aux outputs is not to exceed 10 watts. The maximum load per aux output is 9 watts.
- To maintain regulation when operating the ±Aux at full load, a minimum load of 300 mA is required on the main.
- Measured on each output one at a time with the other outputs at full load.
- Indefinite short circuit protection not guaranteed above 125°C (case).
- Response of each output as all outputs are simultaneously transitioned.  
Main: 50% - 100% - 50% of main full load  
Auxiliaries: 25% - 50% - 25% each, of total auxiliary full load
- Recovery time is measured from application of the transient to point at which Vout is within 1% of regulation.
- Tested on release from inhibit.

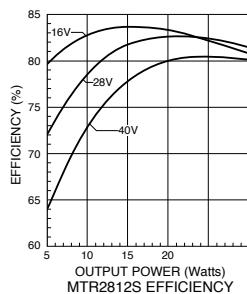
## MTR Single, Dual and Triple DC/DC Converters

### 28 VOLT INPUT – 30 WATT

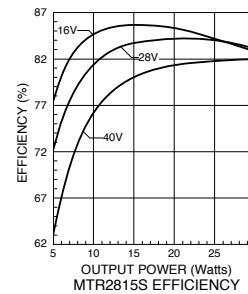
Typical Performance Curves: 25°C Tc, 28 VDC Vin, 100% load, free run, unless otherwise specified.



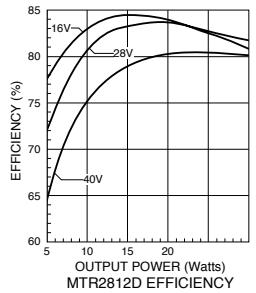
**FIGURE 6**



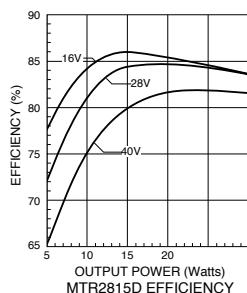
**FIGURE 7**



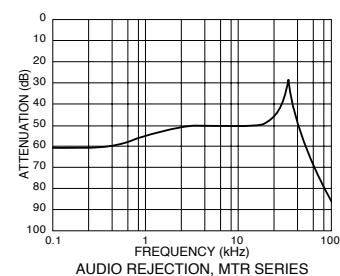
**FIGURE 8**



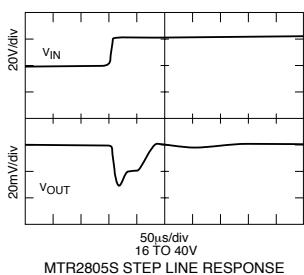
**FIGURE 9**



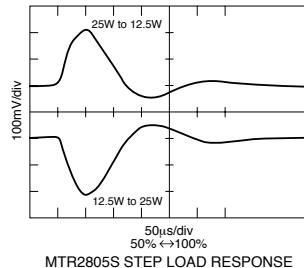
**FIGURE 10**



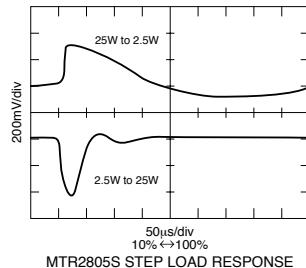
**FIGURE 11**



**FIGURE 12**



**FIGURE 13**



**FIGURE 14**

## MTR Single, Dual and Triple DC/DC Converters

### 28 VOLT INPUT – 30 WATT

Typical Performance Curves: 25°C Tc, 28 VDC Vin, 100% load, free run, unless otherwise specified.

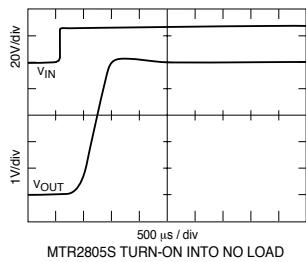


FIGURE 15

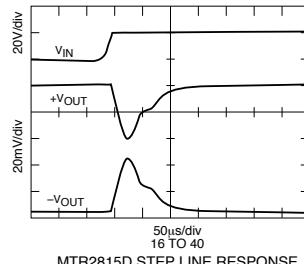


FIGURE 16

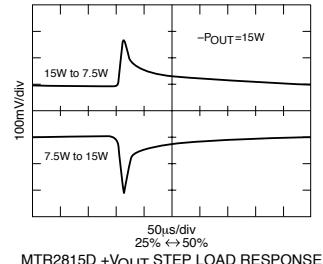


FIGURE 17

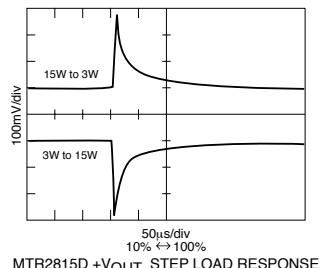


FIGURE 18

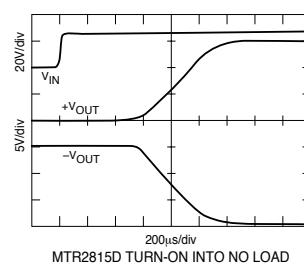


FIGURE 19

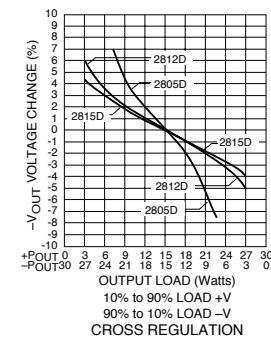


FIGURE 20

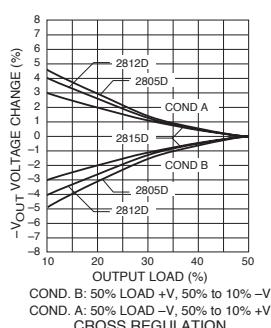


FIGURE 21

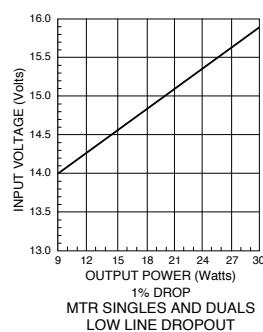


FIGURE 22

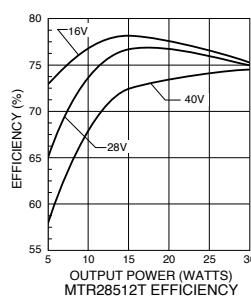


FIGURE 23

## MTR Single, Dual and Triple DC/DC Converters

### 28 VOLT INPUT – 30 WATT

Typical Performance Curves: 25°C Tc, 28 VDC Vin, 100% load, free run, unless otherwise specified.

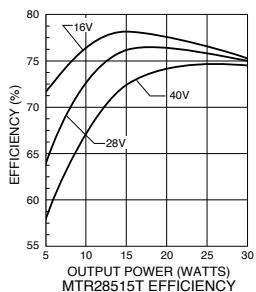


FIGURE 24

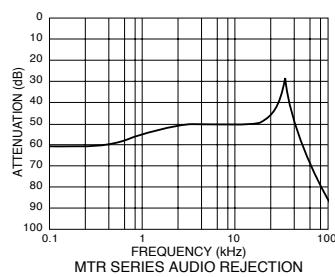


FIGURE 25

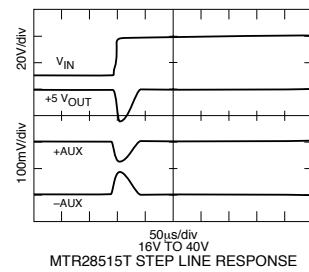


FIGURE 26

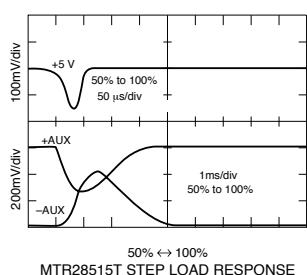


FIGURE 27

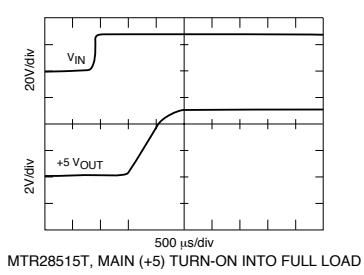


FIGURE 28

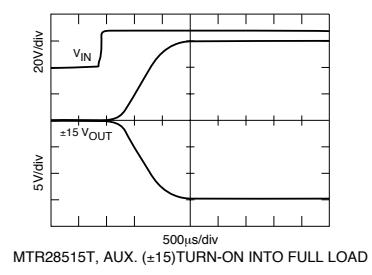


FIGURE 29

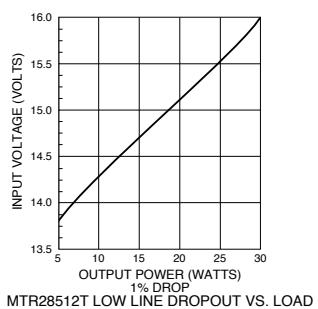


FIGURE 30

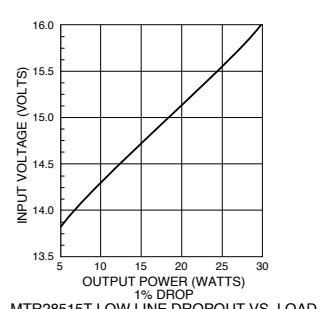
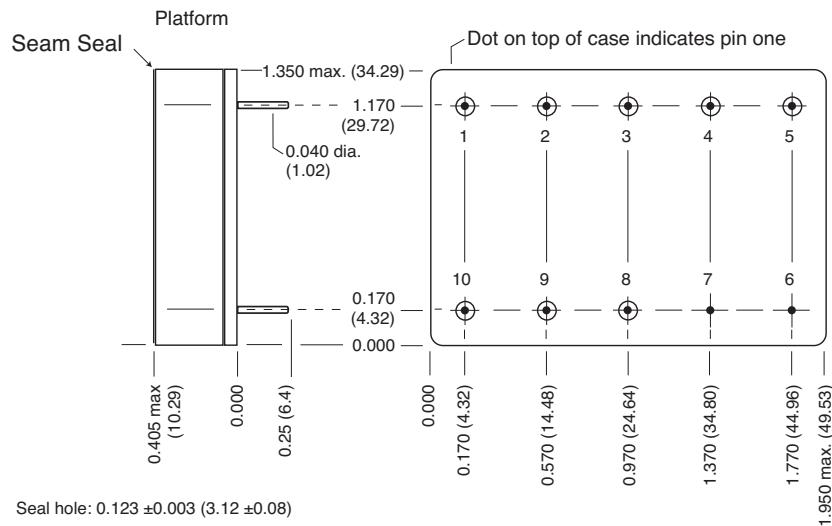


FIGURE 31

## MTR Single, Dual and Triple DC/DC Converter Cases

### 28 VOLT INPUT – 30 WATT

BOTTOM VIEW CASE F1



**Case dimensions in inches (mm)**

Tolerance  $\pm 0.005$  (0.13) for three decimal places  
 $\pm 0.01$  (0.3) for two decimal places  
unless otherwise specified

**CAUTION**

Heat from reflow or wave soldering may damage the device.  
Solder pins individually with heat application not exceeding 300°C for 10 seconds per pin.

**Materials**

Header Cold Rolled Steel/Nickel/Gold  
Cover Kovar/Nickel  
Pins #52 alloy/Gold ceramic seal

Case F1, Rev C, 20051216

Please refer to the numerical dimensions for accuracy. All information is believed to be accurate, but no responsibility is assumed for errors or omissions. Interpoint reserves the right to make changes in products or specifications without notice.

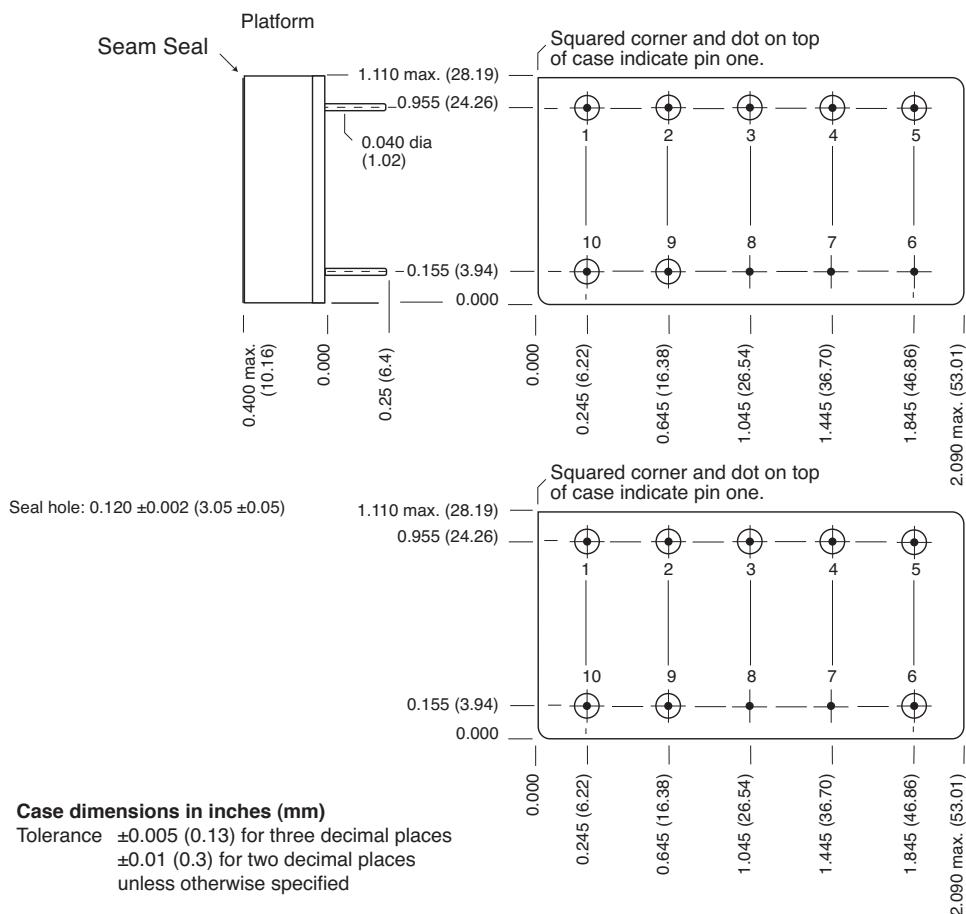
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**FIGURE 32: CASE F1 – TRIPLE MODELS**

## MTR Single, Dual and Triple DC/DC Converter Cases

### 28 VOLT INPUT – 30 WATT

#### BOTTOM VIEW CASE H2



#### CAUTION

Heat from reflow or wave soldering may damage the device.  
 Solder pins individually with heat application not exceeding 300°C for 10 seconds per pin.

#### Materials

Header Cold Rolled Steel/Nickel/Gold  
 Cover Kovar/Nickel  
 Pins #52 alloy/Gold ceramic seal

Case H2, Rev C - 20060109

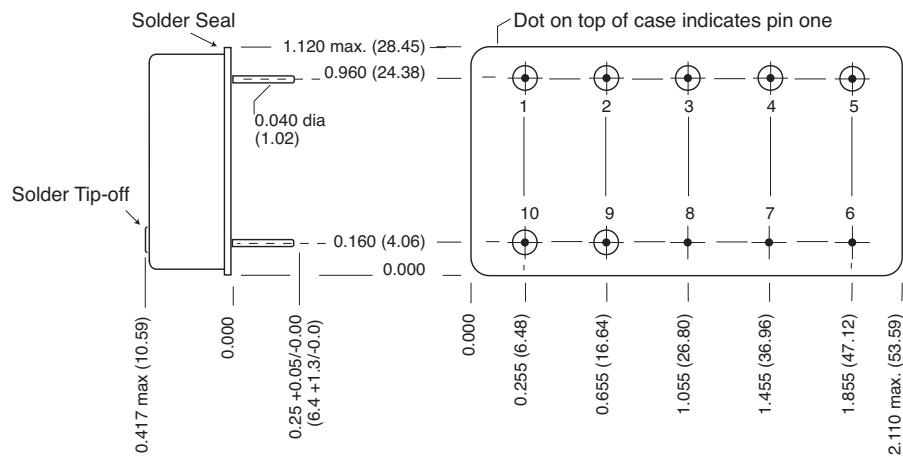
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**FIGURE 33: CASE H2 – DUAL MODELS**

## MTR Single, Dual and Triple DC/DC Converter Cases

### 28 VOLT INPUT – 30 WATT

BOTTOM VIEW CASE H4



Seal hole:  $0.091 \pm 0.005$  (2.31  $\pm 0.13$ )

#### Case dimensions in inches (mm)

Tolerance  $\pm 0.005$  (0.13) for three decimal places  
 $\pm 0.01$  (0.3) for two decimal places  
unless otherwise specified

#### CAUTION

Heat from reflow or wave soldering may damage the device.  
Solder pins individually with heat application not exceeding 300°C for 10 seconds per pin.

#### Materials

Header Cold Rolled Steel/Nickel/Tin  
Cover Cold Rolled Steel/Nickel/Tin  
Pins #52 alloy compression glass seal

Case H4, Rev C - 20060110

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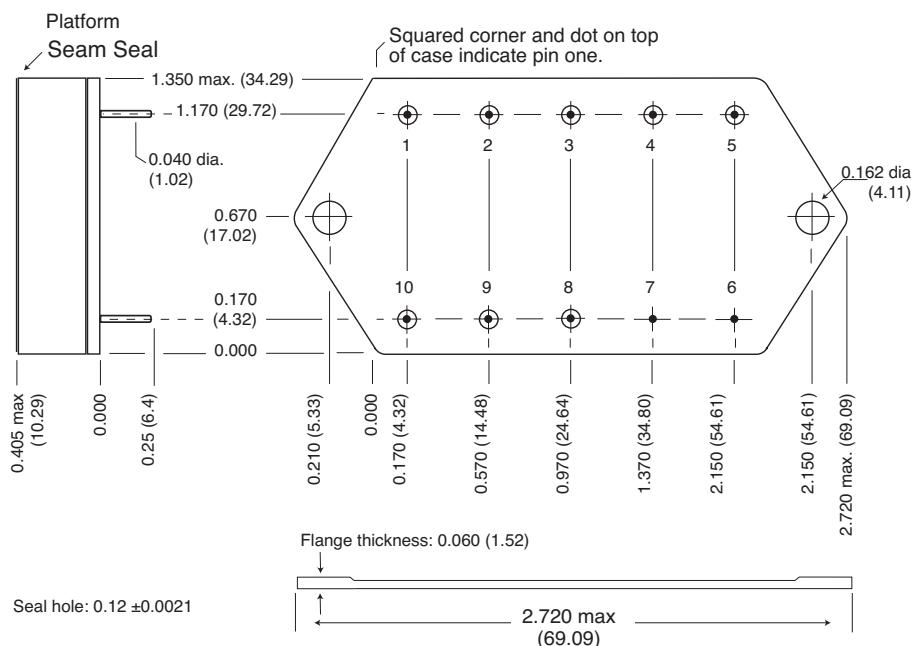
**FIGURE 34: CASE H4 – DUAL MODELS**

## MTR Single, Dual and Triple DC/DC Converter Cases

### 28 VOLT INPUT – 30 WATT

#### BOTTOM VIEW CASE J1

Flanged cases: Designator "F" required in Case Option position of model number.



#### Case dimensions in inches (mm)

Tolerance ±0.005 (0.13) for three decimal places  
 ±0.01 (0.3) for two decimal places  
 unless otherwise specified

#### CAUTION

Heat from reflow or wave soldering may damage the device.  
 Solder pins individually with heat application not exceeding 300°C for 10 seconds per pin.

#### Materials

Header Cold Rolled Steel/Nickel/Gold  
 Cover Kovar/Nickel  
 Pins #52 alloy/Gold ceramic seal

Case J1, Rev C, 20060109 MHV only.  
 Please refer to the numerical dimensions for accuracy. All information is believed to be accurate, but no responsibility is assumed for errors or omissions. Interpoint reserves the right to make changes in products or specifications without notice.  
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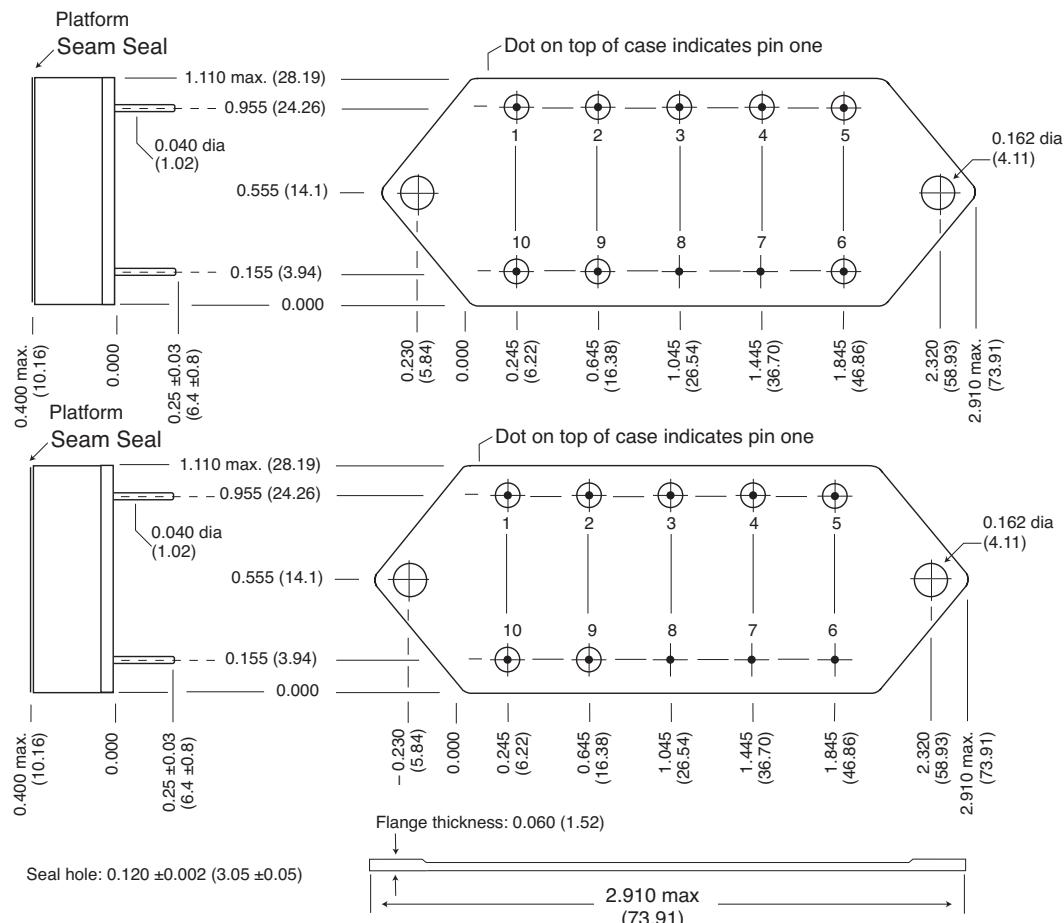
FIGURE 35: CASE J1 – TRIPLE MODELS

## MTR Single, Dual and Triple DC/DC Converter Cases

### 28 VOLT INPUT – 30 WATT

#### BOTTOM VIEW CASE K3

Flanged cases: Designator "F" required in Case Option position of model number.



#### Case dimensions in inches (mm)

Tolerance ±0.005 (0.13) for three decimal places  
 ±0.01 (0.3) for two decimal places  
 unless otherwise specified

#### Materials

Header Cold Rolled Steel/Nickel/Gold  
 Cover Kovar/Nickel  
 Pins #52 alloy/Gold ceramic seal

#### CAUTION

Heat from reflow or wave soldering may damage the device.  
 Solder pins individually with heat application not exceeding  
 300°C for 10 seconds per pin.

Case K3, Rev C, 20060110

Please refer to the numerical dimensions for accuracy.

All information is believed to be accurate, but no responsibility is assumed for errors or omissions.

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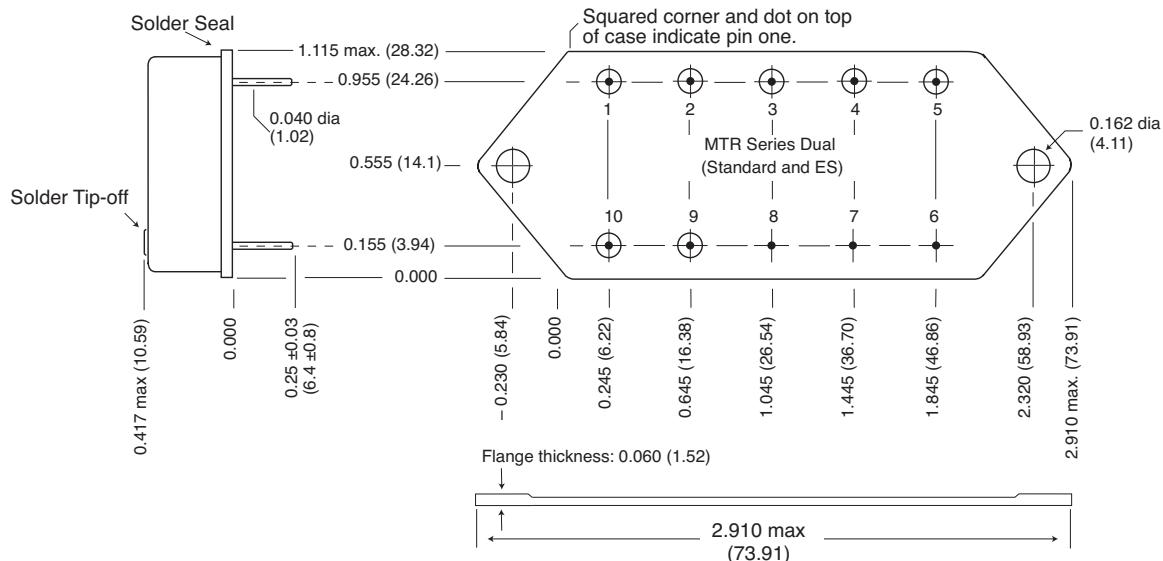
**FIGURE 36: CASE K3 – SINGLE MODELS**

## MTR Single, Dual and Triple DC/DC Converter Cases

### 28 VOLT INPUT – 30 WATT

#### BOTTOM VIEW CASE K5

Flanged cases: Designator "F" required in Case Option position of model number.



Seal hole:  $0.091 \pm 0.001$  (2.31 ± 0.03)

#### Case dimensions in inches (mm)

Tolerance  $\pm 0.005$  (0.13) for three decimal places  
 $\pm 0.01$  (0.3) for two decimal places  
unless otherwise specified

#### CAUTION

Heat from reflow or wave soldering may damage the device.  
Solder pins individually with heat application not exceeding 300°C for 10 seconds per pin.

#### Materials

Header Cold Rolled Steel/Nickel/Tin  
Cover Cold Rolled Steel/Nickel/Tin  
Pins #52 alloy compression glass seal

Case K3, Rev C, 20060109

Please refer to the numerical dimensions for accuracy. All information is believed to be accurate, but no responsibility is assumed for errors or omissions. Interpoint reserves the right to make changes in products or specifications without notice.  
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FIGURE 37: CASE K5 – SINGLE MODELS

## MTR Single, Dual and Triple DC/DC Converters

**28 VOLT INPUT – 30 WATT**

### 883, CLASS H, QML PRODUCTS – ELEMENT EVALUATION

TEST PERFORMED (COMPONENT LEVEL)	ELEMENT EVALUATION		CLASS H, QML	
	STANDARD (NON-QML) <sup>1</sup> M/S <sup>2</sup>	P <sup>3</sup>	M/S <sup>2</sup>	P <sup>3</sup>
Element Electrical (probe)	yes	no	yes	yes
Element Visual	no	no	yes	yes
Internal Visual	no	no	yes	no
Final Electrical	no	no	yes	yes
Wire Bond Evaluation <sup>4</sup>	no	no	yes	yes
SLAM™/C-SAM: Input Capacitors only (Add'l test, not req. by H or K)	no	no	no	yes

#### Definitions:

Element Evaluation: Component testing/screening per MIL-STD-883 as determined by MIL-PRF-38534

SLAM™: Scanning Laser Acoustic Microscopy

C-SAM: C - Mode Scanning Acoustic Microscopy

#### Notes:

1. Non-QML products do no meet all of the requirements of MIL-PRF-38534
2. M/S = Active components (Microcircuit and Semiconductor Die)
3. P = Passive components
4. Not applicable to EMI filters that have no wire bonds

## MTR Single, Dual and Triple DC/DC Converters

**28 VOLT INPUT – 30 WATT**

# 883, CLASS H, QML PRODUCTS – ENVIRONMENTAL SCREENING

TEST	125°C STANDARD non-QML	125°C /ES non-QML	Class H /883 QML
Pre-cap Inspection Method 2017, 2032	yes	yes	yes
Temperature Cycle (10 times) Method 1010, Cond. C, -65°C to 150°C, ambient Method 1010, Cond. B, -55°C to 125°C, ambient	no no	no yes	yes no
Constant Acceleration Method 2001, 3000 g Method 2001, 500g	no no	no yes	yes no
Burn-In Method 1015, 160 hours at 125°C case, typical 96 hours at 125°C case, typical	no no	no yes	yes no
Final Electrical Test MIL-PRF-38534, Group A Subgroups 1 through 6: -55°C, +25°C, +125°C case Subgroups 1 and 4: +25°C case	no yes	no yes	yes no
Hermeticity Test Fine Leak, Method 1014, Cond. A Gross Leak, Method 1014, Cond. C Gross Leak, Dip ( $1 \times 10^{-3}$ )	no no yes	yes yes no	yes yes no
Final Visual Inspection Method 2009	yes	yes	yes

Test methods are referenced to MIL-STD-883 as determined by MIL-PRF-38534.

## **Appendix E:**

### **SEA Design / Reference Information**

#### **Design Information Summary:**

Drawing SC531083:

Reference Schematic Diagram: Power Supply

The part referenced is MTR28515TF DC/DC converter (U2)

The DC/DC converter in question is located in both SEA-A and SEA-B.

The DC/DC converter in question provides regulated +5V, +15V, -15V, and Bilevel voltages to the SEA. These voltages are used by the SEA internally.

The SEA power is not cross-strapped.

#### **Telemetry Points of Interest:**

3SDP5V      +5V

3SDP15V      +15V

3SDM15V      -15V

#### **FMEA References (PA02, Vol.1, 29 Aug 97)**

Item 1.9.01, Loss of all SEA outputs [due to failure power supply or processor]

Item 1.9.01.01c, Overvoltage on secondary power output (+/- 15V) [failure in DC/DC converter]

Common response: Switch to redundant SEA via Ground Command

#### **Also reference IN0071-301:**

Failure Modes and Effects Analysis for AXAF SIM: Rev D: 14 February 1997:

Appendix A: SEA Power Supply

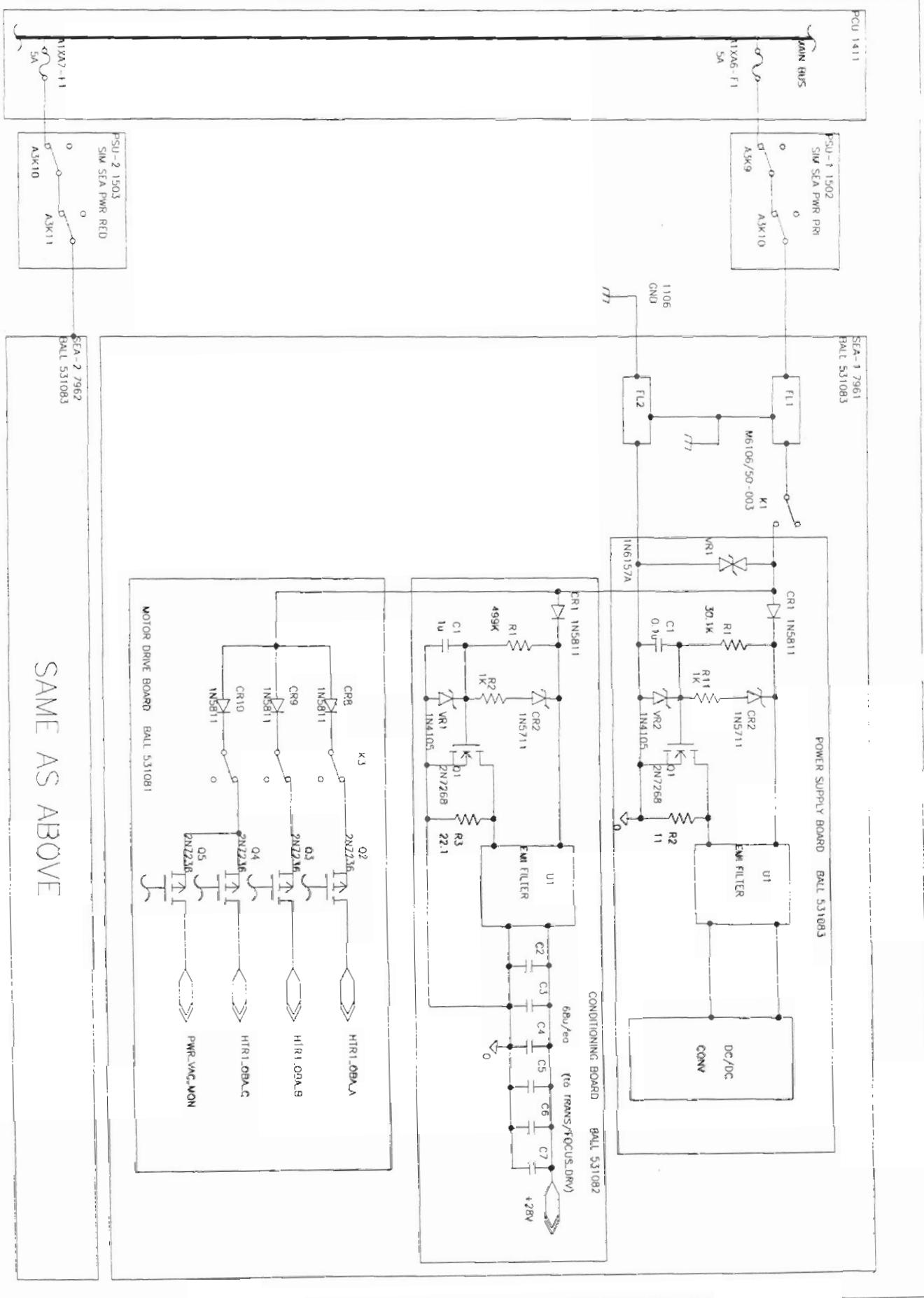
Pages of note are A-1, A-2, A-3, A-4, A-8, A-9

Failure of the DC/DC power converter would result in a failure of the SEA; a swap to the redundant SEA would be necessary to resume operations.

#### **SE14b – Schematics & List, Electrical Diagrams, Vol. 1, Book 1 – System Interface:**

SEA Schematic excerpt in following figure

**Figure 1:** SEA Schematic



SIMPWR001, CLD

SAME AS ABOVE

## **Appendix F:**

### **PEA Design / Reference Information**

#### **Design Information Summary:**

The DC/DC converter in question provides regulated +5V, +15V, -15V voltages in the PEA. These voltages are used by the PEA internally and the Aspect Camera head.

The PEA power is not cross-strapped

The Flip Mirror is not powered via this converter

#### **Telemetry Points of Interest:**

ACV\_PPV    +5V

ACV\_P15V    +15V

ACV\_N15V    -15V

AAPSF       Power Supply Failure Flag

#### **FMEA References (PA02, Vol.1, 29 Aug 97)**

Item 1.1.12a, Loss of Star Data [due to failure of Aspect Camera electronics or PEA]

Item 1.1.12c, Overvoltage in power converter [failure in power converter control logic]

Common response: Switch to redundant ACA focal plane assembly and electronics (includes activation of flip mirror assembly)

#### **SE14b – Schematics & List, Electrical Diagrams, Vol. 1, Book 1 – System**

**Interface:**

**PEA Schematic excerpt in following figure**

**Figure 1:** PEA Schematic

PCU 1411

MAIN BUS

PEA-1 6211  
BALL 531784

N1X012-F5  
2A

K1  
FL1  
EN/DIS  
CR1 1N5811  
VR1  
1N6157A  
R1  
66.5K  
CR2  
1N5711  
C1  
0.1uF  
R11  
1K  
2N7268  
R2  
11  
IN4105

1106  
GND  
r7  
FL2  
EN/DIS  
CR1 1N5811  
VR1  
1N6157A  
R1  
66.5K  
CR2  
1N5711  
C1  
0.1uF  
R11  
1K  
2N7268  
R2  
11  
IN4105

U1  
FILTER  
ON/OFF  
Q2  
2N6990  
CONV

U1  
FILTER  
ON/OFF  
Q2  
2N6990  
CONV

PEA-2 6212  
BALL 531784  
K1  
FL1  
FL2  
EN/DIS  
CR1 1N5811  
VR1  
1N6157A  
R1  
66.5K  
CR2  
1N5711  
C1  
0.1uF  
R11  
1K  
2N7268  
R2  
11  
IN4105

PEAPWR001, CLD

## **Appendix G:**

### **EIO Design / Reference Information**

Design Information Summary:

The DC/DC converter in question provides regulated +5V, +15V, -15V voltages in the EIO. These voltages are used by the EIO internally and the EPHIN unit

There are redundant wires for each output voltage, but only a single power converter (nonredundant)

Telemetry Points of Interest:

5HSE201      +5V

FMEA References (PA02, Vol.1, 29 Aug 97)

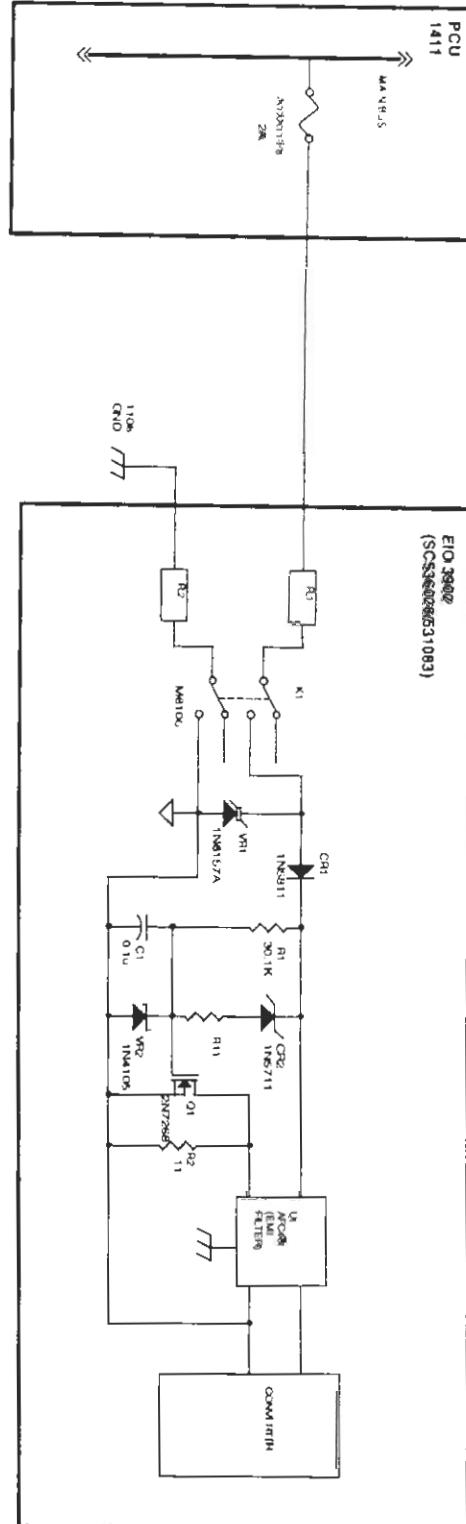
Item 1.10.02a.01, Loss of power to the EPHIN [due to failure of the DC-DC converter (all voltages), a linear reg. (for low level voltages), or a switching reg. (for +27VDC)]

Response: Use of external data sources to warn of high radiation events, or switch to use of HRC data as a replacement for EPHIN data in RadMon process

SE14b – Schematics & List, Electrical Diagrams, Vol. 1, Book 1 – System Interface:

EIO Schematic excerpt in following figure

**Figure 1:** EIO Schematic



EDBWR001.CLD

## **Appendix H:**

### **HRC Design / Reference Information**

#### **Design Information Summary:**

Interpoint converters used in HRC; both A & B sides contain:

MTR 2805SF +5V

MTR 2812SF +12V (two of these are stacked to get +24V)

MTR 2815DF +15V

A failure of any one of these would result in the loss of the A-side of the instrument; resulting in a switch to the B-side to continue HRC operations

#### **Telemetry Points of Interest:**

2C05PALV +5V monitor

2C15NALV +15V monitor

2C15PALV -15V monitor

2C24PALV +24V monitor

#### **FMEA References (PA02, Vol.1, 29 Aug 97)**

Failure of power supplies themselves not directly considered; potentially the same as failure in switching circuits (e.g., Item 1.12.04.01a, CEA LVPS fails to turn ON [due to failure of the LVPS soft switch or the command circuit in the RCTU])

Response: Switch to the B-side and continue HRC operations