Lab 1 – 3-input Majority Gate

EE 238 Digital Systems Design

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Help received: I googled some HTML syntax

# Problem statement

The purpose of this lab is to design, implement, and test a 3-input majority gate using TTL chips. A majority gate is a combinational logic circuit where the output is equal to the majority value of the inputs – if more than half of the inputs are 1, then the output is 1. If more than half of the inputs are 0, the output is 0.

# Design procedure

The truth table for a 3-input majority gate was derived as shown below. The output is a 1 whenever 2 or 3 of the inputs are 1; otherwise, the output is 0.

Table 1: Truth table for 3-input majority gate

|  |  |  |  |
| --- | --- | --- | --- |
| a | b | c | y |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 |

Using the design techniques for combinational logic, a Karnaugh map was drawn, prime implicants were identified, and a Boolean equation was determined.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| A BC | 00 | 01 | 11 | 10 |
| 0 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 1 | 1 |

Figure 1: Karnaugh map and Boolean equation for majority gate

The Boolean equation was translated into the following circuit diagram, using AND and OR gates.

Diagram

Description automatically generated

Figure 2: Circuit diagram for majority gate

This circuit was then translated into a circuit using only NAND gates for implementation.

Diagram

Description automatically generated

Figure 3: Circuit diagram using NAND gates

Since the circuit requires three 2-input NAND gates and one 3-input NAND gate, it can be implemented using a 74HC00 quad 2-input NAND [1] and a 74HC10 triple 3-input NAND [2].

Referencing the pinout diagrams for the 74HC00 and 74HC10 <ADD REFERENCES!>, the following pin assignments were made:

Diagram

Description automatically generated

Figure 4: Circuit diagram showing pin assignments

A Fritzing diagram was then created to show the layout and wiring of the 74HC00 and 74HC10.

A picture containing diagram

Description automatically generated

Figure 5: Fritzing diagram showing circuit layout

The circuit was constructed on the protoboard, using switches S1, S2, and S3 for the inputs a, b, and c, and using one channel of the 8-channel Logic Monitor for the output y.

## Testing procedure

Since this circuit is a combinational logic design with 3 inputs, an exhaustive testing was performed of all 8 possible input combinations. The resulting output values were recorded, as shown in the Results section below.

We iterated throughout all 8 possible combinations of the switches and verified that the circuit showed a 1 when expected and showed a 0 when expected.

# Results

The following outputs were recorded for each of the input tests:

Table 2: Observed circuit outputs

|  |  |  |  |
| --- | --- | --- | --- |
| a | b | c | y |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 |

The output of the circuit matches the design specification, indicating the design and implementation are correct.

# Works Cited

|  |  |
| --- | --- |
| [1] | Fairchild Semiconductor, "74HC00 - 74HC00 Quad 2-input NAND Gate Datasheet," January 2005. [Online]. Available: https://www.futurlec.com/74HC/74HC00.shtml. [Accessed 25 August 2022]. |
| [2] | Phillips Semiconductors, "74HC10 - 74HC10 Triple 3-input NAND Gate Datasheet," December 1990. [Online]. Available: https://www.futurlec.com/74HC/74HC10.shtml. [Accessed 25 August 2022]. |