Hw 1 40243118S 王擎天

1. 設計電路說明(20%):

這次的電路主要透過signal S來決定要進行的運算功能為何.若singal S為00,則將signal A,B,C做AND運算.若singal S為01,則計算signal A,B,C中最小的數為何.若singal S為10,則將signal A,B乘起來.若singal S為11,則將signal A,C加起來.上述所有的運算結果將存到signal Y.

2. 程式碼說明(30%):

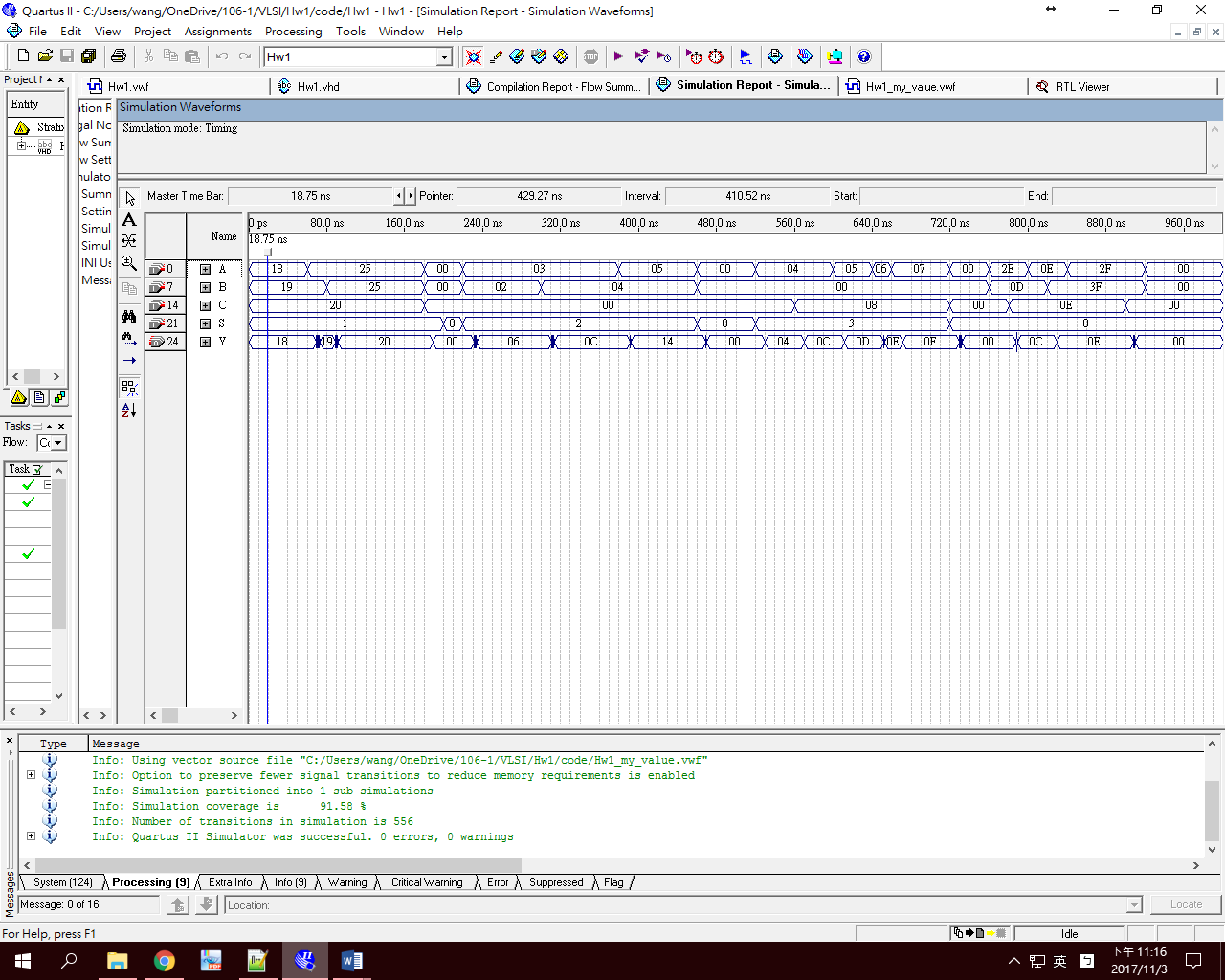
我先將所有輸入和輸出signal連接到各自對應的variable. Mode 1我寫了一個procedure算出兩個variable的AND運算,並用它將三個variable的值用AND運算.Mode 2我寫了一個procedure算出兩個variable的最小值,並用它將三個variable的最小值.Mode 3我將signal A的後三個bit和signal B的後三個bit乘起來後存到signal Y. Mode 4直接將signal A, signal C兩數加起來存到signal Y.

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| library IEEE;  use IEEE.numeric\_std.all;  use ieee.std\_logic\_1164.all;  ENTITY Hw1 IS  PORT(  A,B,C:IN unsigned(5 DOWNTO 0);  Y:OUT unsigned(5 DOWNTO 0);  S:IN unsigned(1 DOWNTO 0)  );  END Hw1;  ARCHITECTURE Hw1\_arch OF Hw1 IS  PROCEDURE min(VARIABLE lhs,rhs :IN unsigned(5 DOWNTO 0);  VARIABLE output :OUT unsigned(5 DOWNTO 0))IS  BEGIN  IF lhs>rhs THEN  output:=rhs;  ELSE  output:=lhs;  END IF;  END min;    PROCEDURE vector\_and(VARIABLE lhs,rhs:IN unsigned(5 DOWNTO 0);  VARIABLE output:OUT unsigned(5 DOWNTO 0))IS  BEGIN  output:=unsigned(std\_logic\_vector(lhs) and std\_logic\_vector(rhs));  END vector\_and;  BEGIN  PROCESS(A,B,C,S)  VARIABLE temp,temp2: unsigned(5 DOWNTO 0);  VARIABLE v\_A,v\_B,v\_C,v\_Y: unsigned(5 DOWNTO 0);  BEGIN  temp:="000000";  v\_A:=A;  v\_B:=B;  v\_C:=C;  IF s="00" THEN  vector\_and(lhs=>v\_A,rhs=>v\_B,output=>temp);  vector\_and(lhs=>temp,rhs=>v\_C,output=>v\_Y);  Y<=v\_Y;  ELSIF S="01" THEN  min(lhs=>v\_A,rhs=>v\_B,output=>temp);  min(lhs=>temp,rhs=>v\_C,output=>v\_Y);  Y<=v\_Y;  ELSIF S="10" THEN  Y<=A(2 DOWNTO 0)\*B(2 DOWNTO 0);  ELSE  Y<=A+C;  END IF;  END PROCESS;    END Hw1\_arch; |

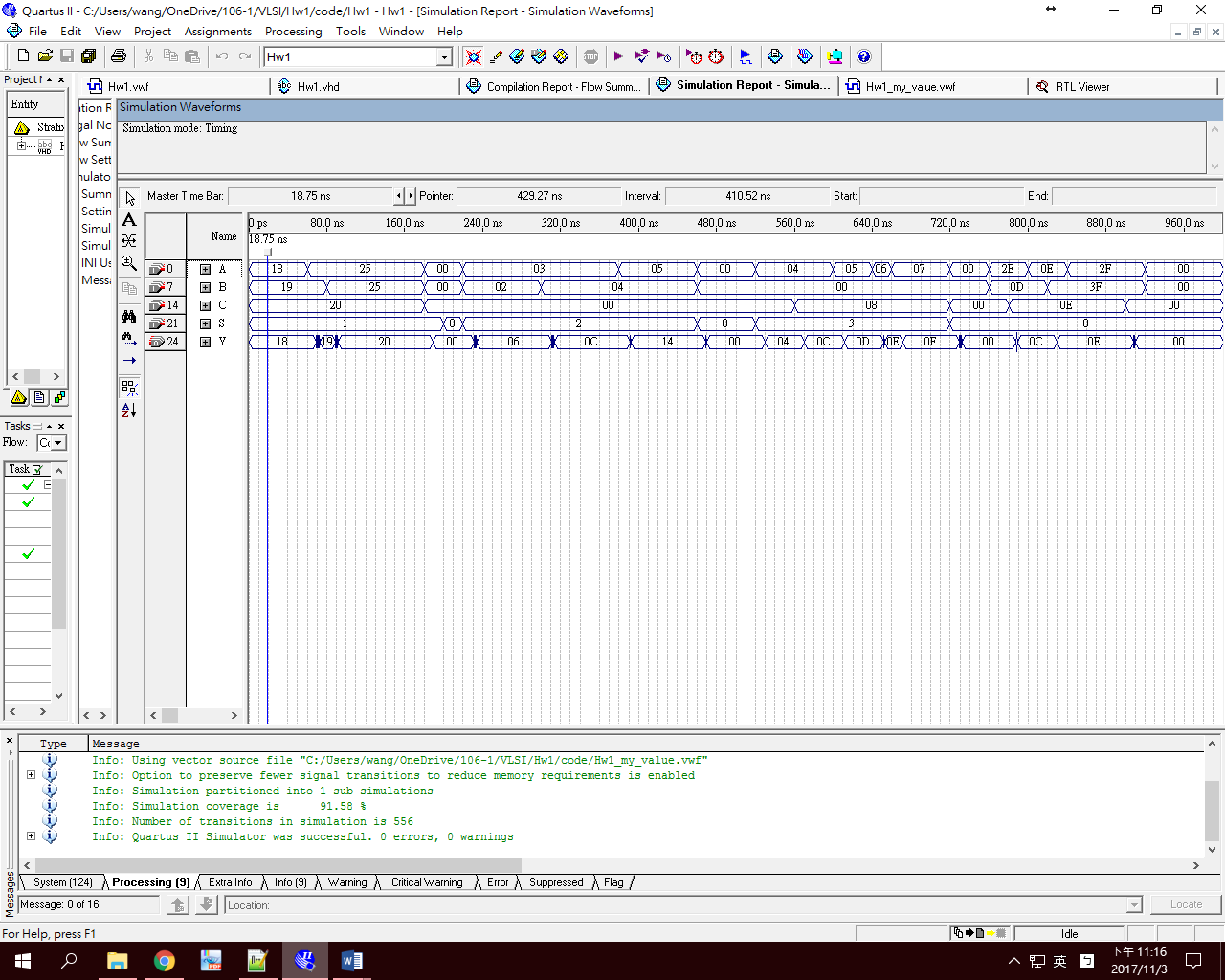
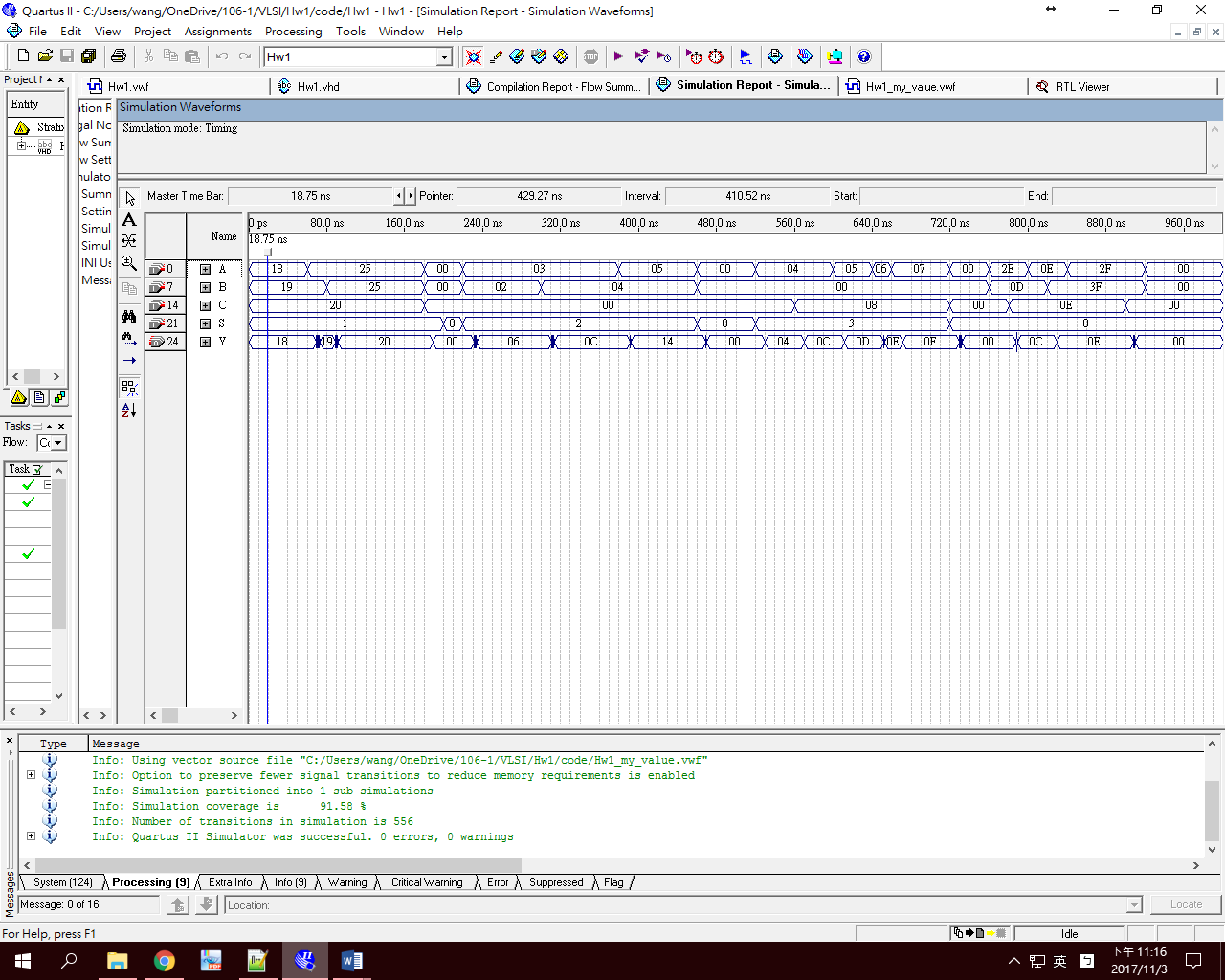
3. 模擬結果說明(30%):

由下圖可以看出VHDL的結果模擬圖所顯示的答案是正確的.

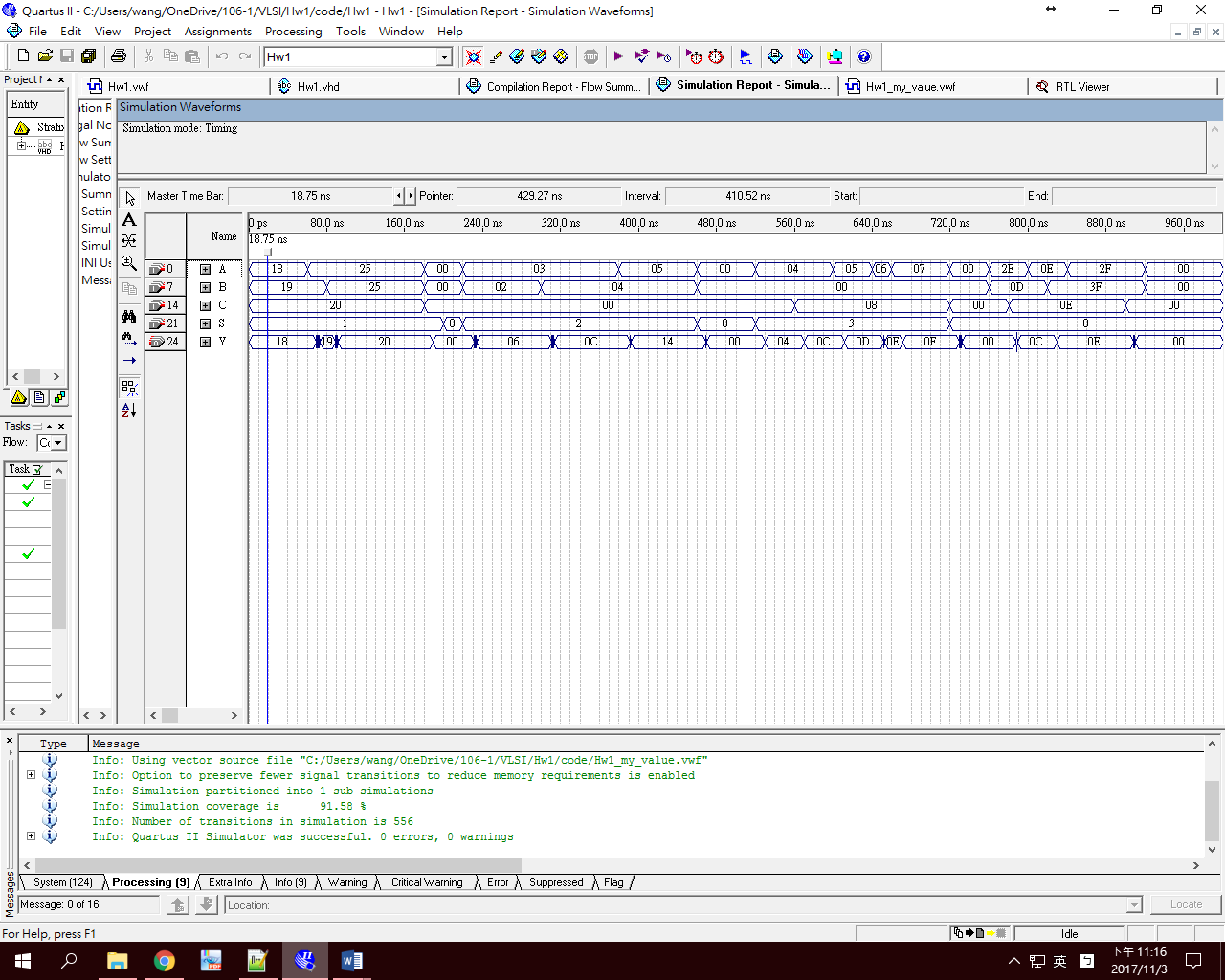
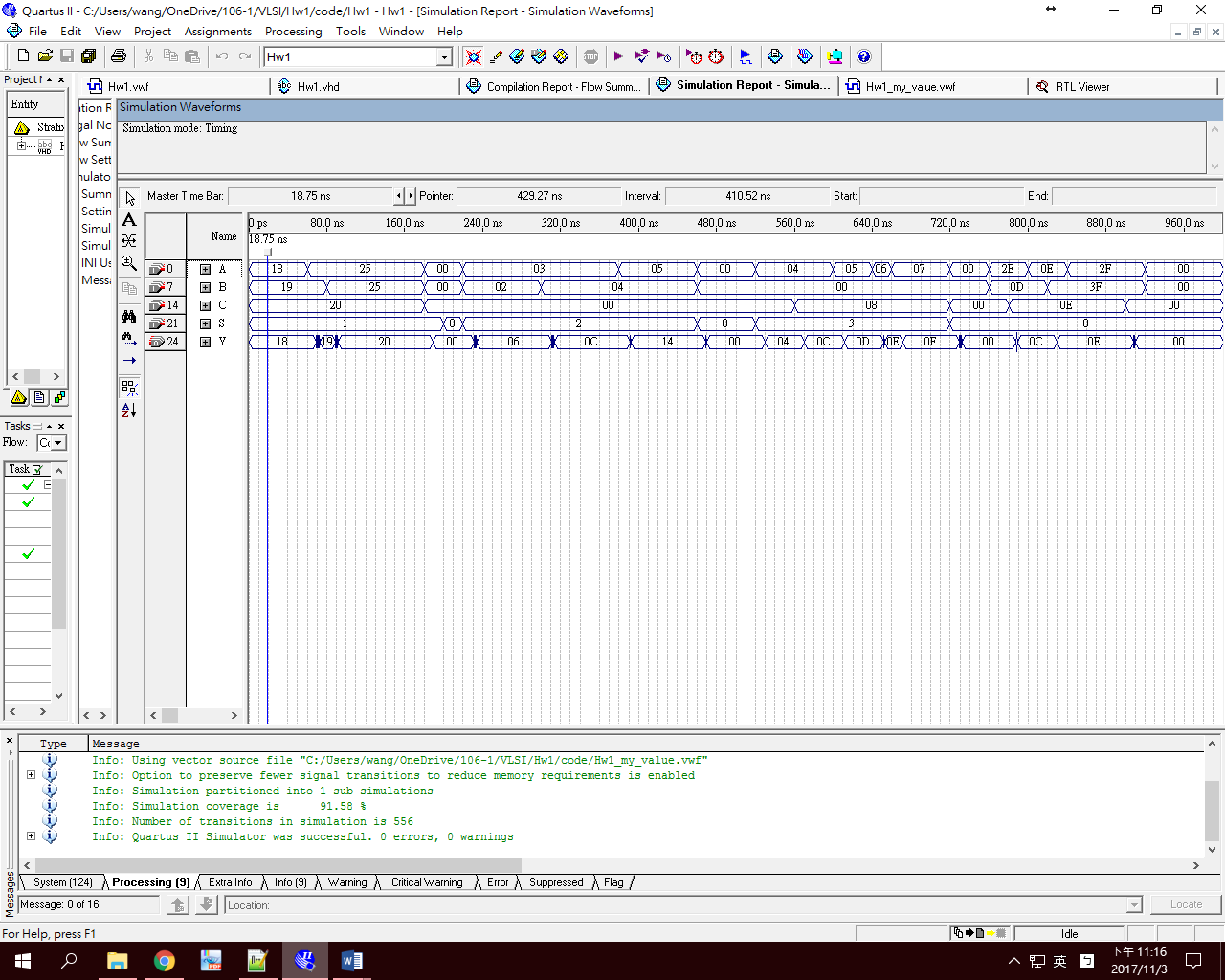
模擬結果全域圖



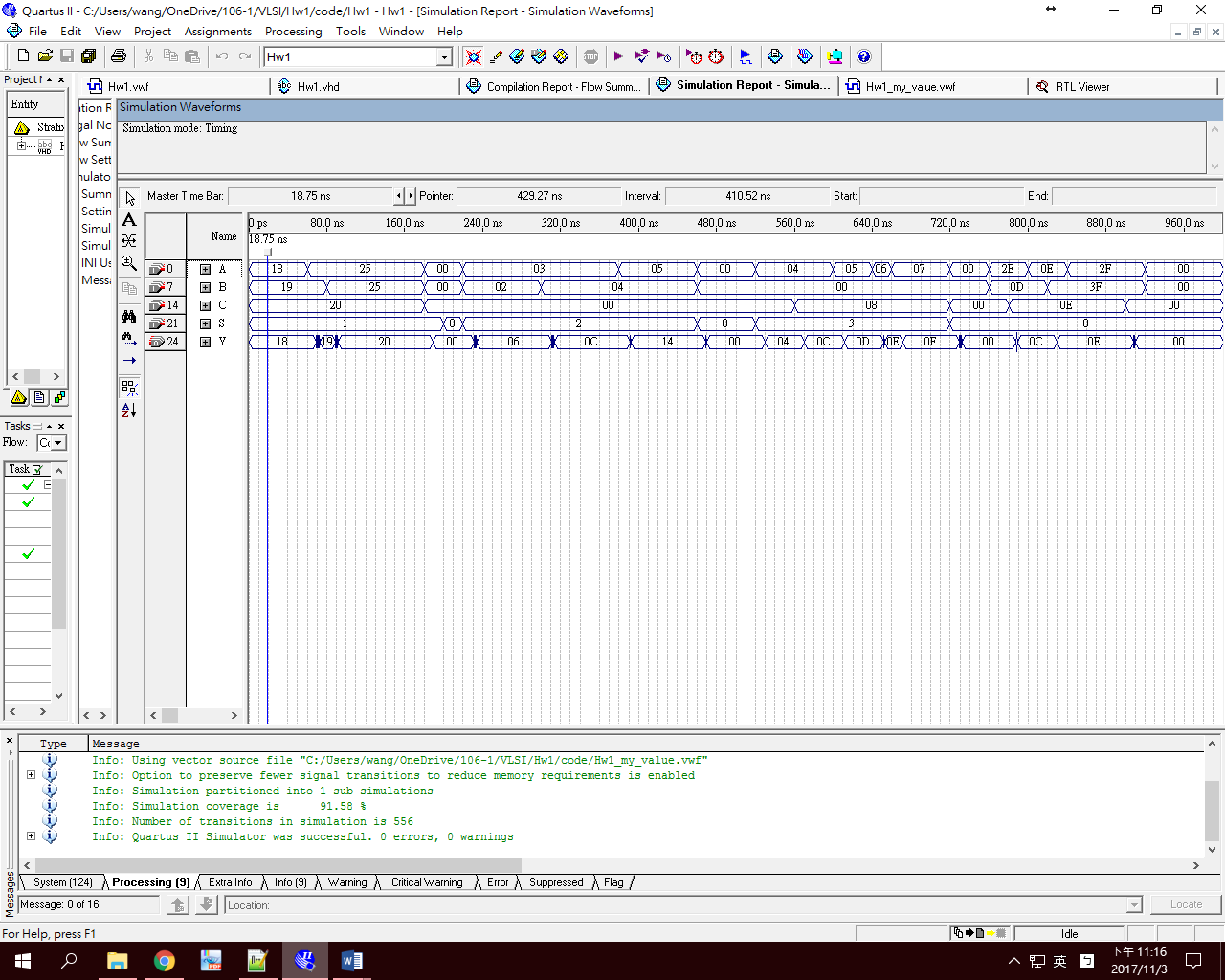
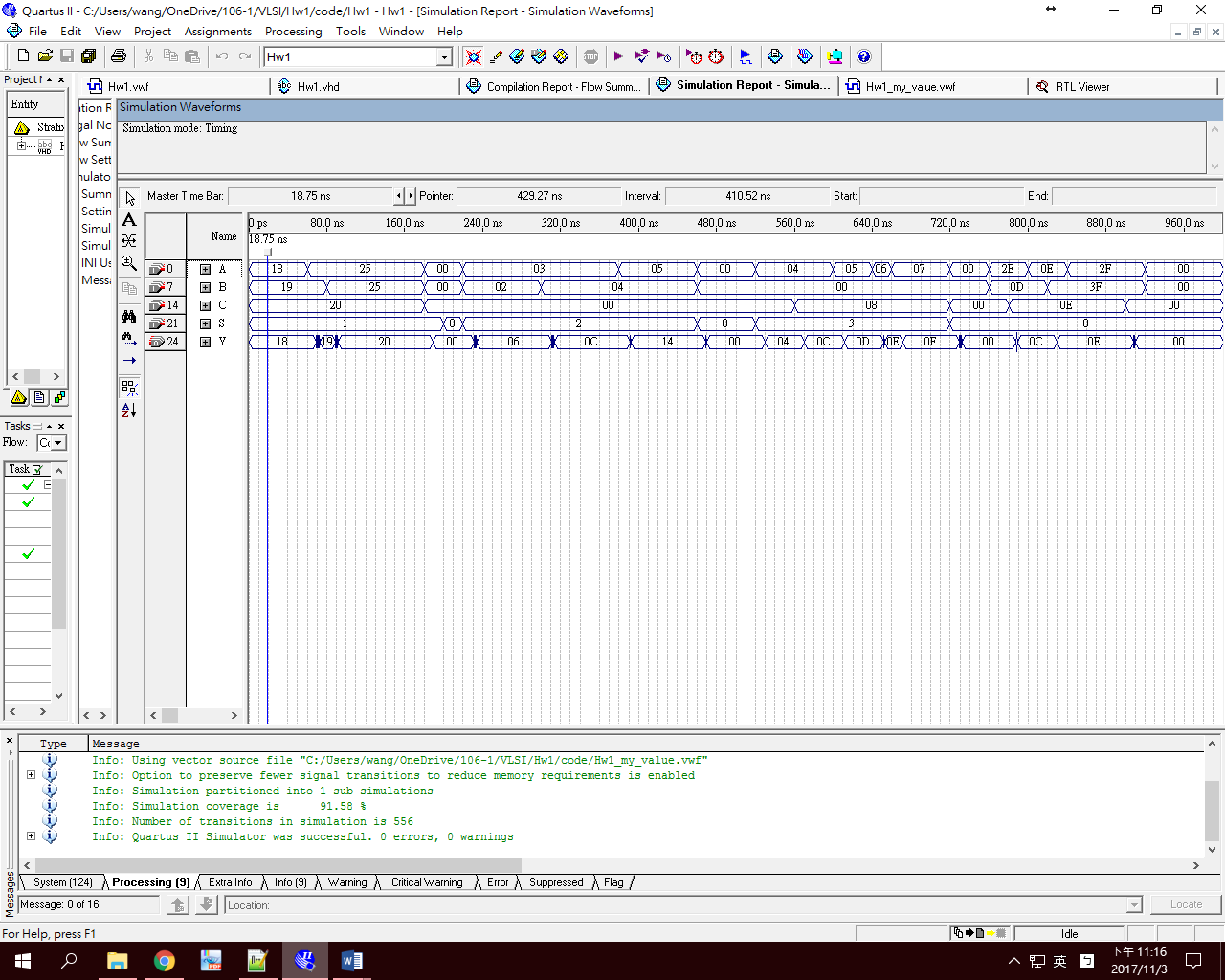
1. Mode 1: Yi=Ai AND Bi AND Ci, i=5,4,3,2,1,0.



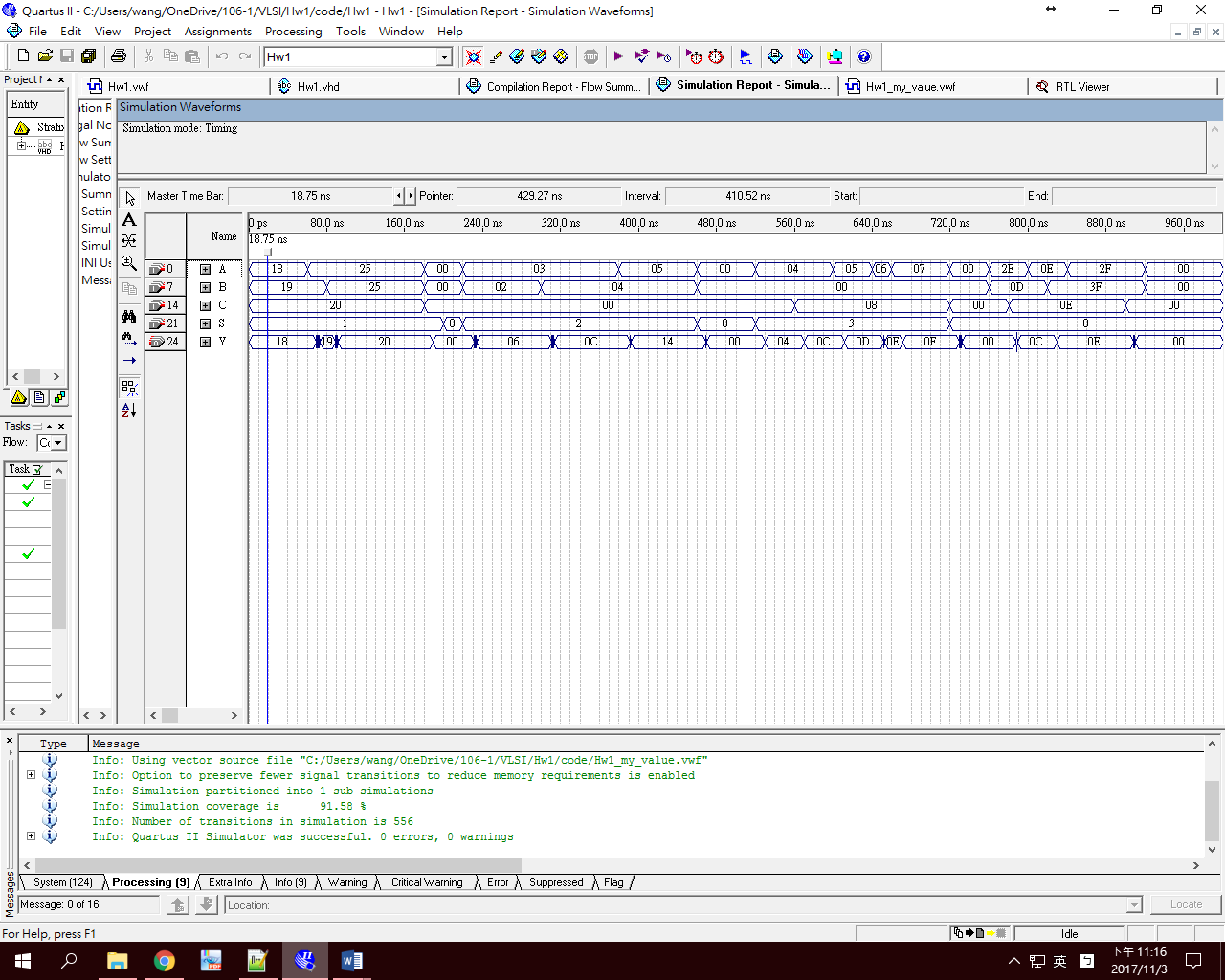
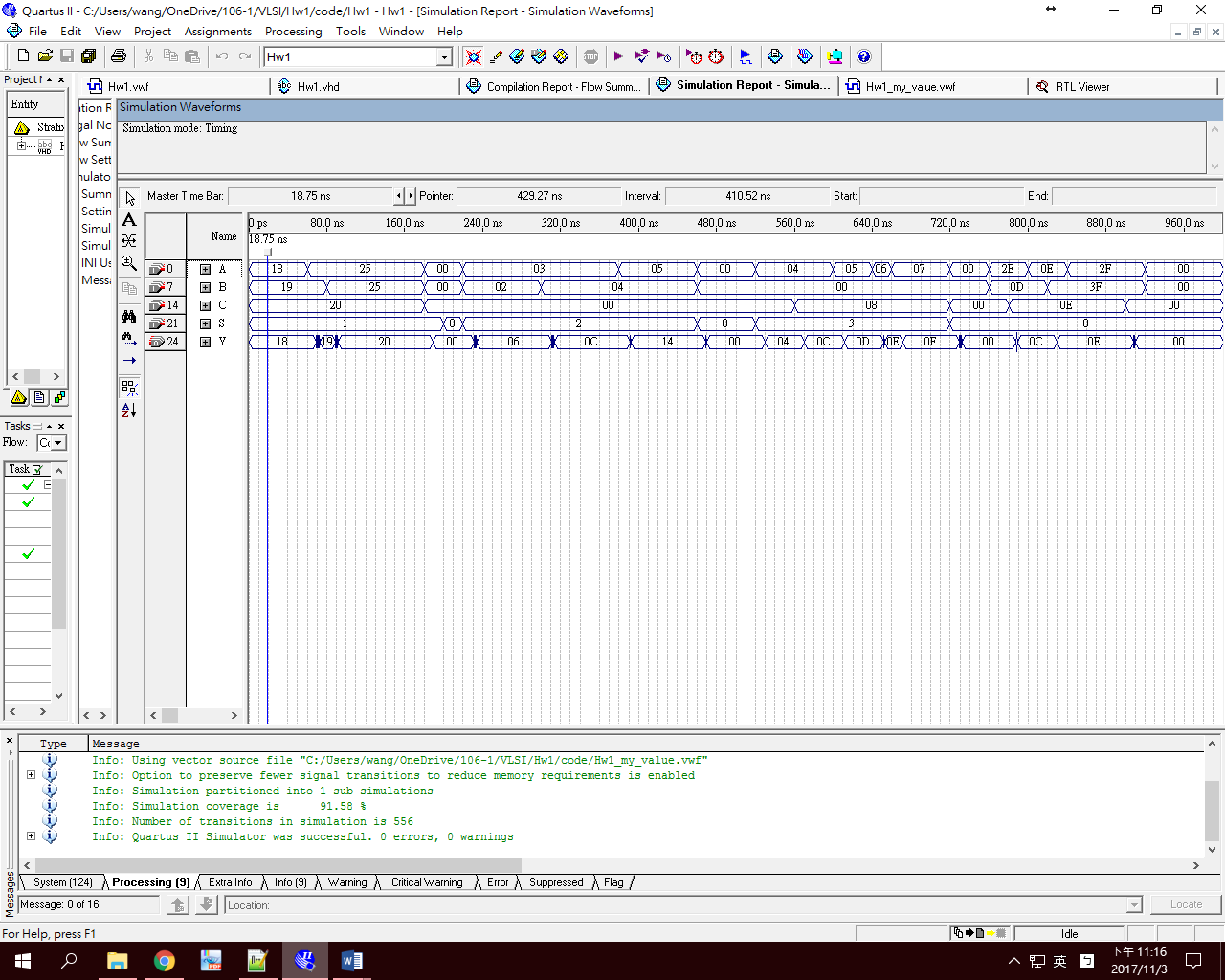
1. Mode 2: Y= min{A,B,C}



1. Mode 3: Y= A\*B



1. Mode 4: Y=A+C



4. 結論及心得(20%):

這次我第一次寫硬體描述語言,能看到自己的程式轉成硬體線路是有很趣味的.這次的作業還不會太難,所以沒什麼太大問題,主要是要熟習VHDL的語法.