HO CHI MINH CITY UNIVERSITY OF TECHNOLOGY
FACULTY OF COMPUTER SCIENCE AND ENGINEERING

LSI Logic Design (CO3098)

MINI PROJECT: ALU

Authors:
Nguyen Thanh Thao Nhi

Student's ID:
2152840

Instructors:

Nguyen Thien An

Completion date: 22th May, 2024

Contents

1 Interface **3**

2 Functional Implement **3**

3 Internal Implement **4**

4 State Machine **5**

5 Schematic **6**

1 Interface

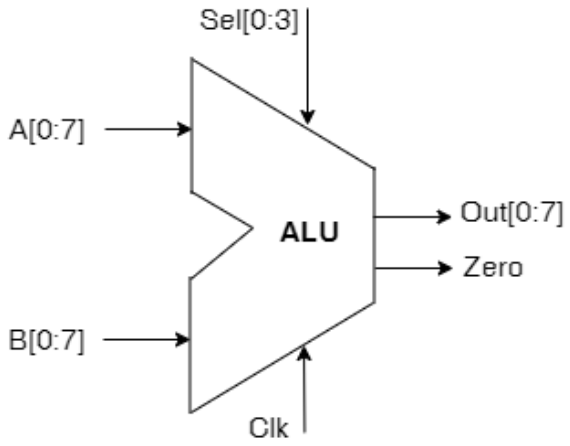

Figure 1: Interface

Description of signals in ALU:

Signal	Width	In/Out	Description
Clk	1	In	A positive edge clock signal is used to operate the state's transition.
A	8	In	The first operand of ALU
B	8	In	The second operand of ALU
Sel	4	In	Control signal used to select an operator (Add, subtract, and, or)
Out	8	Out	The result of ALU after performing selected operation
Zero	1	Out	The zero flag is activated when the output result equals 0

2 Functional Implement

The ALU (Arithmetic Logic Unit) is capable of performing 8-bit operations, including arithmetic addition and subtraction, as well as bitwise AND and OR operations.

1. Inputs:
    - Operand 1 (8 bits): A[0:7]
    - Operand 2 (8 bits): B[0:7]
    - Control Signal (4 bits): Sel[0:3]
2. Outputs:

- Output Result (8 bits): Out[0:7]
- Zero Flag (1 bit): Zero[0]

3. Operation Control Value Mapping:

- ADD: 0010
- SUB: 0110
- AND: 0000
- OR: 0001

3 Internal Implement

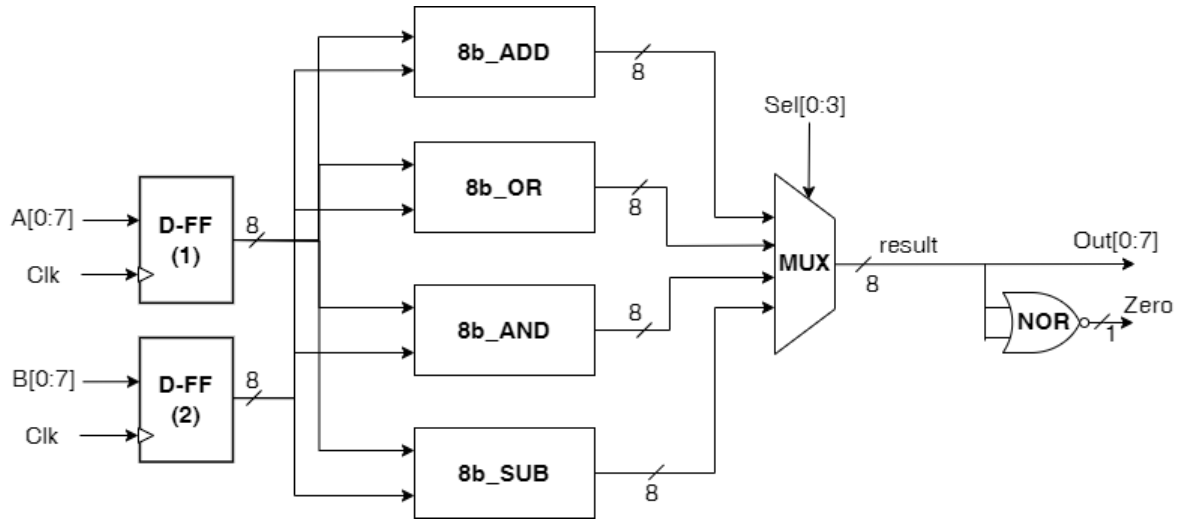

Figure 2: Block diagram

Block diagram of ALU Description:

Name	Type	Description
A	Input	Operand 1
B	Input	Operand 2
Clk	Input	Clock signal (postedge)
result	Reg	Result from the calculation (arthritic or logic operation) based on select signals.
Out	Output	Final output result of ALU
Zero	Output	The zero flag. This equals 1 when output is 0.
D-FF (1)	Control Block	This is a D Flip Flop used to store the value of the first operand to ensure its stability.
D-FF (2)	Control Block	This is a D Flip Flop used to store the value of the second operand to ensure its stability.
8b_AND	Logic Block	This is a digital logic component that takes two 8-bit binary inputs and produces an 8-bit output where each bit represents the result of performing a bitwise AND operation on the corresponding bits of the input.
8b_OR	Logic Block	This is a digital logic component that takes two 8-bit binary inputs and produces an 8-bit output where each bit represents the result of performing a bitwise OR operation on the corresponding bits of the input.
8b_ADD	Logic Block	A digital logic component capable of performing addition operations on two 8-bit binary numbers based on the select signal.
8b_SUB	Logic Block	A digital logic component capable of performing subtraction operations on two 8-bit binary numbers based on the select signal.
MUX	Logic Block	A multiplexer with 4 data inputs, 1 select input, and 1 output, which selects one of the data inputs based on the select input.
NOR	Logic Block	A digital logic gate that performs the logical NOR operation in which output is true when none of the inputs are true.

4 State Machine

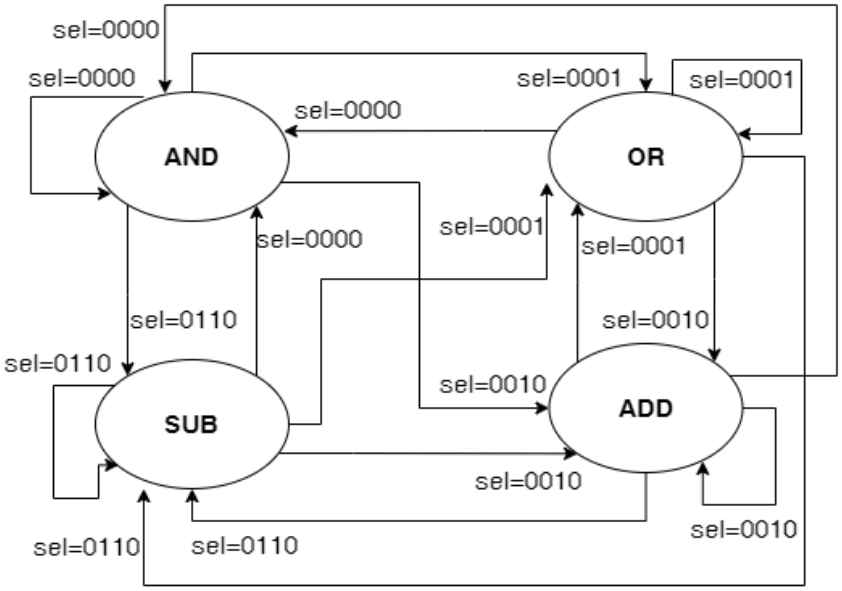

Figure 3: State Machine

The variable name of the State machine:

Variable name	**Description**
sel	The control signal of ALU

State name of the State machine:

State	**Description**
AND	Logical AND operation
OR	Logical OR operations
ADD	Arithmetic operation ADD
AUB	Arithmetic operation SUBSTRACT

5 Schematic

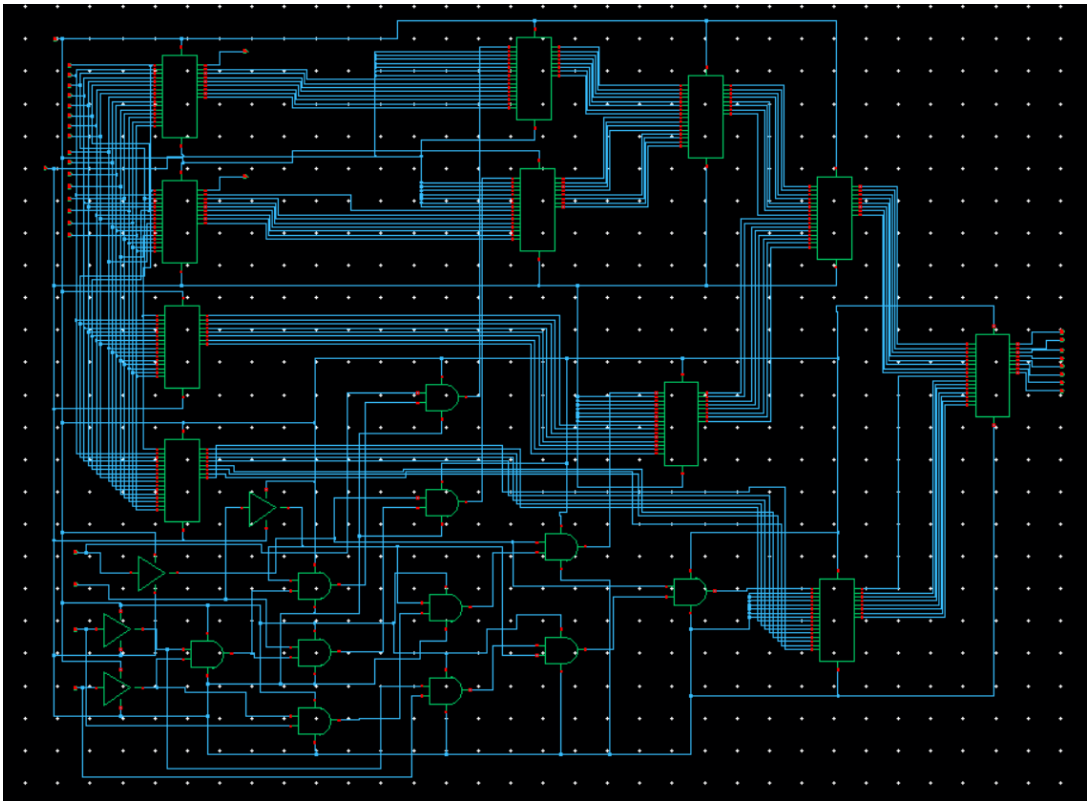

Figure 4: ALU schematic