

QB for NT

Sr. No.	Question
1.	<p>Give detailed account of Czokalski growth technique</p> <p>Czokalski Growth Technique: A Detailed Account</p> <p>The Czokalski growth technique is a method used for growing high-quality single crystals, particularly for semiconductors and optical materials. It is closely related to Czochralski (CZ) crystal growth, which is widely used in silicon wafer production for the semiconductor industry.</p> <p>1. Overview of the Czokalski Growth Technique The Czokalski method is a variant of the Czochralski process, but with specific modifications to improve the quality and structural integrity of grown crystals. It is commonly used for growing large, defect-free single crystals from a melt.</p> <p>2. Basic Principles</p> <ul style="list-style-type: none">• A seed crystal is dipped into a high-purity molten material.• The seed is slowly pulled upwards while rotating to allow controlled solidification.• The temperature, pulling rate, and rotation speed are carefully controlled to achieve high-purity, defect-free crystals. <p>3. Key Features of the Czokalski Growth Method</p> <ul style="list-style-type: none">• Controlled Growth Conditions: The method focuses on minimizing defects, such as dislocations and grain boundaries, by optimizing pulling speed, temperature gradients, and rotation speed.• Refinement of Crystal Structure: The growth conditions ensure that the resulting single crystal has a uniform orientation, reducing impurities and structural defects.• High-Purity Crystals: Used in semiconductor manufacturing and optics, the method ensures minimal contamination. <p>4. Process Steps</p> <ol style="list-style-type: none">1. Melting the Material<ul style="list-style-type: none">○ The raw material (e.g., silicon, gallium arsenide, or other semiconductor materials) is melted in a crucible, typically made of quartz or graphite.○ The temperature is carefully controlled to maintain the liquid state of the material.2. Insertion of the Seed Crystal<ul style="list-style-type: none">○ A high-purity seed crystal with the desired crystallographic orientation is lowered into the melt.○ The seed acts as a template for controlled crystal growth.3. Pulling and Rotating the Crystal<ul style="list-style-type: none">○ The seed is slowly lifted while the rotation helps in uniform solidification.○ The pulling rate determines the diameter of the crystal.○ Controlled cooling prevents thermal stress and cracking.4. Crystal Growth and Shaping<ul style="list-style-type: none">○ The process continues until the desired length and diameter of the crystal are achieved.○ Precise control over temperature and pulling rate minimizes structural defects.5. Cooling and Annealing<ul style="list-style-type: none">○ The grown crystal is slowly cooled to reduce residual stress.○ Some crystals undergo annealing to remove internal defects and improve mechanical properties. <p>6. Applications of the Czokalski Growth Technique</p>

	<ul style="list-style-type: none"> • Semiconductor Industry <ul style="list-style-type: none"> ◦ Production of high-purity silicon wafers for microchips and processors. ◦ Growth of gallium arsenide (GaAs) and indium phosphide (InP) for optoelectronic devices. • Optical Materials <ul style="list-style-type: none"> ◦ Growth of sapphire and yttrium aluminum garnet (YAG) for lasers. ◦ Production of crystals for infrared and UV optical systems. • Research and Advanced Materials <ul style="list-style-type: none"> ◦ Used in material science research for growing defect-free experimental crystals. ◦ Essential for quantum computing and high-speed transistors.
2.	<p>Explain Moore's Law</p> <p>1. Definition of Moore's Law Moore's Law is an empirical observation made by Gordon Moore, co-founder of Intel, in 1965. It states that: "The number of transistors on a microchip doubles approximately every two years, leading to an increase in computing power and a decrease in relative cost." Initially, Moore predicted this doubling every one year but later revised it to every two years in 1975.</p> <hr/> <p>2. Key Aspects of Moore's Law</p> <ul style="list-style-type: none"> ✓ Exponential Growth: The transistor count on integrated circuits (ICs) increases exponentially, resulting in faster and more efficient processors. ✓ Cost Reduction: As transistor density increases, the cost per transistor decreases, making computing more affordable. ✓ Performance Improvement: Increased transistor count improves processing speed, energy efficiency, and computational power. ✓ Miniaturization: Chips become smaller, more powerful, and energy-efficient, enabling portable devices like smartphones, laptops, and IoT devices. <hr/> <p>3. Graphical Representation of Moore's Law If plotted on a logarithmic scale, transistor count vs. time forms a straight line, indicating exponential growth. Example:</p> <ul style="list-style-type: none"> • 1971: Intel 4004 – 2,300 transistors • 1982: Intel 80286 – 134,000 transistors • 1993: Pentium – 3.1 million transistors • 2006: Intel Core 2 Duo – 291 million transistors • 2021: Apple M1 – 16 billion transistors <hr/> <p>4. Implications of Moore's Law</p> <ul style="list-style-type: none"> ◆ Computing Power Explosion: More transistors allow for faster and more powerful computers. ◆ Lower Costs: Manufacturing advancements lead to cheaper consumer electronics. ◆ Advancement in AI & ML: More computing power enables deep learning, AI, and big data processing. ◆ Portable Technology Growth: Smartphones, wearables, and IoT devices benefit from compact, energy-efficient processors. ◆ Cloud & Edge Computing: Efficient chips power high-performance servers and cloud infrastructure.

	<p>5. Challenges to Moore's Law</p> <p>⚠ Physical Limitations: As transistors reach atomic sizes (below 5nm), quantum effects like tunneling disrupt performance.</p> <p>⚠ Heat Dissipation: More transistors increase power consumption and heat production, limiting further miniaturization.</p> <p>⚠ Rising Costs: Advanced manufacturing (e.g., EUV lithography) is becoming expensive and complex.</p>
	<p>6. Future of Moore's Law</p> <p>Although traditional transistor scaling is slowing down, alternative technologies are emerging:</p> <ul style="list-style-type: none"> ◆ 3D Transistors (FinFET, GAAFET) – Improving transistor efficiency. ◆ Chiplet Architecture – Breaking large chips into smaller, modular parts. ◆ Quantum Computing – Moving beyond silicon transistors for computation. ◆ Neuromorphic & Optical Computing – Exploring brain-inspired and photonic processors.
	<p>7. Conclusion</p> <p>Moore's Law has driven technological progress for over 50 years, enabling powerful and cost-effective computing. While physical limits challenge its continuation, innovations in chip design and new materials are extending its relevance. Even if the law slows, its impact on computing and society remains profound.</p>
3.	<p>Explain the bottom-up approach for the fabrication of nanoparticles.</p> <p>The bottom-up approach is a nanofabrication technique where nanoparticles are built atom-by-atom or molecule-by-molecule, similar to how biological systems self-assemble. This method mimics natural growth processes and is widely used for synthesizing high-purity and precisely controlled nanomaterials.</p> <p>This approach contrasts with the top-down method, which breaks down bulk materials into nanosized particles.</p> <p>2. Key Principles of the Bottom-Up Approach</p> <ul style="list-style-type: none"> • Uses chemical, biological, or physical self-assembly to build nanoparticles. • Atoms or molecules assemble into larger structures through nucleation and growth mechanisms. • Controlled by parameters like temperature, concentration, and reaction time. • Achieves uniform size, shape, and high purity. <p>3. Methods of Bottom-Up Nanoparticle Fabrication</p> <p>(A) Chemical Synthesis Methods</p> <ol style="list-style-type: none"> 1. Sol-Gel Method <ul style="list-style-type: none"> ○ Precursor compounds (e.g., metal alkoxides) dissolve in a solvent to form a gel. ○ The gel is then dried and heated to form nanoparticles. ○ Example: Silica (SiO_2) and metal oxide nanoparticles. 2. Co-Precipitation Method <ul style="list-style-type: none"> ○ Metal salts are reduced or precipitated by chemical reactions. ○ Particles form in solution and aggregate into nanoparticles. ○ Example: Magnetic Fe_3O_4 nanoparticles for biomedical applications. 3. Hydrothermal & Solvothermal Synthesis <ul style="list-style-type: none"> ○ Reaction occurs in a high-temperature, high-pressure liquid (water-based for hydrothermal, organic solvents for solvothermal). ○ Produces high-quality, crystalline nanoparticles. ○ Example: ZnO, TiO_2, and quantum dots synthesis.

	<p>4. Microwave-Assisted Synthesis</p> <ul style="list-style-type: none"> ○ Uses microwave radiation to heat reactions quickly. ○ Enables fast and uniform growth of nanoparticles. ○ Example: Gold (Au) and silver (Ag) nanoparticles. <hr/> <p>(B) Physical Methods</p> <ol style="list-style-type: none"> 1. Vapor Deposition Techniques <ul style="list-style-type: none"> ○ Chemical Vapor Deposition (CVD): Gas-phase precursors react to form nanoparticles on a substrate. ○ Physical Vapor Deposition (PVD): Materials evaporate and condense into nanoparticles. ○ Example: Graphene and carbon nanotube fabrication. <ol style="list-style-type: none"> 2. Laser Ablation <ul style="list-style-type: none"> ○ A high-energy laser pulse hits a solid target, ejecting nanoparticles into a surrounding liquid. ○ Produces pure nanoparticles without chemical contamination. ○ Example: Gold, silver, and titanium nanoparticles. <hr/> <p>(C) Biological Synthesis (Green Nanotechnology)</p> <ol style="list-style-type: none"> 1. Microbial Synthesis <ul style="list-style-type: none"> ○ Bacteria or fungi act as biofactories to produce nanoparticles from metal ions. ○ Example: Silver (Ag) nanoparticles synthesized by bacteria. <ol style="list-style-type: none"> 2. Plant-Based Synthesis <ul style="list-style-type: none"> ○ Plant extracts act as natural reducing agents to create nanoparticles. ○ Example: Green synthesis of gold and silver nanoparticles using tea extracts. <hr/> <p>4. Advantages of the Bottom-Up Approach</p> <ul style="list-style-type: none"> <input checked="" type="checkbox"/> High Purity & Fewer Defects – Controlled atomic/molecular assembly. <input checked="" type="checkbox"/> Precise Control Over Size & Shape – Enables uniform nanoparticles. <input checked="" type="checkbox"/> Lower Energy Consumption – More efficient than top-down approaches. <input checked="" type="checkbox"/> Scalability – Useful for industrial applications. <input checked="" type="checkbox"/> Eco-Friendly – Green synthesis methods reduce toxic waste.
4.	<p>Explain the top-down approach for the fabrication of nanoparticles.</p> <p>1. Introduction</p> <p>The top-down approach is a method of fabricating nanoparticles by breaking down bulk materials into nanosized structures using mechanical, chemical, or physical processes. This method is widely used in nanotechnology and semiconductor industries to create precise nanomaterials.</p> <p>It is the opposite of the bottom-up approach, where nanoparticles are built from atoms or molecules.</p> <hr/> <p>2. Key Principles of the Top-Down Approach</p> <ul style="list-style-type: none"> • Starts with a bulk material and breaks it into nanoparticles through physical or chemical processing. • Uses mechanical milling, etching, or lithographic techniques to achieve nanoscale structures. • Requires high-energy input but offers high precision and scalability. <hr/> <p>3. Methods of Top-Down Nanoparticle Fabrication</p> <p>(A) Mechanical Methods</p> <ol style="list-style-type: none"> 1. Ball Milling (High-Energy Milling)

	<ul style="list-style-type: none"> ○ Bulk material is ground into nanoparticles using rotating balls inside a milling chamber. ○ Effective for metal, ceramic, and polymer nanoparticles. ○ Example: Zinc oxide (ZnO) and aluminum oxide (Al_2O_3) nanoparticles. <p>2. Laser Ablation</p> <ul style="list-style-type: none"> ○ A high-energy laser pulse strikes a solid material, ejecting nanoparticles into a surrounding medium. ○ Produces high-purity nanoparticles without chemical contamination. ○ Example: Gold (Au) and silver (Ag) nanoparticles. <hr/> <p>(B) Lithographic Techniques</p> <ol style="list-style-type: none"> 1. Photolithography <ul style="list-style-type: none"> ○ Uses UV light and a mask to create nanopatterns on a substrate. ○ Commonly used in semiconductor manufacturing. ○ Example: Microchips and nanoscale transistors. <ol style="list-style-type: none"> 2. Electron Beam Lithography (EBL) <ul style="list-style-type: none"> ○ Uses a focused electron beam to pattern nanostructures with high precision. ○ Expensive and slow but provides sub-10 nm resolution. ○ Example: Graphene nanoribbons and nanoelectronics. <ol style="list-style-type: none"> 3. Focused Ion Beam (FIB) Milling <ul style="list-style-type: none"> ○ Uses high-energy ion beams to etch nanoscale structures. ○ High precision but damages material structure due to ion bombardment. ○ Example: Nanoscale circuits and sensors. <hr/> <p>(C) Chemical Methods</p> <ol style="list-style-type: none"> 1. Electrochemical Etching <ul style="list-style-type: none"> ○ Bulk material is immersed in an electrolytic solution, and an electric current dissolves material, forming nanoparticles. ○ Example: Silicon nanoparticles for optoelectronic devices. <ol style="list-style-type: none"> 2. Etching with Acids or Alkalies <ul style="list-style-type: none"> ○ Controlled chemical etching dissolves bulk material into nanoparticles. ○ Example: Silver nanoparticles from bulk silver. <hr/> <p>4. Advantages of the Top-Down Approach</p> <ul style="list-style-type: none"> ✓ High Precision & Scalability – Used in large-scale production. ✓ Well-Established Techniques – Common in the semiconductor and electronics industries. ✓ Controlled Shape & Size – Nanoparticles can be tailored using advanced lithography. ✓ Versatile for Various Materials – Works with metals, ceramics, polymers, and semiconductors.
5.	<p>What is Electron Resist. Differentiate between positive electron resist and negative electron resist.</p> <p>An electron resist is a thin polymer film used in electron beam lithography (EBL) to create nanoscale patterns on a substrate. When exposed to an electron beam (e-beam), the resist undergoes a chemical change, allowing selective removal (developing) to create a nanostructure.</p> <p>Key Properties of Electron Resists:</p> <ul style="list-style-type: none"> ✓ High sensitivity to electron beams. ✓ Ability to form high-resolution patterns (sub-10 nm). ✓ Good adhesion to the substrate. ✓ Chemical stability during the etching process.

2. Types of Electron Resists

Electron resists are mainly **classified into two types** based on their reaction to electron beam exposure:

1. Positive Electron Resist
2. Negative Electron Resist

Difference Between Positive and Negative Electron Resists

Feature	Positive Electron Resist	Negative Electron Resist
Definition	Becomes soluble in the developer after exposure to an electron beam.	Becomes insoluble in the developer after exposure to an electron beam.
Reaction to Electron Beam	Polymer chains break due to electron exposure, making the exposed region removable.	Polymer chains cross-link , making the exposed region resistant to the developer.
Development Process	The exposed areas are removed , leaving behind the unexposed pattern.	The unexposed areas are removed , leaving behind the exposed pattern.
Resolution	Higher resolution (can reach sub-10 nm).	Lower resolution (limited by polymer cross-linking).
Examples	PMMA (Polymethyl Methacrylate)	SU-8, HSQ (Hydrogen Silsesquioxane)
Applications	Used for high-precision nanoscale structures , semiconductor devices.	Used for durable patterns , MEMS, and microfluidic devices.

3. Working of Positive and Negative Electron Resists

(A) Positive Electron Resist Process

1. **Coating** – A **thin layer** of positive resist (e.g., PMMA) is applied to the substrate.
2. **Exposure** – The electron beam breaks the polymer chains in **exposed areas**.
3. **Development** – The exposed areas **dissolve**, leaving behind the **unexposed** regions as the pattern.
4. **Etching & Pattern Transfer** – The pattern is transferred onto the substrate via **etching**.

👉 Example: **PMMA** in **semiconductor lithography**.

(B) Negative Electron Resist Process

1. **Coating** – A **thin layer** of negative resist (e.g., SU-8) is applied to the substrate.
2. **Exposure** – The electron beam **cross-links polymer chains** in exposed areas.
3. **Development** – The **unexposed areas dissolve**, while the **exposed regions remain intact**.
4. **Etching & Pattern Transfer** – The pattern is transferred onto the substrate.

👉 Example: **SU-8** in **MEMS** and **microfluidics**.

4. Applications of Electron Resists

- ◆ **Semiconductor Manufacturing** – Used in **chip fabrication**.
- ◆ **Nanotechnology** – Creation of **nanoelectronic components**.
- ◆ **MEMS (Micro-Electro-Mechanical Systems)** – Used in **microfluidics, sensors, and actuators**.
- ◆ **Photonics** – Fabrication of **optical waveguides and gratings**.

5. Conclusion

Electron resists play a crucial role in **electron beam lithography**, enabling the fabrication of **high-resolution nanostructures**. The choice between **positive and negative resists** depends on the **application requirements**, such as **resolution, durability, and processing conditions**.

6. Explain X-ray lithography

1. Introduction to X-Ray Lithography

X-ray lithography (XRL) is an advanced nanofabrication technique used in semiconductor and MEMS industries to create **high-resolution micro and nanostructures**. It utilizes **X-ray radiation** instead of UV or electron beams to transfer patterns onto a **photoresist-coated substrate**.

Key Features of X-Ray Lithography

- High Resolution** – Can achieve feature sizes below **10 nm**.
- Deep Penetration** – X-rays **pass through thicker resists** than UV light, enabling 3D structures.
- Minimal Diffraction** – X-rays have **shorter wavelengths (0.1–10 nm)**, reducing **diffraction effects**.
- High Aspect Ratio** – Used in **MEMS** for tall and precise structures.

2. Working Principle of X-Ray Lithography

(A) Process Steps

1. **Substrate Preparation**
 - A thin film of photoresist (e.g., PMMA) is applied to a **silicon, glass, or metal substrate**.
2. **Mask Preparation**
 - A mask made of **X-ray transparent material (e.g., silicon nitride)** with an **X-ray absorbing pattern (gold or tungsten)** is placed over the resist.
3. **X-Ray Exposure**
 - A **high-energy X-ray source** (e.g., a synchrotron or X-ray tube) is directed onto the mask.
 - X-rays **pass through transparent areas** but are **blocked by the mask pattern**, transferring the design onto the resist.
4. **Development**
 - The exposed areas of the resist are **chemically dissolved** to form the final pattern.
 - If using a **positive resist** (e.g., PMMA), **exposed areas dissolve**.
 - If using a **negative resist** (e.g., SU-8), **unexposed areas dissolve**.
5. **Etching & Pattern Transfer**
 - The pattern is transferred onto the substrate via **etching (dry or wet)**.

3. Types of X-Ray Lithography

Type	Description	Application
Proximity X-Ray Lithography (PXL)	The mask is placed very close (few microns) to the resist.	Microfabrication of ICs and MEMS devices.
Projection X-Ray Lithography (PXL)	Uses lenses or mirrors to focus X-rays onto the resist.	High-resolution nanoelectronics and photonic devices.
LIGA Process (Lithographie, Galvanoformung, Abformung)	X-ray lithography followed by electroplating and molding .	Fabrication of high-aspect-ratio MEMS and biomedical devices.

4. Advantages of X-Ray Lithography

- Superior Resolution** – Can achieve **sub-10 nm feature sizes**.
- Minimal Diffraction Effects** – Due to **short X-ray wavelengths**.
- Deep Exposure & High Aspect Ratio** – Essential for **3D microstructures**.
- High Precision** – Used for **complex nanoscale device fabrication**.

7. Explain ion beam lithography

1. Introduction to Ion Beam Lithography

Ion Beam Lithography (IBL) is an advanced **nano-patterning technique** that uses a **focused ion beam (FIB)** instead of photons (as in UV lithography) or electrons (as in EBL). This technique provides **ultra-high resolution** and is used for **nanofabrication, mask repair, and direct material modification**.

Key Features of Ion Beam Lithography:

- High Resolution** – Can achieve **sub-5 nm patterning**.
- No Proximity Effect** – Unlike Electron Beam Lithography (EBL), there is **minimal scattering**.
- Direct Writing Capability** – Can modify materials **without masks**.
- Material Modification** – Can **implant, mill, and deposit** materials.

2. Working Principle of Ion Beam Lithography

(A) Process Steps

1. **Ion Source Generation**
 - o A focused **ion beam (e.g., Ga⁺ ions)** is produced using a Liquid Metal Ion Source (LMIS).
2. **Ion Beam Focusing**
 - o The **ions are accelerated and focused using electromagnetic lenses** to form a nanometer-sized beam.
3. **Exposure to Resist**
 - o The ion beam is **scanned over a resist-coated substrate, modifying the resist chemistry** in the exposed areas.
4. **Development**
 - o The resist is **developed** to remove the exposed (positive resist) or unexposed (negative resist) areas.
5. **Etching & Pattern Transfer**
 - o The developed pattern is transferred onto the substrate **via dry or wet etching**.

3. Types of Ion Beam Lithography

Type	Description	Application
Focused Ion Beam Lithography (FIBL)	Uses a narrow ion beam for high-precision direct writing.	Used in mask repair, nano-milling, and circuit editing .
Projection Ion Beam Lithography (PIBL)	Uses an ion beam through a stencil mask for pattern transfer.	Used in large-area nano-patterning and semiconductor manufacturing .
Ion Projection Lithography (IPL)	A broad ion beam is used with a stencil mask for fast exposure.	Used for high-speed nano-patterning .

4. Advantages of Ion Beam Lithography

- Ultra-High Resolution** – Achieves **sub-5 nm features**.
- Maskless Direct Writing** – No need for expensive masks.
- Material Versatility** – Works on **metals, semiconductors, and polymers**.
- No Proximity Effect** – Unlike EBL, **no electron scattering issues**.
- Versatile Processing** – Can be used for **patterning, implantation, and material deposition**.

8.	<p>Explain in detail process steps in silicon wafer shape processing.</p> <p>Silicon wafer shape processing involves several steps to convert raw silicon into highly pure, precisely shaped, and defect-free wafers used in semiconductor manufacturing.</p> <p>Steps in Silicon Wafer Shape Processing:</p> <ol style="list-style-type: none"> 1. Crystal Growth (CZ Process or FZ Process) <ul style="list-style-type: none"> o High-purity silicon is melted and grown into a single-crystal ingot using the Czochralski (CZ) process or Float-Zone (FZ) method. 2. Ingot Slicing <ul style="list-style-type: none"> o The silicon ingot is sliced into thin wafers using a diamond wire saw or ID (inner diameter) saw. 3. Edge Grinding <ul style="list-style-type: none"> o The edges of the wafers are ground to achieve a uniform diameter and prevent chipping during handling. 4. Lapping <ul style="list-style-type: none"> o This process removes surface damage from slicing, ensuring uniform thickness. 5. Etching <ul style="list-style-type: none"> o A chemical etching process removes the damaged layer introduced during sawing and lapping. 6. Polishing <ul style="list-style-type: none"> o Wafers are chemically and mechanically polished to obtain a mirror-like, smooth surface. 7. Cleaning <ul style="list-style-type: none"> o Wafers are cleaned using RCA cleaning to remove any organic and metallic contaminants. 8. Inspection & Packaging <ul style="list-style-type: none"> o Wafers undergo quality control checks and are then packaged in cleanroom conditions.
9.	<p>Write note on silicon impurities and discuss production of silicon in Siemens's process.</p> <p>(A) Silicon Impurities</p> <p>Silicon impurities impact the electrical properties of semiconductors.</p> <p>Types of Impurities:</p> <ol style="list-style-type: none"> 1. Intentional Dopants (Controlled Impurities) <ul style="list-style-type: none"> o N-type (Donors): Phosphorus (P), Arsenic (As), Antimony (Sb). o P-type (Acceptors): Boron (B), Gallium (Ga), Indium (In). 2. Unintentional Impurities <ul style="list-style-type: none"> o Oxygen (O₂): Introduced during crystal growth (CZ method). o Carbon (C): Comes from the quartz crucible. o Metallic Impurities: Iron (Fe), Copper (Cu), Aluminum (Al) – affect wafer performance. <p>(B) Siemens Process for Silicon Production</p> <p>The Siemens Process is an industrial method for producing high-purity polycrystalline silicon for semiconductor and solar applications.</p> <p>Steps in the Siemens Process:</p> <ol style="list-style-type: none"> 1. Trichlorosilane (SiHCl₃) Production <ul style="list-style-type: none"> o Quartz (SiO₂) and Carbon (C) are heated in an electric arc furnace to produce metallurgical-grade silicon (MG-Si).

	<ul style="list-style-type: none"> ○ MG-Si reacts with HCl (Hydrochloric Acid) at 300°C to form trichlorosilane (SiHCl_3). $\text{Si} + 3\text{HCl} \rightarrow \text{SiHCl}_3 + \text{H}_2$ <p>2. Purification by Fractional Distillation</p> <ul style="list-style-type: none"> ○ Trichlorosilane (SiHCl_3) is distilled to remove impurities. <p>3. Chemical Vapor Deposition (CVD) for Polycrystalline Silicon</p> <ul style="list-style-type: none"> ○ SiHCl_3 is decomposed at 1100–1200°C on heated silicon rods in a reactor, depositing high-purity silicon: $\text{SiHCl}_3 + \text{H}_2 \rightarrow \text{Si} + 3\text{HCl}$ ○ The process results in ultra-pure polysilicon rods, which are later used for wafer fabrication. 												
10.	<p>Discuss in detail UV-lithographic processes</p> <p>Introduction to UV Lithography</p> <p>UV Lithography (UltraViolet Lithography) is a microfabrication technique used to pattern semiconductor wafers in the integrated circuit (IC) industry. It utilizes UV light (wavelength: 365 nm - 193 nm) to transfer patterns from a mask onto a photoresist-coated wafer.</p> <hr/> <p>Steps in UV Lithography:</p> <ol style="list-style-type: none"> 1. Wafer Preparation <ul style="list-style-type: none"> ○ The silicon wafer is cleaned to remove any particles or contaminants. ○ A thin layer of photoresist is applied to the wafer via spin coating. 2. Soft Baking <ul style="list-style-type: none"> ○ The wafer is baked at 90–120°C to remove excess solvents from the photoresist. 3. Mask Alignment & Exposure <ul style="list-style-type: none"> ○ A photomask containing the circuit pattern is aligned with the wafer. ○ UV light is shone through the mask, exposing the photoresist. ○ The areas exposed to UV light undergo a chemical change. 4. Development <ul style="list-style-type: none"> ○ The wafer is placed in a developer solution to dissolve either: <ul style="list-style-type: none"> ▪ Exposed areas (Positive Resist) ▪ Unexposed areas (Negative Resist) 5. Hard Baking <ul style="list-style-type: none"> ○ A second baking step at 150–200°C hardens the resist to improve adhesion. 6. Etching <ul style="list-style-type: none"> ○ The developed pattern is transferred onto the wafer using: <ul style="list-style-type: none"> ▪ Wet Etching (Chemical) ▪ Dry Etching (Plasma or RIE - Reactive Ion Etching) 7. Photoresist Removal (Stripping) <ul style="list-style-type: none"> ○ The remaining photoresist is removed using a plasma ash or chemical solvents. <hr/> <p>Types of UV Lithography:</p> <table> <thead> <tr> <th>Type</th> <th>Description</th> <th>Resolution</th> </tr> </thead> <tbody> <tr> <td>Near-UV Lithography (365 nm)</td> <td>Traditional UV lithography with mercury lamps.</td> <td>> 500 nm</td> </tr> <tr> <td>Deep-UV Lithography (DUV, 248 nm/193 nm)</td> <td>Uses excimer lasers (KrF - 248 nm, ArF - 193 nm).</td> <td>< 100 nm</td> </tr> <tr> <td>Extreme-UV Lithography (EUV, 13.5 nm)</td> <td>Uses X-ray wavelengths for next-gen chips.</td> <td>< 7 nm</td> </tr> </tbody> </table>	Type	Description	Resolution	Near-UV Lithography (365 nm)	Traditional UV lithography with mercury lamps.	> 500 nm	Deep-UV Lithography (DUV, 248 nm/193 nm)	Uses excimer lasers (KrF - 248 nm, ArF - 193 nm).	< 100 nm	Extreme-UV Lithography (EUV, 13.5 nm)	Uses X-ray wavelengths for next-gen chips .	< 7 nm
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Advantages of UV Lithography

- High Throughput** – Suitable for mass production of ICs.
- Cost-Effective** – Cheaper than E-beam or X-ray lithography.
- Scalability** – Can be extended with DUV and EUV for advanced nodes.

Disadvantages of UV Lithography

- Resolution Limits** – Traditional UV lithography is limited to **sub-500 nm** features.
- Proximity Effect** – Pattern distortions due to light diffraction.
- Expensive Mask Fabrication** – High-precision masks increase costs.

Applications of UV Lithography

- ◊ **Semiconductor Manufacturing** – Used in fabricating **transistors, ICs, and MEMS**.
- ◊ **Display Technology** – Production of **LCD, OLED panels**.
- ◊ **Microfluidics & MEMS Devices** – Fabrication of **lab-on-a-chip devices**.