Report

on

COEN 316 Laboratory Experiment #5

**Datapath/Control Unit Integration and system testing**

Submitted to

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Date: December 5th, 2016

Due Date: December 6th, 2016

By

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# Objectives

The objective of this laboratory is to design the CPU datapath and control unit and combine all previous labs to obtain a working CPU.

# Theory

VHDL is used as a tool that allows the possibility to read the behavior of an electrical circuit that can be written by the user and it can also be converted to a physical component. It uses computers to design the digital circuits and it helps in the creation of more complex circuits as well

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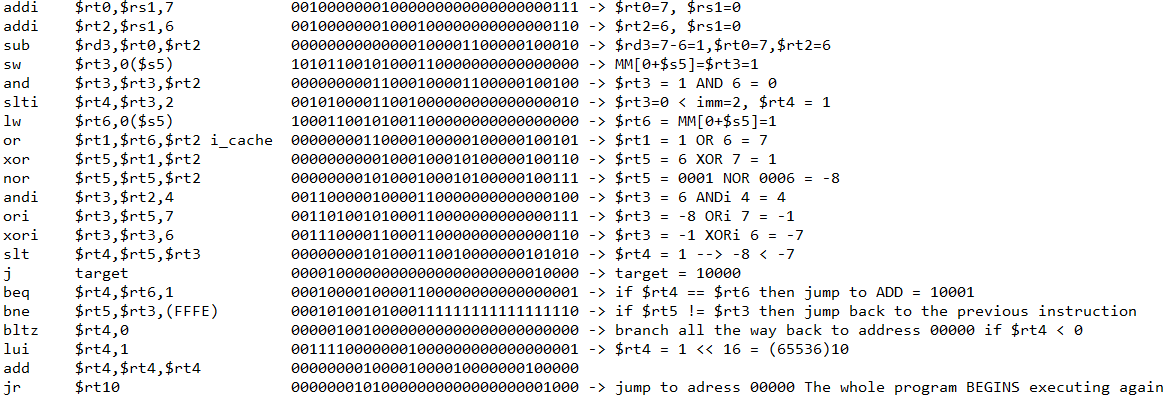
We also use Modelsim during this lab, it is a software that can simulate the HDL circuits you design with VHDL. It is used to test and debug the circuits mostly. We must also use the precision tool to get a schematic and the Xilinx software to obtain files needed for testing onto the hardware.

The control unit in this implementation is a combinational logic circuit whose inputs are the opcode and function fields of the instruction and the outputs are the 10 control signals. It will be used within the CPU’s datapath when port mapping each component and ensure it correctly executes the code by pinpointing each function within his code.

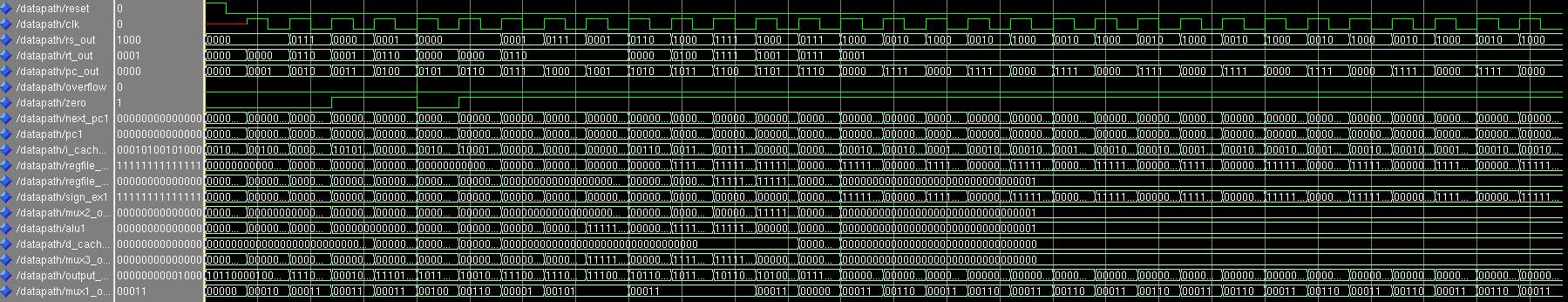
# Observations

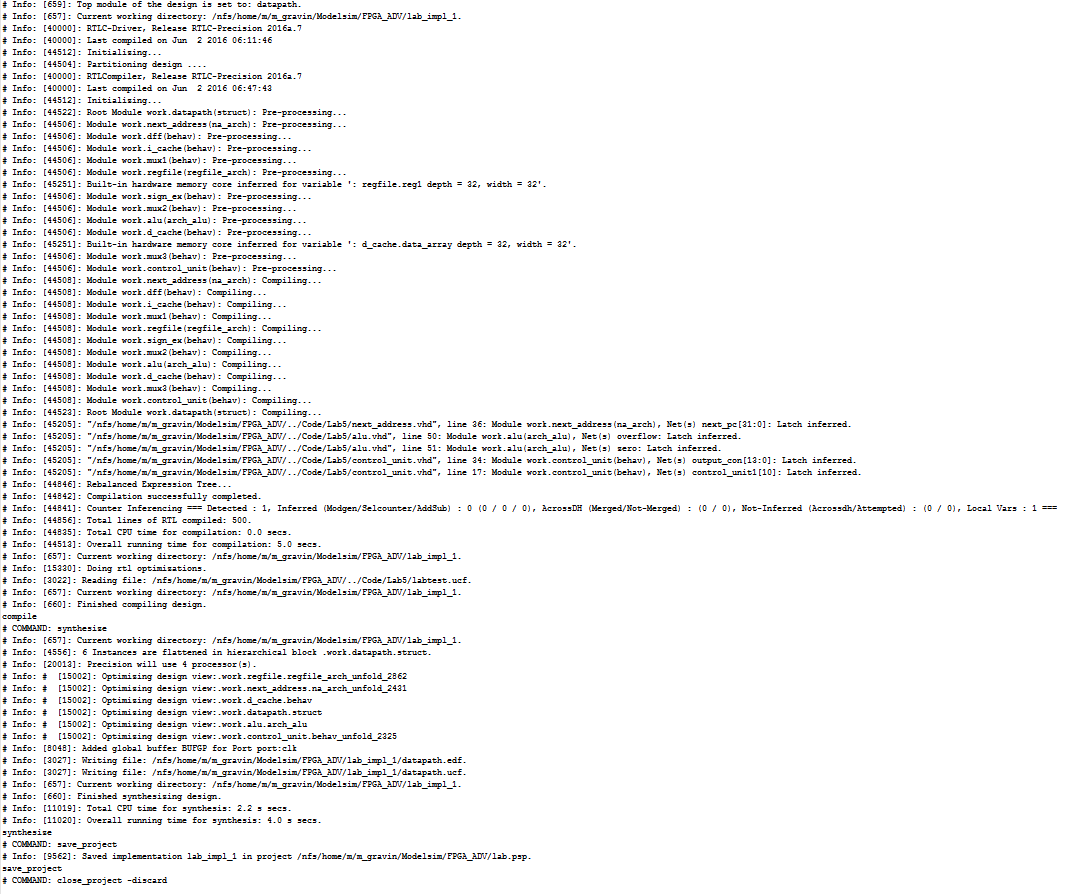
In designing the datapath of this CPU I had to make a lot of components that the other 3 labs did not cover. When looking at the diagram of the CPU within the given lab manual I observed 3 mux’s needed to be created, 1 sign extend block, 1 data cache, 1 intruction cache and 1 pc register. Once all remaining parts are created within VHDL, we can then start writing the CPU datapath. Within another VHDL file, we add all components to the cpu within the architecture of the CPU entity, this will be the final CPU once we port map all signals to their respective positions and with the newly created control unit, everything will work harmoniously.

Here are the Instructions that I will be simulating within the modelsim results displayed shortly after:



This is the ModelSim depicting every case with regards to the instructions in the previous figure:

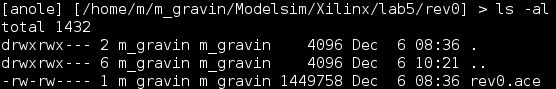


Here are the last 70 lines or so of the precision.log file:

Here is the impact.log (last 30 lines or so):



And finally the listing of the working directory with the rev0.ace file:



# Conclusion

All in all this lab accomplished what it needed, I achieve the objectives that it set us out to complete. Because of this experiment I am more familiar using VHDL to design a CPU datapath as well as been reacquainted with the simulation software ModelSim and other related software to properly use it in the future. The hardest part of this lab was probably understanding what the lab manual wanted the CPU datapath to be and how exactly to implement it in an optimized and clear way without doing much debugging. This lab has helped me immensely with the material of this course and has bettered my understanding of CPUs and microprocessors and will definitely be of great help in my future endeavors.

# Source Code

Control\_Unit.vhd



Datapath.vhd

