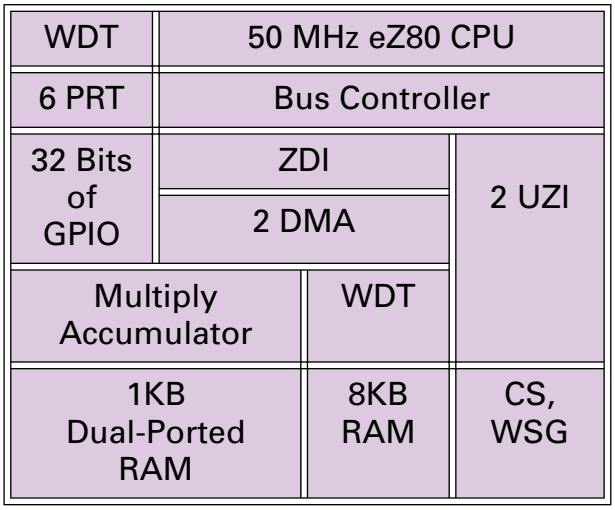
eZ80190

eZ80 Webserver

PB005201-0900

Product Brief

Product Block Diagram



Features

- eZ80 Core
  - Upward-code-compatible from Z80 & Z180
  - 50 MHz
  - 16 MB linear addressing
  - Optimized pipeline architecture
  - 24-bit registers and ALU
  - 16x16-bit Multiply with dual 40-bit Accumulators
    - 1KB Dual Ported SRAM for DSP applications
- 2 Universal ZiLOG Interface (UZI) Channels (I2C, SPI, UART)
- 8KB High Speed SRAM
- 2 Channel DMA Controller
- Four Chip Selects with Individual Wait State Generators
- Six Counter Timers with Pre-scalars
- Watch Dog Timer
- ZiLOG Debug Interface (ZDI)
- 32 Bits of General Purpose I/O
- On Chip Oscillator

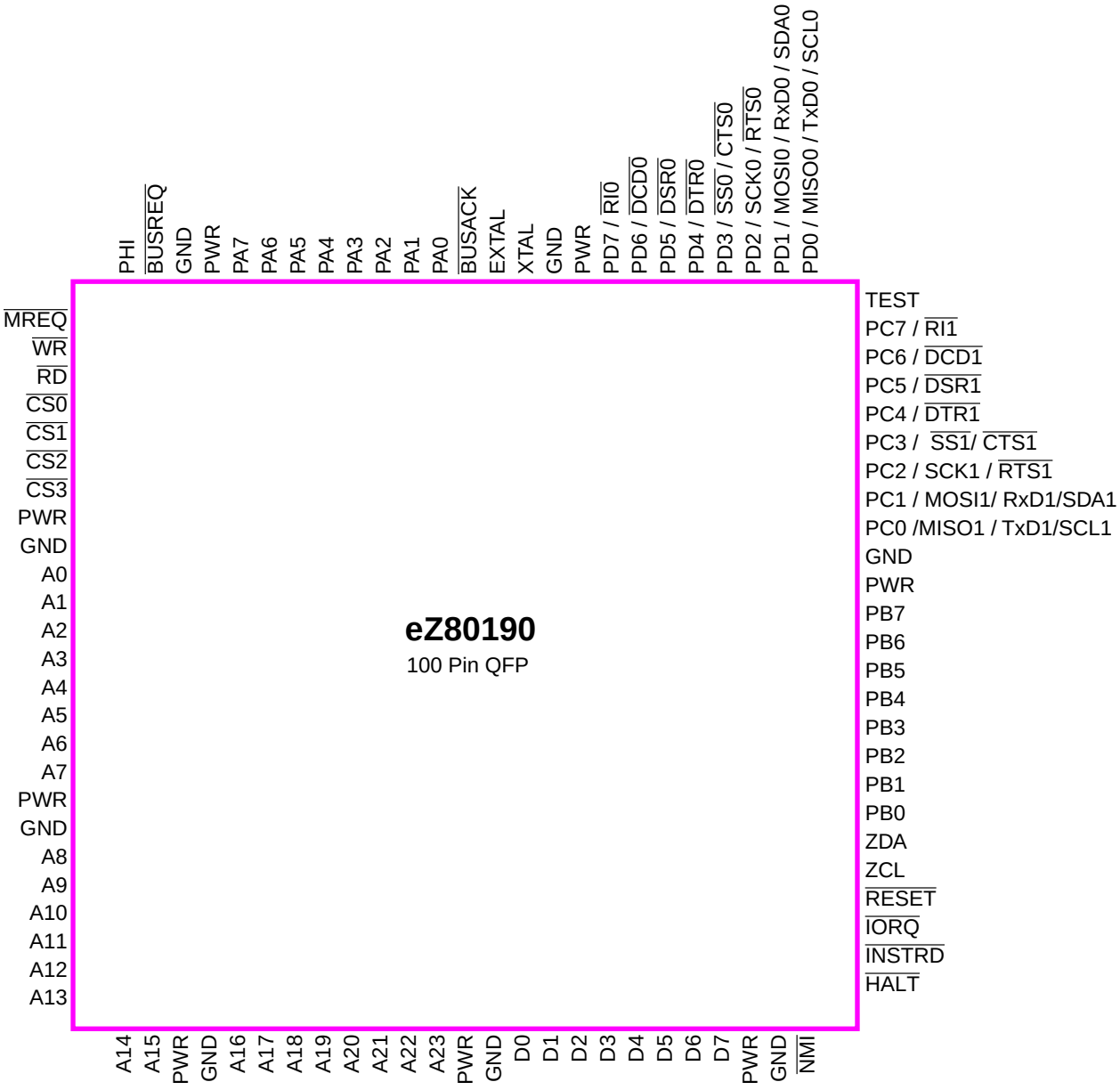
General Description

The eZ80190 Webserver is a high speed, optimized pipeline architecture microprocessor, operating at 50 MHz. It is the first in a line of new eZ80 based standard products targeted toward embedded internet applications.

The eZ80 is one of the fastest 8-bit CPUs available today, executing code four times faster than a standard Z80 operating at the same clock speed. In addition the eZ80 Webserver includes a high performance Multiply Accumulator, ideal for signal processing.

The eZ80 can operate in Z80-compatible (64 KB) mode, or full 24-bit (16 MB) addressing mode. Considering both the increased clock speed and processor efficiency, the eZ80's processing power rivals the performance of 16-bit microprocessors, and encroaches on 32-bit.

PIN-OUT



CORE DESCRIPTION

The eZ80 core is an 8-bit microprocessor that performs in either a 16 or 24-bit addressing mode.

The ez80 improves on the world famous Z80 architecture. Like the Z80, it has dual bank registers for fast context switching.

eZ80190 Peripheral Description

Universal ZiLOG Interface (UZI)

There are three serial communication controller blocks, SPI, UART, and I2C, along with control registers and a Baud Rate Generator (BRG) common to all three serial devices. Only one of the serial devices is active at any time.

- The **Baud Rate Generator** provides a lower frequency clock from the system clock. This module consists of a 16-bit counter, two 8-bit pre-load registers and associated decoding logic.
- The **UART** module implements all the logic required to support asynchronous communications. The module also contains 16-byte deep FIFOs for both transmit and receive.
- The **SPI** is a synchronous interface allowing several SPI-type devices to be interconnected. The SPI may be configured as either a master or a slave.
- The **I2C** operates in four modes: Master Transmitter, Master Receiver, Slave Transmitter and Slave Receiver.

RAM

On-board memory consists of 8K x 8 general purpose RAM and 1K x 8 dual-port RAM for the Multiply Accumulator. Both RAMs can be individually enabled or disabled and can be relocated to the top of any 64K page.

DMA Controller

The DMA controller can be used for direct memory to memory data transfers without CPU intervention. There are two DMA channels, channel 0 and channel 1. Each channel has independent registers. Transfers can be either in burst mode or cycle-steal mode.

Chip Select/Wait State Generator

There are four chip selects for external devices. Each chip select may be programed for either memory or I/O space. Each memory chip select can be individually programmed on a 64K boundary. The I/O chip selects can choose a 16-byte section of I/O space. Each chip select may be programmed for up to seven wait states.

Programmable Reloadable Counter/Timers

The eZ80 Webserver has six Programmable Reloadable Counter Timers (PRT). Each timer is a 16-bit down counter and has a 4-bit clock prescaler with four selectable taps for CLK/2, CLK/4, CLK/8 and CLK/16. The timers' two modes of operation are single-pass and continuous count mode. The timer can be programmed to start, stop, restart to continue, or restart from an initial value.

Watch Dog Timer (WDT)

The WDT has four programmable time-out periods: 2^{18}, 2^{22}, 2^{25}, 2^{27} Clock Cycles. It allows the user to monitor the status of a time-out and generate a RESET or Non-Maskable Interrupt.

General Purpose Input/Output (GPIO)

There are 32 bits of General Purpose Input or Output. All port signals can be individually programmable in either the Input or Output mode of operation.The 32 port bits can be used as vectored interrupt sources. The pins can be set to recognize either level- or edge-triggered interrupts.

ZiLOG Debug Interface (ZDI)

ZDI incorporates most of the functions of an In-Circuit Emulator on chip. ZDI allows the user to single step code, change registers, edit programs and view status of internal registers.

On-chip Crystal Oscillator

The eZ80 Webserver has an on-chip crystal oscillator that supplies clocks to both the internal eZ80 CPU core and peripherals and to an external pin. The clock circuitry uses three dedicated pins: EXTAL. XTAL and PHI.

Multiply Accumulator

The Multiply Accumulator on the eZ80 Webserver performs DSP functions without incurring the overhead associated with a separate DSP.

Feature include:

- A 16x16-bit multiplier feeds 32-bit product into one input of the adder. The other input of the adder is fed from one of two 40-bit accumulators.
- Two dual-port RAMs called X and Y. One port of each RAM is 16-bit read-only and feeds one side of the multiplier. The second port is 8-bit read/write and is connected to the microprocessor bus. This allows the RAM to simultaneously be part of the multiprocessor's memory space (von Neumnn) and constitute the X and Y banks of the Multiply Accumulator (Harvard).
- A set of registers in the microprocessor's I/O space start the Multiply Accumulator, determine when the Multiply Accumulator has completed a calculation, and retrieve the resulting accumulation. Software can provide calculation parameters to these registers.

Applications and Support Tools

The following development tools are available for the programming and debug of this device:

- Evaluation boards
- Embedded Internet Software Suite including TCP/IP stack and HTTP server
- Real Time Operating System
- C-Compiler
- ZiLOG Development Suite (ZDS) including, assembler, linker, debugger and simulator

Electrical Features Summary

- Power supply: 3.3 V ± 300 mV
- Temperature range: 0° C to 70° C
- Extended temperature range: -40° C to +85° C

Related Products

Other Integrated Controllers of interest are:

Z84C00	Z80™ CPU (up to 20 MHz)
Z84C15	Z80™ + 2 SIO + 4x8 CTC + 2 PIO + WDT (up to 16 MHz)
Z80S180	Improved Z80 + 1MByte MMU + 2 DMA +2-16bit PRT + 2 UARTs + CSIO (up to 33MHz)
Z80181	Z8S180™ (see above) + SCC+CTC+ 16 GPIO (up to 33MHz)
Z80182	Z8S180™ (see above) + 2 ESCC + 24 bit GPIO+ 16550 Mimic interface (up to 33MHz)
Z80189	Z8S180™ (see above) + 24 GPIO + 16550 Mimic interface (up to 33MHz)
Z80S188	Z8S180™ (see above) + 2 SIO + 4x8 CTC + 2 PIO + WDT+ POR + 4K Boot ROM + 1K SRAM

Ordering Information

Part	PSI	Description
Z80S190AZ050SC	50 MHz, Standard Temperature	eZ80
Z80S190AZ050EC	50 MHz, Extended Temperature	eZ80

Pre-Characterization Product

The product represented by this Product Brief is newly introduced and ZiLOG has not completed the full characterization of the product. The Product Brief states what ZiLOG knows about this product at this time, but additional features or nonconformance with some aspects of the CPS may be found, either by ZiLOG or its customers in the course of further application and characterization work. In addition, ZiLOG cautions that delivery may be uncertain at times, due to start-up yield issues.

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