called a register pointer

→ This is one of the address reg

Eg MOVE.L (A0), D2 → [D2] ← [M([A0])]

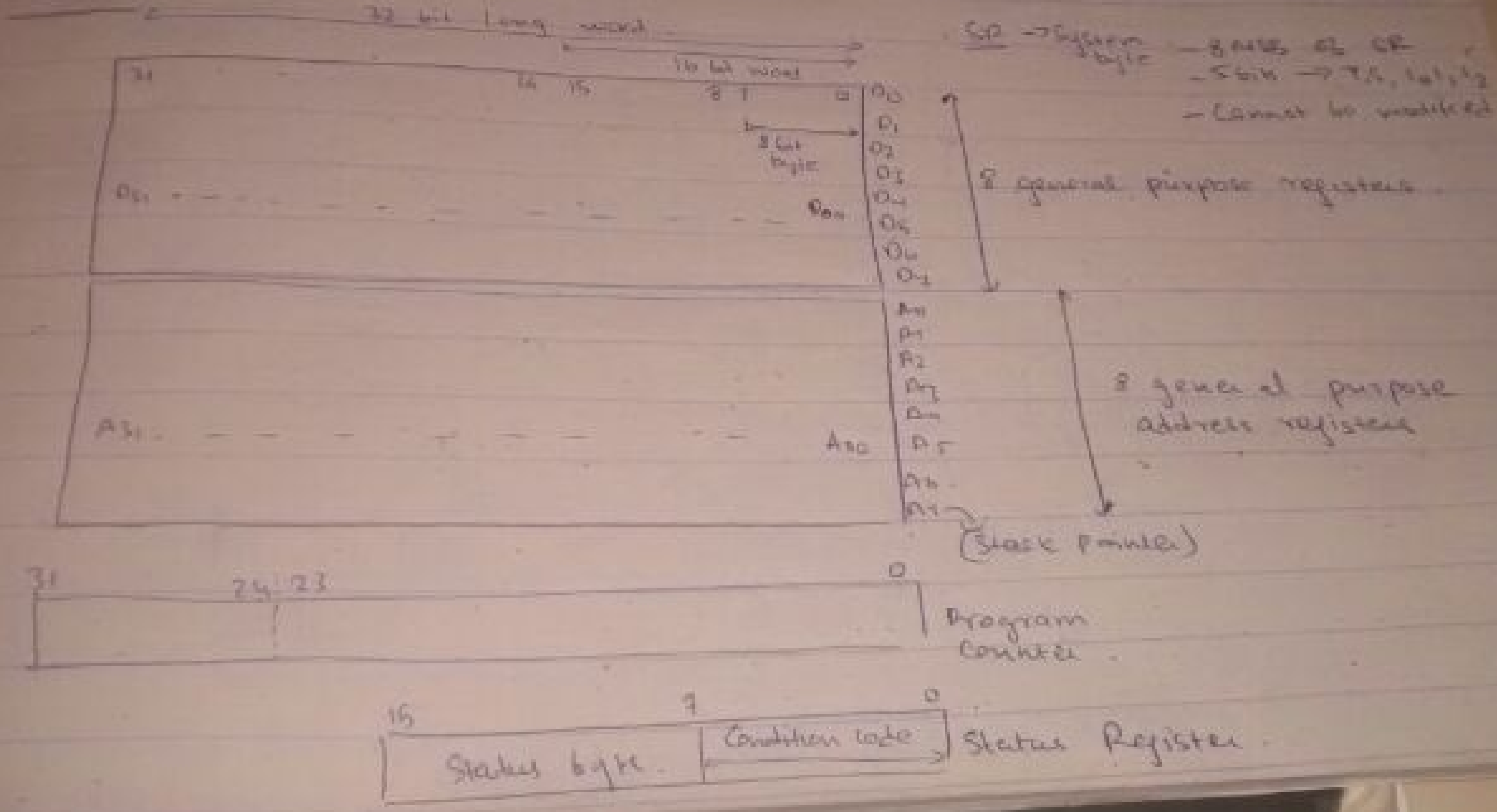
(5) Programmer Model of 68k

Rest of program counter & System byte of SR

PC → 32 bit wide & contains address of the next instruction to be executed
→ enables look ahead

SR → System byte
– 8 MSB of SR
– 5 bit → T, S, I0, I1, I2
– cannot be modified

<u>Model :-</u>



④ 68000

① Absolute addressing mode

→ Instruction directly contains the operand address

Eg MOVE.L D3, $1234 → [M($1234)] ← [D3(16-31)]
[M($1236)] ← [D3(0-15)]

② Address Register Indirect Add Mode

→ Address of an operand in the register
→ Register will be called a register pointer
→ This is one of the address reg.

Eg MOVE.L (A0), D3 → [D3] ← [M(A0)]

⑤ Programmers Model of 68k

Role of program counter & System byte of SR

PC → 32 bit wide & contains address of the next instruction to be executed

② SMM
(System Management Mode)

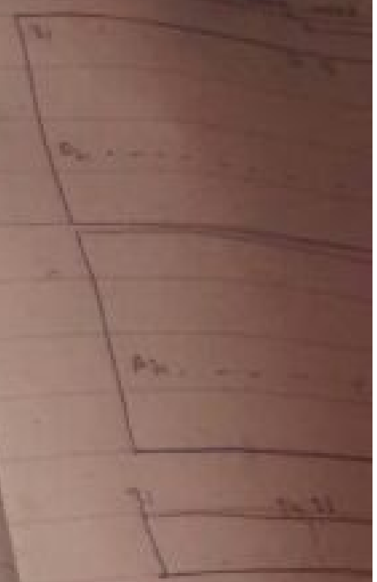
Simplifies the system
Same level as protected mode, real & virtual mode
Functions as manager
o Functions - power management, security

① Access → new external hardware applied on SMI when activate processor
② executes system level software in area of memory
③ called System Management RAM (Relocates SMRAM before normal
④ → SMI - disables interrupts
→ Return from SMM is with RSM, returns to intr program
executes that auto restart & I/O trap

Stores state of pentium in dump record - Helps to enter a sleep mode & reactivate at point of interruption.

Used before normal OS is placed in memory.

Model –



The McGraw-Hill

(2)

(c) APIC :-

(Advance Rogammable Interrupt Controller)

↳ Provides interrupt support for SMP implementation

↳ Consist of 2 distinct elements — I/o APIC & local APIC

APIC bus connects all APIC agents, allow routing of interrupt message

APIC id Unique id used by all APIC agents during transfer

First developed by intel & replaces 8259 interrupt controller

Used for dual or multiprocessing

Add support for multiple processor

(2) SMM :-

(System Management Mode)

a) Parity

PERR - checks if there is an error in during read o/p i.e DP 0/3

DP0-3 - generated even parity bit for each byte

- Compares parity with DP sig.

parity generation/ detection for Memory R/W

b) Bus Control :-

ADS - Becomes 0 to show address bit has valid memory

BD4 - Non burst cycle is complete so stop MP from wait state into timing

c) Bus Arbitration

1. HOLD
2. HLDA
3. BUSY
4. BREQ

Same as 1

d) Interrupts :-

INTR -
RESET -
NMI -

Same as 8086

e) Data bus :-

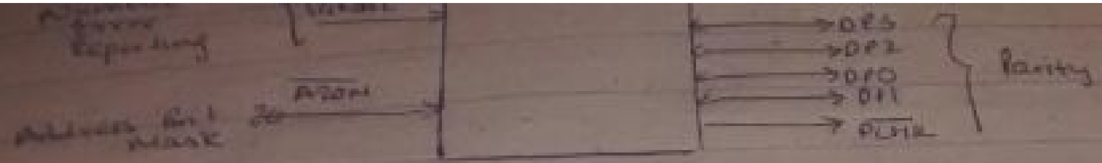
Output data.

BE3 → D31-24

BE2 → D23-16

BE1 → D-15-8

BE0 → D-7-0



c) Bus Size Control :-

$\overline{BS16}$ - Structure that size to bus word mode

$\overline{BS8}$ - Bus size 8 byte mode

b) Bus Arbitration :-

1. Hold - Another master req access.
2. HLDA - After recieving hold next clock cycle.
3. $\overline{BOFF}$ - High impedance state.
4. BREQ - internal bus req of 80486

a) Bus Cycle Definition :-

1. M/$\overline{IO}$ - Memory or I/O
2. D/$\overline{C}$ - Data R/W or Control word transfer
3. W/$\overline{R}$
4. LOCK, PLOCK - Output → 0 ~~...~~ current o/p more than 1 bus cycle

MP Assignment 5

10 Signal block diagram for 80486