TECHNISCHE UNIVERSITÄT DRESDEN

Fakultät Informatik Institut für Technische Informatik, Professur für VLSI-Entwurfssysteme, Diagnostik und Architektur

Brief Description of the Terasic DE0 Board

1 FPGA

Altera Cyclone® III 3C16 FPGA
Designation: `EP3C16F484C6`

2 Pin Assignments for I/O Devices

Operating voltage for I/O Pins (unless otherwise specified): `3.3-V LVTTL`

2.1 Clock

50 MHz *(primary)*	50 MHz *(secondary)*
(G21)	(B12)

2.2 Buttons

The buttons are low-active. Depending on board revision buttons may be debounced. Assume buttons beeing not debounced.

BTN2	BTN1	BTN0
(F1)	(G3)	(H2)

2.3 Switches

The switches are high-active and not debounced.

SW9	SW8	SW7	SW6	SW5	SW4	SW3	SW2	SW1	SW0
(D2)	(E4)	(E3)	(H7)	(J7)	(G5)	(G4)	(H6)	(H5)	(J6)

2.4 LEDs

Each LED is driven directly by an I/O pin on the Cyclone III FPGA (i.e. LEDs are high-active).
Current strength: `8 mA`
Slew rate: `2`

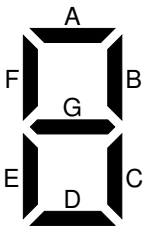
LEDG9	LEDG8	LEDG7	LEDG6	LEDG5	LEDG4	LEDG3	LEDG2	LEDG1	LEDG0
(B1)	(B2)	(C2)	(C1)	(E1)	(F2)	(H1)	(J3)	(J2)	(J1)

2.5 7-Segment Display

Each of the 4 digits consists of 7 segments and a dot. The individual segments are enabled through the LED's cathode (low-active).

Segment Selection (Cathode Control)

	A	B	C	D	E	F	G	Dot
Digit 3	(B18)	(F15)	(A19)	(B19)	(C19)	(D19)	(G15)	(G16)
Digit 2	(D15)	(A16)	(B16)	(E15)	(A17)	(B17)	(F14)	(A18)
Digit 1	(A13)	(B13)	(C13)	(A14)	(B14)	(E14)	(A15)	(B15)
Digit 0	(E11)	(F11)	(H12)	(H13)	(G12)	(F12)	(F13)	(D13)



2.6 PS/2 Connector

Default		**Extension**	
CLK	DATA	CLK	DATA
(P22)	(P21)	(R21)	(R22)

For using two PS/2 devices simultaneously an extension PS/2 Y-Cable is needed.

2.7 VGA Connector

RGB signals are high-active, sync signals low-active.

Red			
Red[3]	Red[2]	Red[1]	Red[0]
(H21)	(H20)	(H17)	(H19)

Green			
Green[3]	Green[2]	Green[1]	Green[0]
(J21)	(K17)	(J17)	(H22)

Blue			
Blue[3]	Blue[2]	Blue[1]	Blue[0]
(K18)	(J22)	(K21)	(K22)

Sync	
HSync	VSync
(L21)	(L22)