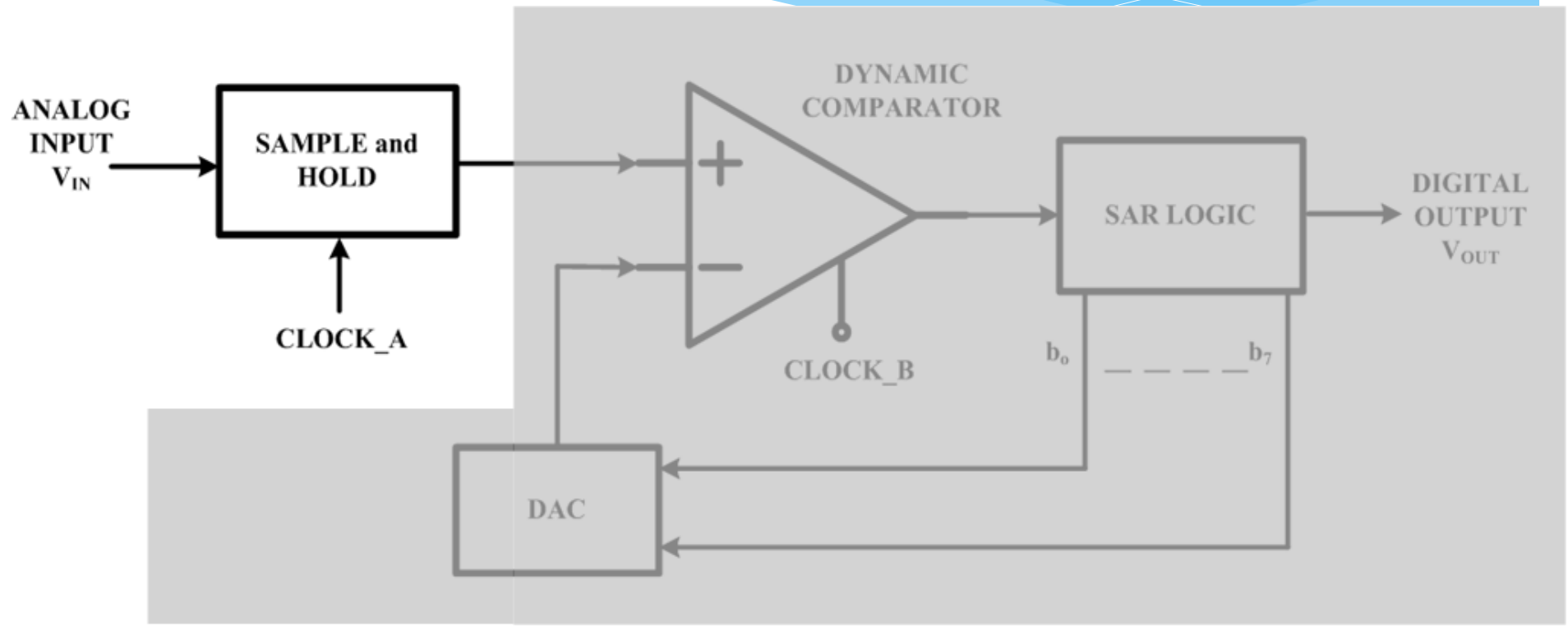
Sample and Hold



Sample and Hold

Sample and Hold – contains a switch and a capacitor.

Tracking Mode – sampling signal is high, switch is ON

- tracks the analog input signal

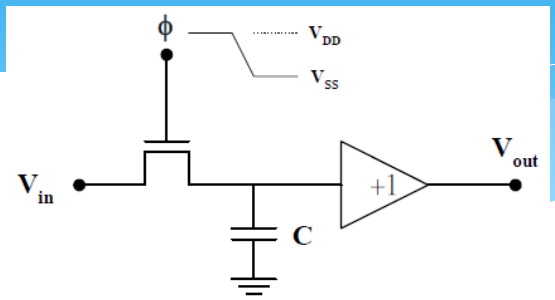
Hold Mode – sampling signal is low, switch is OFF

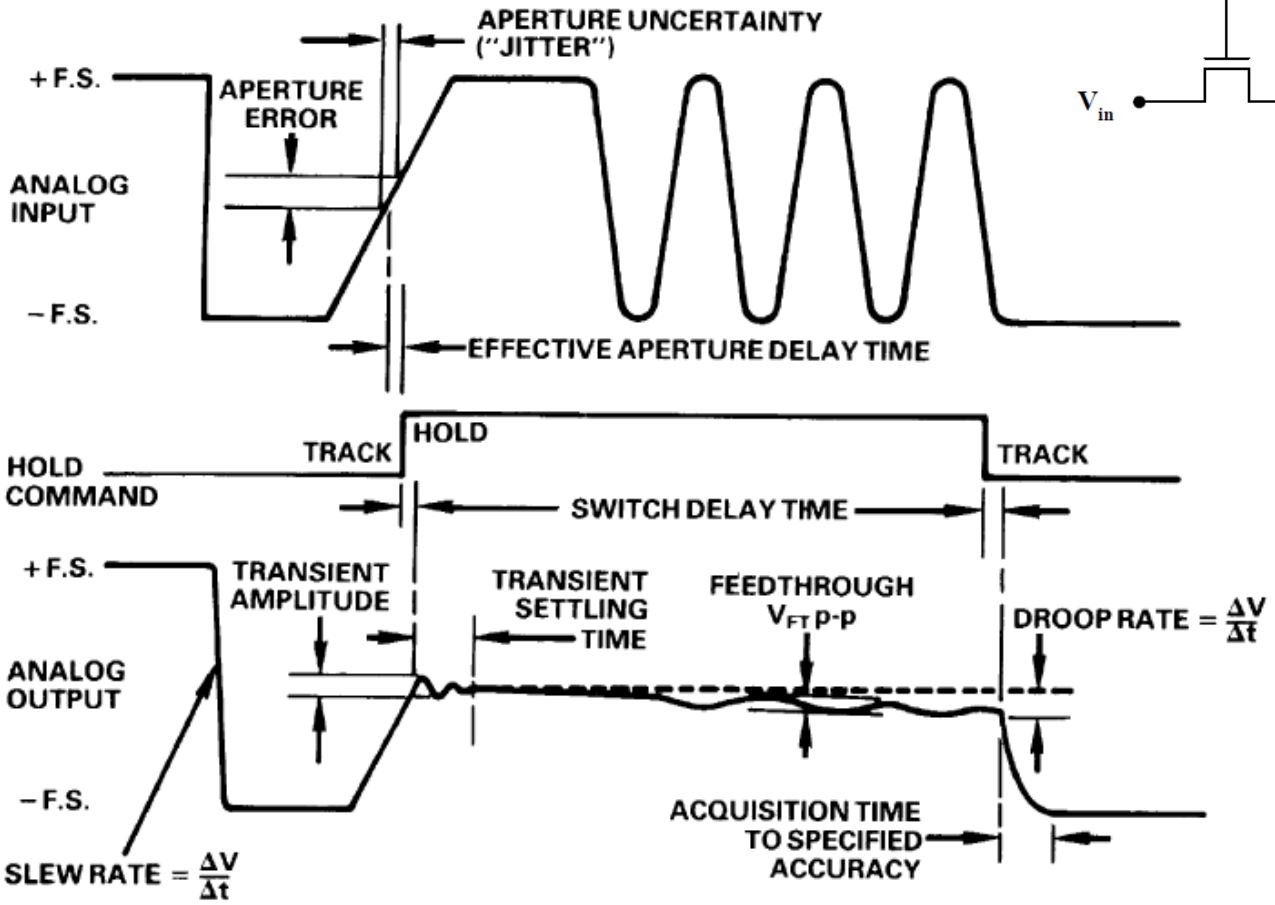
- holds the value

Sampling operation has a great impact on the dynamic performance of the ADC such as SNDR

Sample and Hold

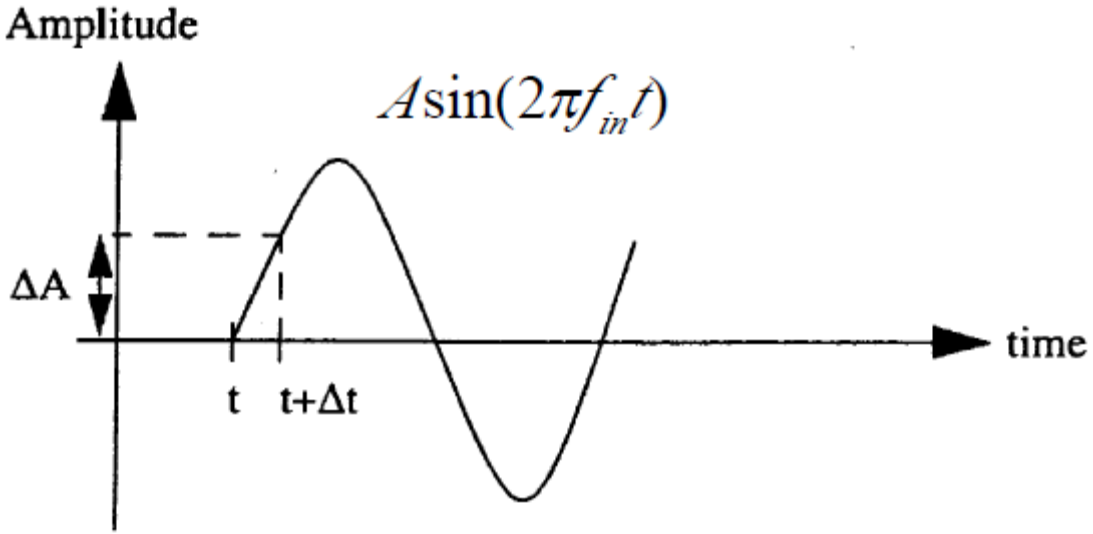
Sampling Time Uncertainty





Sample and Hold

Effects of Sampling Time Uncertainty



Peak Error

$$\Delta A_{\max} = \Delta t \cdot \frac{\partial}{\partial t} V_{in}(t)\,|_{t=0} = 2\pi f_{in} A\cos(2\pi f_{in} t)\Delta t\,|_{t=0} = 2\pi f_{in} A \Delta t$$

Sample and Hold

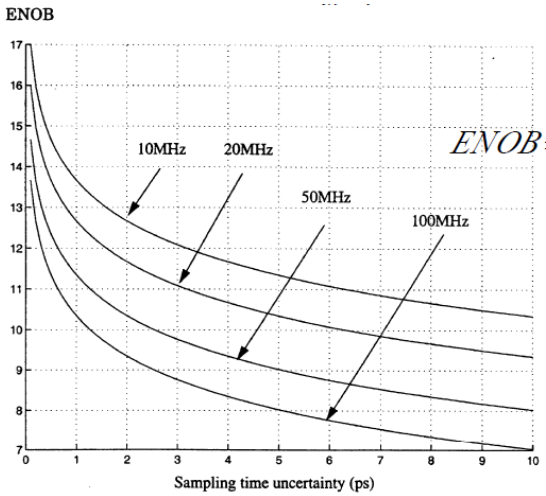
SNDR

Assuming the clock jitter in the switch is a random noise with variance σ_t^2 , one has the error power given by

$$v_{jn}^{\ 2} = \sigma_t^2 \frac{1}{T}\int_0^T \left(\frac{\partial}{\partial t} V_{in}(t)\right)^2 dt = (2\pi f_{in} A)^2 \sigma_t^2 / 2$$

The SNDR is limited by

$$SNDR = 10\log\frac{1}{(2\pi f_{in}\sigma_t)^2}$$



$$ENOB = \frac{10\log\frac{1}{(2\pi f_{in}\sigma_t)^2} - 1.76}{6.02}$$

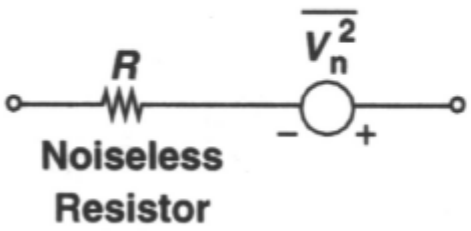
Sample and Hold

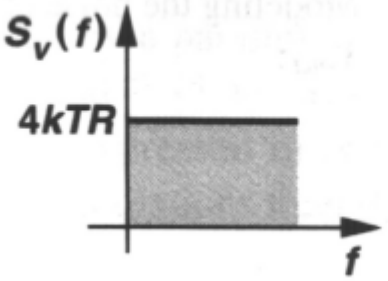
- Nonlinearity

  - the nonlinearity of the input S/H must be at least as good as the resolution of the ADC.

- Thermal Noise

  a) Thermal noise of the resistor





$$V_n^2(f) = 4kTR$$

k: Boltzmann's constant

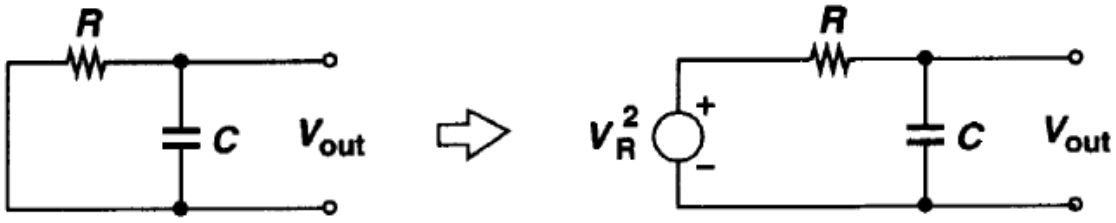
$(1.38 \times 10^{-23}\ \mathrm{JK}^{-1})$

T: absolute temperature

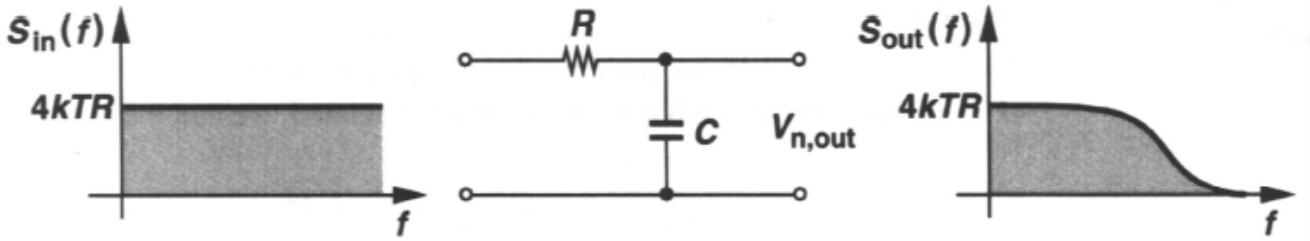
Sample and Hold

- Thermal Noise

  b) Noise filtering



$$H(s) = \frac{1}{RCs+1} = \frac{1}{1+s/2\pi f_o} \qquad \text{where } f_o = \frac{1}{2\pi RC}$$



Noise spectrum shaping by a low-pass filter

Sample and Hold

- Thermal Noise

  b) Noise filtering

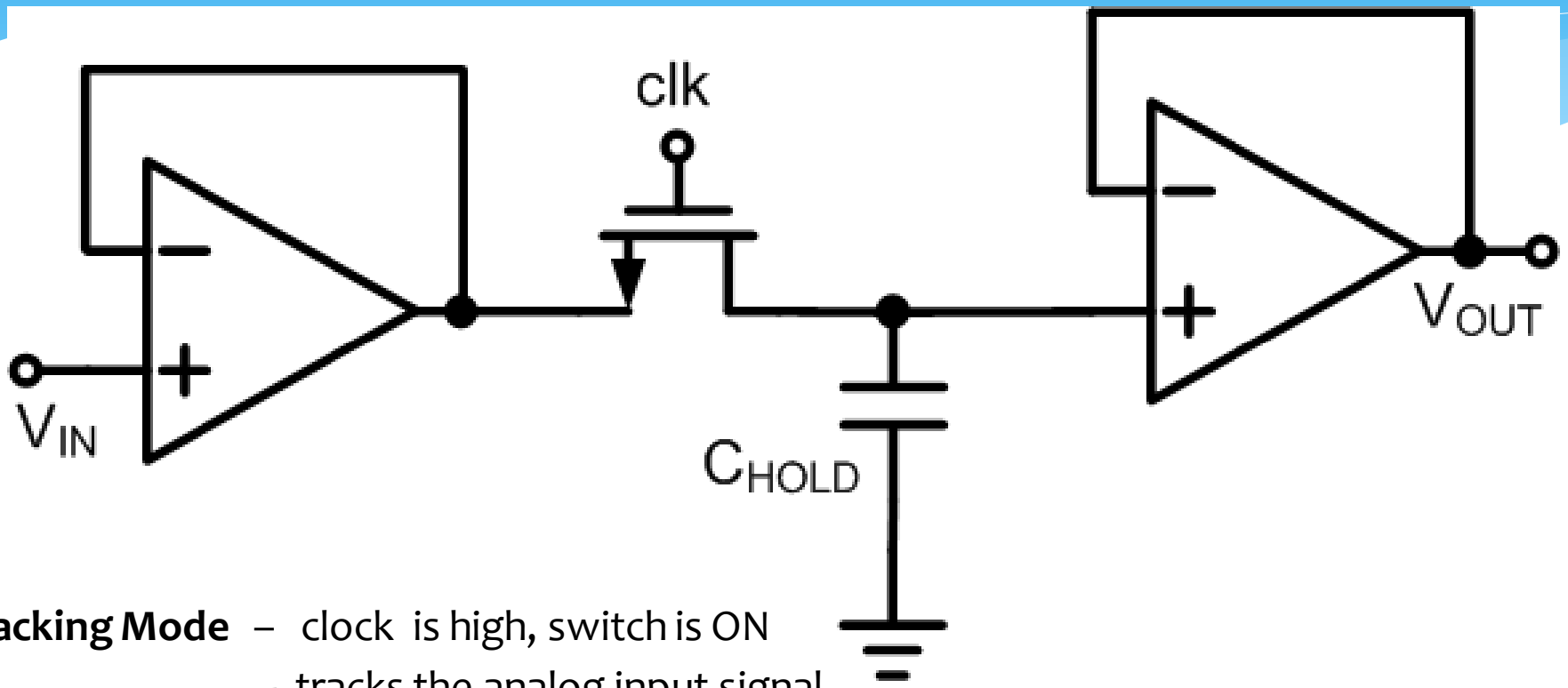
$$|H(f)| = \sqrt{\frac{1}{1+(f/f_o)^2}}$$

$$V_{n,out(rms)}^{\ 2} = \int_0^{\infty} \frac{V_R^{\ 2}}{1+(f/f_o)^2} df = V_R^{\ 2} f_o \tan^{-1}\left(\frac{f}{f_o}\right)\Big|_0^{\infty}$$

$$= V_R^{\ 2}\left(\frac{\pi f_o}{2}\right) = \frac{kT}{C}$$

$$SNR = 10\log\left(\frac{V_{in}^{\ 2} C}{2kT}\right)$$

Sample and Hold



Tracking Mode – clock is high, switch is ON
- tracks the analog input signal

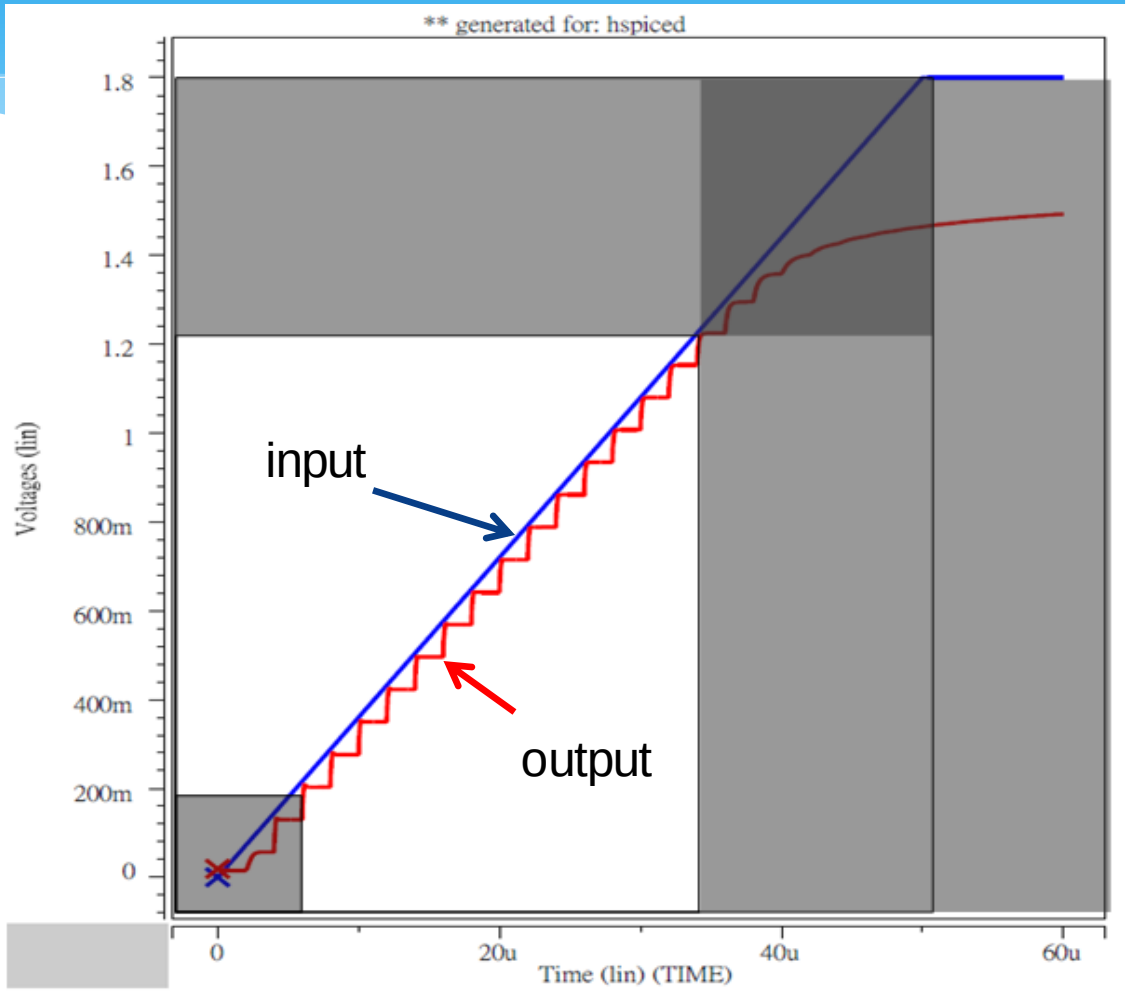
Hold Mode – clock is low, switch is OFF
- holds the value

Sample and Hold Simulation Result

Sample and Hold uses an PMOS input pairs

Can operate well at the input range from

200mV to 1.1V



Activity Number 3: Sample/Hold Circuit

1. Simulate a sample/hold circuit.
2. From the given circuit diagram in slide number 9,

Simulate the following:

a. S/H circuit with an ideal op-amp

b. S/H circuit with your own op-amp

Prepare a progress report during the ECE132.1 class

Submit a technical report once you are done with the activity.

Thank you!!!