CSE 577 Spring 2011

Sample & Hold Circuits

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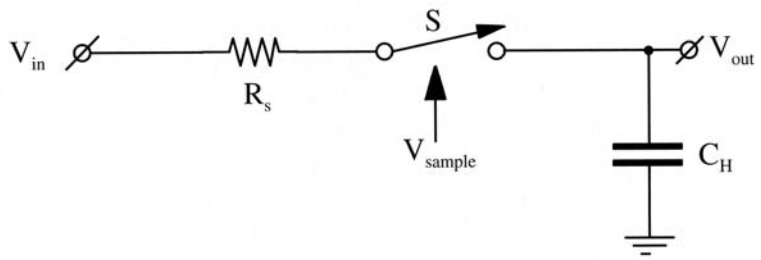
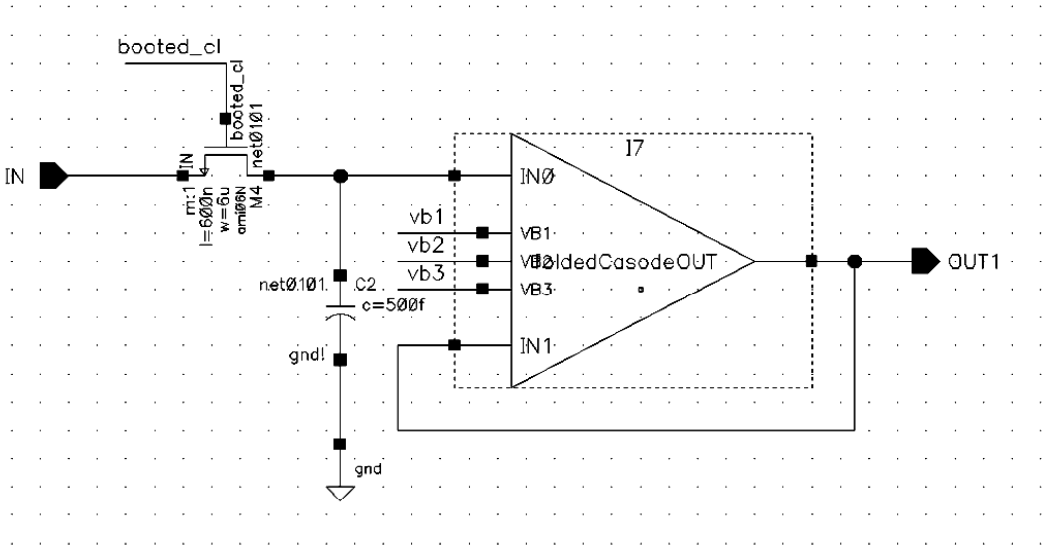
Basic Sample and Hold Circuit Configuration

- Concept



- MOSFET S&H Circuit

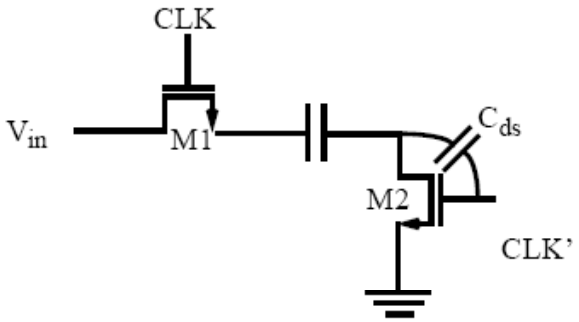


Design Issues of CMOS S&H

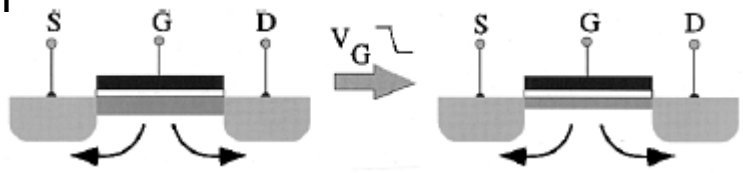
- Sampling Moment Distortion
  - Finite Clock rising/falling time results in distortion

$$\Delta t_s = 2\frac{a}{V_{clock}} t_{rise}$$

- Clock Feed-through
  - Overlap cap. of MOS Switch creates an sampling error during clock transition time

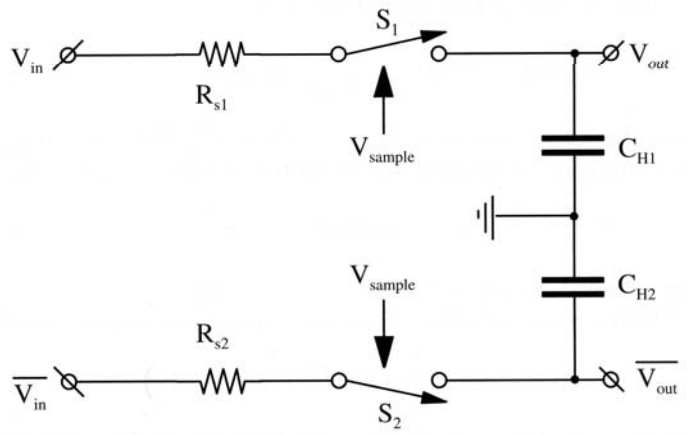


- MOS Switch Charge Injection
  - Some charge in the MOS channel flow to Source and Drain, then result in an error.
  - $\Delta Q = C_{ox}(V_{GS} - V_{Th}), \qquad \Delta V_{hold} = \frac{\Delta Q}{C_H}$



Solutions for Reducing Sampling Distortion

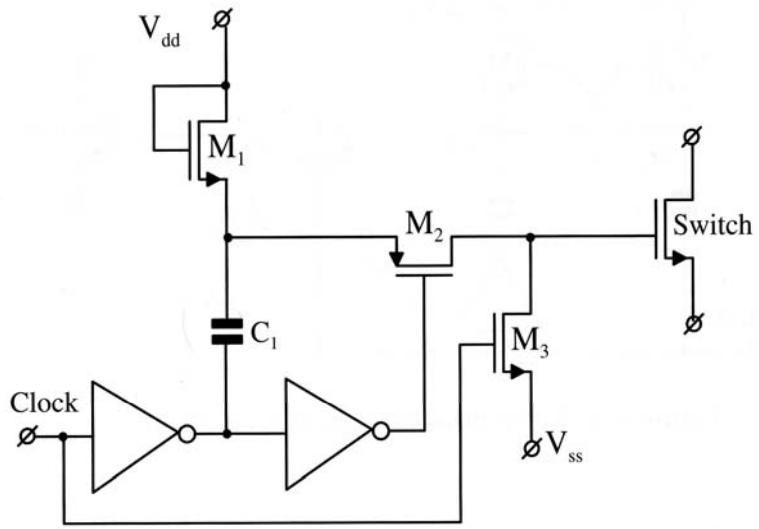
- Differential S&H Circuit

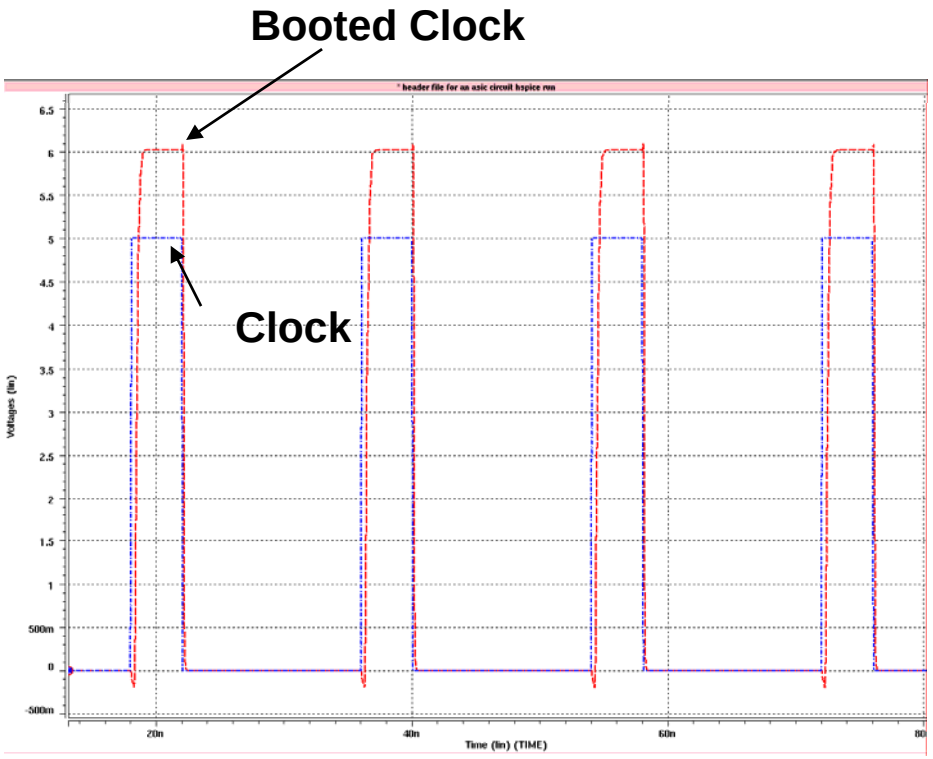


- Sample Clock Bootstrapping
  - Sampling distortion can be reduced by increasing clock amplitude

Sample Clock Bootstrap Circuits (I)

- Basic clock bootstrap circuit

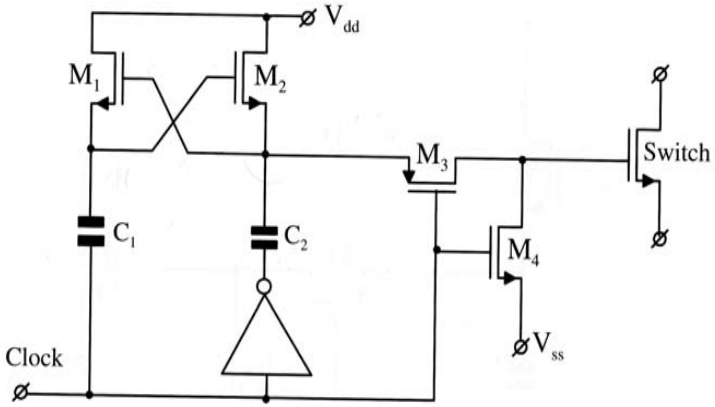


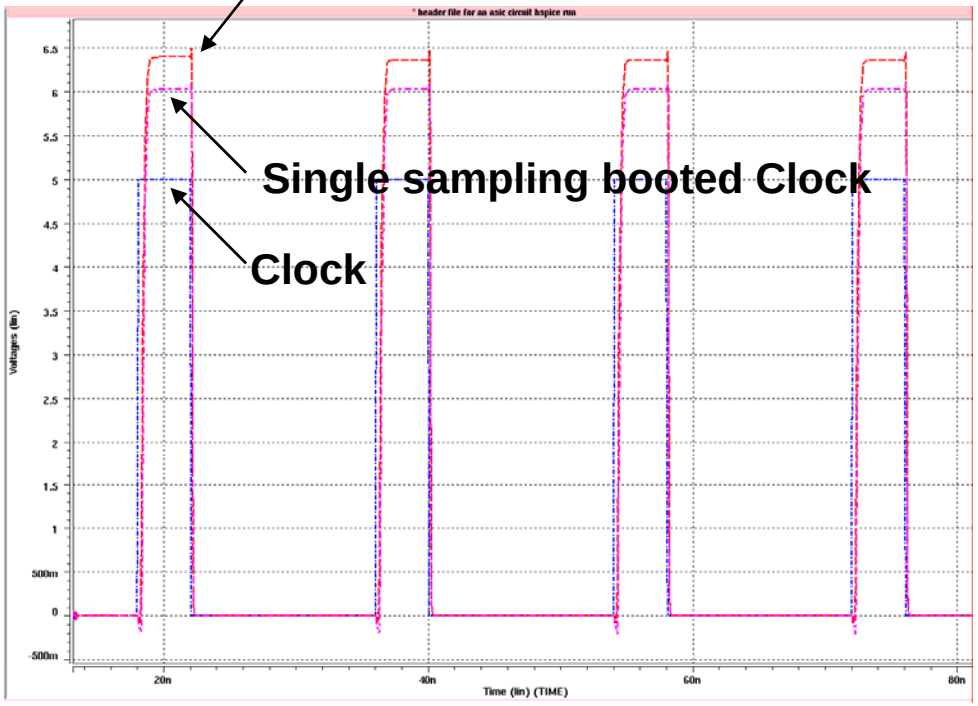


Simulation Result

Sample Clock Bootstrap Circuits (II)

- Differential sampling clock bootstrap circuit

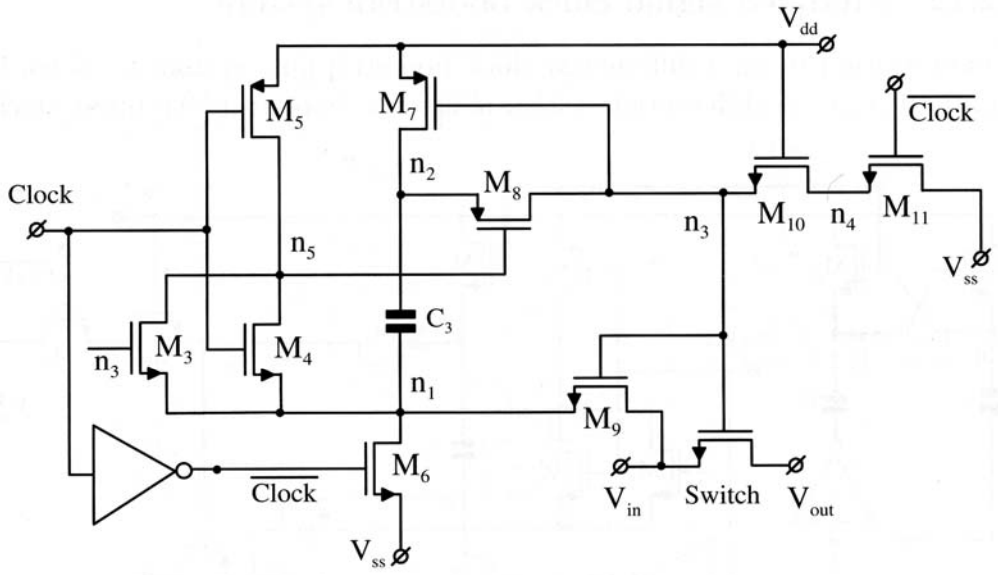




Simulation Result

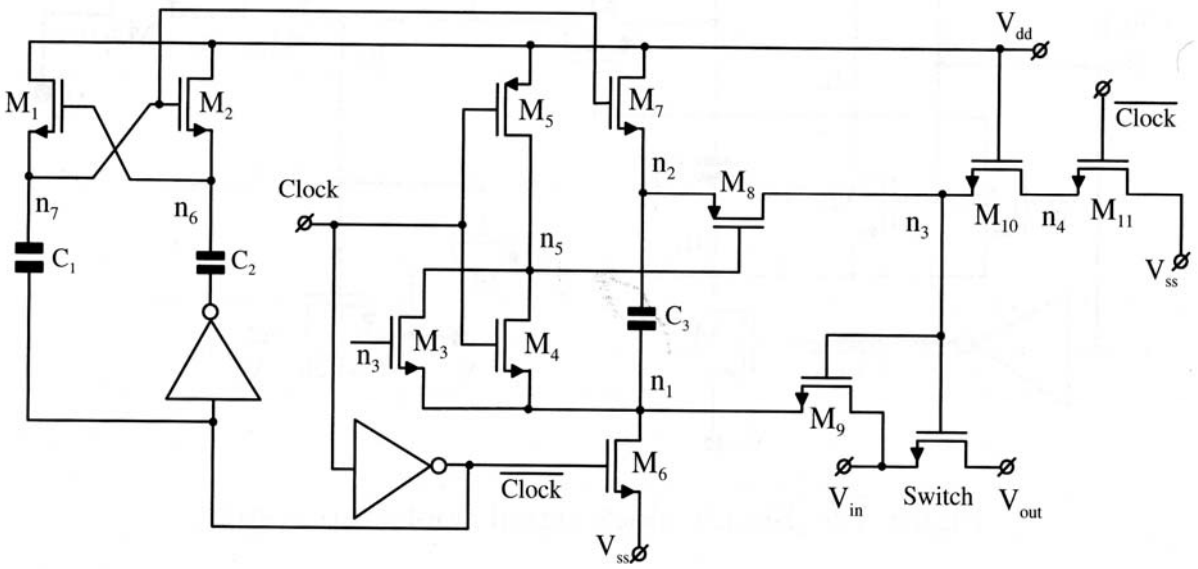
Signal Dependent Clock Bootstrapping (I)

- The problem of clock bootstrap circuit
  - Vgs of MOS switch can vary according to the input voltage level
  - → Ron of MOS Switch also vary
  - → It can cause an error in holding voltage
- Signal Dependent clock bootstrap circuit



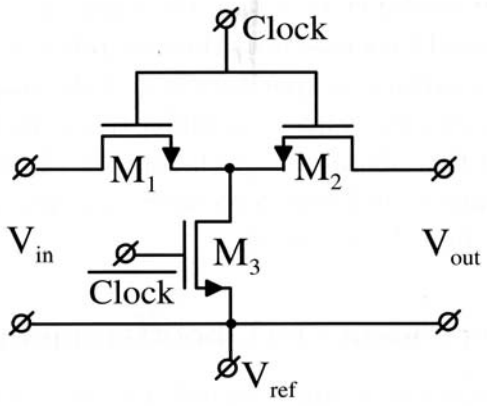
Signal Dependent Clock Bootstrapping (II)

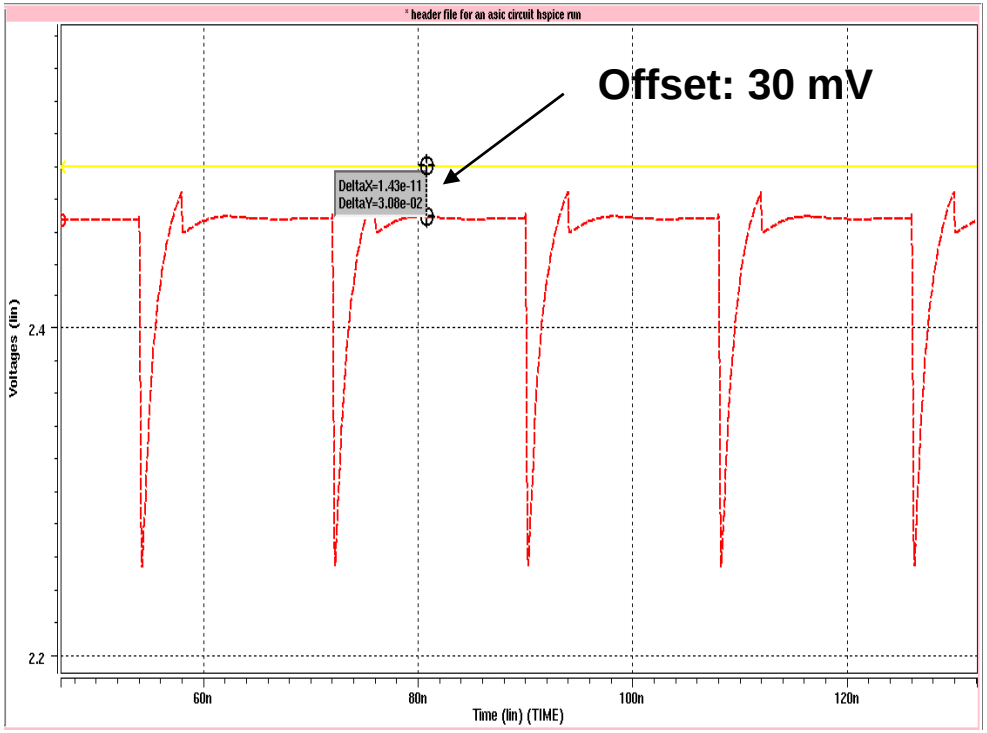
- Modified Circuit



Low Signal Feed-through Switch

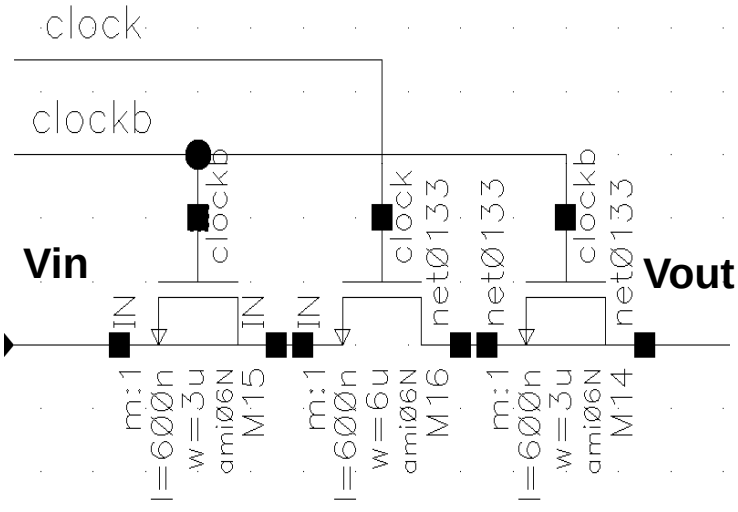
- Schematic

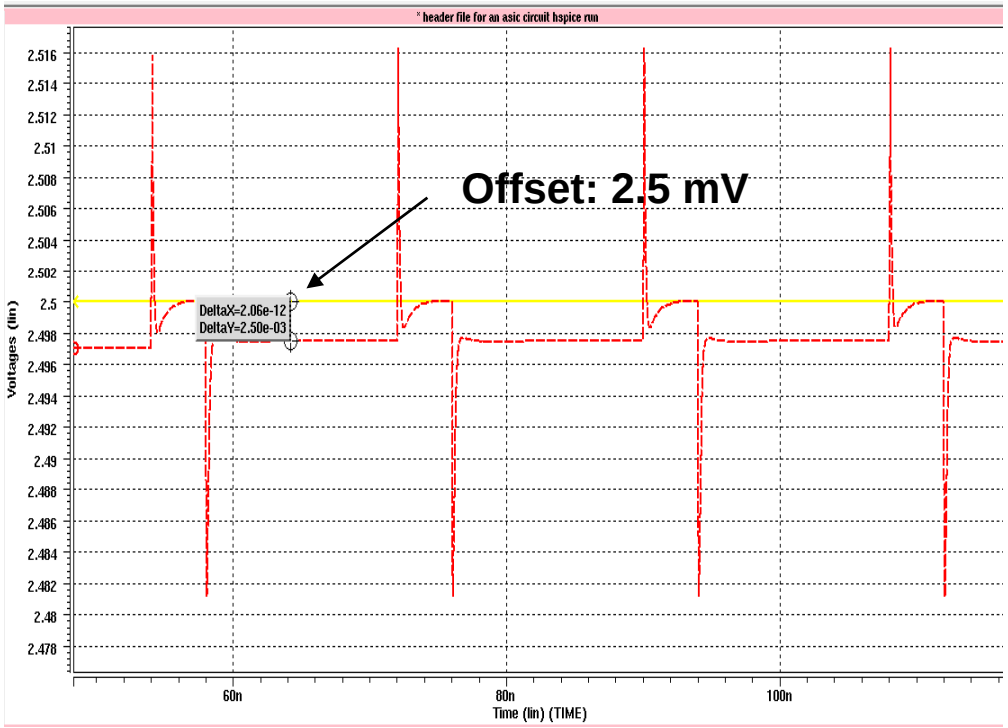




Simulation Result

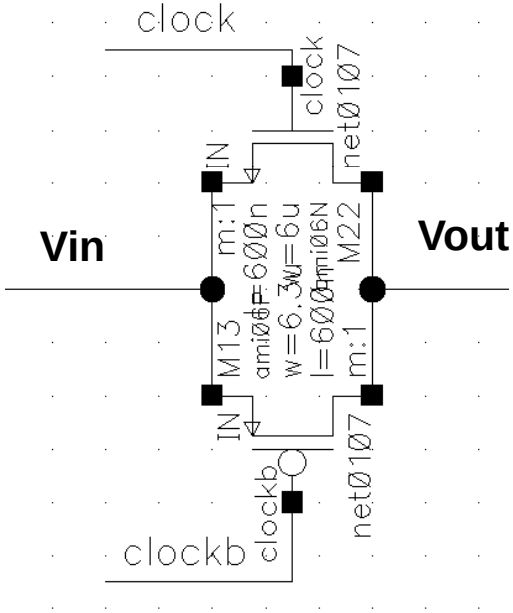
Charge injection Compensation Switch (I)

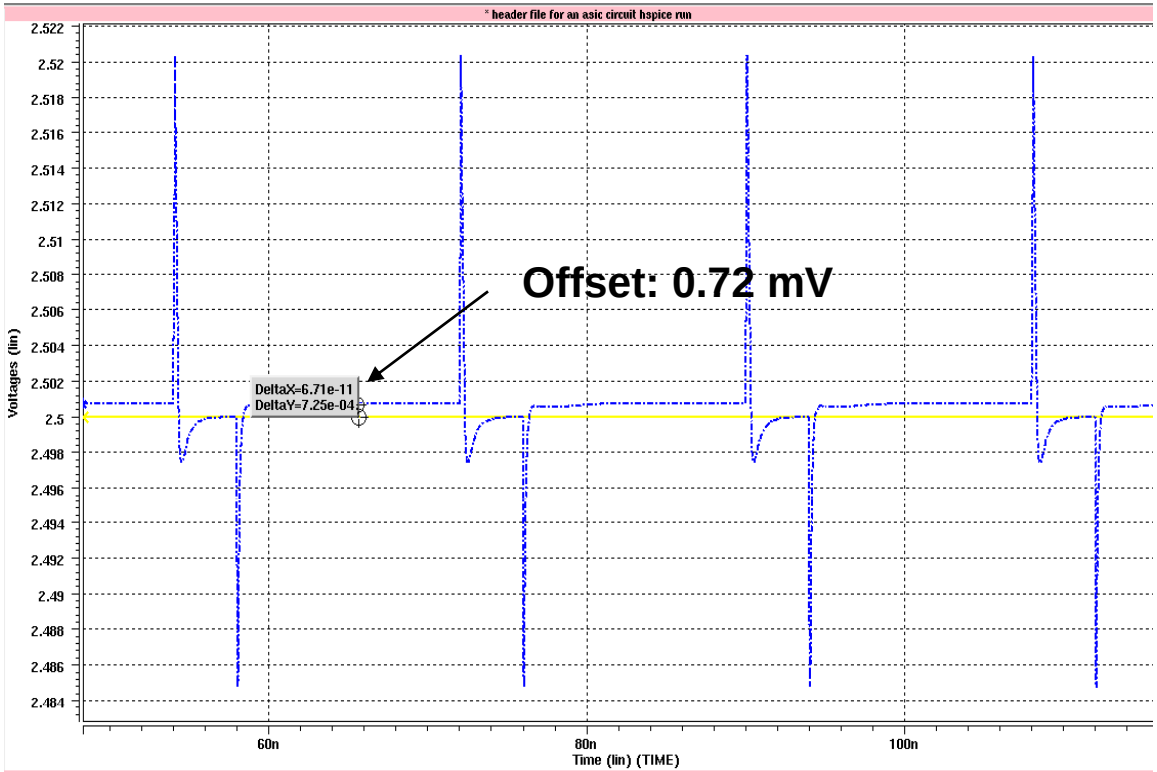




Simulation Result

Charge injection Compensation Switch (II)

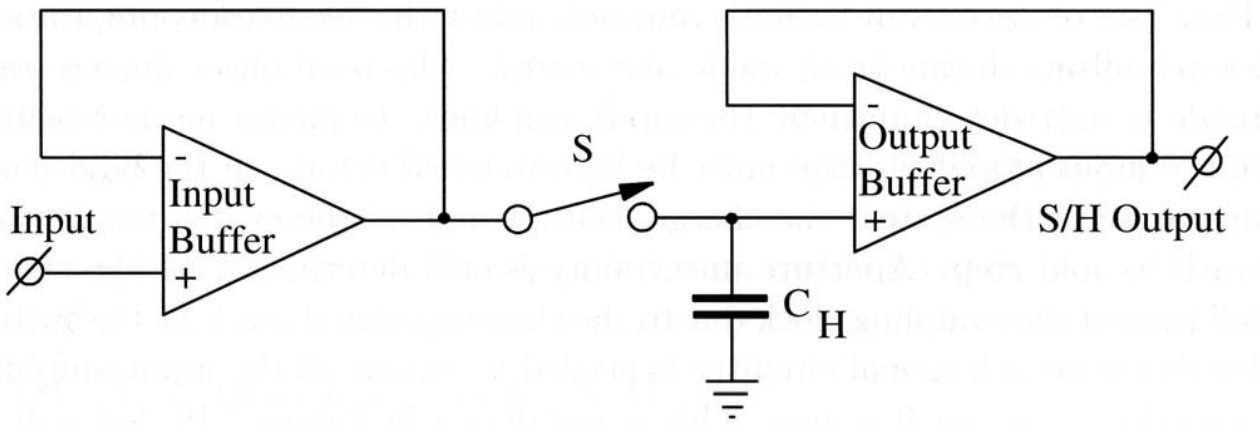




Simulation Result

Actual Implementation S&H Circuits

Double Buffered S&H Configuration



Advantages:

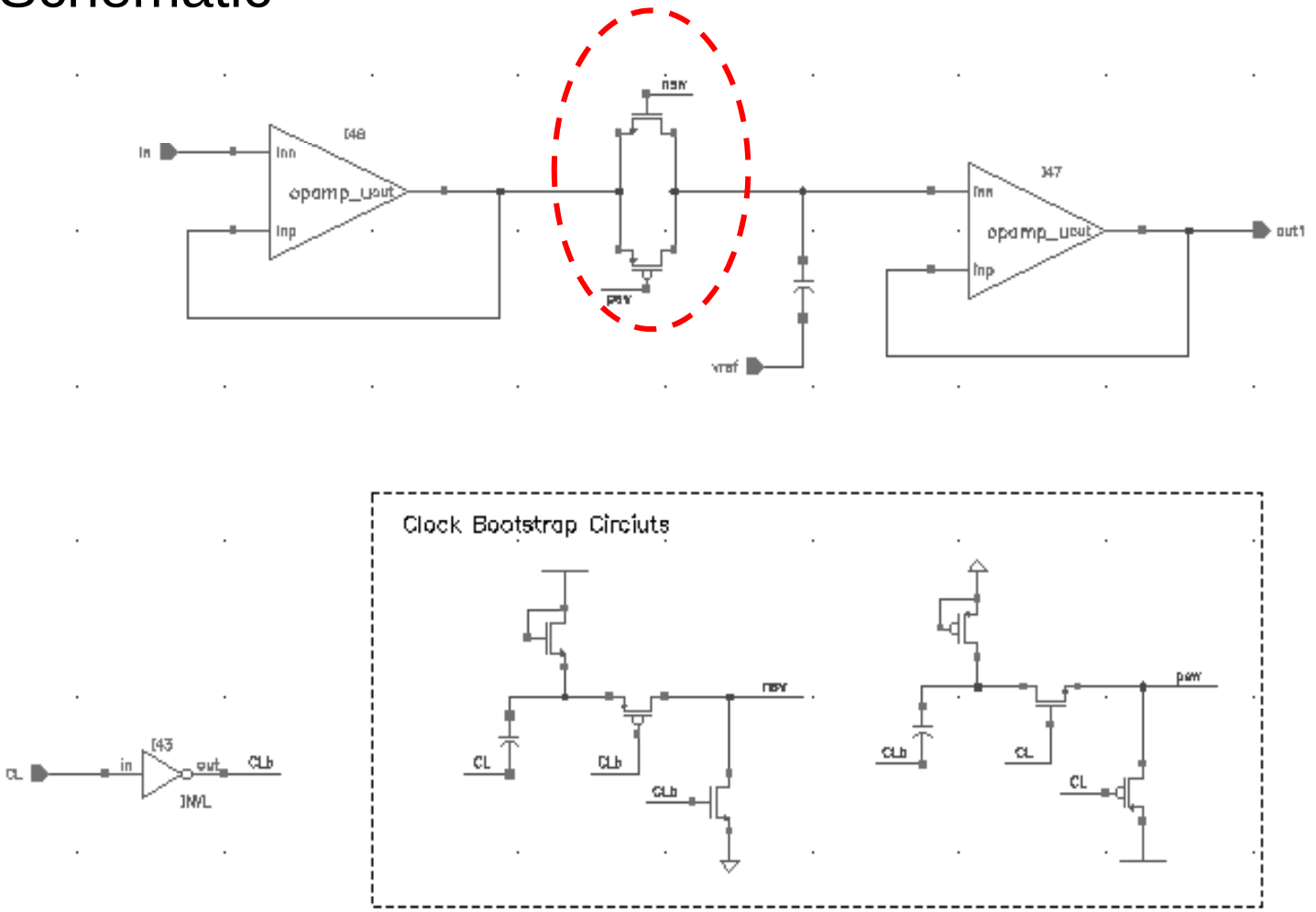
- Obtain a low droop rate during holding mode
- Stability is determined by the stabilities of OP Amps

Disadvantages:

- OP Amps offset can constrain the accuracy of SHA

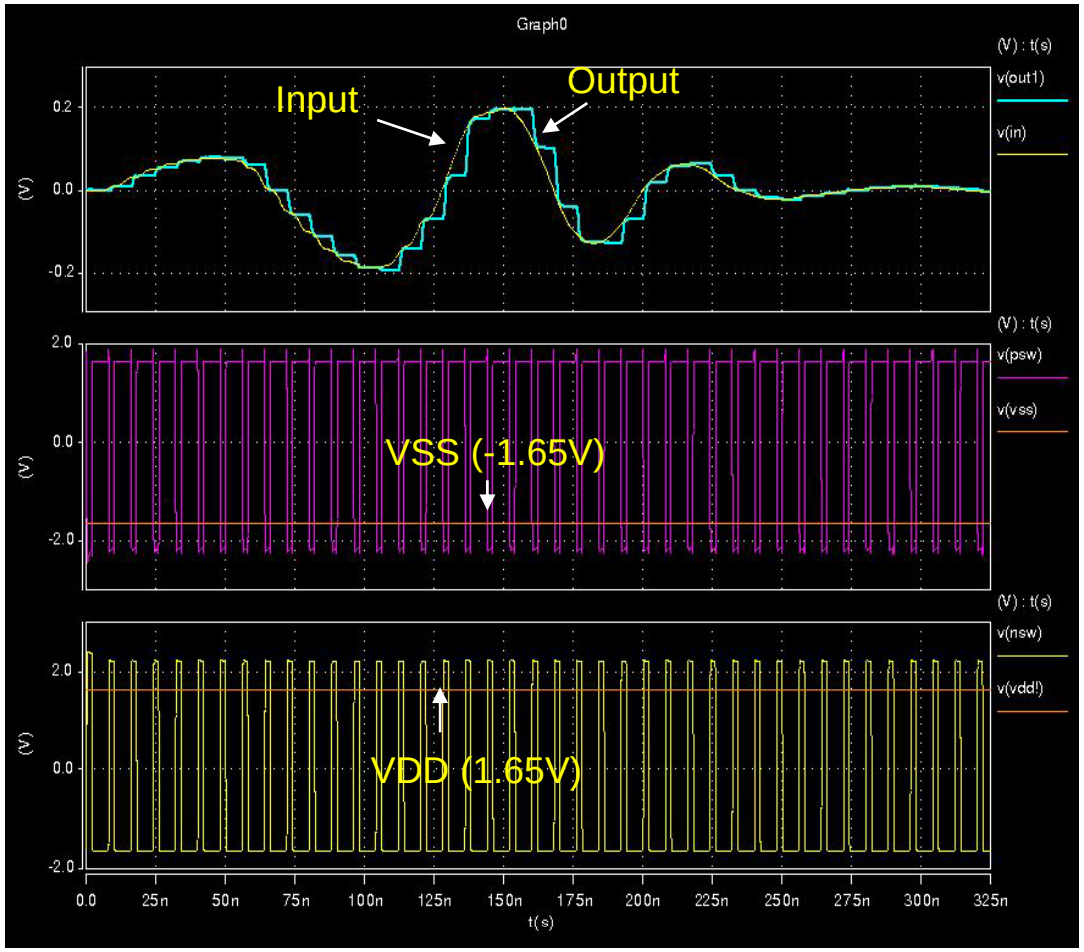
Double Buffered S&H Circuit with CMOS Switch

- Schematic

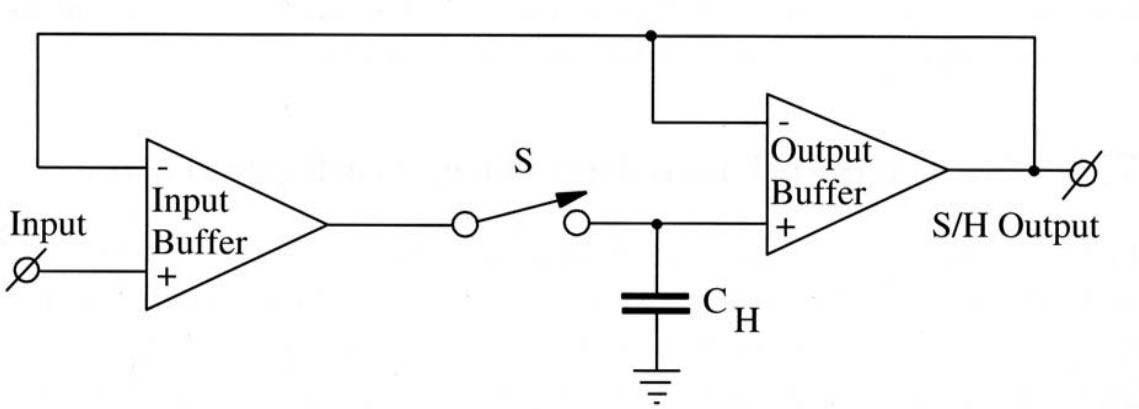


Double Buffered S&H Circuit with CMOS Switch

- Simulation Result



Feedback Improved S&H Circuit



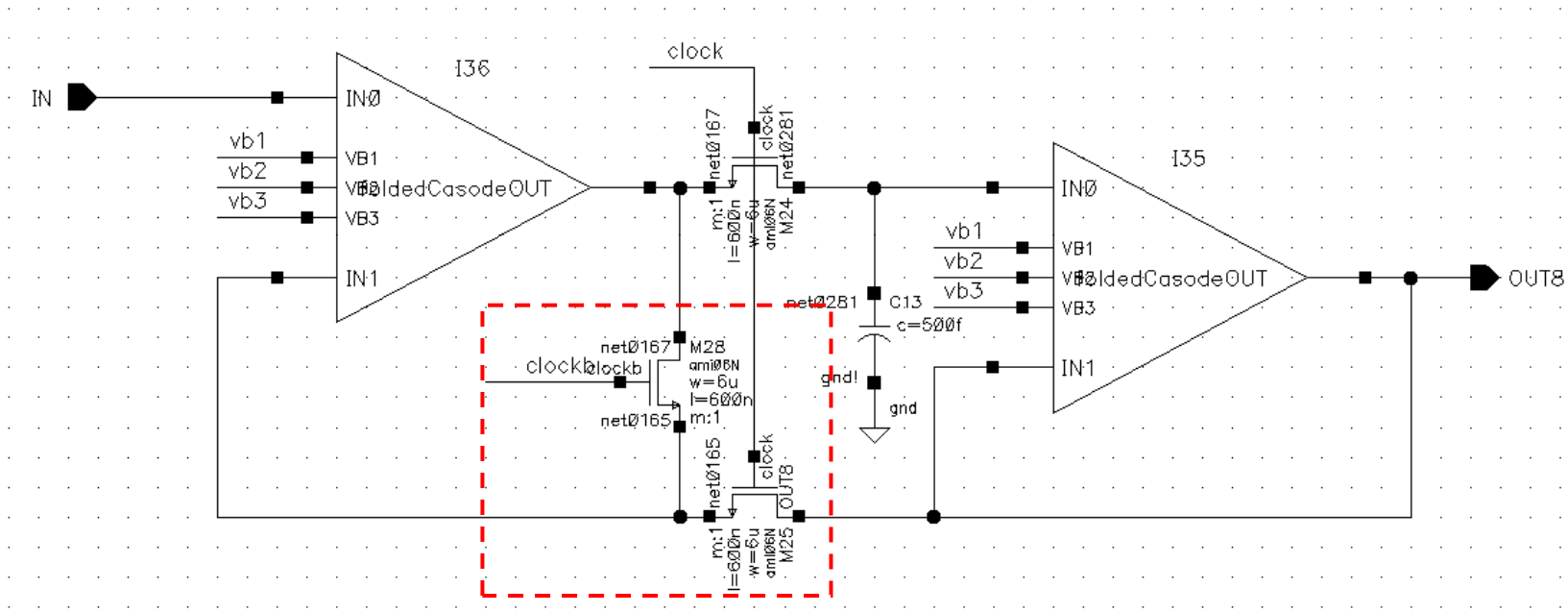
Advantages:

- Offset free → More accurate than double buffered SHA

Disadvantages:

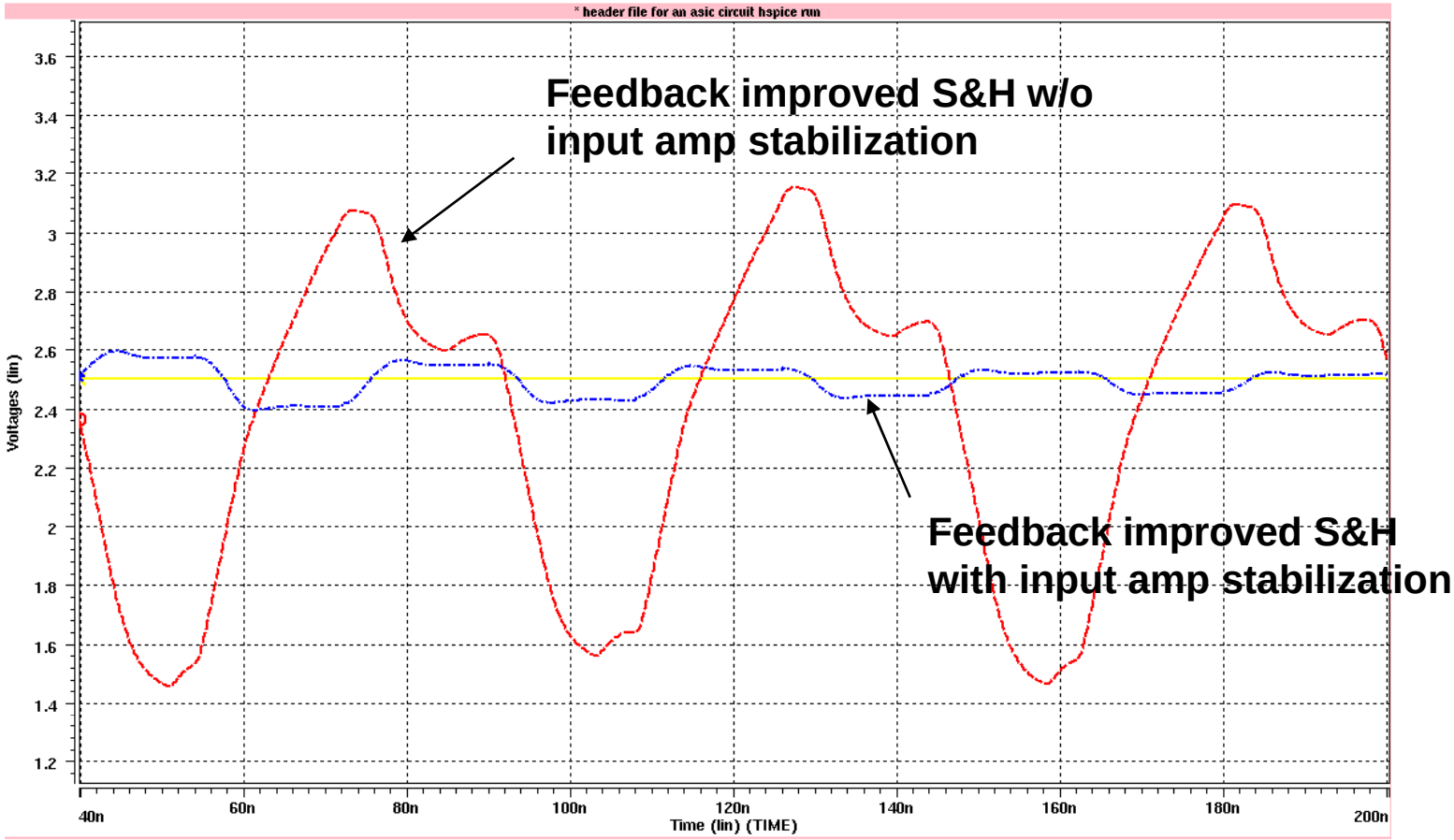
- Common Mode Rejection of the Input OP amp must be high
- Special Care must be taken to obtain stability of SHA
- Needs a special circuitry to stabilize the input amplifier during the holding mode

(cont'd) Feedback Improved S&H Circuit



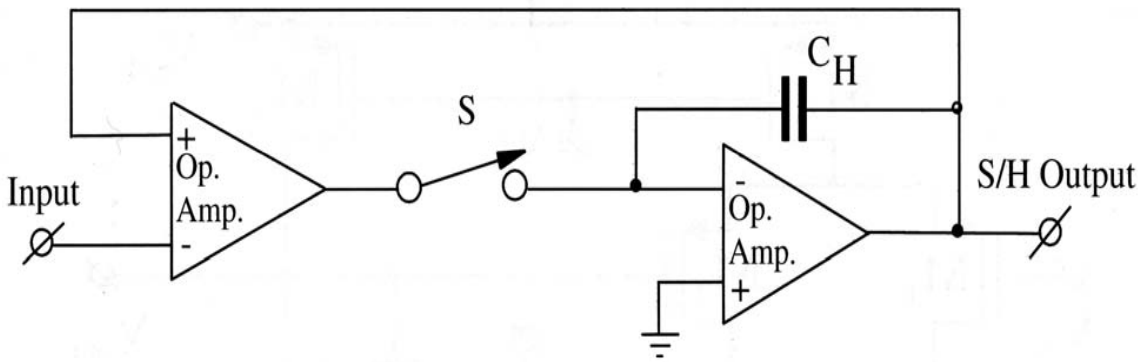
Simple stabilization circuit for input amplifier

(cont'd) Feedback Improved S&H Circuit



Simulation Result

Integrating S&H Circuit



Advantages:

- Switching moment and charge feed-through can be controlled very well

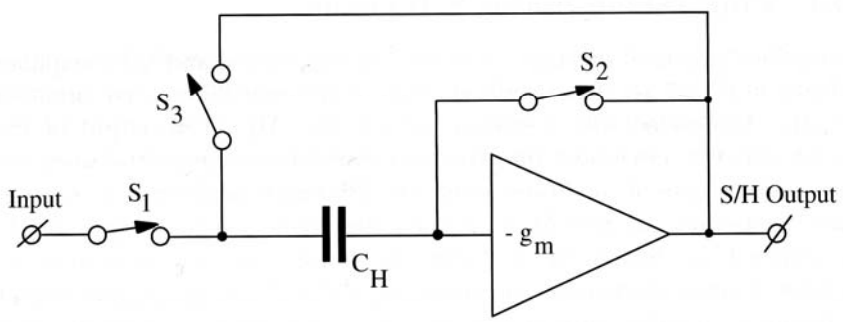
Disadvantages:

- Common Mode Rejection of the Input OP amp must be high
- Special Care must be taken to obtain stability of SHA
- Needs a special circuitry to stabilize the input amplifier during the holding mode

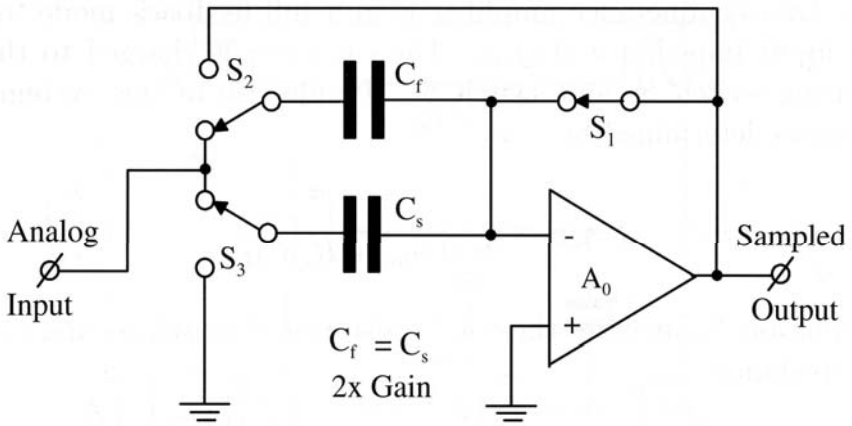
S&H Circuit using Miller Cap.

Switched Capacitor S&H Circuit

- Basic Configuration



- Common implementation for pipelined ADCs



References

- Rudy van de Plassche, “CMOS Integrated Analog-to-Digital and Digital-to-Analog Converters- 2nd Edition,” Kluwer Academic Publishers, 2003.
- B. Razavi, “Principles of Data Conversion System Design,” IEEE Press, 1995.