ANALOG DEVICES

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APPLICATION NOTE

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Applying IC Sample-Hold Amplifiers

by Walt Jung

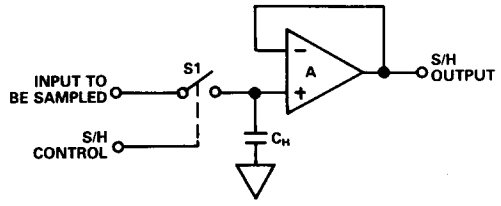
The sample-and-hold (S/H) function is one which is basic to the data acquisition and A/D conversion processes. A S/H amplifier circuit has two basic and distinct operational states. In one state, an input signal is sampled and simultaneously transmitted to the output (SAMPLE). In the second, the last value sampled is held (HOLD) until the input is sampled again. In most applications, the S/H is used as a "front end" to an A/D converter in data acquisition systems. Used as such, it is the purpose of the S/H to maintain the analog input voltage at a constant level for the period of time required to perform an A/D conversion.

More specifically, the S/H is a system functional block necessary in data conversion systems, where the A/D converter in use requires a constant and accurate analog input during the period of its conversion process. An example of such a use is with a successive approximation type A/D. Ideally, the S/H "freezes" the last instantaneous input voltage prior to its HOLD command, and presents this voltage unaltered to the A/D converter. The A/D then converts the voltage to a corresponding digital word. In practice, there are many error factors which come into play in the process of implementing a S/H. Thus this application note will discuss these basic considerations, as well as representative device topologies and some representative applications.

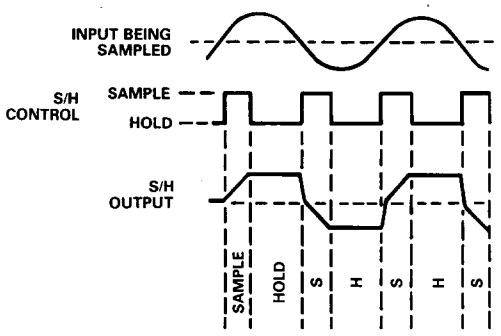
BASIC OPERATION OF S/H AMPLIFIERS

Some S/H basics are illustrated by Figure 1, with the most basic form of S/H circuit operation diagrammed in 1a. Here, an analog input signal to be digitized is applied directly to the electronic switch, S1. Depending on the state of S1, the signal will be either transmitted to the holding capacitor, C_H, or it will be blocked. The state of switch S1 is controlled by the S/H control line, which is a digital input.

When S1 is closed, the input signal appearing across C_H is buffered by A1. It also appears at the S/H output (possible low-pass filter effects are disregarded for this discussion). If S1 is connected for a period of time as the input varies (as with an ac waveform), the operation may also be said to be *tracking*; that is, any input changes are also transmitted to the output.



a. A Basic S/H Circuit, Consisting of Switch, Hold Capacitor, and Buffer Amplifier



b. S/H Waveforms Showing the Input Being Sampled (Top), the S/H Control (Middle), and the S/H Output (Bottom)

Figure 1. S/H Basics

When S1 is opened, the last input voltage value is retained on C_H as a charge; that is, it is held. A1 continues to read this voltage until the next SAMPLE period. This action is illustrated by the input, output, and control waveforms in Figure 1b. S/H circuits are used for a wide variety of signal-processing functions; not only A/D interfaces, but also more general analog memory functions such as auto-zero amplifiers can be implemented.

The S/H operational waveforms of Figure 1b are nearly ideal and assume perfect switching, perfect tracking, ideal holding characteristics, and load/source immunity. In practice, S/H errors are found to exist for each of the four states of the device. These states are:

(1) HOLD-to-SAMPLE transition
(2) SAMPLE interval
(3) SAMPLE-to-HOLD transition
(4) HOLD interval

These errors are obviously potentially important to many applications, and for high accuracy applications (>10 bits, or accuracies of 0.1% or less), all are important. They are defined and illustrated below.

HOLD-TO-SAMPLE TRANSITION ERRORS

These errors are associated with the time interval when the device is switched from the HOLD state to the SAMPLE state. Since the input may have changed a large amount since the last sampled voltage (i.e., by as much as full scale), the S/H must reacquire the input signal and settle once again to within its rated accuracy band. This is shown in Figure 2.

Acquisition time is the time required for the S/H to acquire and then track the input signal after the SAMPLE command. It is usually specified for a full scale level change (−10V to +10V and vice versa), since this represents the worst case in terms of time necessary to acquire an arbitrary level signal. The output must assume the desired level to within a rated error band consistent with the level of accuracy required for the conversion or sample. For example, this may be 0.01% or 0.1%. An illustration of a HOLD-to-SAMPLE acquisition waveform is shown in Figure 2a.

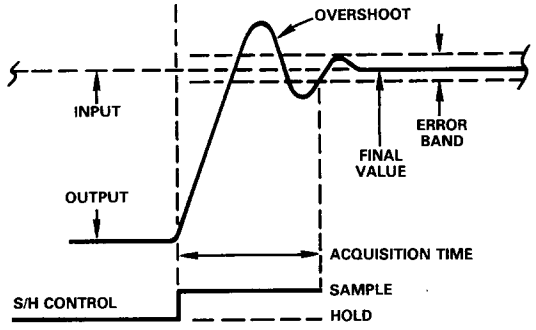


Figure 2a. HOLD-to-SAMPLE Node Acquisition Time Showing Acquisition of a New Signal (Top), and the S/H Control (Bottom)

A major portion of acquisition time for large HOLD-to-SAMPLE changes will be taken up by an initial slewing interval. After this high error interval, the output may overshoot, whereupon it will settle to within a rated accuracy band of ±2mV, which would be ±0.01% for a 20V scale for example. Note that acquisition time ends when the signal has settled and *remains* within the rated error band.

Acquisition time is the major HOLD-to-SAMPLE error component and is the primary determinant of how fast the S/H portion of a conversion system can be operated. Typical times are on the order of several microseconds to accuracies of 0.1% or 0.01% or better. Acquisition time is strongly dependent upon the value of the holding capacitor used as this capacitance (usually) influences slew rate.

Illustrated in Figure 2b is the **HOLD-to-SAMPLE transient**, a switching transient produced at the time of the transfer from HOLD into SAMPLE mode. Note that this transient will be present even in the case where there is no large difference between the previously held voltage and the new

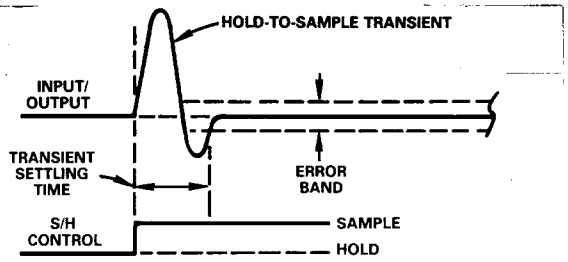


Figure 2b. HOLD-to-SAMPLE Mode Transient, and Settling Time

sample. Since the amplitude of this transient may be well in excess of the rated S/H accuracy (as much as several hundred millivolts), it must be allowed a sufficient time period to die out before the output voltage sample can be considered valid.

Since the settling time of this transient continues beyond the initiation of the HOLD-to-SAMPLE command, system timing must allow for this. However, in practice the settling time associated with any HOLD-to-SAMPLE transients will typically be much less than that of acquisition time. Thus, a time interval equal to the worst case (or acquisition time) will usually take into account the HOLD-to-SAMPLE transient error and its associated settling time automatically.

SAMPLE ERRORS

During the SAMPLE interval, the S/H device is tracking the input signal in a fashion which is very much like an op amp. In fact, most S/H devices are either specialized op amps or they are constructed using op amps with characteristics which are particularly suited to S/H use. Therefore, since most S/H amplifiers reduce to, or are equivalent to either an op amp voltage follower or an inverter, their SAMPLE mode errors can be calculated in a similar fashion.

Pure scaling errors within a S/H can generally be regarded as a benign error as they by and large can be easily nulled with a calibration adjustment. Usually, a convenient point for this to be done is at the A/D reference as this can remove all of the system scaling errors at once. Of course, this approach applies to the conventional usage, i.e., one S/H per A/D. If a number of S/H's are used in front of an A/D or if a S/H is just being used as part of another circuit, it may need to be gain trimmed locally via gain scaling resistors.

In any event, the worst case deviation from the ideal S/H scale factor must be known for use in the error budget. Typically, the scale factor will be 1 ± an error of 0.001% or less. That is, the type of gain error associated with a voltage follower hookup.

In the case where gain resistors are used, such as when the S/H is to be used for noninverting gains other than unity, resistor tolerances will increase this error substantially. For inverting mode operation S/H's, gain scaling resistors must be used, regardless. In either case, it is highly advantageous to have application resistors on the S/H chip, since they will have higher pretrimmed accuracies and a specification for their worst case drifts. The trend of

recent devices is towards sets of pretrimmed resistors to accommodate popular gains of −1, +2, etc.

Note that while a true gain (scaling) error can be adjusted by a system scale calibration, a gain *nonlinearity* is a non-trimmable error.

Gain nonlinearity is a critical S/H error and it appears as a deviation from the ideal transfer characteristic. This component is the dynamic deviation from the ideal numeric S/H gain (i.e., +1, +2, −1, −2, etc.) as the unit is exercised over its rated signal output range, usually ±10 volts. Its largest component is usually input stage common-mode error which will be typical of the case of a follower type hookup (by and large the most prevalent). In the case of an inverter type hookup, the common-mode errors disappear, but resistor matching errors can become an error source.

Typical S/H nonlinearity figures are 0.001% to 0.01% over the ±10V signal range. Obviously, the S/H nonlinearity must be better than the overall nonlinearity as established by the A/D in use to preserve system performance. A good rule of thumb for S/H nonlinearity is a figure of an order of magnitude better than the basic converter resolution. For example, a S/H nonlinearity of 0.01% or better would be used with a 10-bit converter. Note that the user may need to calculate nonlinearity from the S/H's CMRR, such as an 80dB CMRR, equivalent to 0.01% nonlinearity.

Offset is the dc shift which occurs between the input and the output with the S/H input grounded. It is usually adjustable to zero via an optional trimpot. A typical dc offset specification will be on the order of ±2mV or less. Pure offset by itself is not usually a major problem with S/H applications, as it can always be trimmed to zero as part of the overall system calibration. This can be part of the A/D trim calibration, either done manually or via software.

Offset temperature *drift* is another story, since it cannot readily be distinguished from real signal(s). Unless an auto-zero calibration cycle is included, S/H offset drift will be a nonreducible error component and will cause errors as temperature varies. Drifts for S/H's are typically on the order of 1 to 10μV/°C, so this error can be a serious one either for the higher accuracies or for wide temperature ranges.

S/H offset voltage will also vary with supply voltage to some degree, and this should also be specified. Typically, supply rejection is on the order of 80dB or 100μV/V. This parameter is usually not of major importance with well regulated supplies or with the use of auto-cal cycles.

Settling time is applicable to the SAMPLE mode for rapid input voltage changes. When tracking an input signal, a S/H is governed by dynamic limitations similar to other op amp configurations.

Settling time is governed by slew rate and small signal bandwidth, with slew rate being dominant for large scale step changes. Typical slew rates are 5 to 10V/μs, and settling times in the 5-10μs region. As noted under acquisition time, the exact specifications are strongly dependent upon the holding capacitor.

SAMPLE-TO-HOLD TRANSITION ERRORS

Aperture time or aperture delay is the time which elapses between the point when a HOLD command is issued and the actual opening of the S/H switch. With a rapidly changing input voltage, this time will introduce an error by determining the voltage which is actually held. The resulting voltage error will be equal to the change in input voltage which occurs during the effective aperture time interval.

Figure 3 generally illustrates aperture time related errors, of which Figure 3a shows how aperture delay creates an error in the voltage held. With a high rate-of-change input voltage, the S/H voltage will be changing by an amount which may be approaching 1/2LSB during the time the switch is passing from on to off.

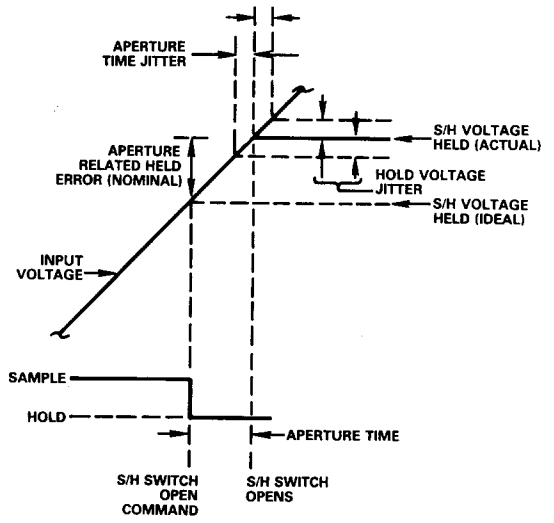


Figure 3a. Aperture Related Time/Voltage Errors. Analog Input/Output at Top, SAMPLE/HOLD Drive at Bottom.

As a general example of the effect of aperture time, consider an input signal with a rate of change (signal slope) of 1V/μs which is sampled with a 10ns aperture time. This will result in a 10mV sampled error due to the aperture time related dV/dt error.

This sort of error is usually significant. The effective aperture delay can be compensated by advancing the in system HOLD command timing the amount of nominal aperture delay, but this is not the entire picture.

If the nominal aperture delay is subtracted, the remaining error is known as the aperture *jitter* (or uncertainty) which is the true limit to S/H sampling errors with high signal slope inputs. Aperture jitter is defined as the net variation in the actual S/H switch timing from sample to sample. This jitter places the ultimate limit on aperture timing related error. For the 1V/μs slew rate example, a 1ns aperture jitter would result in a ±1mV voltage uncertainty.

A general relationship showing the limiting aperture time and the resulting allowable full scale level sine-wave input frequency can be drawn. This is shown in Figure 3b. This graph is based upon the maximum (full scale) sine-wave input frequency which will result in no more than 1/2LSB of error. This frequency, f_{max}, is calculated as:

$$f_{max} = 1/[2^{(n+1)} \pi t_a] \quad (1)$$

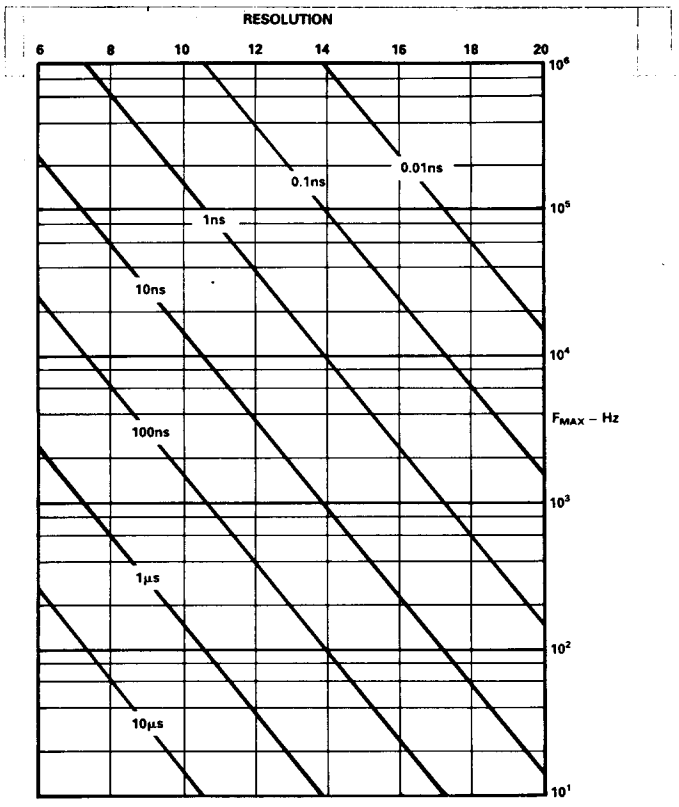


Figure 3b. Maximum Input Sine Wave Frequency (f_{max}) at Full Scale Level, for Various Aperture Times and Resolution(s)

where $\pi = 3.14$, t_a is the limiting aperture time, and "n" is the resolution of the converter in bits.

Since the data is for a limiting aperture case, it can be used for an A/D with a S/H or for an A/D operating alone. In the latter case, the A/D's conversion time will define the effective aperture time.

The data clearly illustrates the value of a S/H for maximizing the allowable input frequency. A 10µs 8-bit A/D without a S/H can only accept a maximum input frequency of roughly 60Hz. On the other hand, with the use of only a 100ns aperture S/H, the same A/D can accept a 6kHz maximum frequency. Note also a more general relationship; as the conversion resolution is increased, f_{max} is lowered for a given conversion time. Therefore, the need for a S/H becomes more critical as either resolution or frequency is increased.

Obviously, the lower the aperture time in a S/H, the better, as it will place less of a limit on the A/D used with it. While the times quoted for illustration are typical for medium speed I.C. S/H circuits, they are not the final limit to system timing since the maximum *throughput frequency* will often occur before the aperture time limited frequency.

S/H offset (also called S/H "pedestal", "jump" or "step") is the resulting analog error induced by a transient charge on the HOLD capacitor when the S/H switches from SAMPLE-to-HOLD. It is caused by the finite capacitance of the S/H switches used, and to a lesser extent, the layout and/or package capacitances. These capacitances feed through a portion of the digital control signal directly into the HOLD capacitor. In general, this error can be reduced with larger value HOLD capacitors since the parasitic coupling capacitance is fixed within a given device and layout. The effect is illustrated in Figure 4.

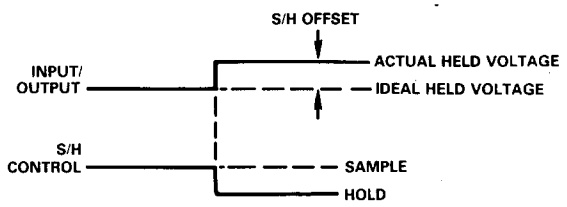


Figure 4. SAMPLE-to-HOLD Offset (Top), and S/H Control (Bottom)

This error, which may be on the order of several mV, can in some cases be compensated for by feeding an antiphase control signal into the HOLD capacitance via a small external coupling capacitor. Generally, this error is reducible by reducing the p-p level of the digital control signal to an absolute minimum as well as by screening/guarding the coupling paths between this signal and the C_H node.

Note that SAMPLE-to-HOLD offset may not always be directly specified as such, particularly in IC devices which use *external* holding capacitors. In such cases, a specification may be given in terms of *charge*, in units of pC. In these cases, the S/H offset may be then calculated as:

$$\text{S/H offset}_{(V)} = \text{Charge (pC)}/C_H\text{ (pF)} \qquad (2)$$

A 10pC charge transfer with a 1000pF C_H would for example cause a S/H offset of 10mV. Obviously, the lower the charge transferred, the lower this error will be. In better units, charge transfer is as low as 1pC or less.

S/H offset can initially be considered as a trimmable error, just as can pure dc offset. If, however, it should change with time, input voltage, and/or temperature, these instabilities must also be considered. In some S/H units which use floating switches (see Figure 7b, type 2), the S/H offset will change with the value of the input signal. This is obviously not desirable, as it is difficult if not impossible to compensate. S/H type 3 (Figure 7c) does not show this problem, as the switch is maintained at a constant level (a virtual ground).

Sample-to-hold settling time is time for the S/H output to settle to within its rated accuracy following the HOLD command. It includes the time required for any switching transient to die out.

HOLD INTERVAL ERRORS

Droop, also called tilt, is the change in the HOLD voltage (ΔV) during the HOLD interval (Δt). It is caused by the net leakage current(s) into (or from) the HOLD capacitor. Since the currents which cause droop may be of either sign from one S/H to the next, droop current will cause the voltage on the capacitor to ramp either up or down, as shown in Figure 5. However, it is the magnitude of the error over the HOLD interval and not the sign that is important. Droop is governed by the simple charge/voltage relationship:

$$\Delta V/\Delta t = I_L/C_H \qquad (3)$$

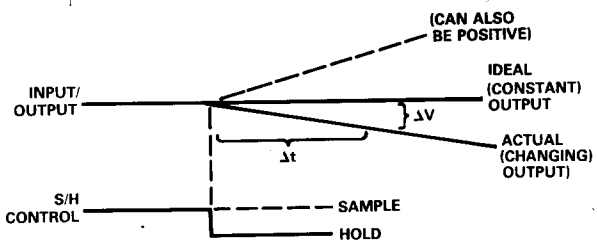


Figure 5. Droop Error Voltage (Top), and S/H Control (Bottom). Note that "Droop" Can Be Either Positive or Negative.

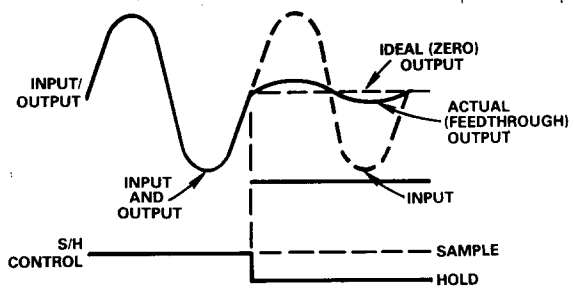


Figure 6. Feedthrough Error Voltage (Top), and S/H Control (Bottom)

where I_L is the leakage current and C_H is the HOLD capacitor value. As an example, a 1nA droop current with a C_H of 100pF will cause a droop rate of 10μV/μs. Over a HOLD period of 10μs, this will yield a max droop error of 100μV which is not likely to be a problem.

Within a given S/H device, the current I_L is given by a specification, but C_H is (usually) under user control. Therefore, droop can be adjusted by C_H and will become smaller as C_H is increased.

There is a tradeoff, however. As C_H is increased to lower droop, this typically results in longer acquisition times. This is because the current needed to charge C_H for acquisition slewing is fixed. As a result, it is usually desirable to hold the leakage current I_L as small as is practical in order to minimize droop. Typically, this parameter will be due to the S/H output amplifier's input bias current and switch leakage which usually increase with temperature. Droop is worst at high temperatures. Note that the value of I_L used to calculate droop should account for this temperature dependence of net leakage current. With FET input buffers, bias current doubles for each 10°C rise.

In practice, typical droop rates at medium temperatures in a S/H will be on the order of 1μV/μs, a fairly insignificant error. This may not necessarily remain so when maximum bias currents at the highest temperature are calculated. The leakage current which will be seen at the highest expected temperature can be calculated in order to determine the worst case droop rate.

Feedthrough is an analog error caused by leakage of ac signals through the S/H switch in the HOLD (off) state. Like S/H offset, it is basically caused by switching capacitance but it can also be influenced by layout dependent capacitive coupling. Since the switch capacitance and the HOLD capacitance form a voltage divider, feedthrough decreases for higher values of HOLD capacitance just like droop and S/H offset. The effect of feedthrough is shown in Figure 6.

Feedthrough is usually specified with a full scale peak-to-peak sine-wave input at a high frequency, such as 10kHz. Typically it will be on the order of 80dB (or more) in a good S/H. This is equivalent to a feedthrough error of 0.01% (or less). This parameter is important in cases where the S/H follows a multiplexer which can select high level inputs during the HOLD state and potentially cause errors due to the signal feedthrough.

DIELECTRIC ABSORPTION

With some common capacitor types, the dielectric does not completely release all of its energy after a charge/discharge cycle. The result of this phenomenon is an error in stored voltage after a period of time in the HOLD mode. This effect is minimized using certain dielectrics, in particular, the films. Dielectrics specified for low DA, such as Teflon, polystyrene, and poly propylene should be used. Note that consideration of DA will be most applicable in S/H's which either use an external C_H or where an external C_H is used to augment an internal one.

DRIFT AND NOISE

A S/H can possess different drift characteristics in the HOLD mode than those in the SAMPLE mode. In the HOLD mode, the output terminal sees only the drift of the *output* buffer amplifier. In the SAMPLE mode, it sees either the input amplifier alone or the composite drift of two series amplifiers.

Ordinarily, this different drift characteristic for HOLD versus SAMPLE is not detrimental. A conversion is usually made within a few microseconds, long before drift errors due to temperature can be a problem. For unusually long HOLD times, it may need to be considered.

Noise, however, can be a different story. Consider the S/H types 2 and 3 of Figure 7, for example, when in the HOLD mode. If the output amplifier has excessive noise, it will be seen during HOLD and digitized along with the desired signal. If this noise is high and the converter linearity is not well below 1/2LSB, certain codes will be in error due to noise modulation.

MOSFET input buffers are used in some S/H's for their very low input currents. Unfortunately, these types often have relatively high input voltage noise which can limit overall accuracy for some applications. JFET inputs will not have as low an input current as MOSFETs, but will have appreciably lower noise voltages.

S/H DESIGN TYPES

There are great numbers of S/H devices available today. Except for the very highest limits of performance, most of them tend to fall into a few categories of design topologies. These are illustrated below with a brief discussion on each. An understanding of the different circuit types is helpful in choosing a S/H best suited for a given application.

Similar to the elementary circuit of Figure 1a, the circuit of Figure 7a is an actual S/H amplifier type. Here A1, C_H, and the switch operate as described before, but an input stage buffer A 2 is also added.

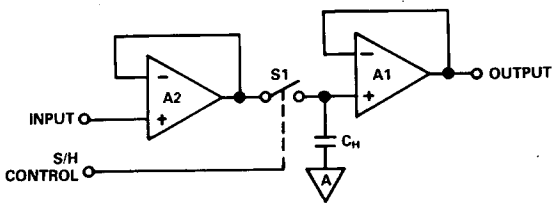


Figure 7a. Open Loop, Cascaded Follower S/H (Type 1)

The addition of the buffer provides increased charging current for C_H. This provides faster acquisition time without loading the source. In this S/H type, both amplifiers must have high slew rates, fast settling times, low offset voltages and low drift for best accuracy, since these errors are cumulative. A1 should be a FET input device to minimize loading of C_H, but this is not necessarily true for A2. This S/H type tends to be good for high-speed acquisition uses.

The S/H configuration of Figure 7b has the advantage that an overall feedback loop is returned around both amplifiers in the SAMPLE mode. As a result, the errors of A1 are minimized for the SAMPLE state, although they do appear in the HOLD mode. This circuit has potentially higher accuracy, but with some potential sacrifice in overall settling characteristic due to the multistage loop dynamics.

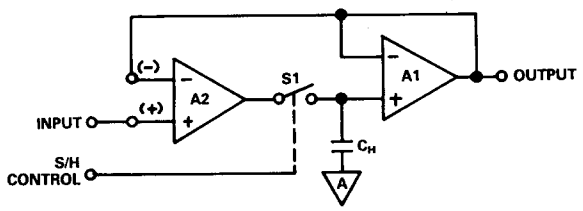


Figure 7b. Closed Loop, Follower Output S/H (Type 2)

Note that in this type of S/H connection, the input stage can be wired to have both the (+) and (–) input terminals available for external options, although this may not always be done in all types. With this flexibility, the S/H can be connected as either an (overall) inverting or noninverting type S/H. Application resistors may or may not be made available.

The third circuit in Figure 7c is similar in that it connects feedback around the two op amps and in this sense has advantages similar to 7b. In this case, the switch is operated at the virtual ground input of A1 and C_H is an integrator capacitor around the output amplifier stage.

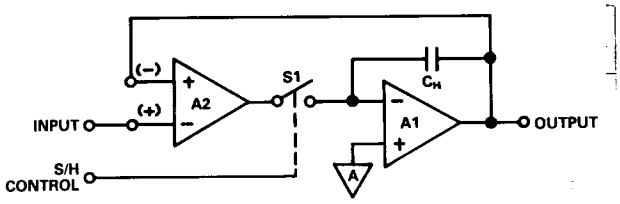


Figure 7c. Closed Loop, Integrator Output S/H (Type 3)

Note that in this type of S/H connection, the input stage can also have both the (+) and (–) input terminals available for use as previously noted. Therefore, this type can be connected as either an (overall) inverting or noninverting type S/H.

S/H APPLICATIONS

Implementing a conversion system with modern A/D and S/H devices, while never trivial, can be greatly aided by the applications versatility of the hardware employed. The 12-bit stand-alone A/D + S/H conversion system of Figure 8a is an example of a hookup which is easy to implement as shown but can also be easily modified for other scales, etc.

This circuit uses an AD585 S/H, connected in the noninverting unity gain mode, with $\overline{\text{HOLD}}$ active. The A/D is an AD574A connected for a unipolar 0 to +10V scale, with system GAIN and OFFSET calibration set by R_2 and R_1, respectively. The STATUS output of the AD574 drives the $\overline{\text{HOLD}}$ input of the AD585 A1, for the lowest possible S/H offset. This requires inversion in the TTL stage.

As shown, conversion is started by a CONVERT signal and begins on the falling edge, whereupon the STATUS line goes HIGH and the S/H goes to HOLD. For a 12-bit conversion, the AD574A will require 35 (max) μs to perform a conversion. The end of conversion is signaled by a STATUS LOW signal.

The A/D calibration trims shown provide for change of system gain and offset, sufficient to accommodate both S/H and A/D errors.

The maximum throughput time of this system is based on three factors, as it is represented here. These are: the A/D conversion time and the S/H aperture delay and acquisition time. The conversion time will be:

$$T = t_c + t_{ad} + t_{acq} \quad (4)$$

Respectively, these individual times will be 35μs + 35ns + 3μs, or 38.035μs, total. Maximum throughput frequency can be calculated, as the inverse of this time, as:

$$f_{throughput} = 1/T = 26.3\text{kHz} \quad (5)$$

This frequency assumes a *single* sample per cycle; to meet the Nyquist criteria of 2 data points per cycle, the frequency would be halved. (Note also that any additional settling time period preceding the S/H also may need to be accounted for and can include an IA and/or a multiplexer, when used.)

A source of potential error in the application of high-speed successive approximation A/D's with S/H amplifiers is a *kickback error* from the A/D. A successive

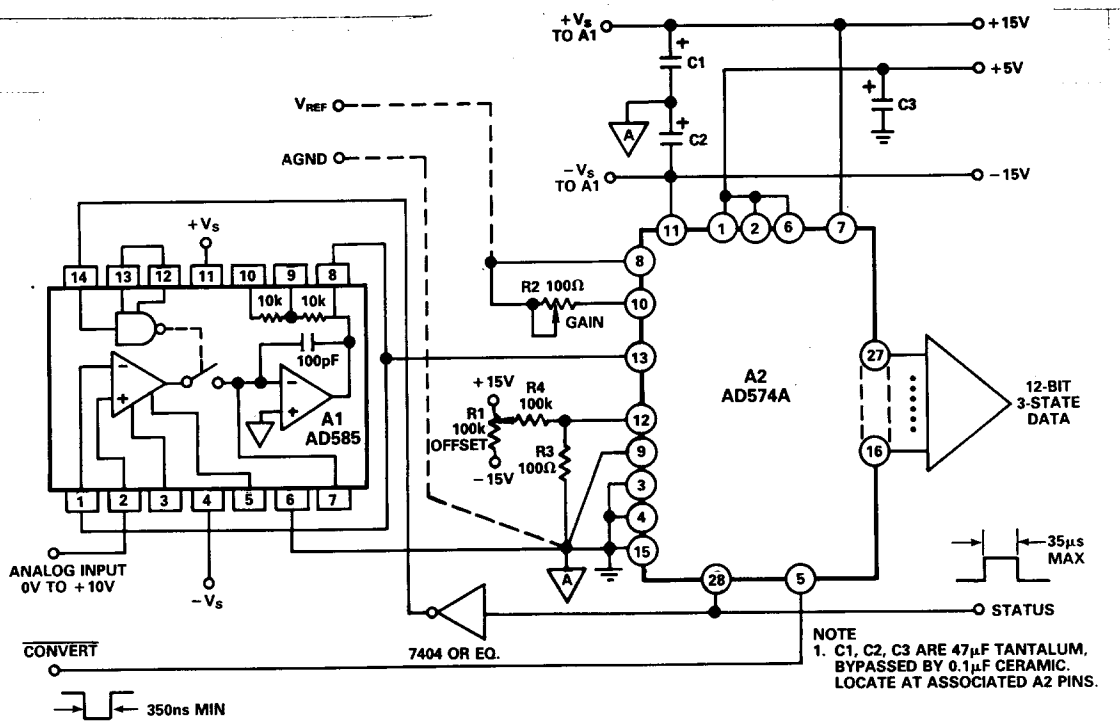


Figure 8a. Stand-Alone 12-Bit Unipolar A/D with S/H

approximation A/D represents a *dynamic* load to the S/H, and the MSB loading at the start of the conversion cycle can cause a transient at the A/D input voltage (S/H output) due to nonzero S/H output impedance. If the S/H impedance is not sufficiently low at high frequencies, the kickback error can exceed an LSB.

The solution to this particular problem lies in the use of a S/H with an intrinsically low impedance output stage or one with high feedback, for low kickback error. With the impedance sufficiently low to render the dynamic voltage error negligible, A/D loading will not cause a problem. The AD585 output stage has been designed for a low dynamic output impedance to minimize this error. As a demonstration of this, an expanded scale photo of an AD585 output driving an AD574A during conversion is shown in Figure 8b. Note that the negative going transient error at the MSB switch point is both low and short in its duration.

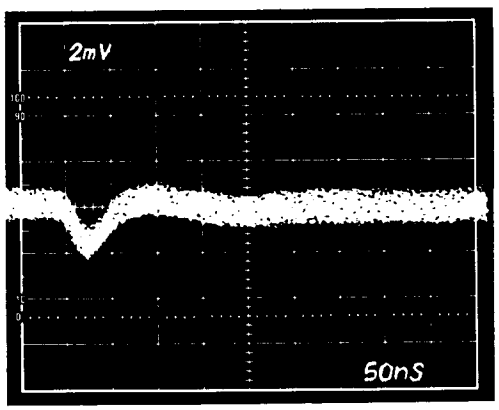


Figure 8b. Output of AD585 S/H Amplifier Driving AD574A, MSB Transition

For applications which demand both a fast acquisition time and a low droop rate, these conflicting performance parameters can be met together using a cascaded S/H. Figure 9 shows such a circuit with the $\overline{HOLD}_1$ and $\overline{HOLD}_2$ control lines driven as shown in the timing diagram. The basic idea is that the first S/H of the cascade acquires the input rapidly before the second has time to settle to its rated accuracy. The first S/H is then put into HOLD and the second one continues to acquire the "input" as it appears at the *output* of the first (fast) S/H. Since this constitutes a series path for the input signals, the errors of the two S/H's are additive.

This circuit uses two series connected AD585's with the first one configured normally for fast acquisition. Using the internal capacitor of the AD585, this stage will have a 1mV/ms (max) droop rate. This stage samples for a 5µs period (the width of the $\overline{HOLD}_1$ signal). The second S/H samples the output of the first for 500µs or the width of $\overline{HOLD}_2$. During this 500µs period, the output of the first stage will droop, up to 0.5mV. This is generally the $HOLD_2$ width (in ms), times 1mV/ms.

The second AD585 uses a 0.01µF external C_H, which will minimize droop of this stage by a factor of 100 (the ratio of the second to first stage C_H's). The effective droop of the entire circuit then becomes 0.5mV (first stage), plus 0.01mV/ms (second stage). For HOLD intervals in the second stage of up to tens of ms, the net droop of this cascaded S/H will therefore be close to that seen in the 500µs interval, or in this case, ≈0.5mV.

Of course, the tradeoff of this scheme is that the overall signal throughput is reduced. Practically speaking, there may be little or no penalty, as the application may be intended to be used with slower A/D's. Also, if a number of cascaded S/H's are being used before a multiplexer, this

scheme can be very useful, while maintaining a high overall throughput rate even if individual channels are sampled infrequently. Note that the effective f_{max} in terms of aperture time of this cascade will still be determined by the *first* of the two S/H's. In this example, non-inverting unity gain S/H's are shown. In principle either (or both) S/H may be used with other scales.

There are some generally important practical rules for layout that the user should abide by. Whenever an external C_H is used, care should be taken to surround the PC trace associated with pin 7 with a guard trace. This should be tied to analog ground and the lead to this pin should be kept as short as possible. The external C_H should be a low DA capacitor type, with the outside foil connected to the S/H output (pin 8). Note also that many S/H applications will never require an external C_H or the use of pin 7. In such cases, it can be clipped off near the package, which will cut pickup to an absolute minimum.

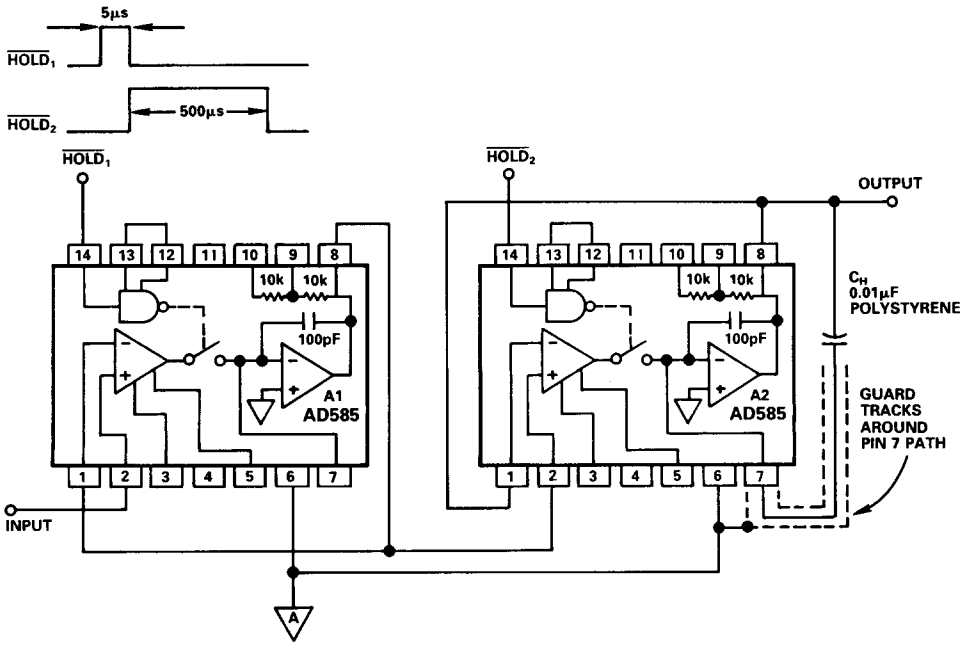


Figure 9. Loop Droop Cascade S/H