Bandgap Reference Circuit

I. General Descriptions:

In this contest, the goal is to design a "bandgap reference (BGR)" which has been popular for many years. Fig.1 shows the main circuit of the bandgap reference, two groups oftransistors running at different emitter current densities and cause voltage difference between the two groups. Typically, the two voltages add up to around 1.35 volts and that is approximately the band-gap of silicon. Modern systems-on-a-chip (SoC) depends on a bandgap circuit to start up and bias all other circuits. Thus, the band-gap must be designed to be good power supply rejection ratio (PSRR) and this is the major grading item in this contest. The reference circuit of OPAMP is shown in Fig.2.

Note that CIC 0.18um virtual process is used in this contest in which NMOS is fabricated on the P-Substrate and it may suffer from the body effect if its source is not connected to P-substrate.For BJT device formation, please refer to Fig. 3. Only two sizes of the emitter area (5x5 um^2 and 10x10 um^2) are allowable for this virtual process.

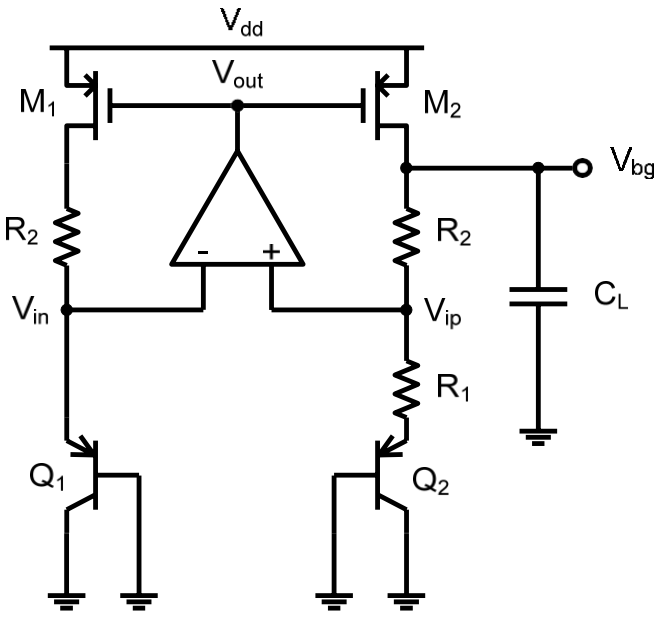

Fig.1: Bandgap reference circuit

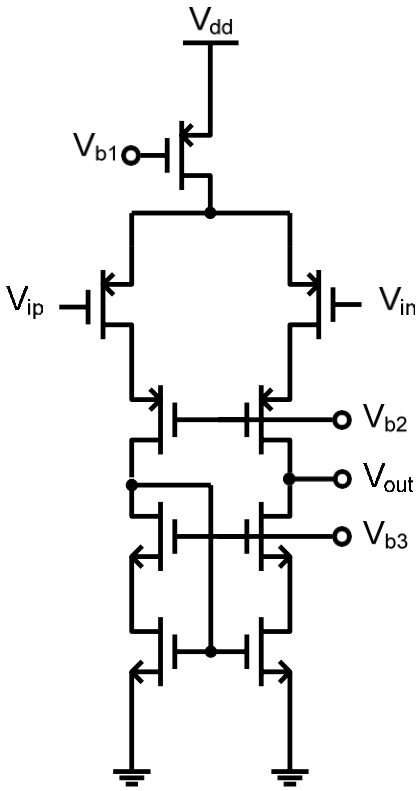

Fig.2: OPAMP circuits used in the bandgap reference design

II. Design Specifications:

1. Please use CIC 0.18um 1.8V 1P6M CMOS virtual process to design the whole circuit. Device model is HSPICE Level 49. The final results should include the netlist, layout and all the verification files (DRC and LVS reports).
2. Please use RNHR1000 poly resistor when implementing resistors (R_1 and R_2), you can refer to "CIC 0.18um 1.8V/3.3V 1P6M Virtual Mixed Mode/RFCMOS Process Device Formation" page 11 for details.
3. This bandgap circuit operates with 1.8V supply voltage. No negative bias source is allowed in your design.
4. The output loading C_L is 2pF.
5. Definition of "temperature coefficient":

$$TC = \frac{V_{BG\_max} - V_{BG\_min}}{\left(V_{BG\_max} + V_{BG\_min}\right)/2} \times \frac{1}{T_{max} - T_{min}} \quad \text{PPM/°C,}$$

   here V_{BG_max} and V_{BG_min} are the maximum and minimum V_{BG} when sweeping operation temperature from T_{max} to T_{min}.
6. Beside the above requirements, the post-simulation (R+C+CC extraction, no inductance is necessary) results of this BGR circuit should also meets the following specifications under the typical transistor parameters (TT corner):
   - PSRR at 100Hz > 60dB
   - PSRR at 1KHz > 40dB
   - Temperature coefficient (from 0°C to 70°C) < 40PPM
   - Power consumption < 1mW

Others:

1. The OPAMP bias circuit is NOT included in this design. However, **the designers should put the bias circuit and value in the Table 1 and upload this WORD file with their design files**. This information is important when scoring your design.
2. Netlist file naming: the subckt name of xCalibre output file should be “bgr.sp”, the top cell should be named as “bgr”, and output node is Vbg. Supply power is “Vdd” and ground is “GND”. Please be noted that the total five nodes are referred and please refer the following example:

   .subckt bgr VDD GND Vb1 Vb2 Vb3 Vbg * note: pin sequence is important

   MM1 net1 net2 VDD VDD PCH L=x W=y

   …..

   …..

   .ends

V_{b1}	V_{b2}	V_{b3}

Table 1: OPAMP bias table, please put the design value here