Table of Contents

List of Figures

List of Tables

1.0 Introduction

This paper describes the design and analysis of a bipolar Widlar bandgap reference. The Widlar bandgap reference is a well known solution for generating low voltage references which are first order independent of temperature variations. The objective of this project was to design and simulate a Widlar Bandgap Reference cell according to the requirements given in Table 1. The proposed design is a 2.1 mW cell with a temperature coefficient (TCF) of 19 PPM over the commercial temperature range and centered at 27.1 C.

The following sections describe the operation in “Theory of Operation” on page 7, simulation results and descriptions in “Verification” on page 17 and further improvements and discussions are concluded in See “High Power/Low Power Comparison” on page 39..

The design was implemented in a C-PI bipolar process and simulated using the Tektronix Analog Design Simulator (ADS). The main schematic is shown in Figure 2 with the current mirror and startup circtuits shown in Figure 4 and Figure 11. The resistor values are summarized in Table 1, and the schematics for the resistors are shown in “Resistor Schematics” on page 45.

In an attempt to reduce the TCF of the bandgap cell an 15mW nominal, 18mW worst case solution was examined. This solution demonstrated a TCF of 4 PPM over the military temperature range. It appears that temperature stability and power dissipation are inversely related. See “High Power/Low Power Comparison” on page 39.

Table 1: Requirements/Specifications

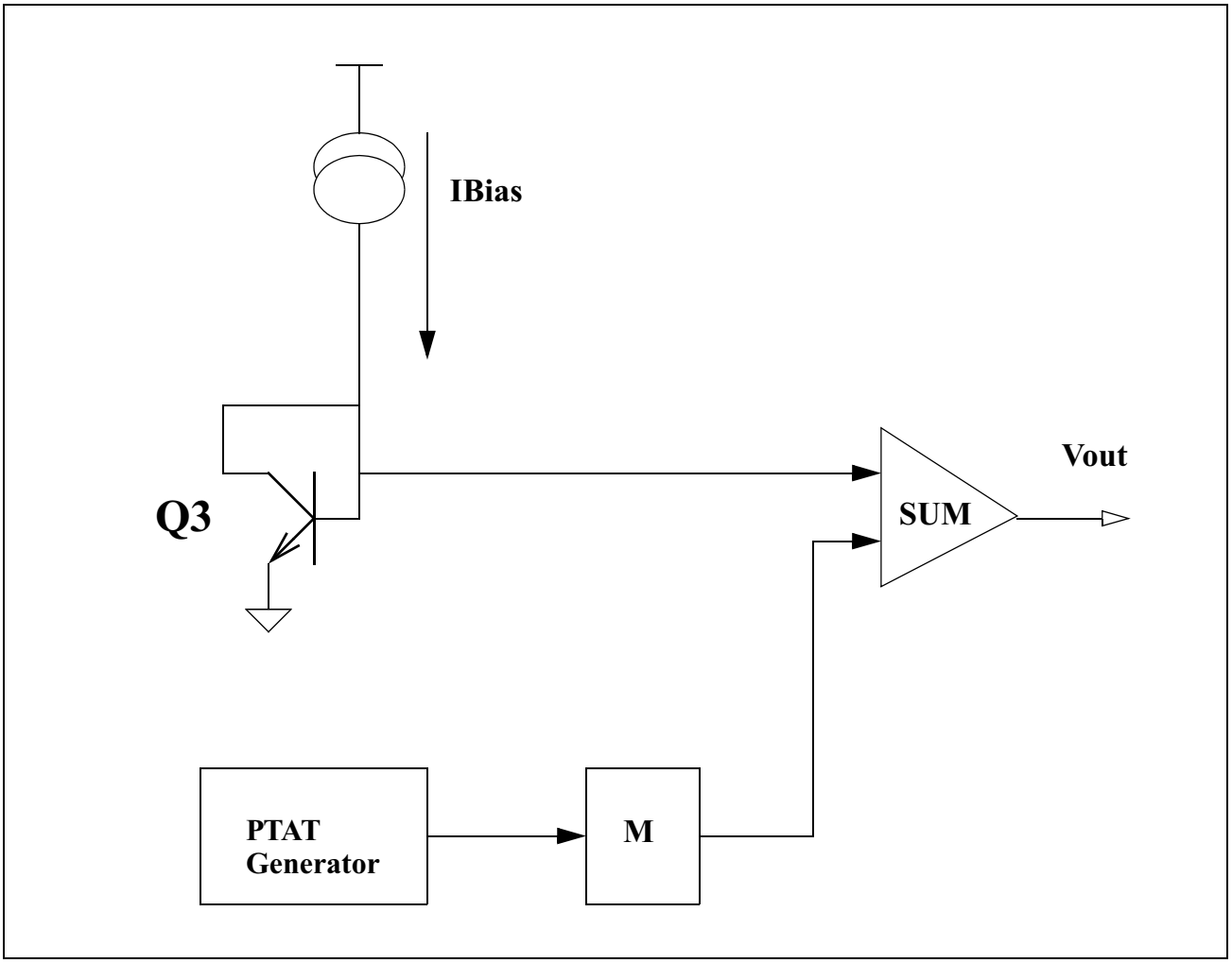
Item	Symbol	Units	Required Value	Measured Performance
Output Impedance	Zout	Ohms	1	0.6
Maximum Power	Pmax	mWatts	10	2.1
Power supply Rejection Ratio (DC)	PSSR0	db	60	64
TC at 27 C	0	-	0	0 @ 27.1
Temp coefficient (military Range)	TCF	V/deg C	-	55 ppm
Q1 Collector Resistor	RC1(R1)	Ohms		4.304 K
Q2 Collector Resistor	RC2(R2)	Ohms		8 K
Q2 Emitter Resistor	RE2(R3)	Ohms		1 K
Area Ratio Q2/Q1				2*WN8/1*WN2
Peak Voltage		Volts	-	1.2814

Table 2: Requirements/Specifications High Power Cell

Item	Symbol	Units	Required Value	Measured Performance
Output Impedance	Zout	Ohms	1	0.27
Maximum Power	Pmax	mWatts	10	18mW @ 125C
Power supply Rejection Ratio (DC)	PSSR0	db	60	64
TC at 27 C	0	-	0	0 @ 23
Temp coefficient (military Range)	TCF	V/deg C	-	4 ppm
Q1 Collector Resistor	RC1(R1)	Ohms		163
Q2 Collector Resistor	RC2(R2)	Ohms		8 K
Q2 Emitter Resistor	RE2(R3)	Ohms		1 K
Area Ratio Q2/Q1	-	-	-	WN2/WN8

2.0 Theory of Operation

Figure 1: BandGap Reference



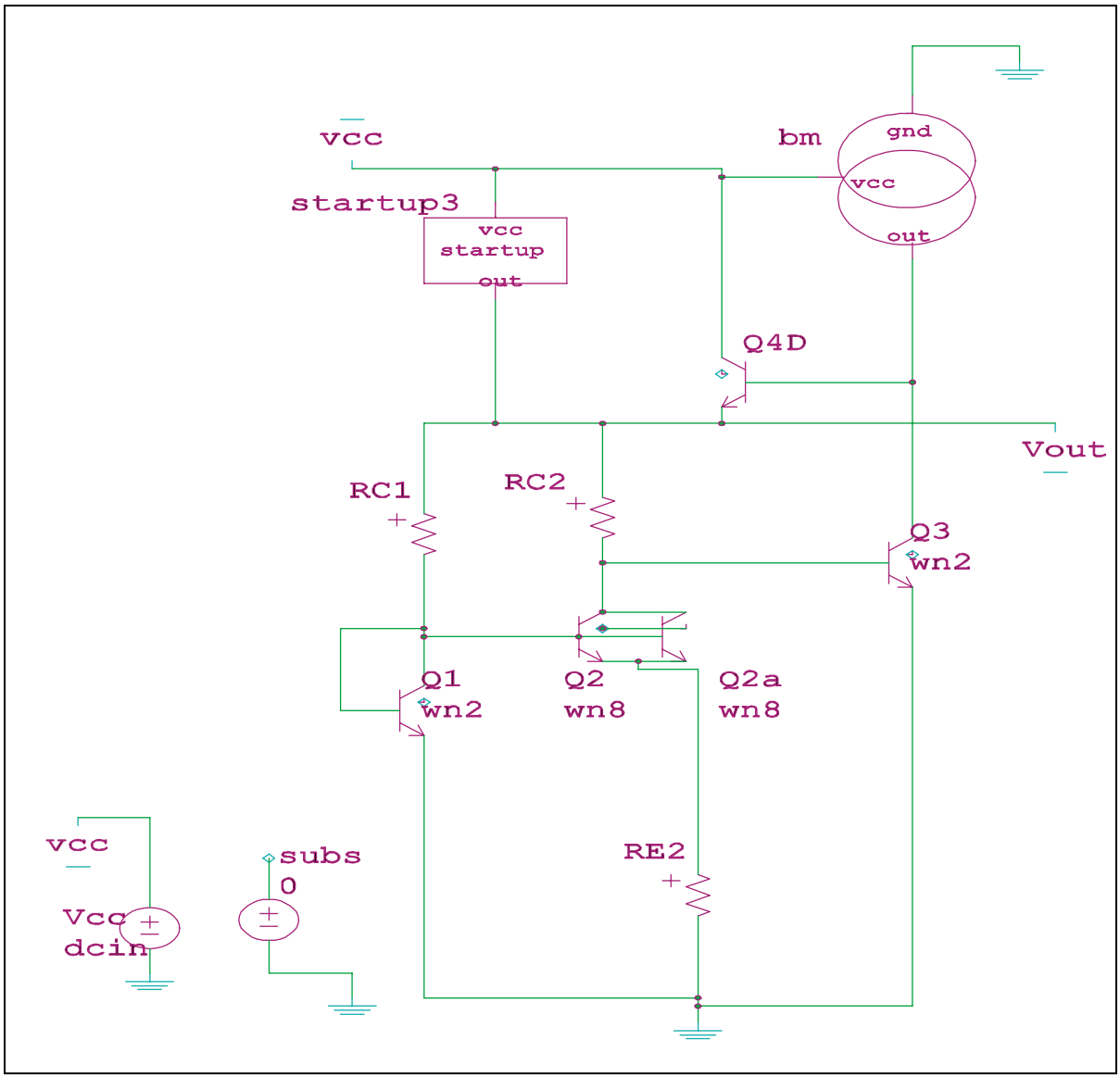
A Bandgap reference generates a temperature independent voltage source by summing a voltage proportional to absolute temperature (PTAT) with a voltage possessing a negative temperature coefficient. When added together, it results in a voltage that is independent of temperature variations up to a first order approximation for a restricted range of temperatures. As shown in Figure 1, a voltage with a negative temperature coefficient is attained with a forward biased PN junction. This is commonly implemented with a diode connected transistor whose collector current is biased from a constant current source. A PTAT voltage is generated by taking the difference of two VBE voltages:

$$\Delta Vbe = Vbe1 - Vbe2 = \frac{kT}{q}\ln\left(\frac{IS2}{IS1}\frac{IC1}{IC2}\right)$$

(EQ 1)

Figure 2 is the Widlar BandGap reference which implements the system shown in Figure 1. Referring to Figure 2, The vbe generator consists of a current source, bm, and transistor Q3. Q1,Q2 constitute the dVBE voltage which appears across RE2, Q2's emitter resistor. This current is reflected back to Q2's collector where a the resistor ration RC2/RE2 and IC2 generate at PTAT voltage across RC2. The voltage drop across RC2 is the PTAT and M-multiplier network in Figure 1. The output voltage is then the sum of the base emitter voltage VBE3 and the voltage drop across RC2, (EQ 2)

Figure 2: Widlar BandGap Reference



$$Vout \cong Vbe3 + \frac{R2}{R3}(Vbe1 - Vbe2) \quad \text{(EQ 2)}$$

The dVBE voltage can be expressed as a ratio of collector currents and emitter area ratios or saturation currents.(EQ 3)

$$Vbe1 - Vbe2 = VTLn\left(\frac{IC1}{IC2}\frac{IS2}{IS1}\right) \quad \text{(EQ 3)}$$

R1 sets the collector current in Q1 and thus biases Vbe1:

$$IC1 = \frac{Vout - Vbe1}{R1} \quad \text{(EQ 4)}$$

Neglecting base currents and assuming large BF, IC2 is

$$IC2 \cong \frac{Vbe1 - Vbe2}{R3} \quad \text{(EQ 5)}$$

Substituting (EQ 4),(EQ 5) into (EQ 2):

$$Vout \cong Vbe3 + VT\frac{R2}{R3}Ln\left(G\frac{R3}{R1}R\right) \quad \text{(EQ 6)}$$

where K is the ratio of the emitter areas.

$$R = \frac{IS2}{IS1} \quad \text{(EQ 7)}$$

and P is somewhat constant for selected values and was measured to be approximately 7.4:

$$P = \frac{Vo - Vbe1}{Vbe1 - Vbe2} \quad \text{(EQ 8)}$$

2.1 Methodologies

The following design methodology was developed based on the above equations.

1. Choose a low power current source with good power supply rejection ratios and minimal temperature coefficients, See “Current Source” on page 13.

1. To minimize the area specify the R2./R3 ratios as a ratio of convenient multiples of 250, 4K ohm resistors available in this technology.
2. Select Vout=1.26 volts and VBE3 to be.750 volts based on the current source output. This voltage will determine the M factor from (EQ 6). M is approximately 19-25.
3. For simplicity fix the R2/R3 ratio to a convenient ratio where R3 is an integer array of R2 resistors in parallel. In this technology, 4K and 250 ohm resistors are available. Therefore R2/R3 ratio was chosen as 8:1 gain made up of 4K resistors.
4. Set K to a value of 8:1 or more. A larger R (EQ 6), allows the use of a smaller R3/R1 ratio and allows R1 to be made larger and therefore generates less Q1 current and less power.
5. Now R2 and R1 can be chosen as follows.
6. Set R2(RC2) to give a voltage nominally 1.26-1.28 volts at 27C.
7. Adjust R1 (RC1) to move the curve so that the zero temperature coefficient is at 27C. This is easily done by running a temperature sweep and plotting diff(Vout) which is the first derivative of output voltage with respect to temperature.
8. Once R2/R3 ratio is set to give Vout approximately 1.26 volt reference, R1 can be tuned to set the temperature coefficient. R1 has a smaller affect on the output voltage because it is entirely in the Log term and so can be used to fine-tune the output curves

The above equations and methodology give us an idea of how to begin the design of the bandgap reference. The first step is to design the VBE generator, Q3 and its current source, See “Current Source” on page 13.

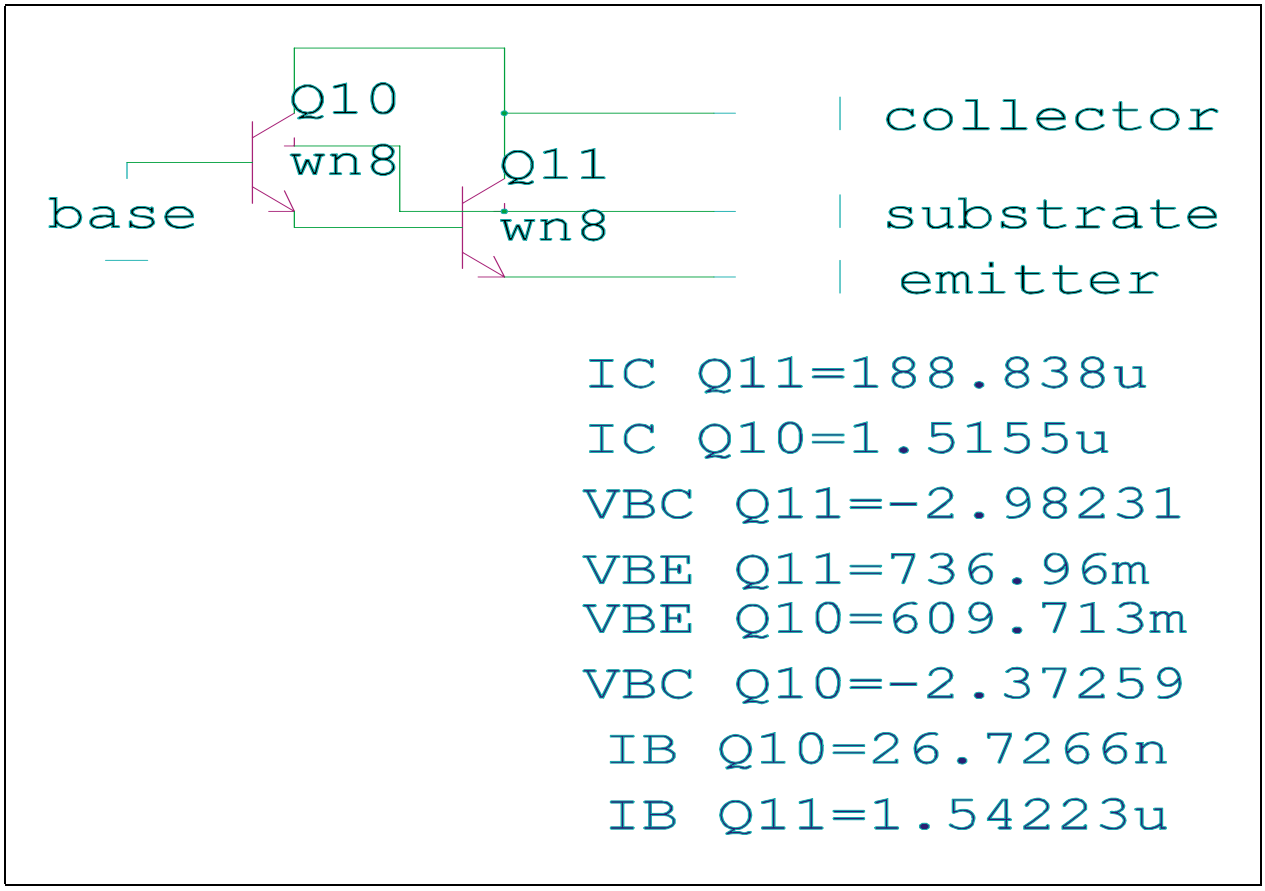
I

2.2 Increasing Output Impedance

A voltage reference requires a low output impedance. In the design transistor Q4 was added to create a negative feedback loop which resists changes to the output voltage. For instance, referring to Figure 2, suppose the current source steps its output current which causes VBE3 to increase and thus Vout to increase by that same amount. As VBE3 rises, VCE rises and VBE2 decreases since VBE2=(VCE3-Vout). When VBE2 falls, Q4 will decrease its output current and force its emitter voltage down. Thus Q4 opposes any positive changes in Vout. Also, Q4 will oppose negative changes in Vout, therefore Q4 is in a negative feedback loop which keeps the output voltage constant. This feedback loop provides a low impedance to the output because the feedback resists any output changes as load current changes.

A single WN2 transistor was at first used for Q4. With the single Q4 transistor, the output impedance was measured to be 3.5 ohms. A darlington pair formed by two WN8 transistors was substituted which lowered to output impedance to 0.6 ohms. A further decrease in output impedance was measured when a WN2 darlington pair was added. The Q4 darlington pair and bias points are shown in Figure 3.

Figure 3: Q4 CC-CC Pair



2.3 Current Source

A self biased VBE referenced current source was chosen to generate the bias current needed for the VBE generator of the bandgap reference. Self biasing greatly reduces the power supply sensitivity which is specified to be no more than 1mv/V or 60db. Figure 4, shows the bootstrap current source used in this design.

R2 was used to adjust the current to approximately 30 uA. Emitter degeneration resistors in the current source contributed to a gain of 15-20db of PSRR.

$$Iout = \frac{(VT)}{R2} Ln\left(\frac{Iin}{Is}\right) \quad \text{(EQ 9)}$$

Assuming the gain of the simple current mirror is approximately 1:

$$Iout \approx Iin \quad \text{(EQ 10)}$$

The current source is fundamental to the proper operation of the bandgap reference because it must provide a constant collector current to the VBE generator (Q3) in Figure 1, “BandGap Reference”. It must be insensitive to temperature and power supply variations which necessitates a bootstrapped or self reference configuration, Figure 4

Here, Q1,Q2,Q3 form a vbe referenced current source with beta helper whose current is set as shown in (EQ 9). R2 was chosen to generate 30 uA of current to bias Q3 in the active region and to consume less power. A lower IC also increases the output impedance because ro=VA/IC.

The current mirror requires a startup to provide enough initial current to turn transistors Q8 and Q7 on so that the feedback is greater than unity. At the stable operating point, the startup circuit’s diode, Q21, become reversed biased and draws negligible power.

The original current mirror provided about 46db of PSRR due to its finite output impedance. The output was boosted by adding emitter degeneration resistors to Q3,Q4 and Q19. About 12K ohms (Figure 32, “RMEDEG”) were added to the emitters to boost the PSRR to 61db. Further improvements can be made by switching to cascoded mirrors

The temperature variation of the current source was plotted in Figure 5. In general the bias current generator has a temperature dependence as shown in (EQ 11). From the current vs Temperature plot it appears that alpha=1 and the current is approximately first order linearly proportional to temperature.

$$I1 = GT^{\alpha} \quad \text{(EQ 11)}$$

Figure 4: Current Mirror

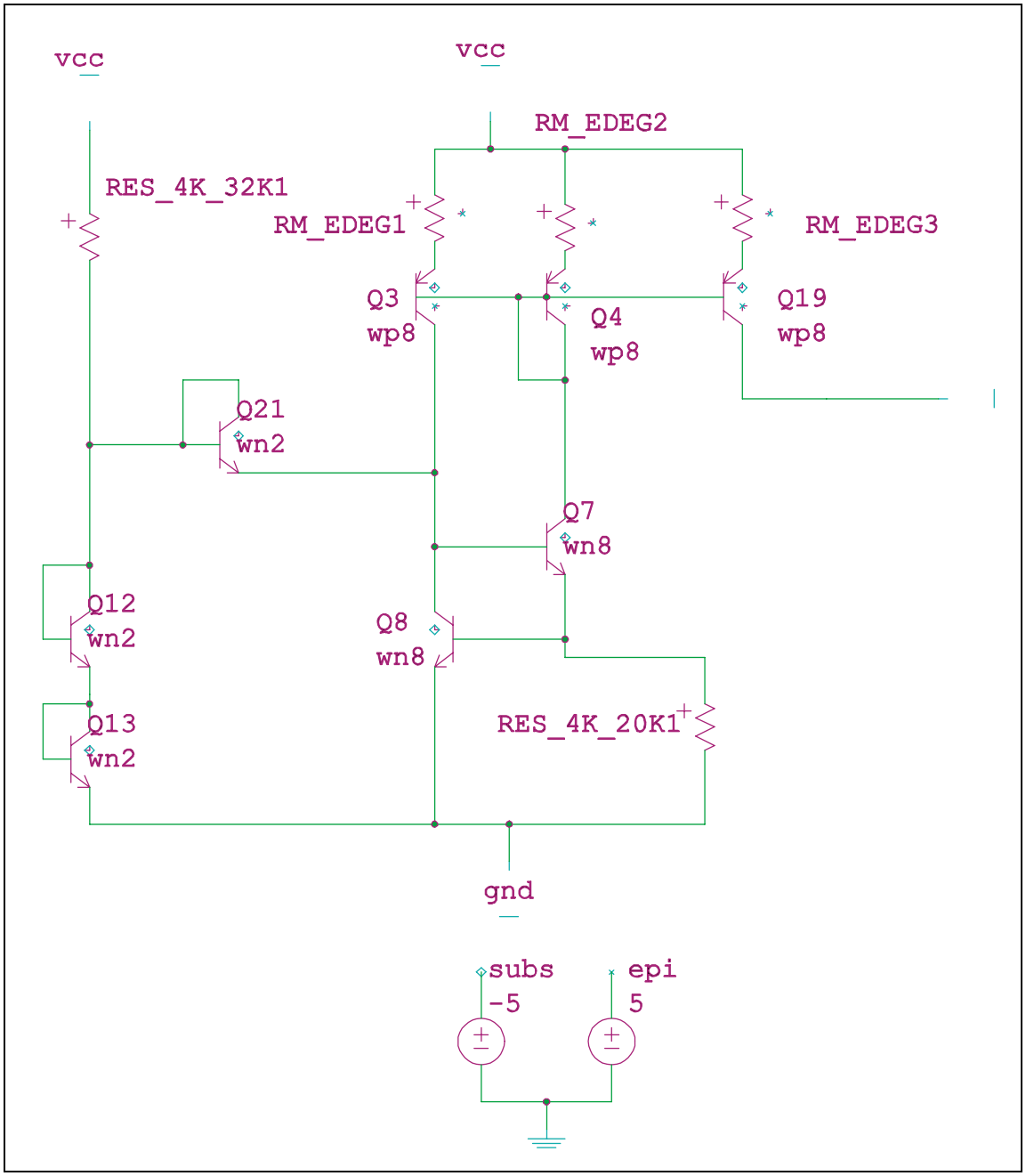
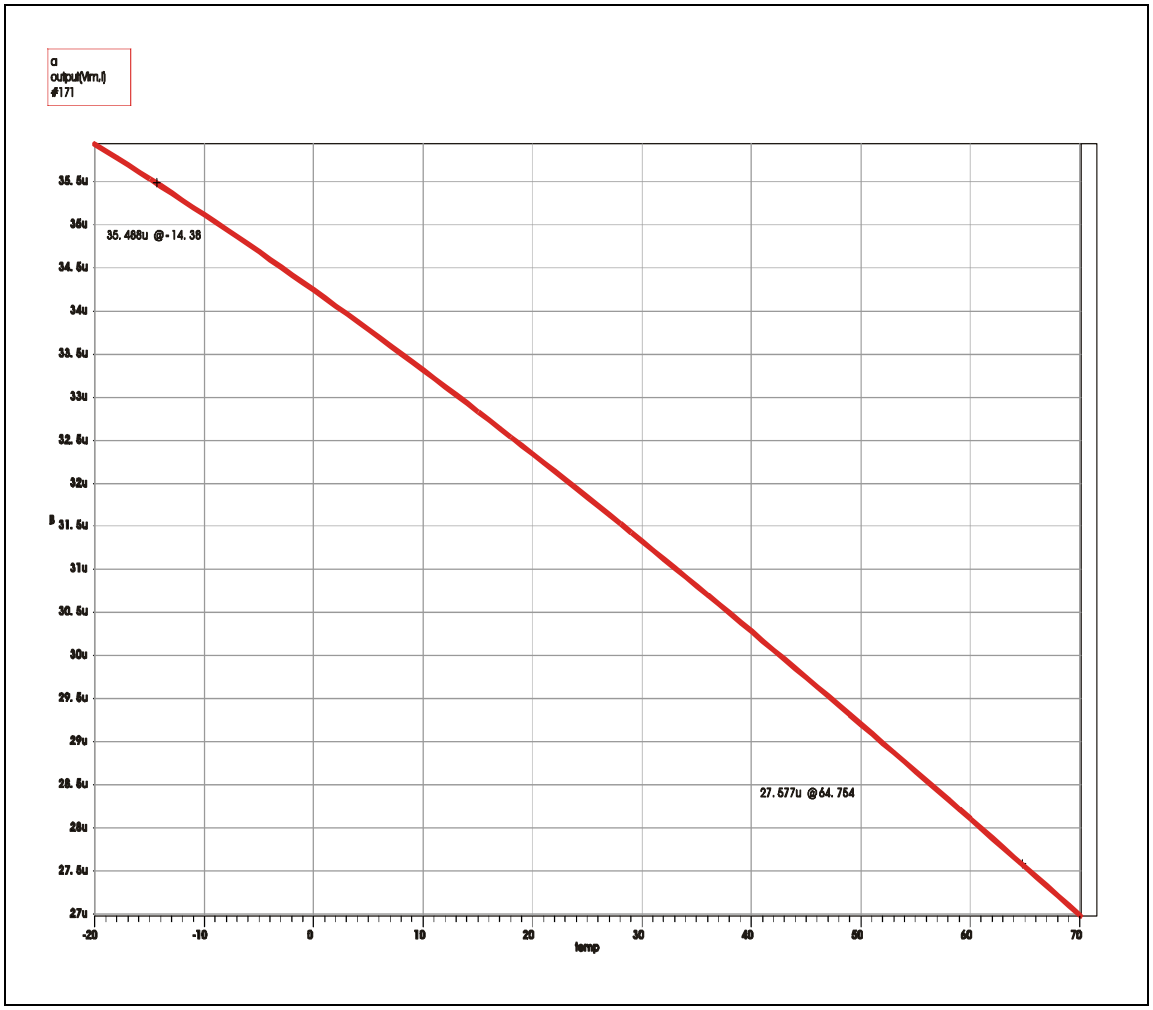


Figure 5: Current Source Temperature Variation



3.0 Verification

3.1 Temperature Sweep

3.1.1 Output Voltage and Temperature coefficient

Figure 6 displays the output voltage for a temperature sweep across the military temperature range of -55C to 125C. The reference maintains a stability of 17ppm across the commercial temperature range, (0c-70C) and a 50 ppm stability across the military temperature range. Figure 7 shows the zero temperature coefficient (TCF) point, about 27.1C when the TCF versus temperature is plotted. TCF is the first derivative of volts with respect to temperature and is plotted as uV/C in Figure 7.

Figure 6: Output Voltage vs Temperature

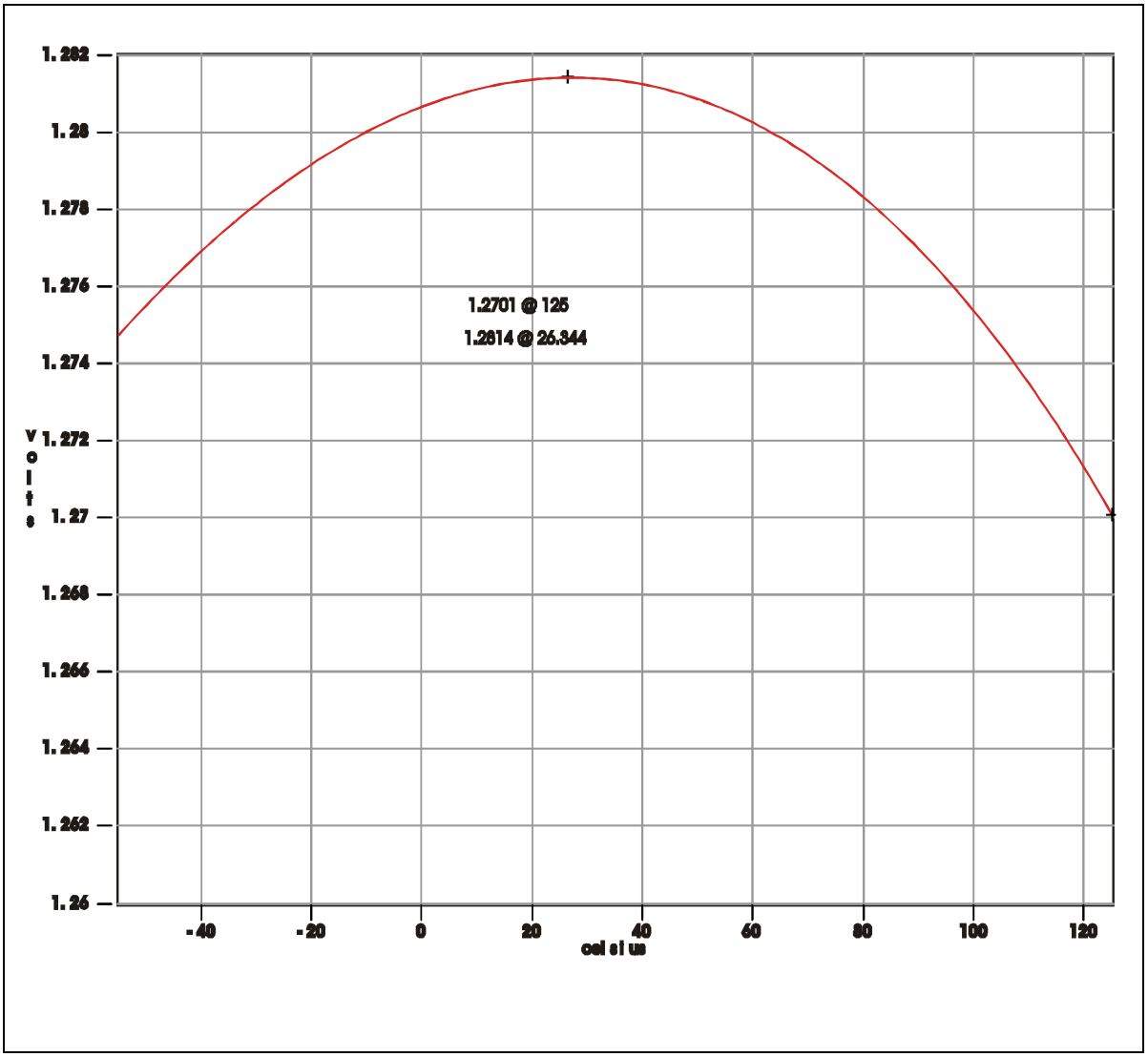
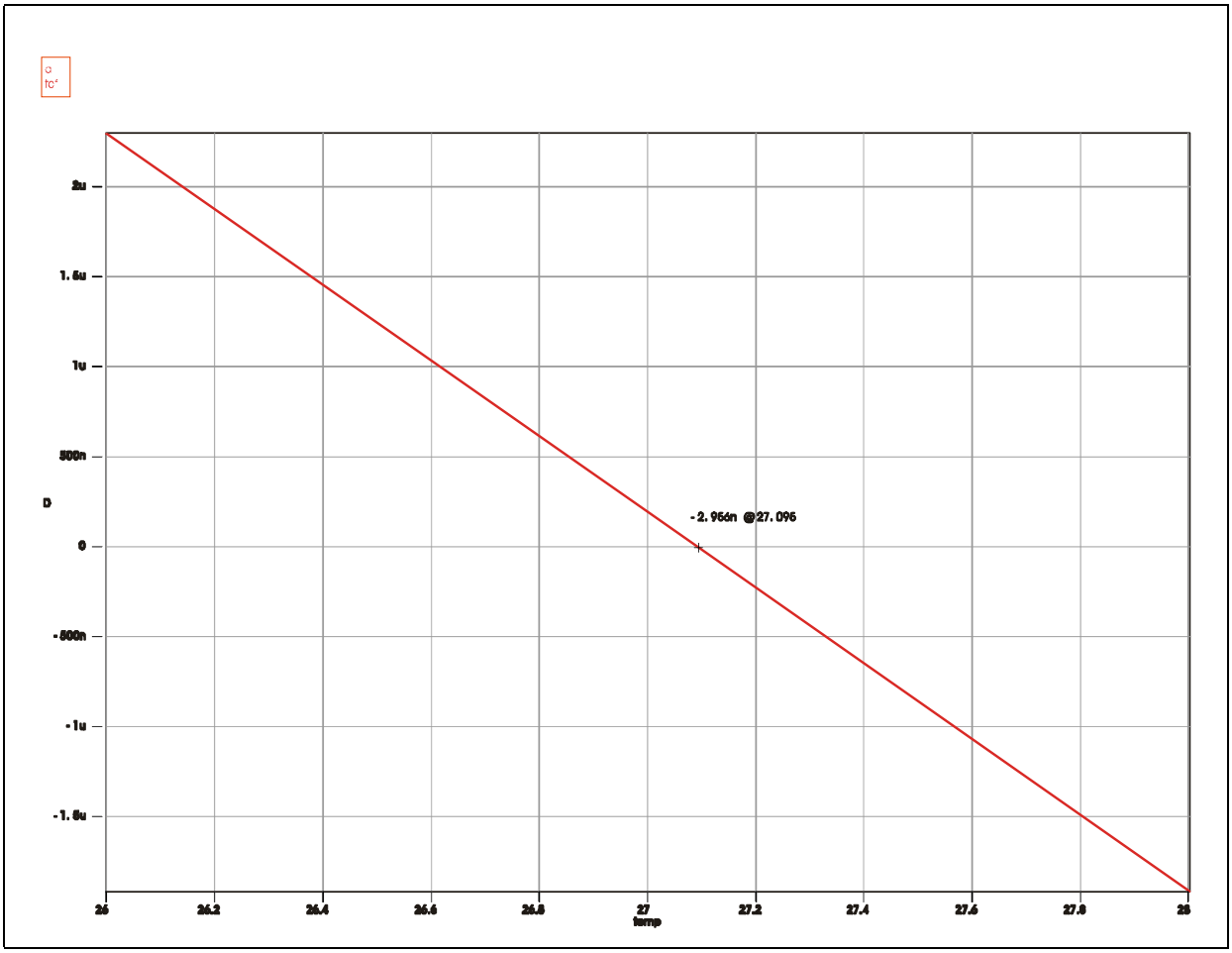


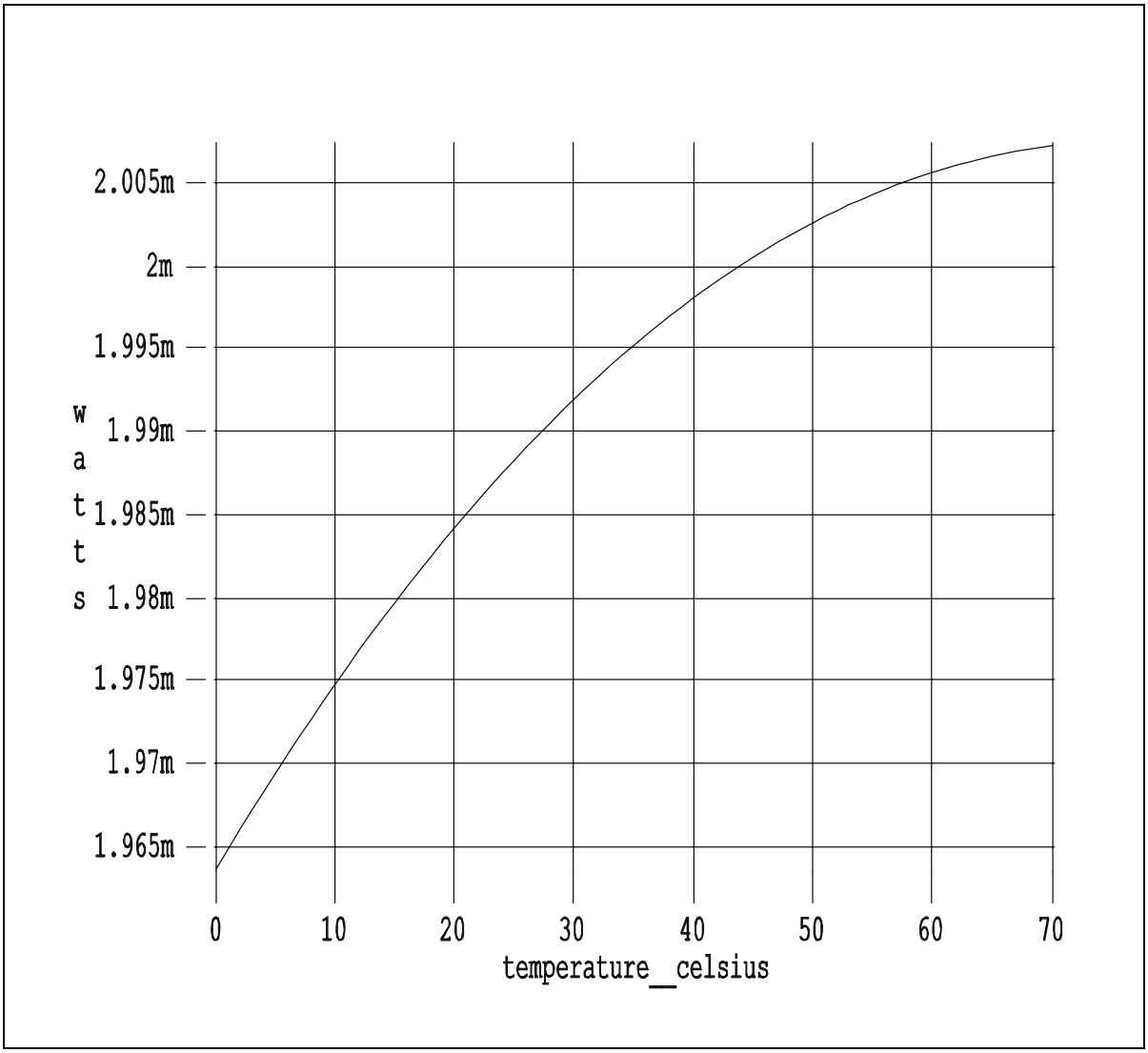
Figure 7: TCF vs Temperature



3.1.2 Power dissipation

Power dissipation with respect to temperature in Figure 8. The worst case power dissipation occurs at high temperatures and was measured at 2.1 mWatts.

Figure 8: Power Dissipation vs Temperature



3.2 Start Up Test

A start-up transient test was performed to verify the circuit did not fall into any quasi-stable state. The start-up circuit forces the bias point of the output voltage to reach an appropriate voltage of approximately 1.1 volts. After the output voltage reaches its nominal voltage the startup circuit shuts off and does not draw any power. Inclusion of this circuit guarantees the output will reach a stable bias point.

The startup circuit was implemented as a chain of diodes connected to Vcc and the output circuit. Six diodes in series provides a low impedance to charge the output to approximately 1.1 volts. In normal operation, the last diode is reversed biased which draws pico-amps of current from the output node.Figure 9, Figure 10 show the transient response and the startup circuit current.

In Figure 9, the power supply, VCC was stepped from 0-5 volts in 500ps. The output settled to its nominal voltage after about 16 NS. Figure 9 shows the startup circuit shuts off after about 14 ns.

Figure 9: StartUp Transient response

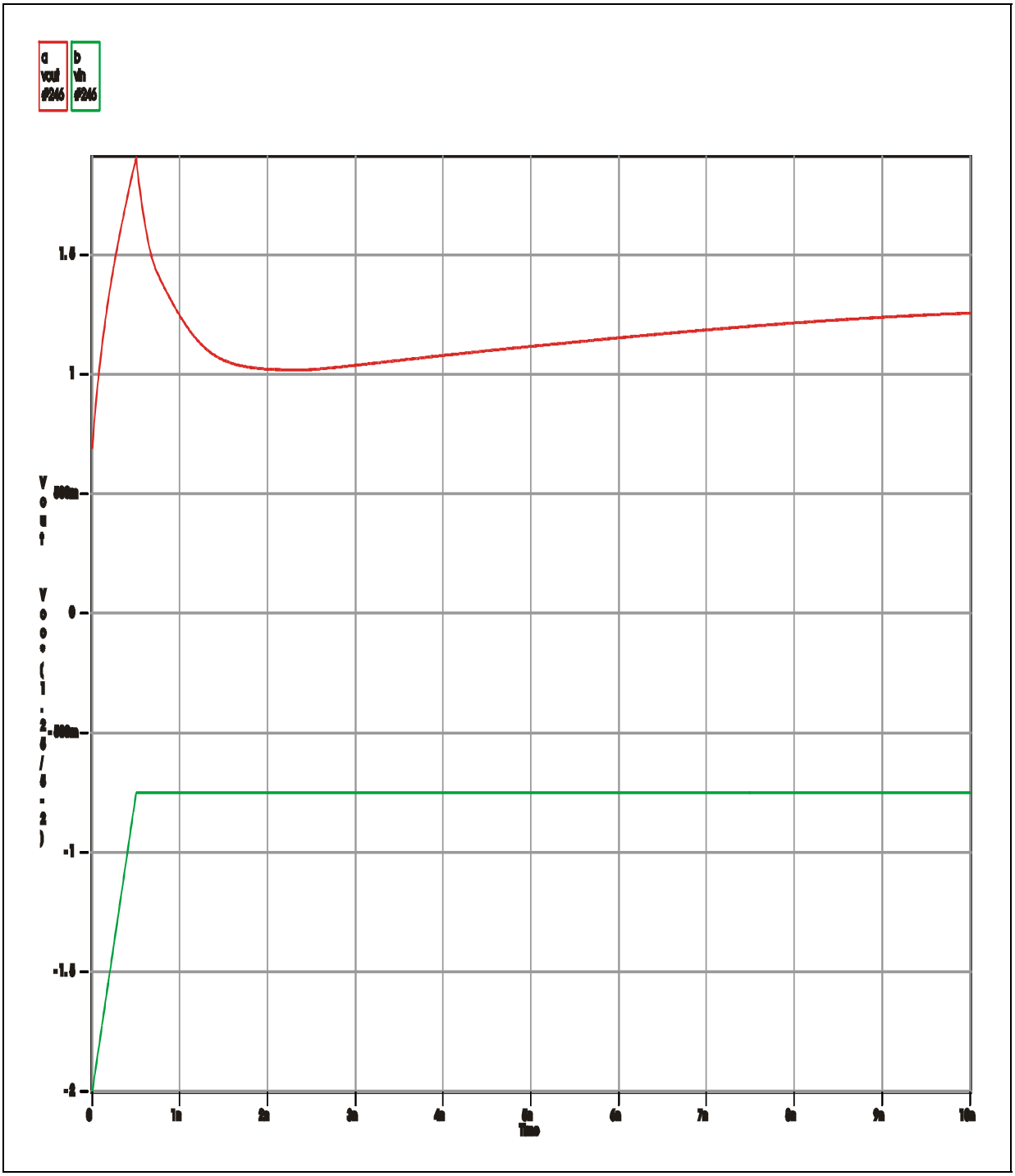


Figure 10: Startup Circuit Current

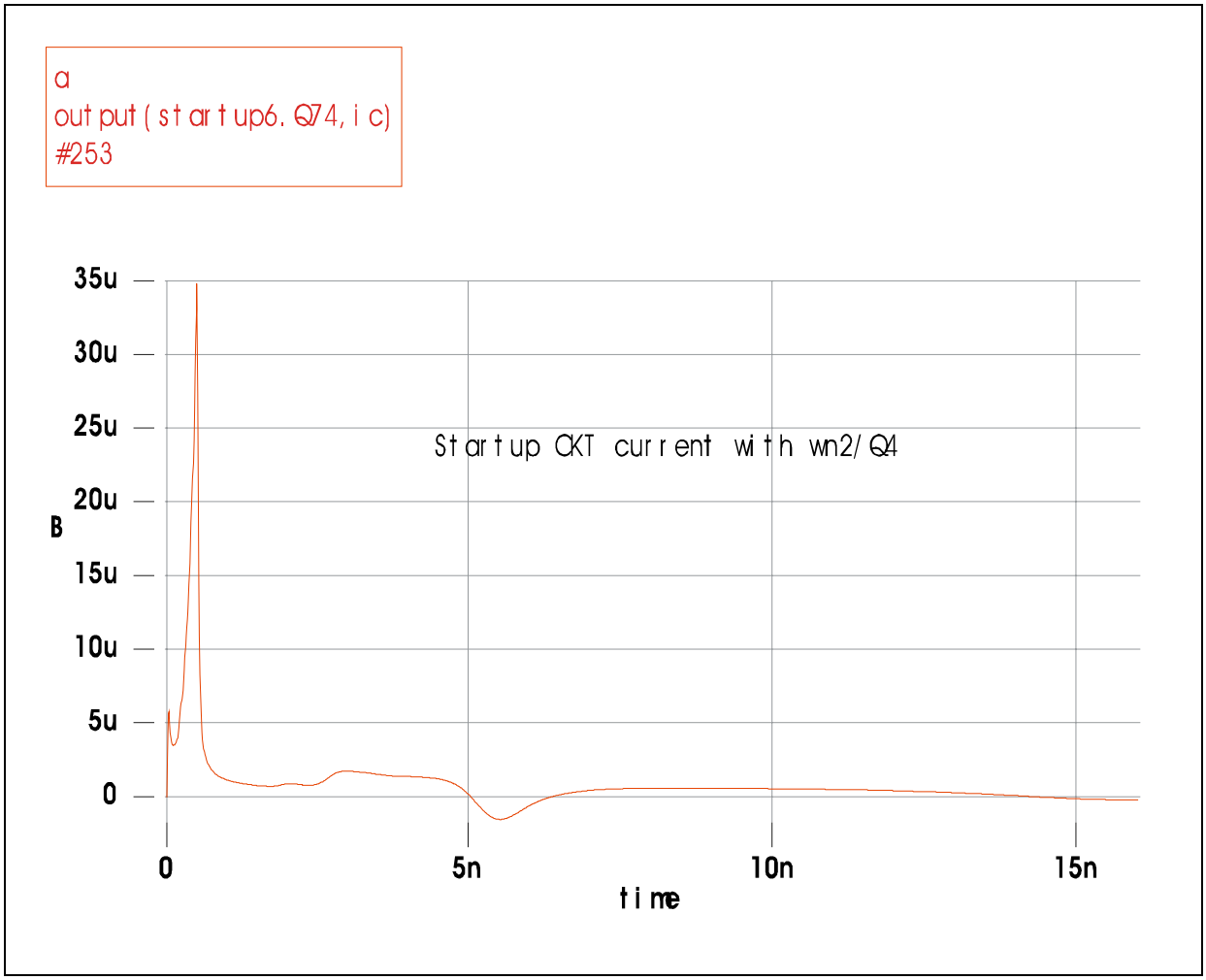
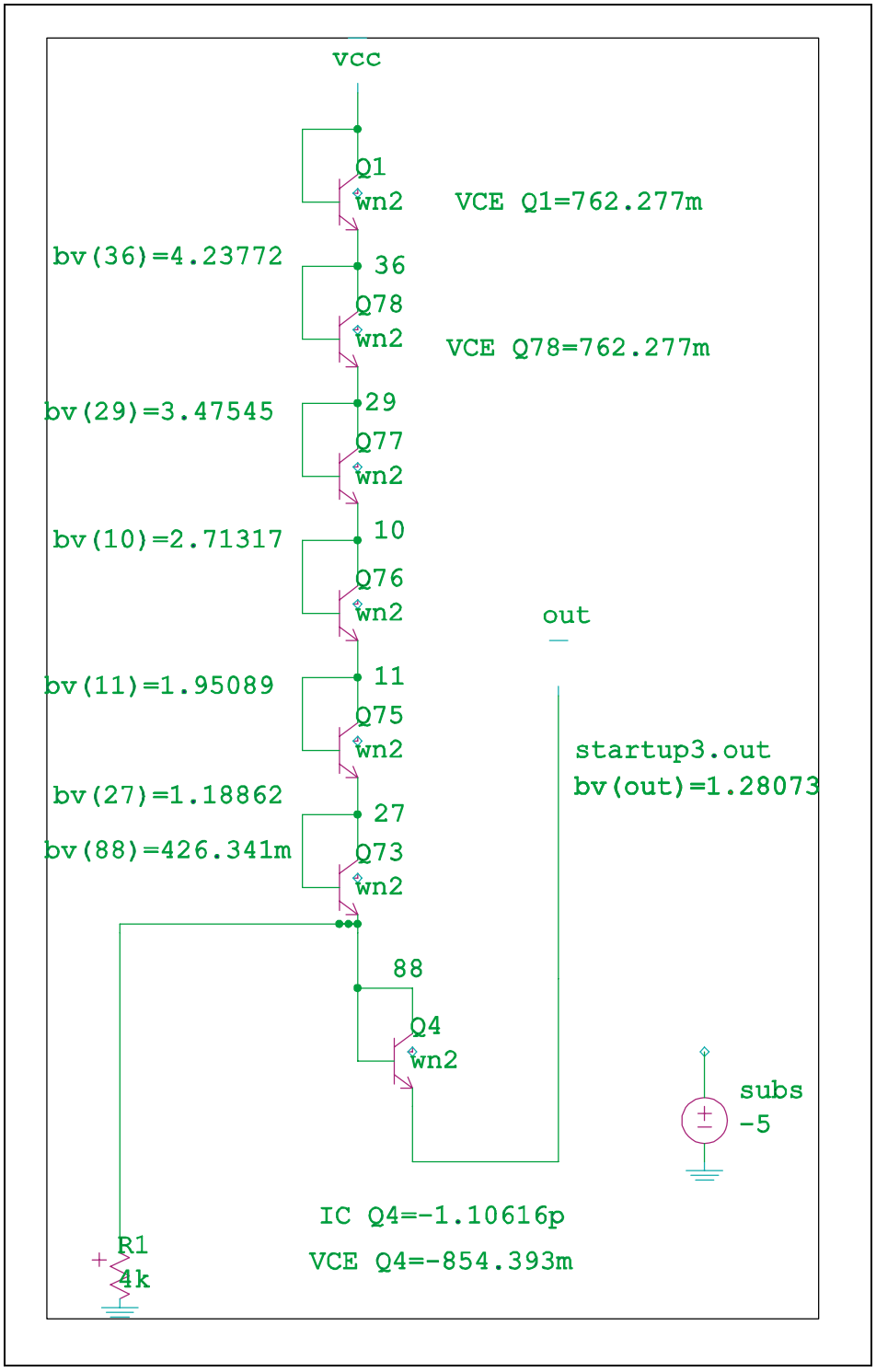


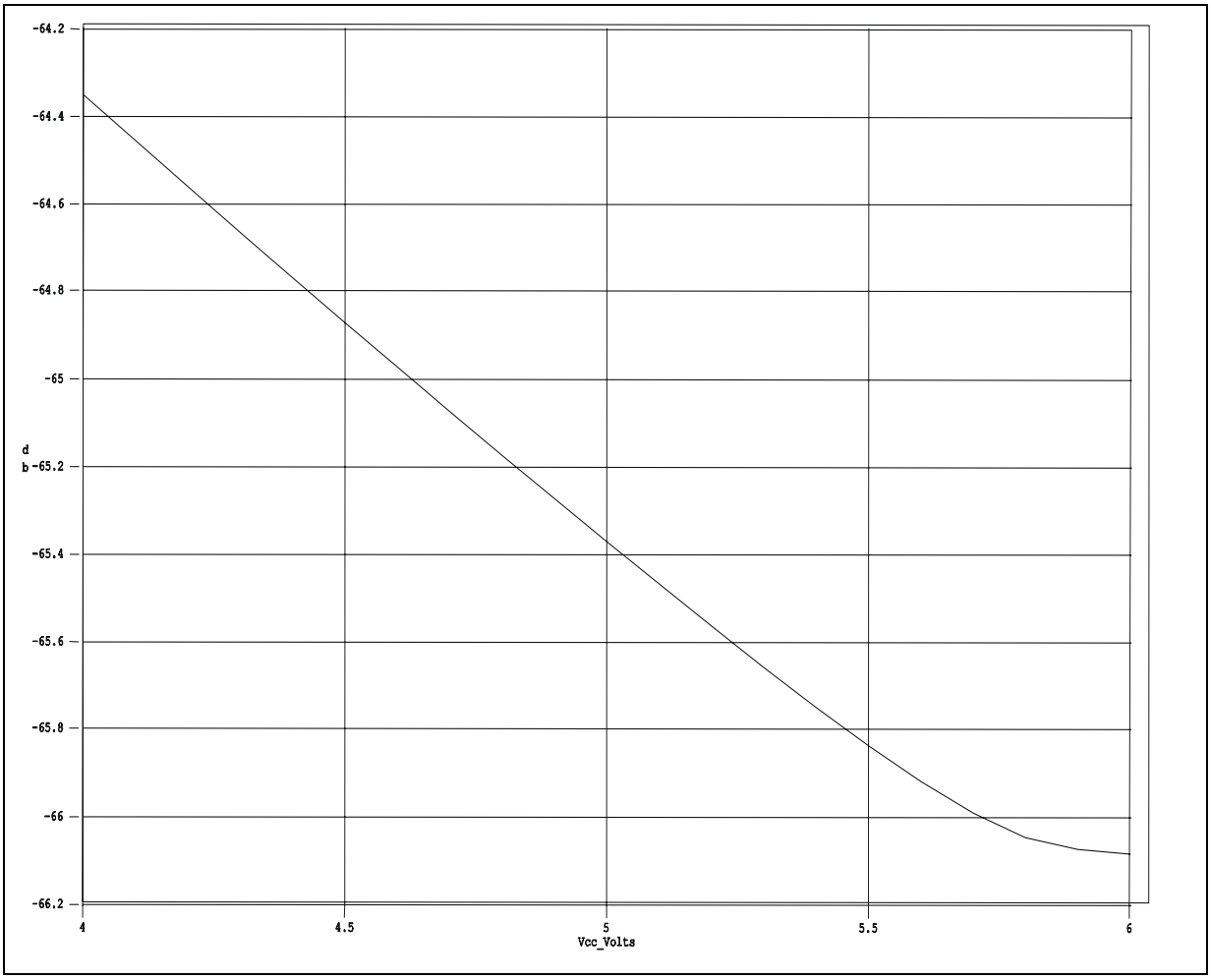
Figure 11: Startup Circuit



3.3 Power Supply Rejection Ratio Measurement

The DC power supply rejection was measured by sweeping the power supply voltage from 4 to 6 volts and observing the nominal change in output. A 64 db power supply rejection was measured as shown below in Figure 12.

Figure 12: DC Power Supply Rejection Ratio

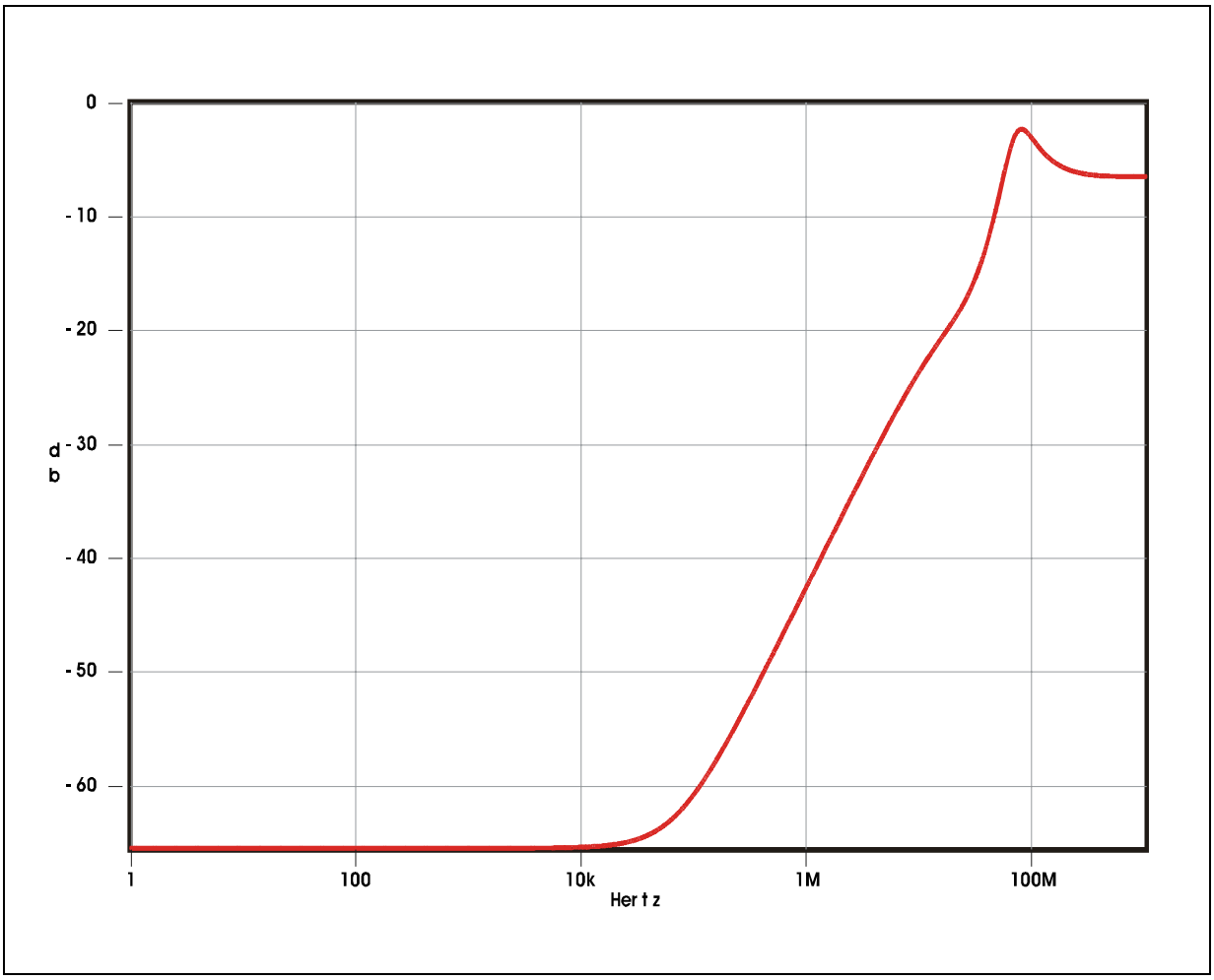


3.4 AC Power Supply rejection.

The AC power supply rejection ratio was measured by applying a 1V ac voltage to the power supply and measuring its magnitude at the output, Figure 13. At DC frequencies the PSRR begins at -60db and sweeps upward in magnitude at a rate of 40db/decade. It levels

off at approximately 990KHZ where peaking is present. This suggests a complex set of poles exist at 990 MHZ and a set of zeros near 20KHZ. The complex poles present at 900 MHZ, complicate the design of a filtering network because complex zeroes are needed to suppress the peaking at 990 MHZ. Peaking at this frequency will remain without the use of complex zeroes which indicates that using simple decoupling caps will not flatten out the magnitude response. An appropriate low pass second order AC power supply filter with a set of poles near 990 MHZ are needed to flatten out the AC response. This will require capacitors and inductors, (ferrite beads possibly) to be added to the power supply inputs of this circuit. A simple first order low pass filter will reduce the magnitude response above and below the complex pole location but still leave the peak.

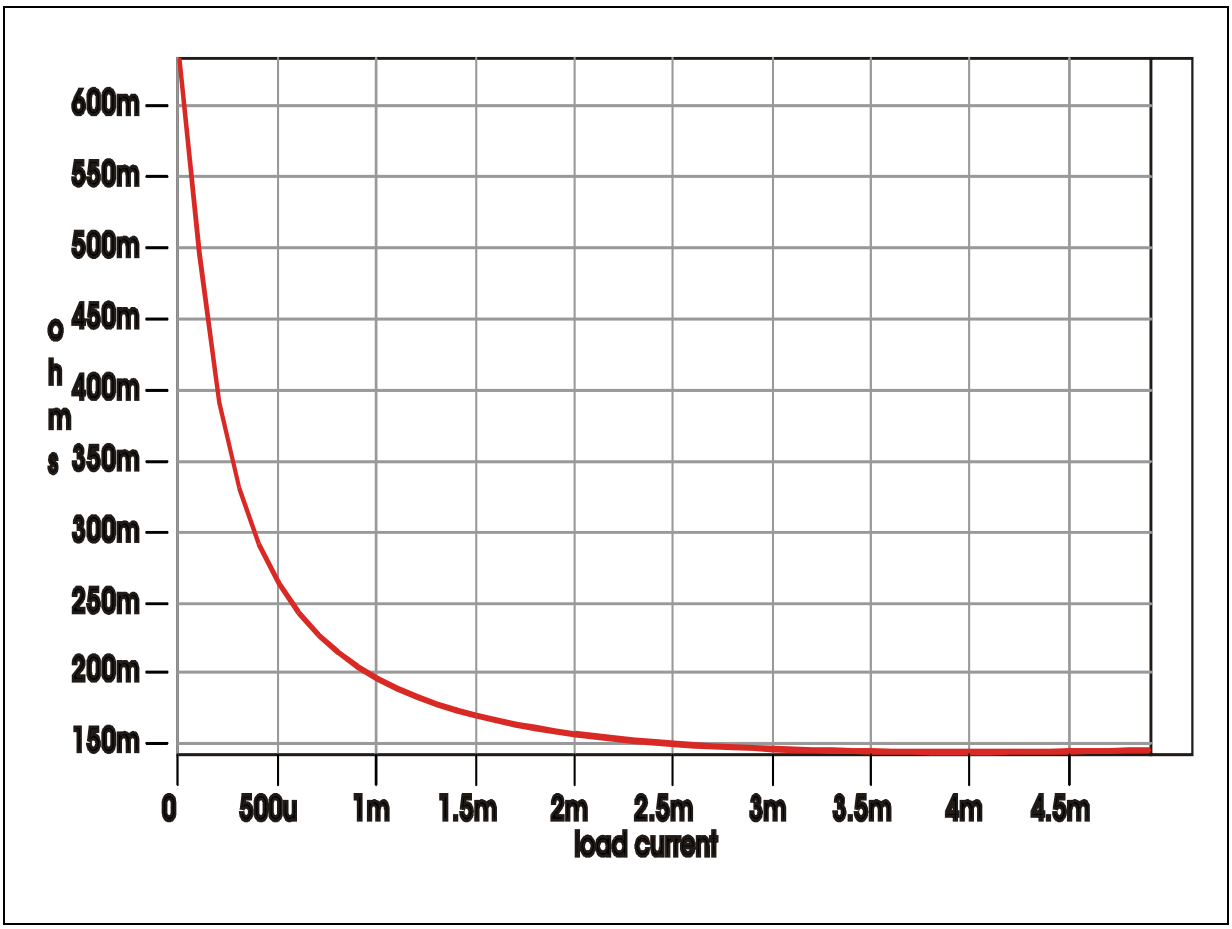
Figure 13: AC PSRR



3.5 Output Impedance Test

The output impedance was measured by applying a test current load on the output and sweeping the current from 1 nA to 5mA, Figure 14. At 1 nA the impedance was measured at 633 mOhms and decreased to about 150 mOhms at 5 mA. Further improvements can be made by replacing the wn-8 darlington pair with a wn-2 darlington pair. The darlington pair with smaller emitter ratios was tested and resulted in approximately have half the output impedance as shown Figure 14.

Figure 14: Output Resistance vs Load Current



3.6 Load Stability

Load stability was measured by applying a 1 ma step load at the output of the circuit. The load was stepped from 1ma to 2ma in 100 ps and the output voltage was plotted in Figure 15, the input step is also shown in Figure 20. Figure 15 shows the resulting closed loop step response. The response is clearly under-damped and settles within 35 ns. No continuos oscillations were observed so the system is stable. Ideally, a voltage reference should be slightly under-damped to filter out load transients and maintain a stable reference. From Figure 15, the damping factor can be estimated along with the natural frequency to characterize the system as a two-pole dominant response, where a pair of complex poles completely dominate the transient response over other less dominant poles.

The damping factor can be increased by inserting a compensation capacitor across the emitter of the Q4 darlington pair and ground. This is the point at which feedback is applied and should slow down the response time of the circuit. The compensated response is shown in Figure 16. Here various load values ranging from 0.1 to 9.1 pf were inserted. A value of approximately 4.1 pf yielded a critically damped response.

Figure 15: Uncompensated Load Step Response

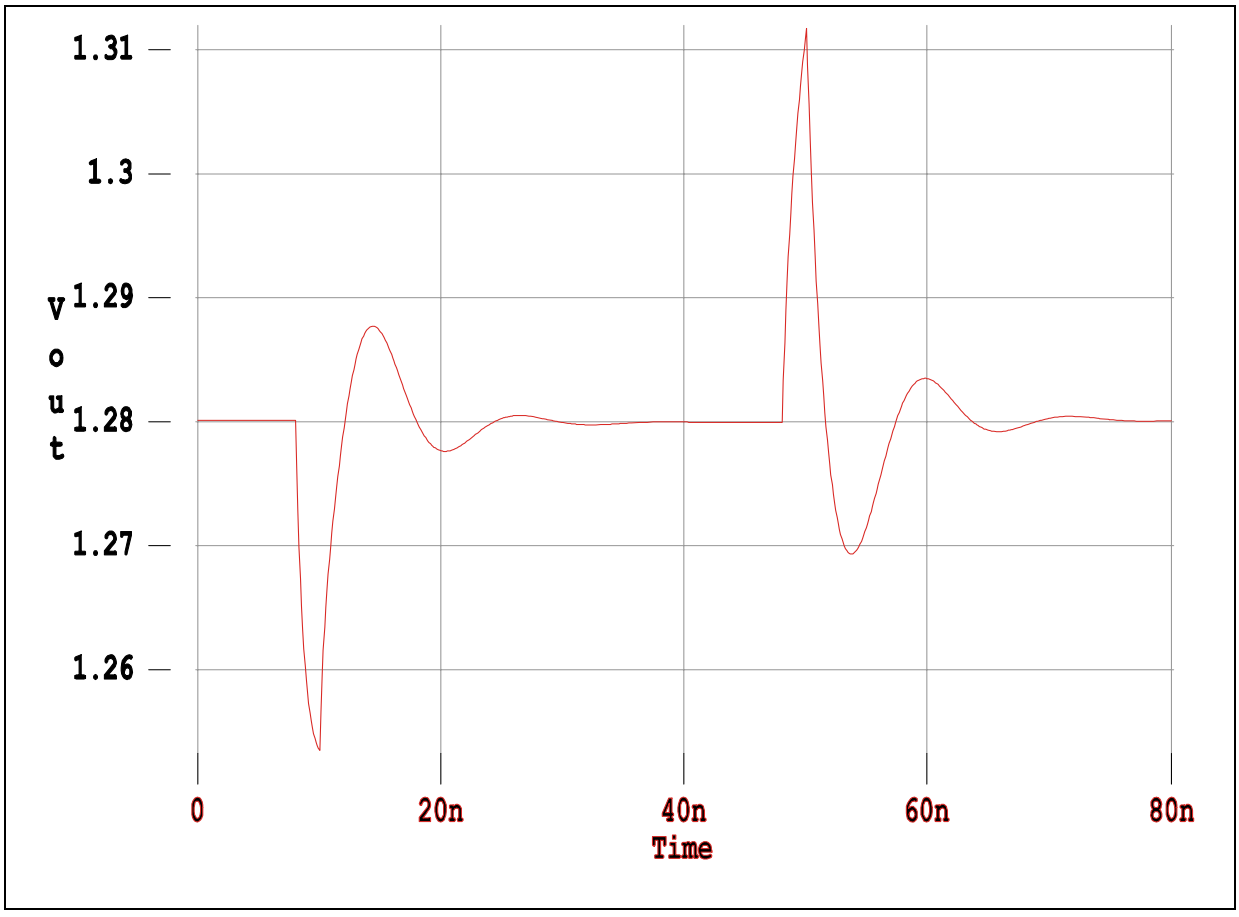
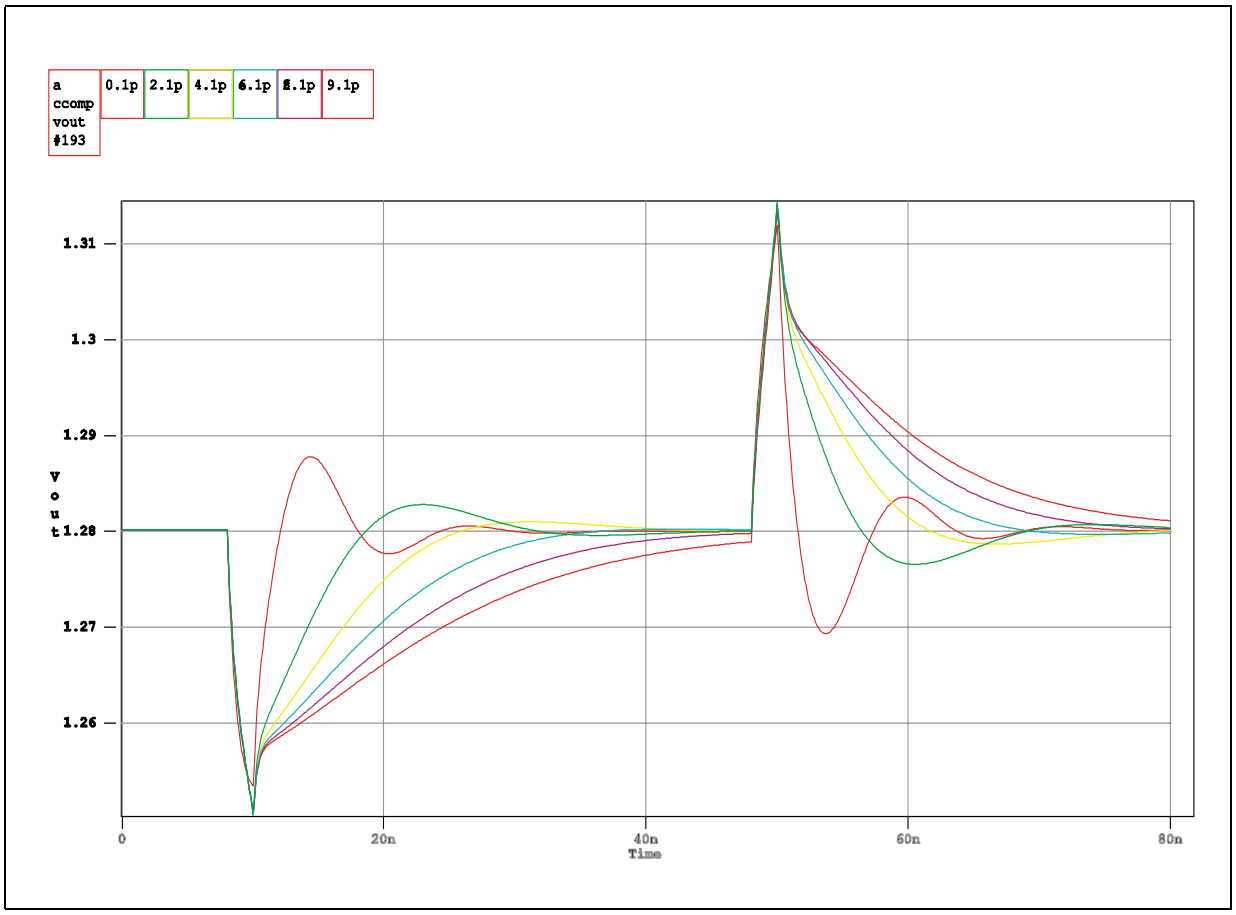


Figure 16: Compensated Output Transient Response



3.7 Stability Measurement and Analysis

Stability can only be guaranteed by measuring the phase margin of the open loop response. Adding phase margin will insure that the system will remain stable despite variations in component values due to aging, temperature or process. Phase margin is measured by plotting the response of the loop transfer function (open loop) and measuring the phase at which the loop gain is unity. The open loop transfer function was measured in SPICE using a method developed by Rosenstark [1]

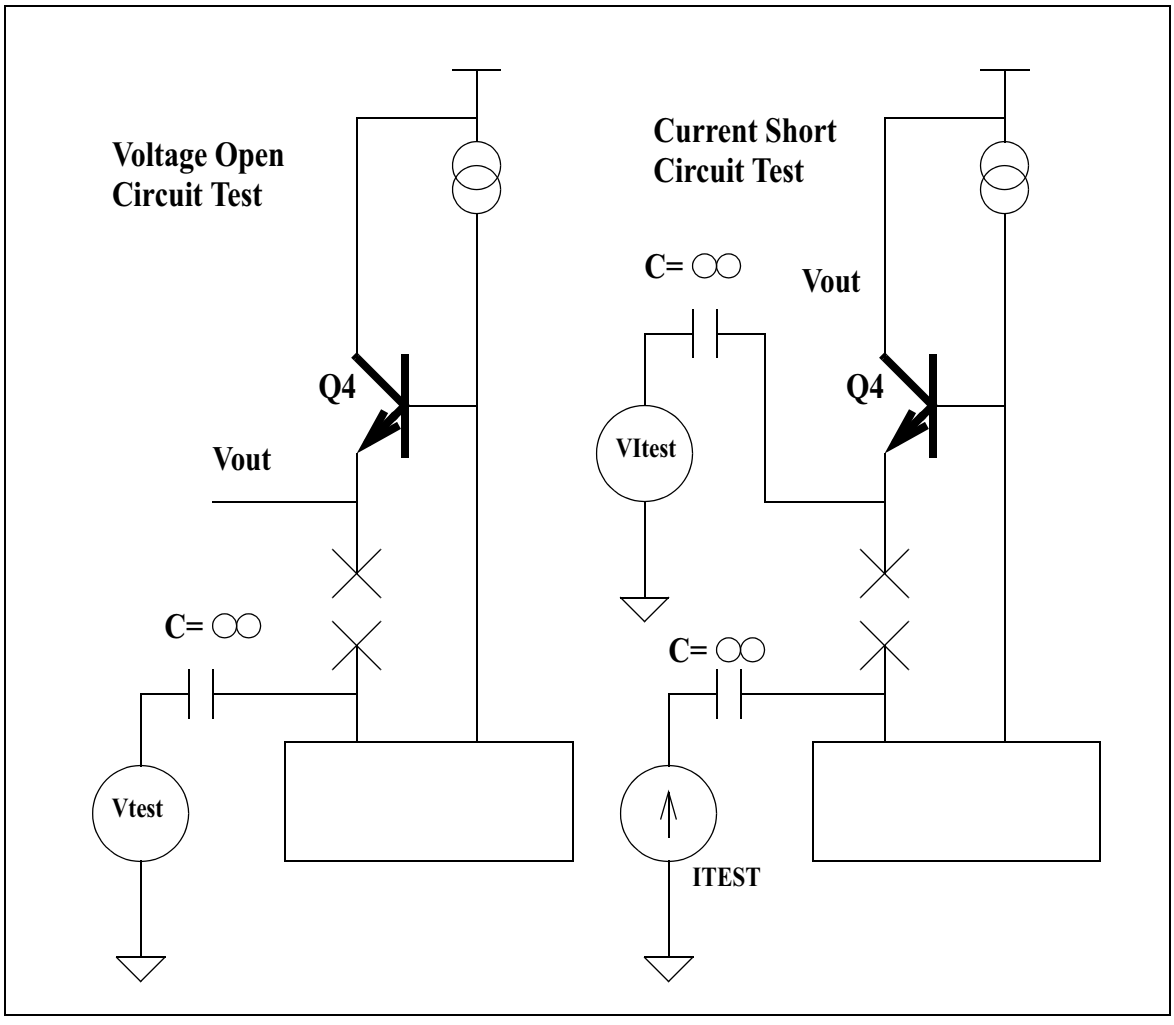
The Rosenstark method breaks the closed loop at a convenient location and applies two test circuits, an open circuit voltage measurement and a short circuit current measurement. The sum of these two output responses can be shown to be equal to the loop response by the following formula:

$$AB = -\frac{1}{\frac{1}{VOC} - \frac{1}{ISC}} \quad \text{(EQ 12)}$$

where ISC is the current gain of the short circuit response and VOC is the voltage gain of the open circuit test.

The Rosenstark method involves breaking the loop at a convenient location, applying a voltage at one end and measuring the response at the other end. Similarly, the current response is measured by applying a current at one end of the break and measuring the current at the other end of the break. This is shown conceptually in Figure 17. Q4's emitter was chosen for the location of the break.

Figure 17: Open Loop Test Fixture



Breaking the loop must be done in such a manner as to not interfere with the DC biasing of the circuit. This is accomplished by inserting a huge inductor at the breakpoint of the feedback loop. The inductor values of 1e6 henries have been simulated and work well. Lower values of 1e4 henries affect the lower frequency response of the circuit. The shorting network is applied by inserting a current source coupled with a huge capacitor at the break and shorted at the other end of the break with a voltage source to measure the current. The transfer function is easily simulated by making two copies of the circuit, applying the two test fixtures to them and pasting both of them on the same schematic. An ac simulation is run next to generate the two responses and the control program will generate the open loop response according to (EQ 12). The test program used to run the simulation is shown in Table 3. Figure 21 shows the test circuit used to measure the open loop response, Figure 22 shows the voltage measurement test circuit and Figure 23 is the short circuit current measurement circuit.

Table 3: Test Program

```
clear
ccomp=4p
ac analysis freq: 1e3, 1e9, 15 type=dec itl1=10k itl7=50 itl8=10
endac
vtmag=mag(v(Vtest))
vtphase=phase(v(Vtest))
;plot vtmag
;plot vtphase
;vact=vtmag*atan(vtphase)
;plot vact
vVtest=v(Vtest)
cvt=imag(vVtest)
rvt=real(vVtest)
itest=output(Vtest,i)
;plot itest
cvti=imag(itest)
rvti=real(itest)
;plot cvt
;plot rvt
tf=-1/(1/itest + 1/vVtest)
plot vVtest
plot itest
plot phase(tf)
plot db(mag(tf))
```

The open loop magnitude, Figure 18, and phase response, Figure 19 are shown below. The open loop magnitude response is clearly below unity and should result in stable operation. Furthermore, the phase shift occurs at ~200MHZ where the gain is clearly below unity. Both of these simulations were performed with a compensation capacitor of 4pf.

Figure 18: Open Loop Magnitude Response

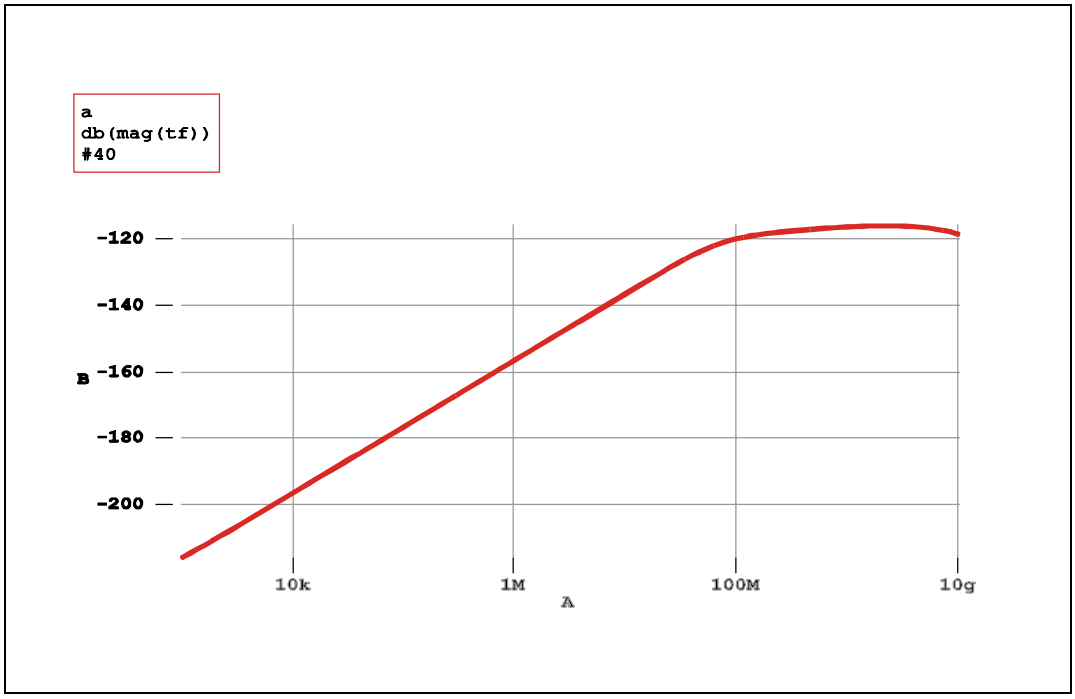


Figure 19: Open Loop Phase Response

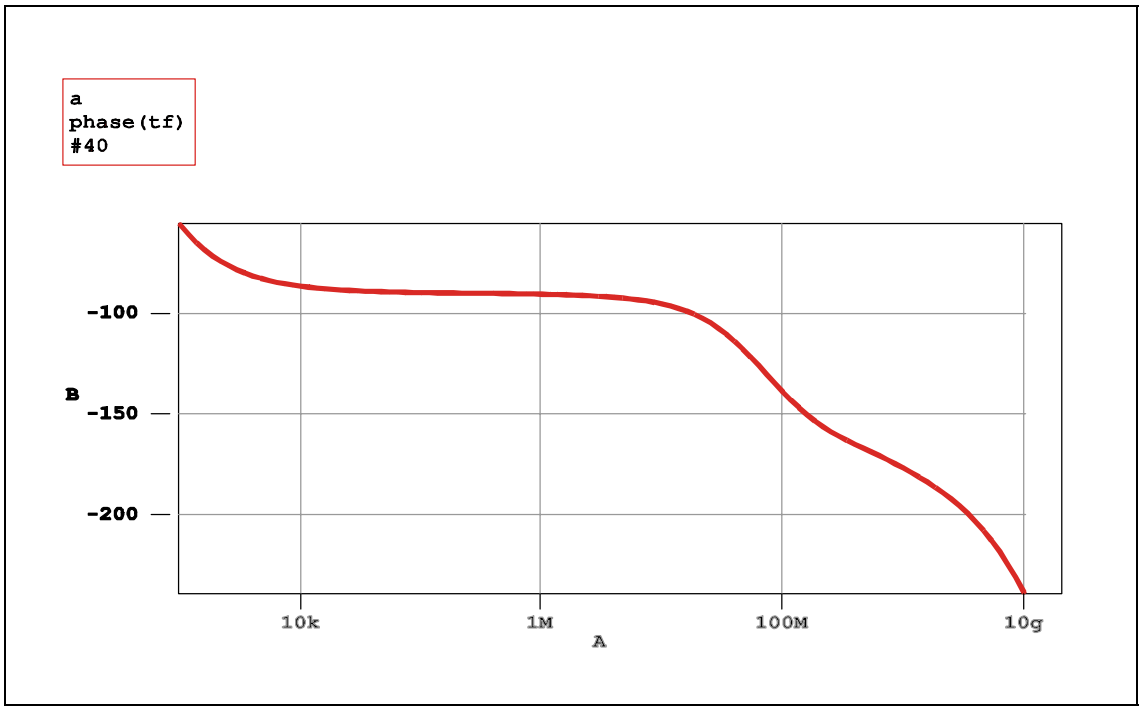


Figure 20: Unit Step Load

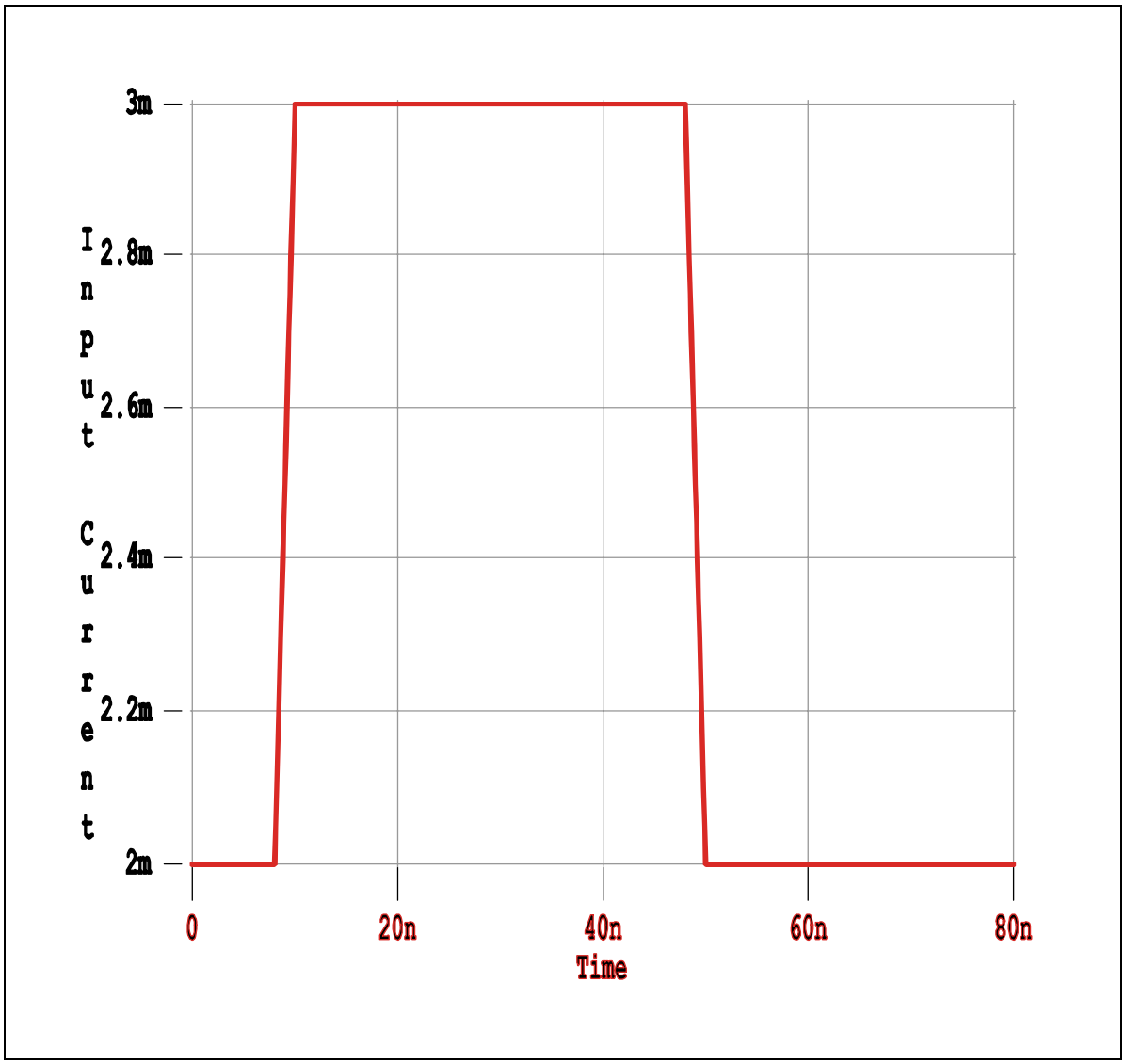


Figure 21: Open Loop Test Fixture

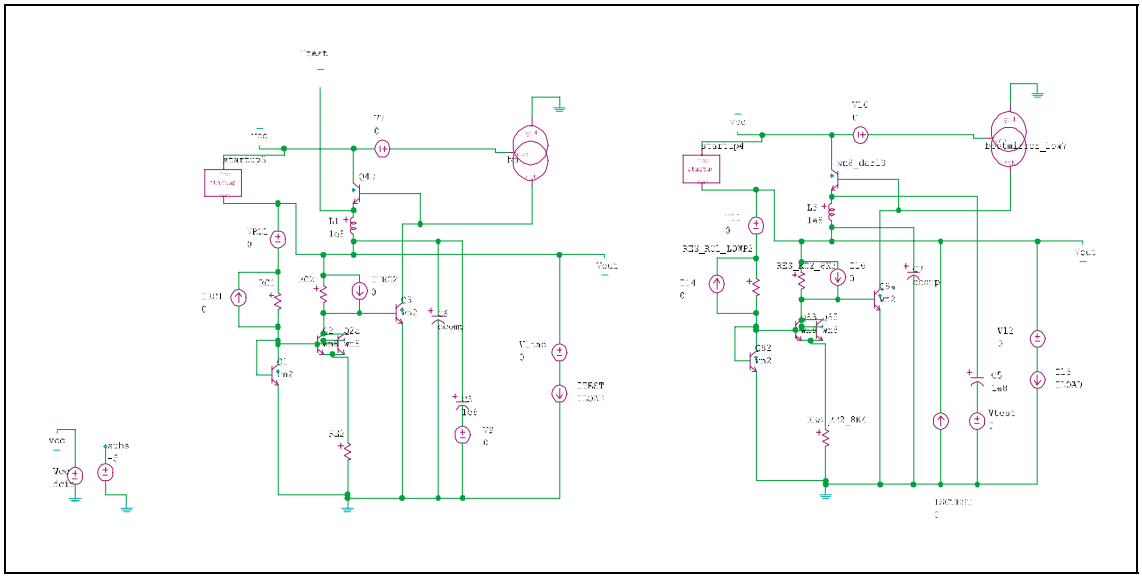


Figure 22: Open Circuit Open Loop Test Fixture

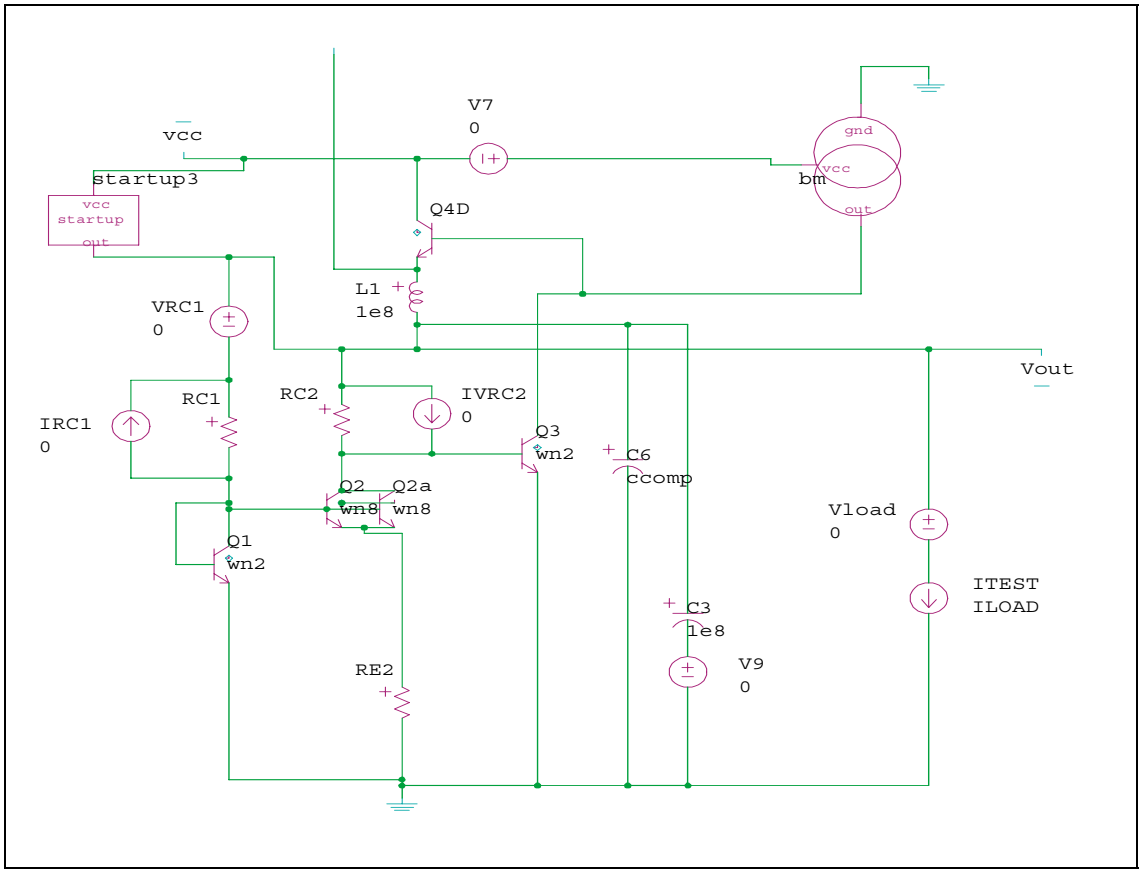
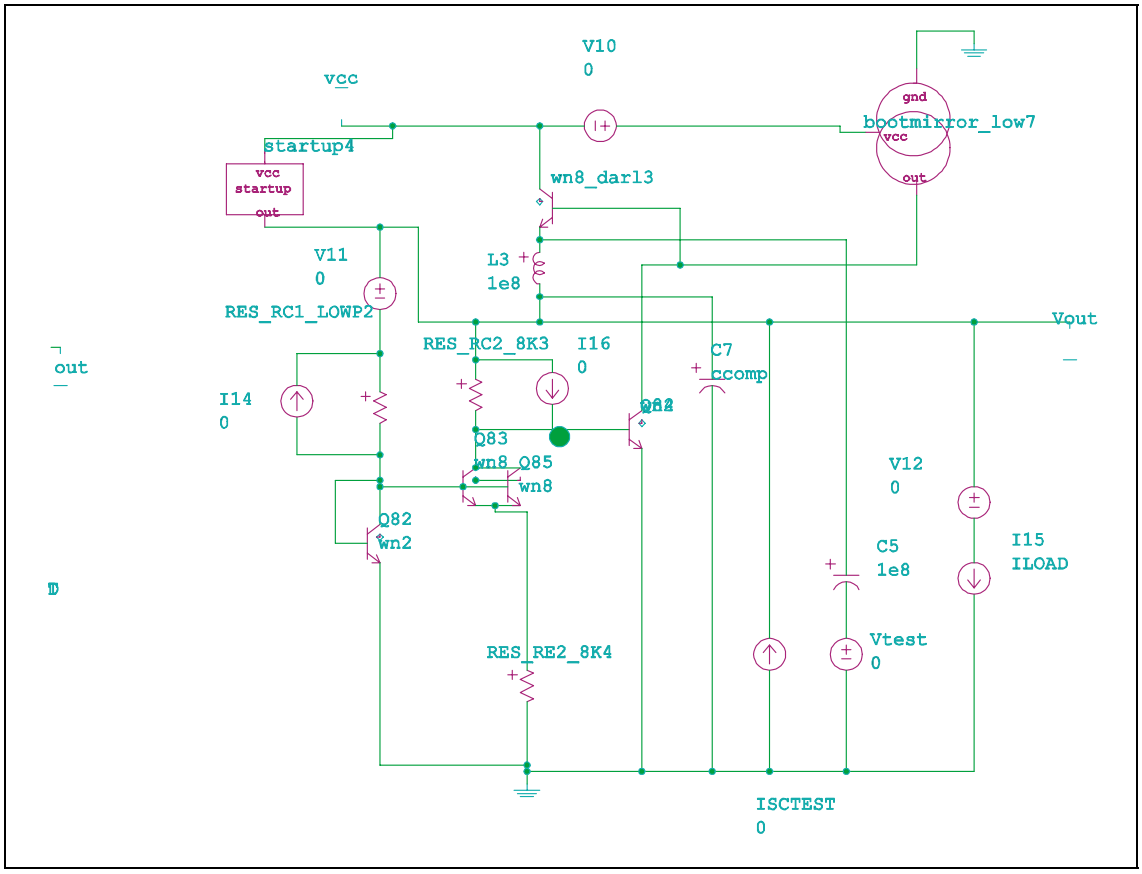


Figure 23: Short Circuit Open Loop Test Fixture



A. High Power/Low Power Comparison

The following set of figures show the output voltage, power disspation and TCF for the high power cell. Figure 24, is the TCF for the high powered cell. The outstanding TCF is due to the well matched slope of the dVBE3/DT, Figure 29, and dIRC2 curves which when summed max out to a 20 uV/C temperature coefficient. These two curves represent the two voltages which are summed together to form the output voltage. Matching the first and second order derviatives of these voltages is necessary for a superior voltage reference. The high power cell has both a first and second order compensation. The first order compensation is done by merely adding the VBE3 and voltage across RC2 which have opposite temperature coefficients. In the low powered cell, the voltage across RC2, Figure 27, does not have a 2nd derivative (slope) which is equal and opposite to the dVBE voltage, Figure 29. On the other hand, the high powered cell's RC2 voltage drop, Figure 28, has a slope nearly equal and opposite to the dVBE/DT voltage of Figure 29. This situation will be investigaged further.

Figure 24: TCF (Dv/DT) High Current cell

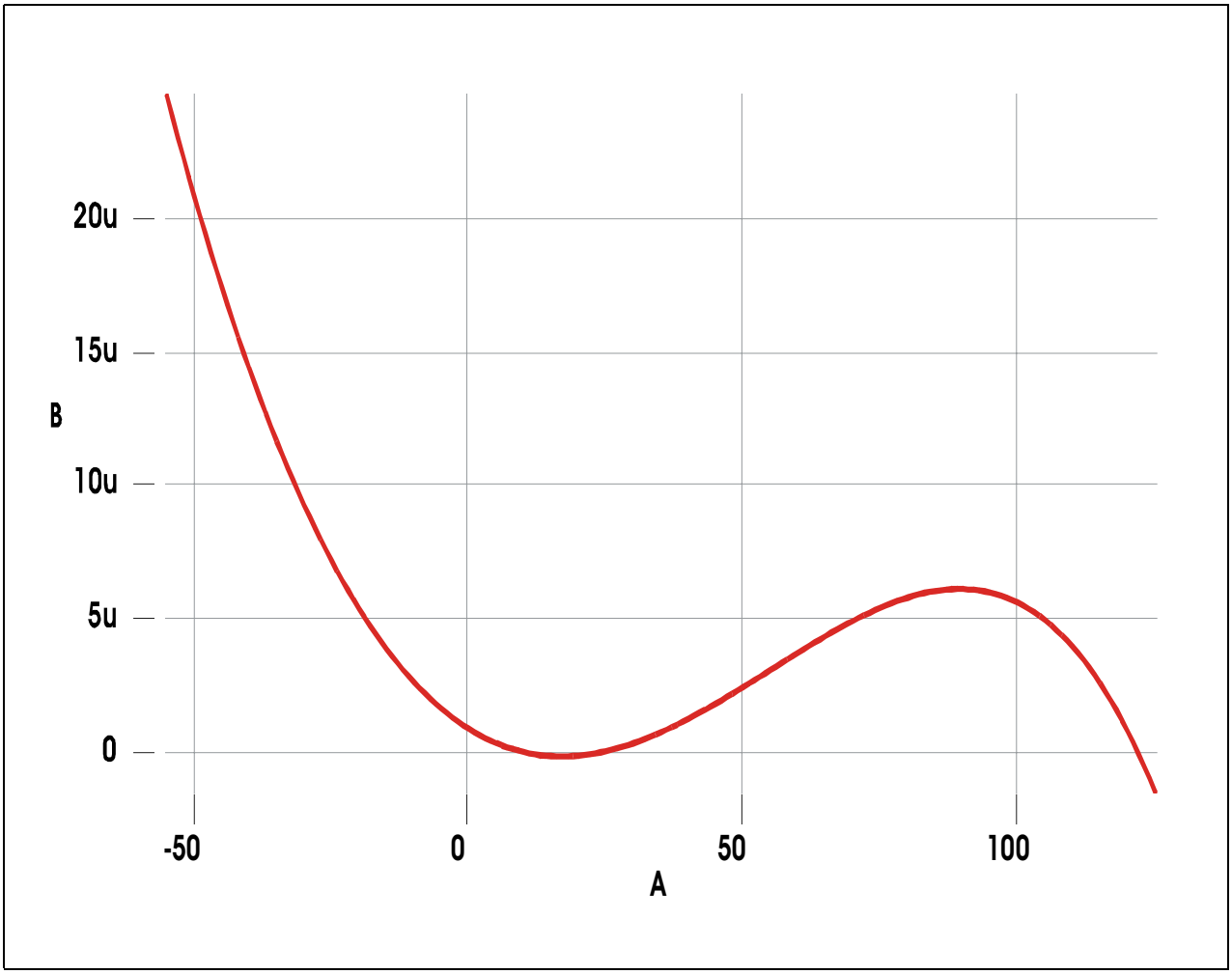


Figure 25: Output Voltage High Current cell

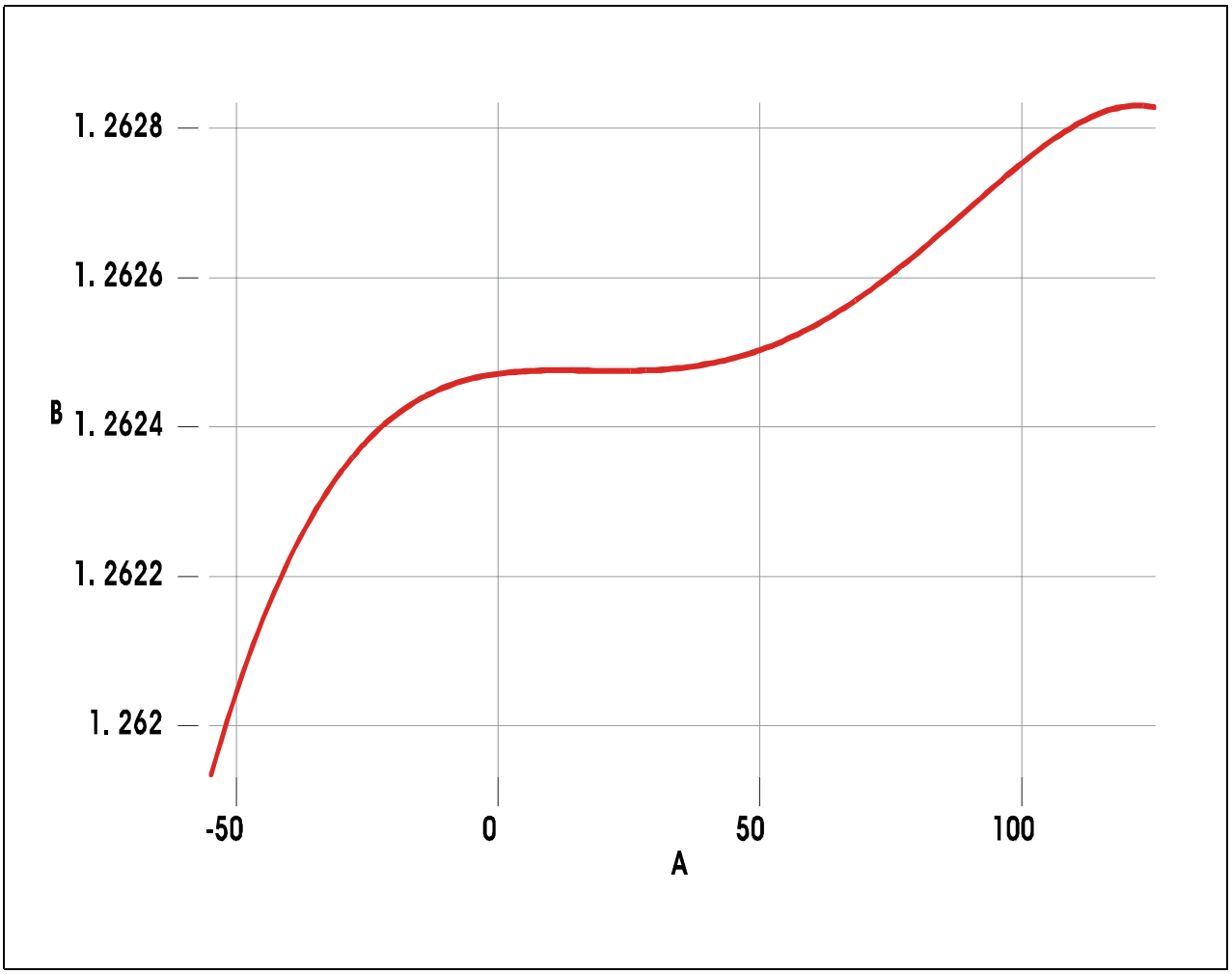


Figure 26: Power Dissipation High Current cell

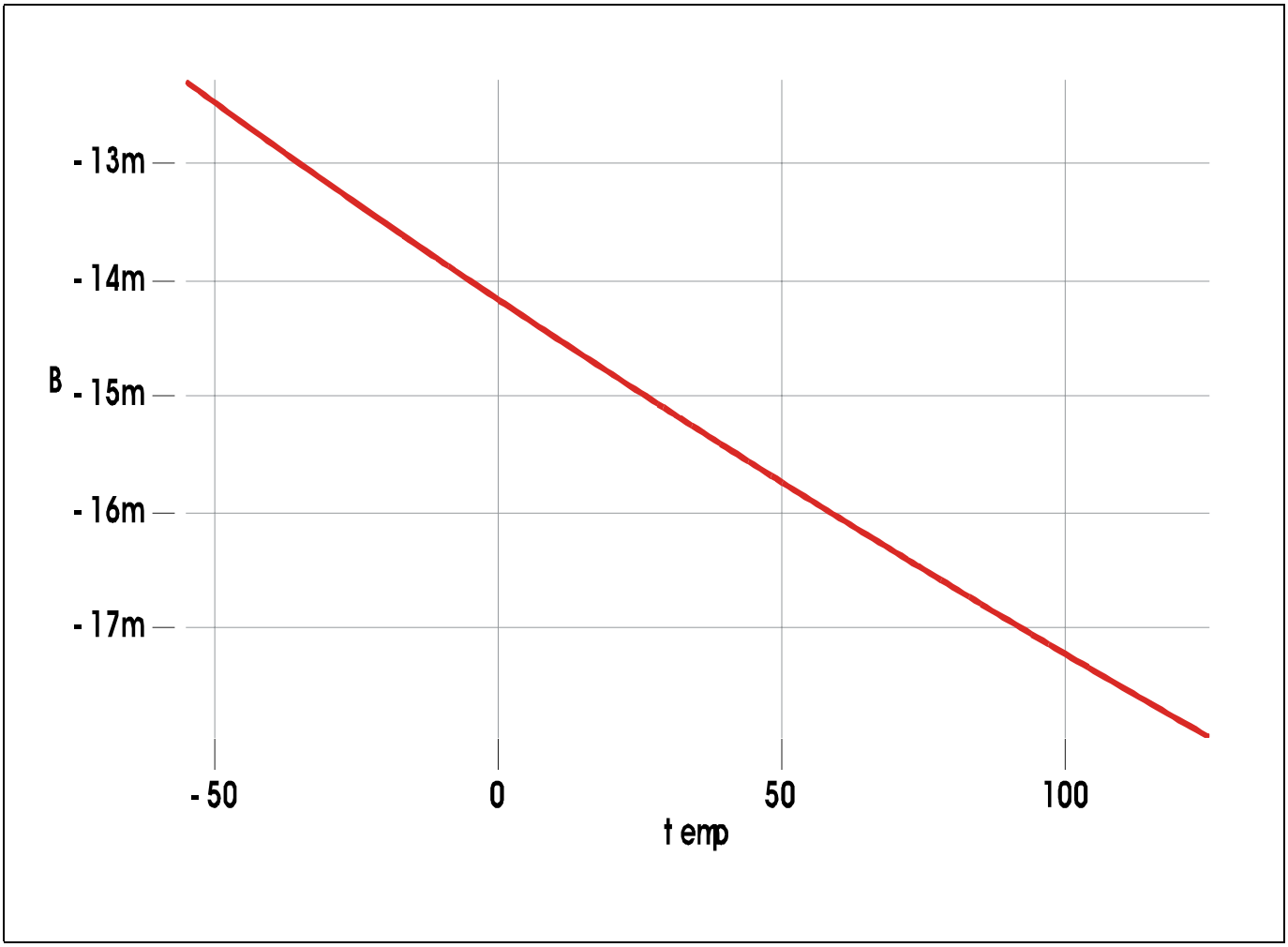


Figure 27: Diff(IRC2/DT) Low Power Cell

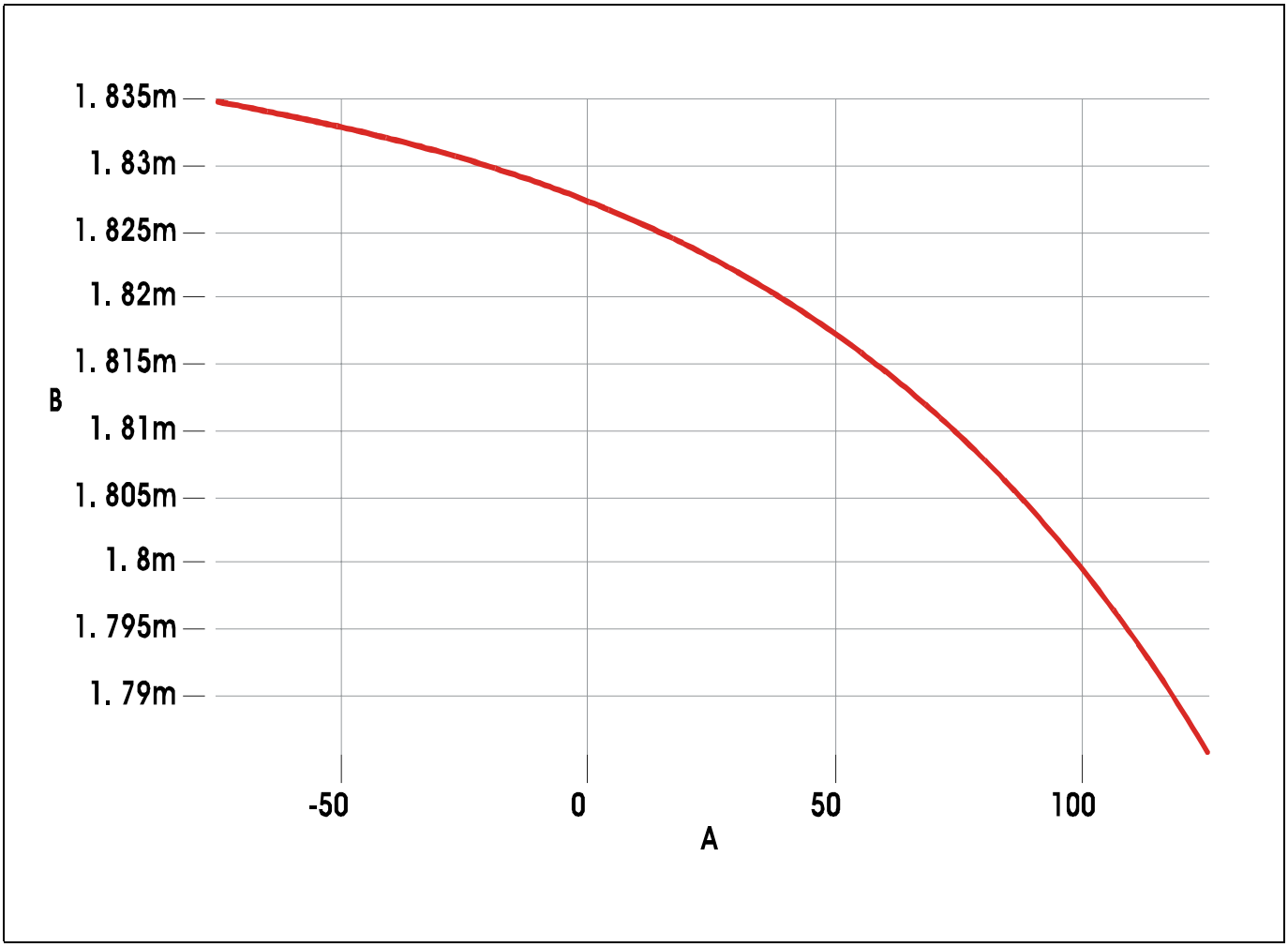


Figure 28: Diff(IRC2/DT) High Power Cell

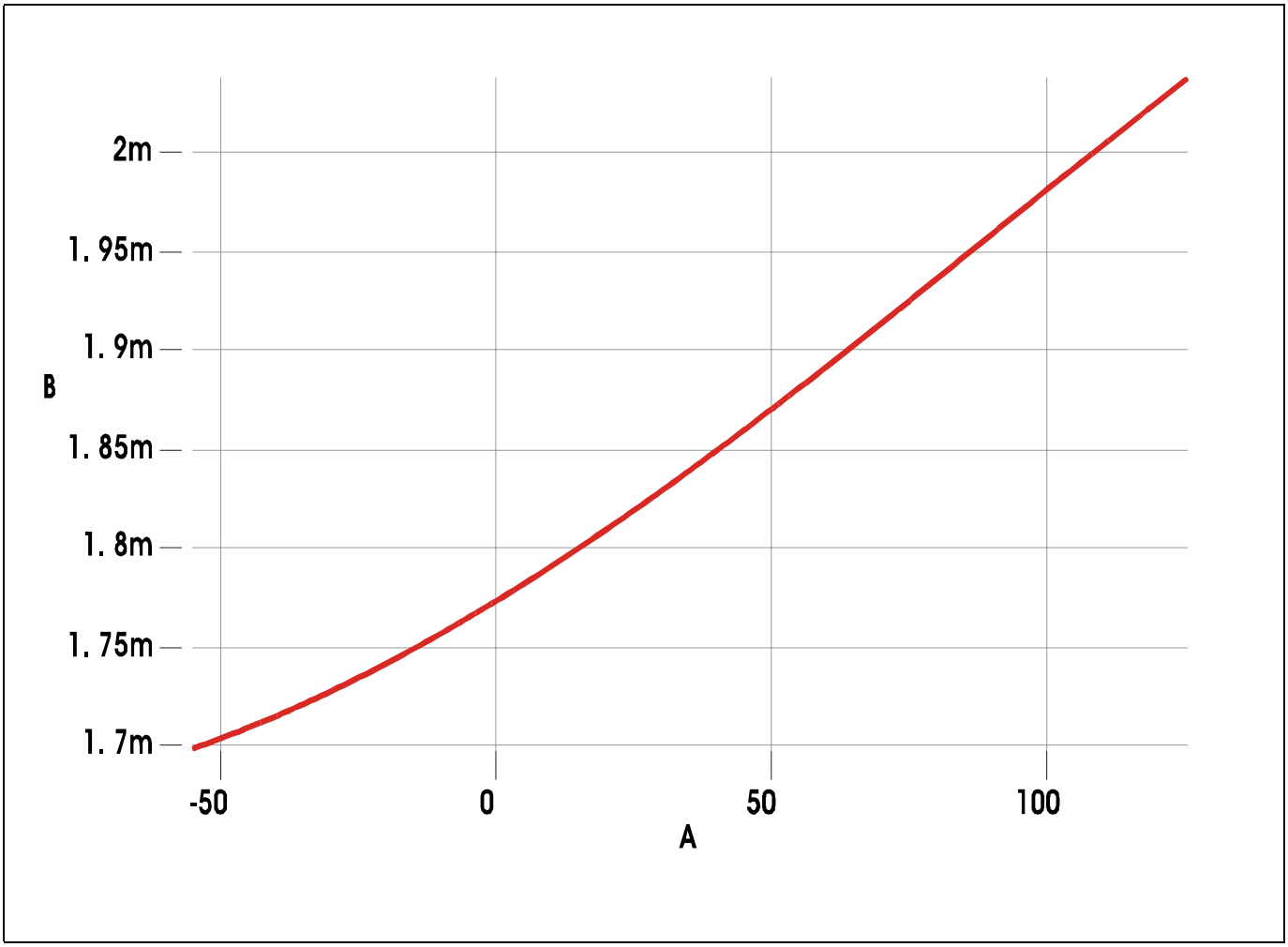
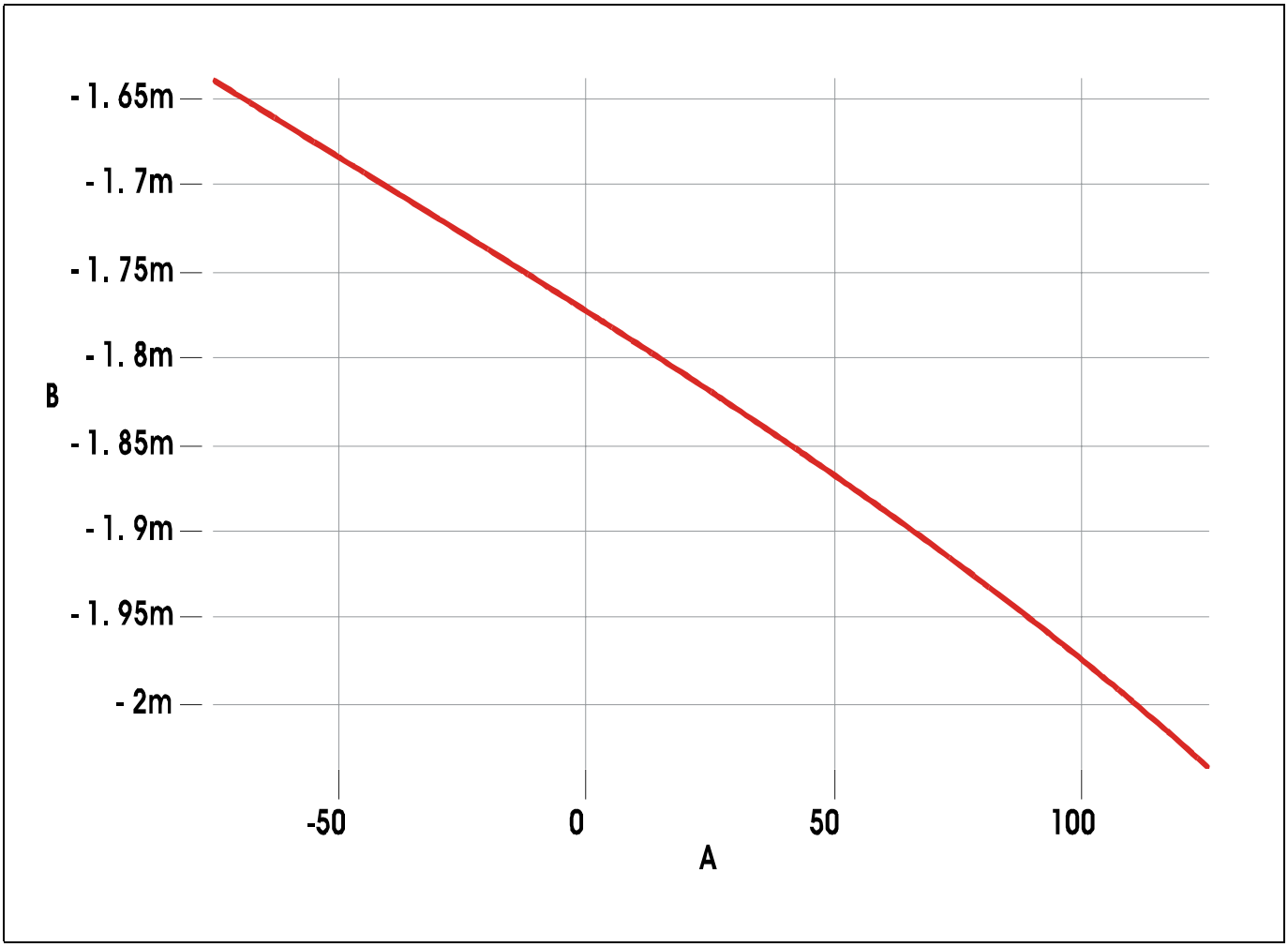


Figure 29: Diff(VBE3) Low Power Cell



4.0 Appendices

B. Resistor Schematics

Figure 30: R20K

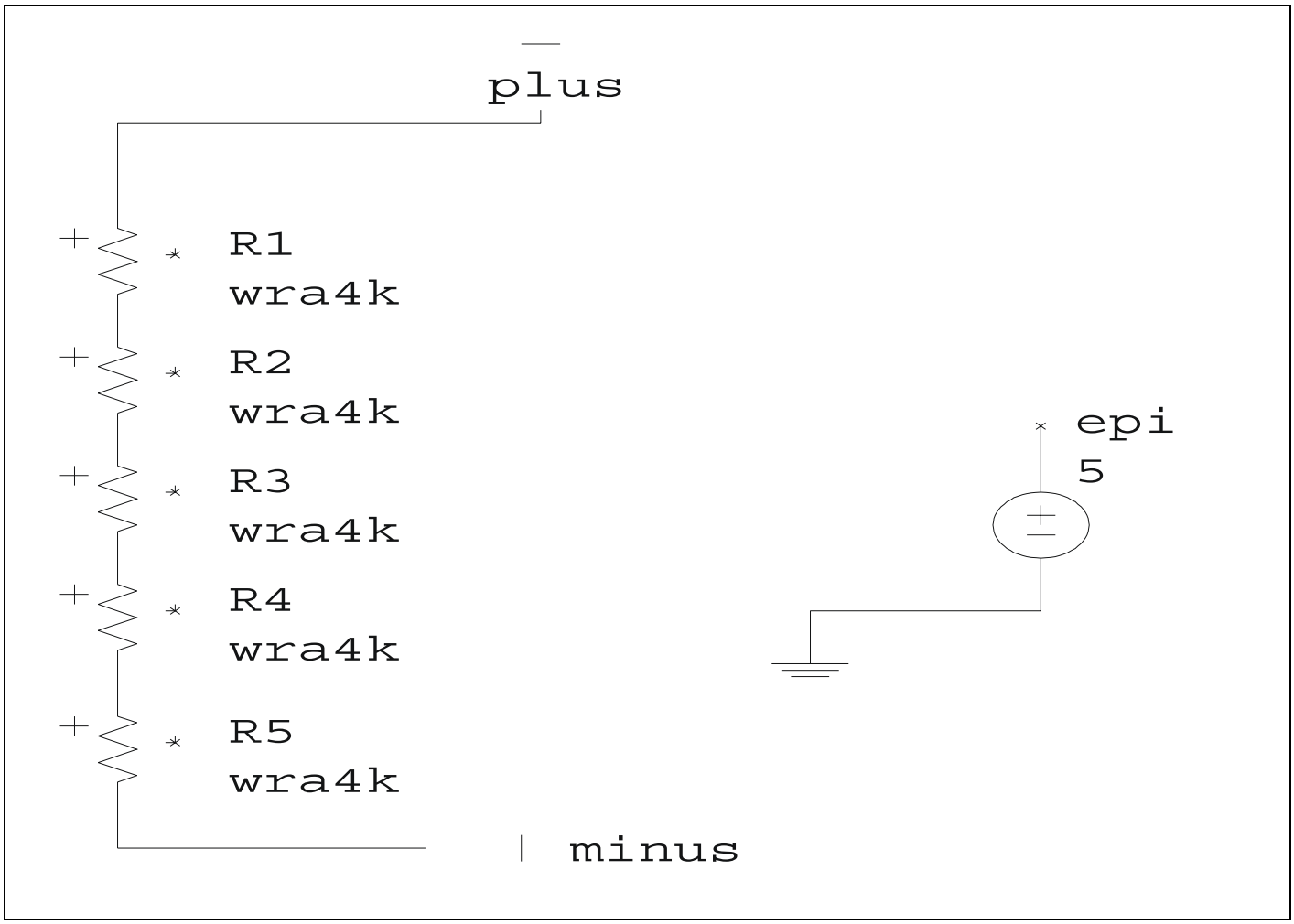


Figure 31: R250(125k)

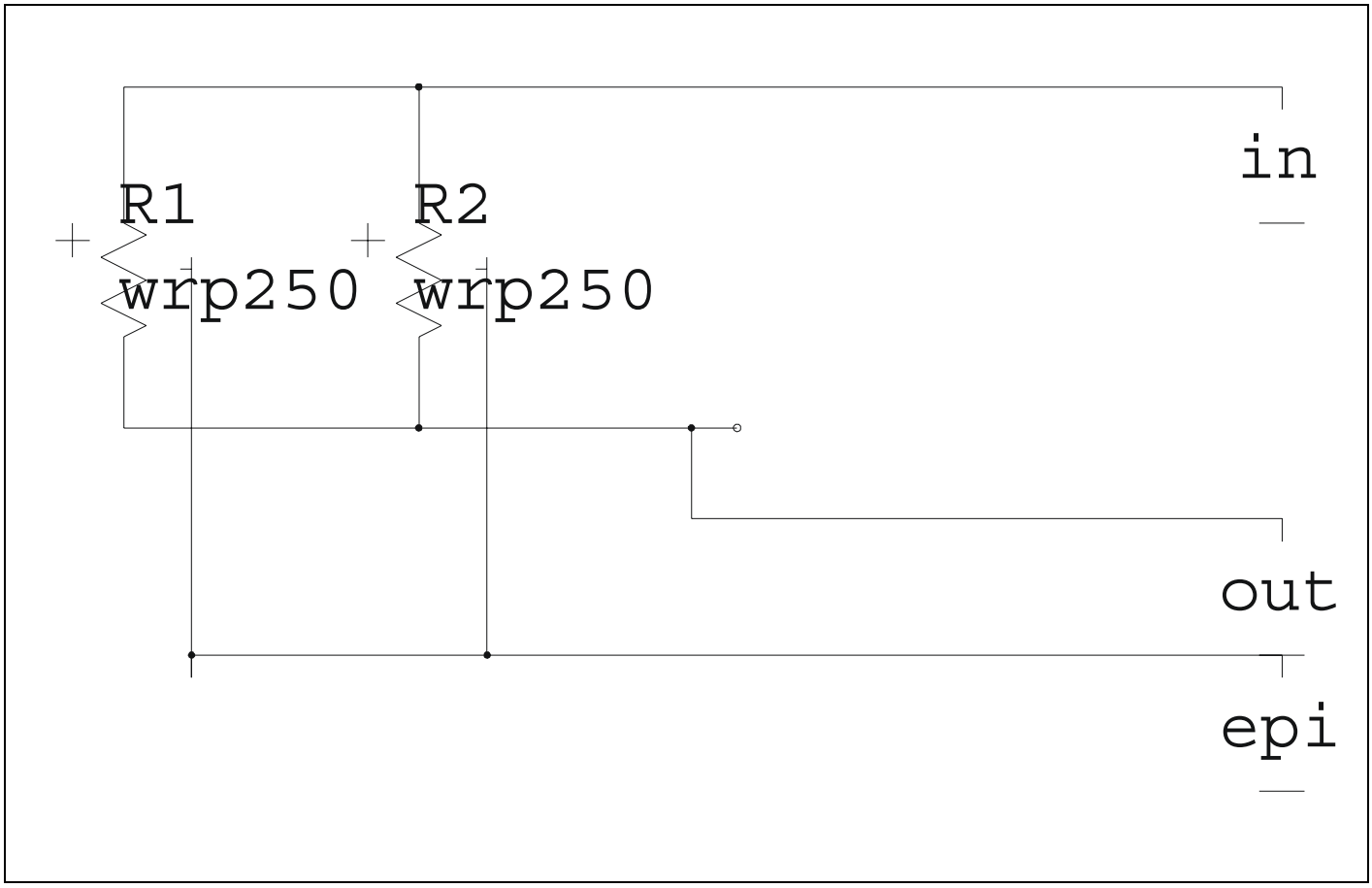


Figure 32: RMEDEG

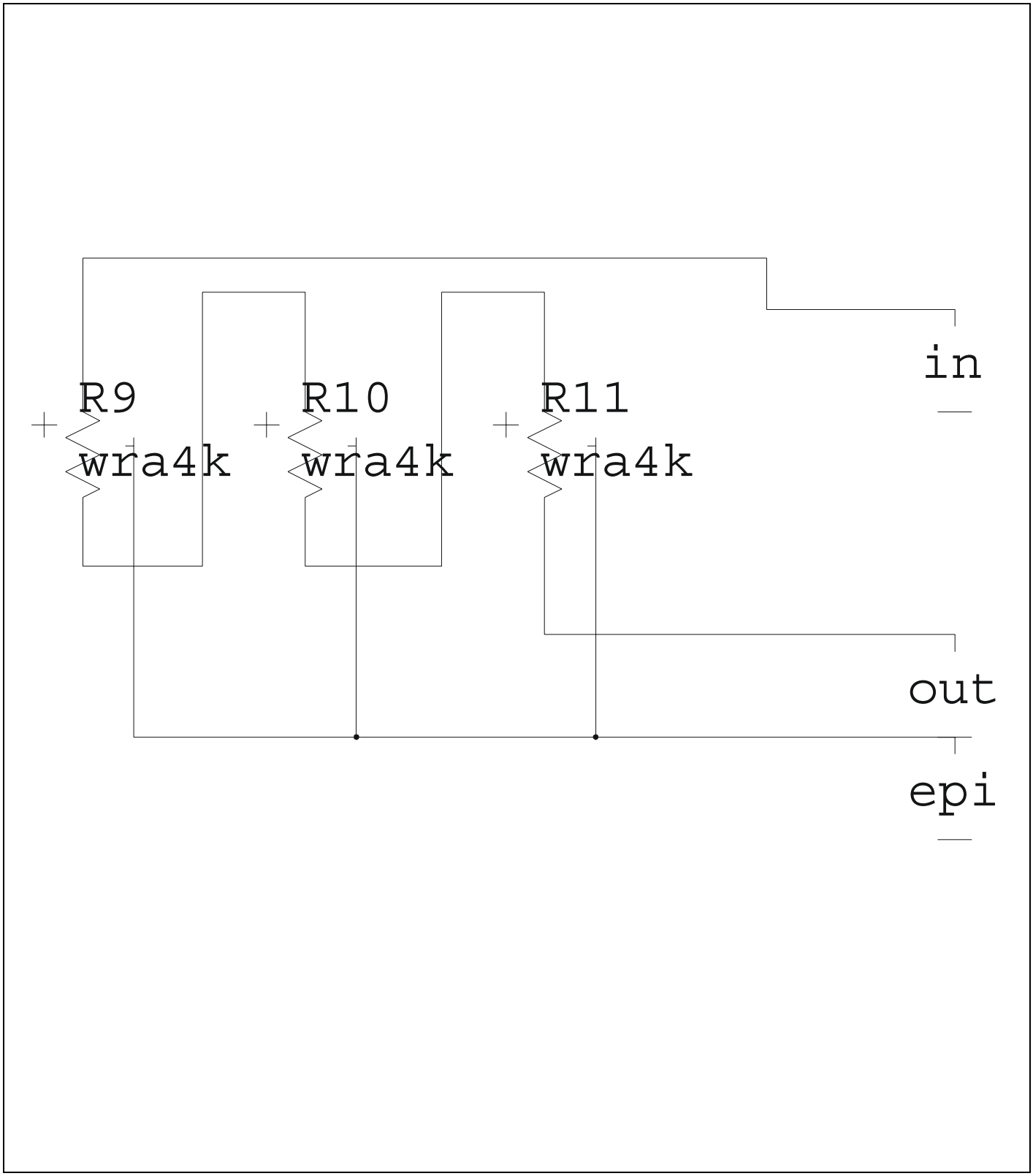


Figure 33: RE2

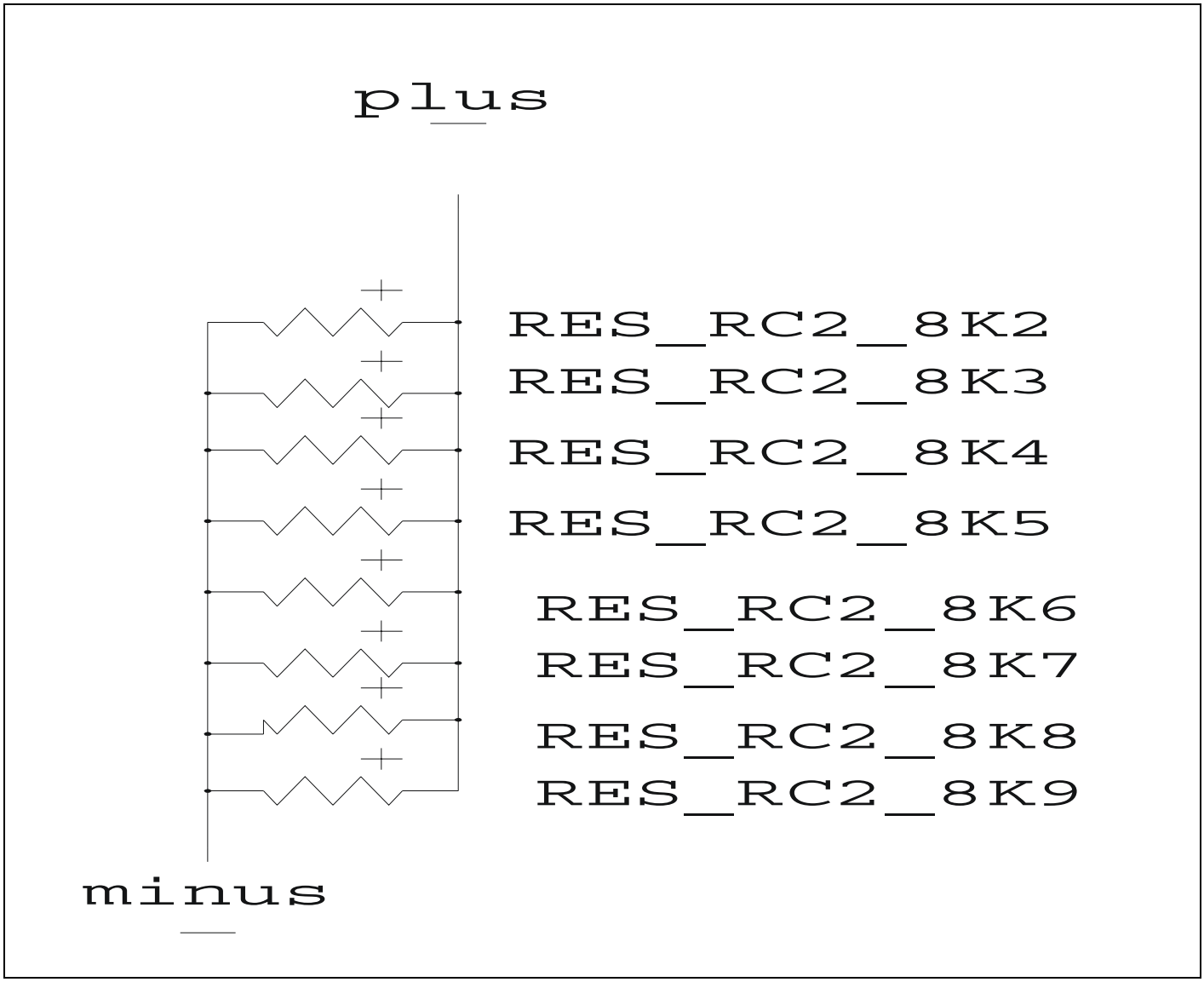


Figure 34: RC2,R8K

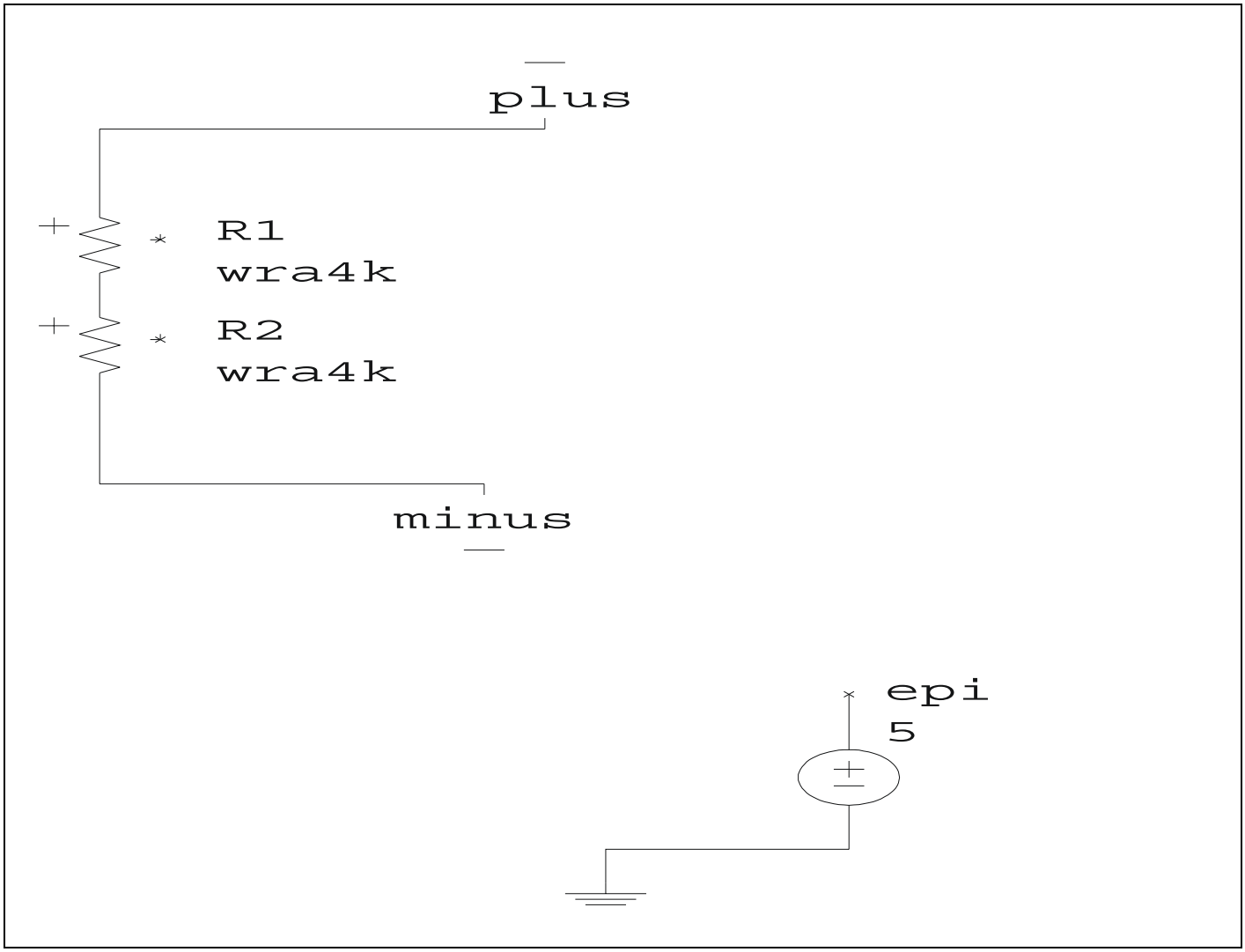


Figure 35: RC1

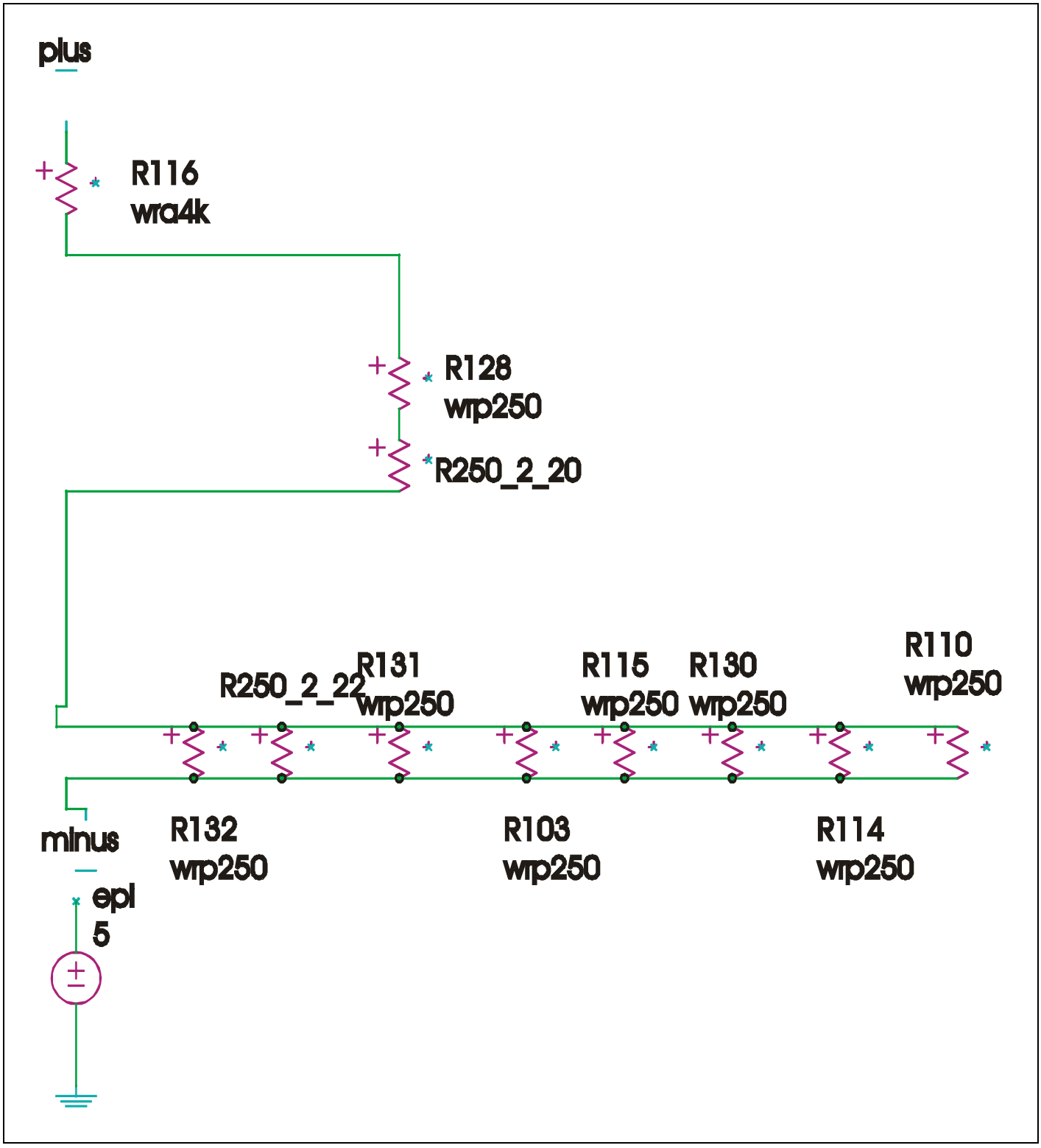
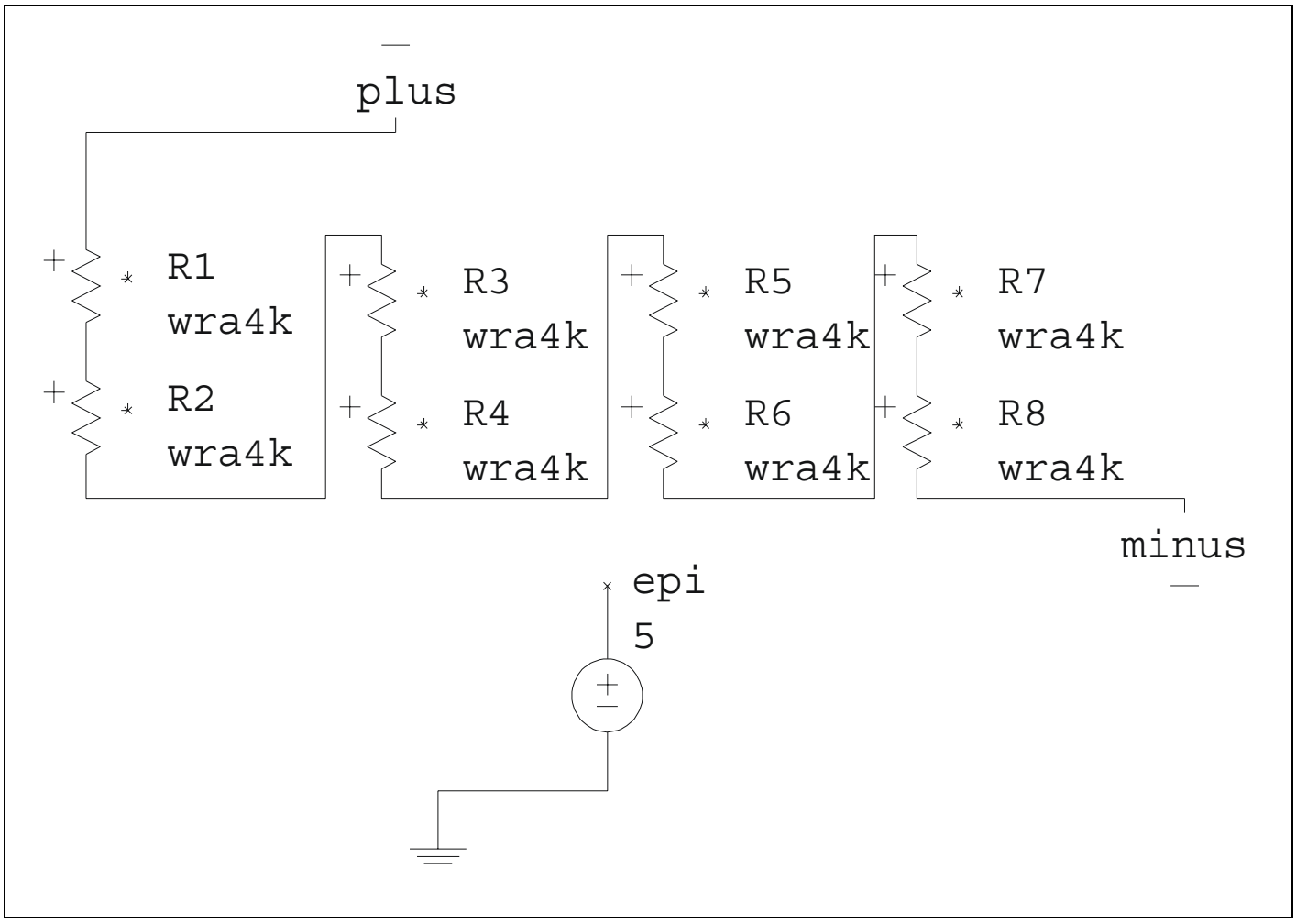


Figure 36: R32K



C. Bibliography

[1],[SedraSmith] J. A. Sedra,K.Smith Microelectronic Circuits, 4th Ed. Oxford University Press, pp. 738-739,1998

[GM] P. Grey, R. Meyer, S. Lewis, P. Hurst. Analysis and Design of Analog Integrated Circuits, 4th Ed.. John Wiley & Sons, 2001.