Digital design
An Example

digital flow in China

中国 数字 的工作流程

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Agenda

April 16
9:00-9:10: agenda
9:10-9:40: introduction
Name, responsibility
9:40-18:00 digital IC design process
development software tools, hardware tools etc.
digital IC design simulation
digital IC layout design
I/O port structure
OTP/flash structure
Vpp voltage
Vdd(3.3V), Vdd(1.8V)
April 17
9:00-18:00: IC specification explanation(status and dynamic)
Power reset and hot reset
Test mode
AD converter sampling sequence,
I/O power on status sequence
UART timing
JTAG timing
OTP programming timing
Capture input timing
I2C timing
SPI timing
Gatekill, Itrip timing
IC testing

April 18
9:00-18:00: IC application
MCE mechanism
8051 operation
detail of time wheel mechanism, Any restrict/requirements to use
Q&A
The spike at Q-counter for 401
What's the function of vfsx? Why is it bonded out to DNC pin of 312 since it is not used?
The delay mechanism of PFC output when hot reset(reset happen when is running motor), any delay happen for motors' PWM output?
Any problem for Vpp connects to P1.5 for K171? Midea found Vpp impendence reduced after program OTP
Ain5 is also floating for 171. will it have same Ainx input saturate issue as 343?
Risk of bonding Ainx to Vac+ and Ifbo
Tiny MCE brainstorm

Glossary

- HDL - hardware design language. a way to describe the design in high level.
- Verilog - popular HDL. rather old. had few face lifts over the years. 1995, 2000 and recently there is a buzz about SystemVerilog.
- VHDL - HDL invented by DOD and should stay there.
- RTL - register transfer level. using RTL, design looks like software. Both Verilog and VHDL have ability to describe the design in RTL levels. sometimes called verilog-D
- GateLevel - verilog language, but here the design is expressed as bunch of cell instances and web of wires (nets) connecting them.
- Synthesizable Verilog : subset of verilog suitable for synthesis. not easily defined. the final judge is always the synthesis tool.

Chores: the long list

version management

backup management

flow management

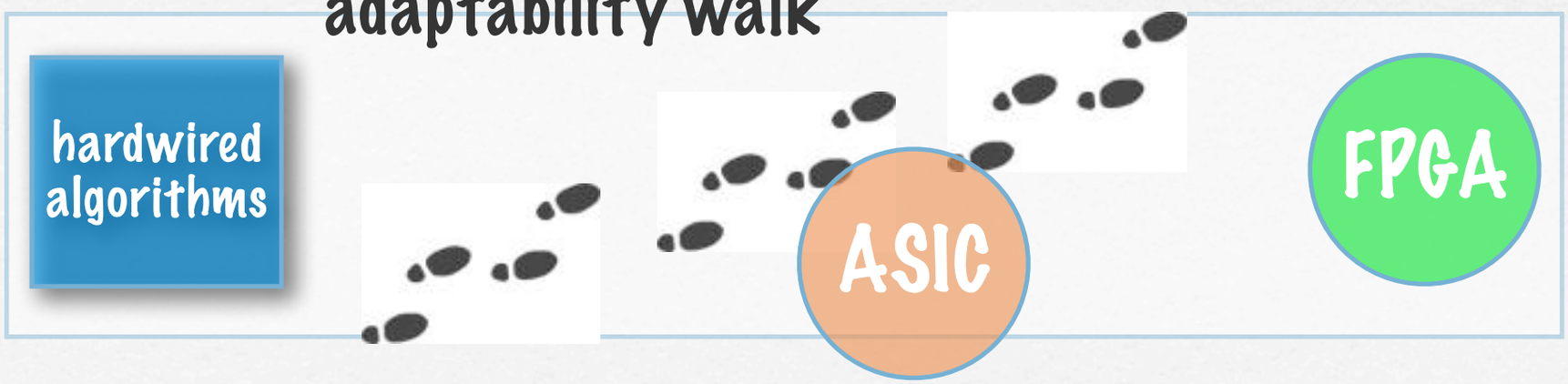
activity	tools	comments
architecture & IP sel	experience	libraries, process ...
timing & system intgr	building the system	clocking, power, IO
build floorplan	script+encounter	
rtl implementation	check integ. Lec	mvlg design mngr.
functional verification	NCverilog + nelsim	testbench, coverage and more
fpga verification	fpga + software	xilinx board
analog intgr & verif	AMS spectre	checking the I/F
dft	experience	bist, scan, visibility
synthesis	synplicity	used also for scan insertion
floorplan	encounter SOC	built by script
place & route	nano encounter	
power : IR drop, noise	encounter SOC	
atpg	encounter Test	scan by synplicity
sta	synplicity	
lec	verplex	
lvs, antenna & drc	assura	
loadboard & tester		working with vendors
bring up board	board design	enables to verify the silicon
application board	board design	debugs the application and can be shown to customers
software tools	C compiler, MCEdesigner	the software that goes with the project, both internal use and customer visible.

Main Steps (there is more)

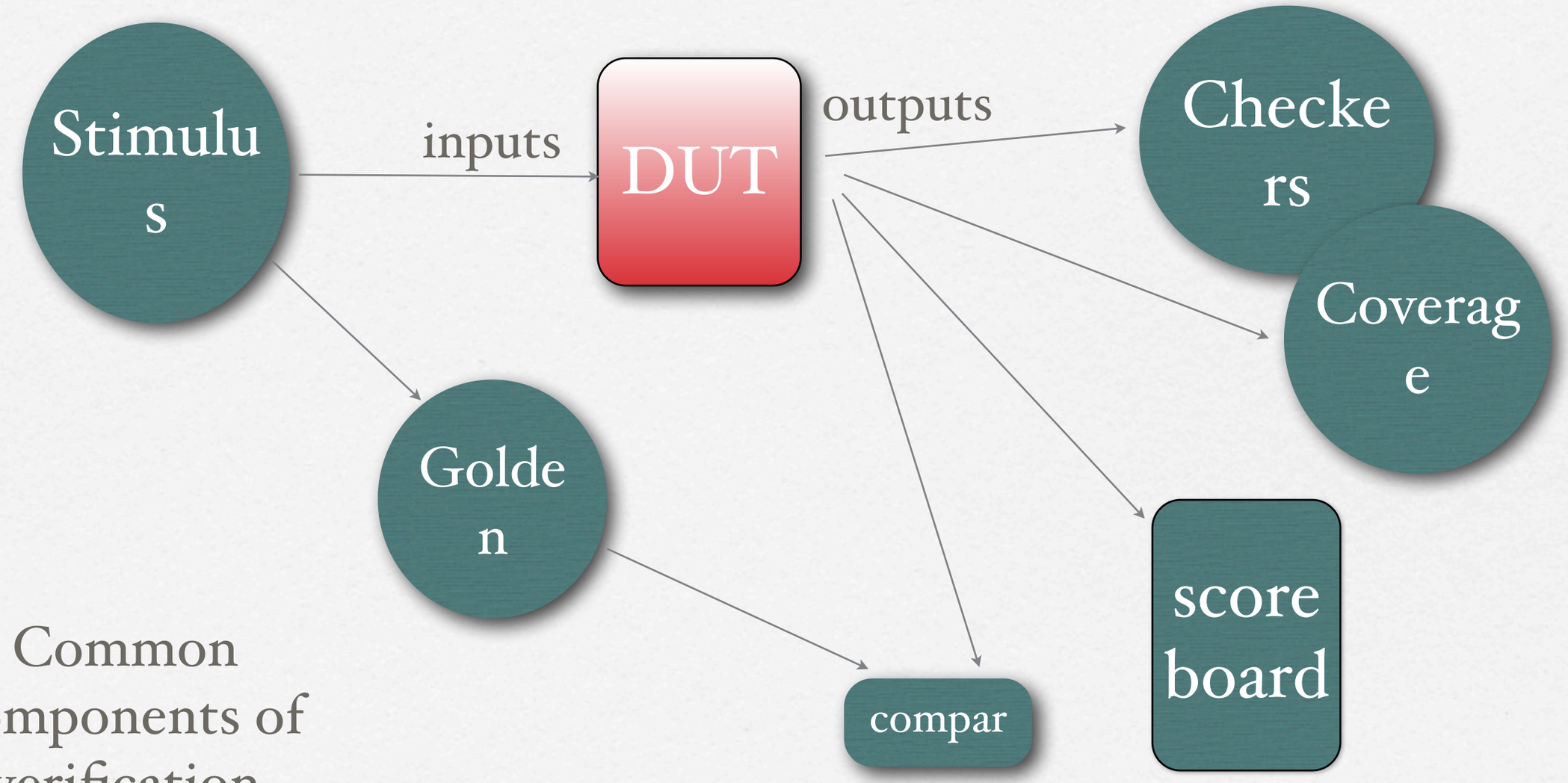
- architectur
- IP sel
- design in rtl
- simulator
- verification
- fpga
- synthesis
- software
- floorplan
- place & route
- final checks
- production testing

Main Architectural challenge

- disconnect the silicon from the application.
- one silicon should serve several applications and customers.
- it should have flexibility in application space.
- keep the number of tapeouts and derivatives to minimum

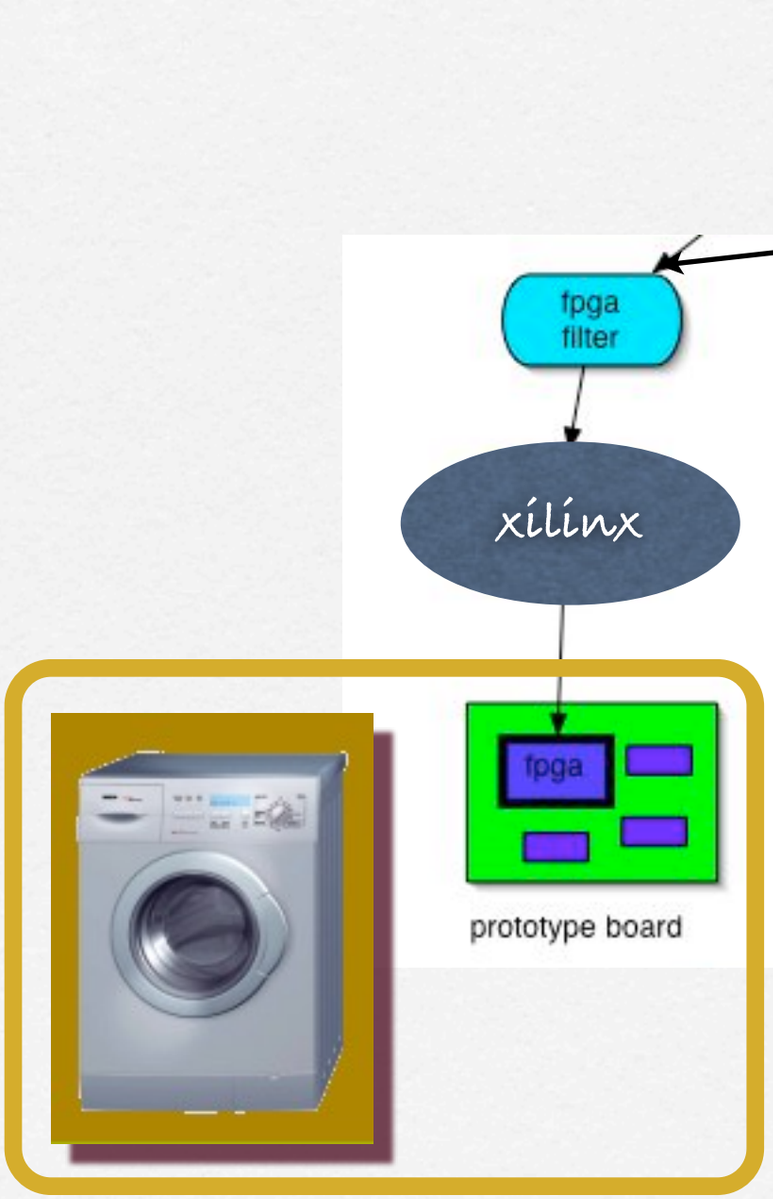


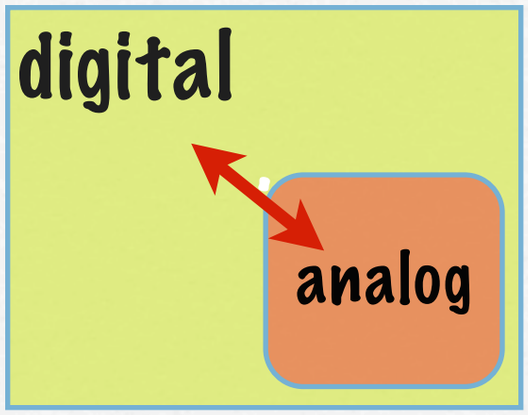
Verification components



Common components of verification environment.

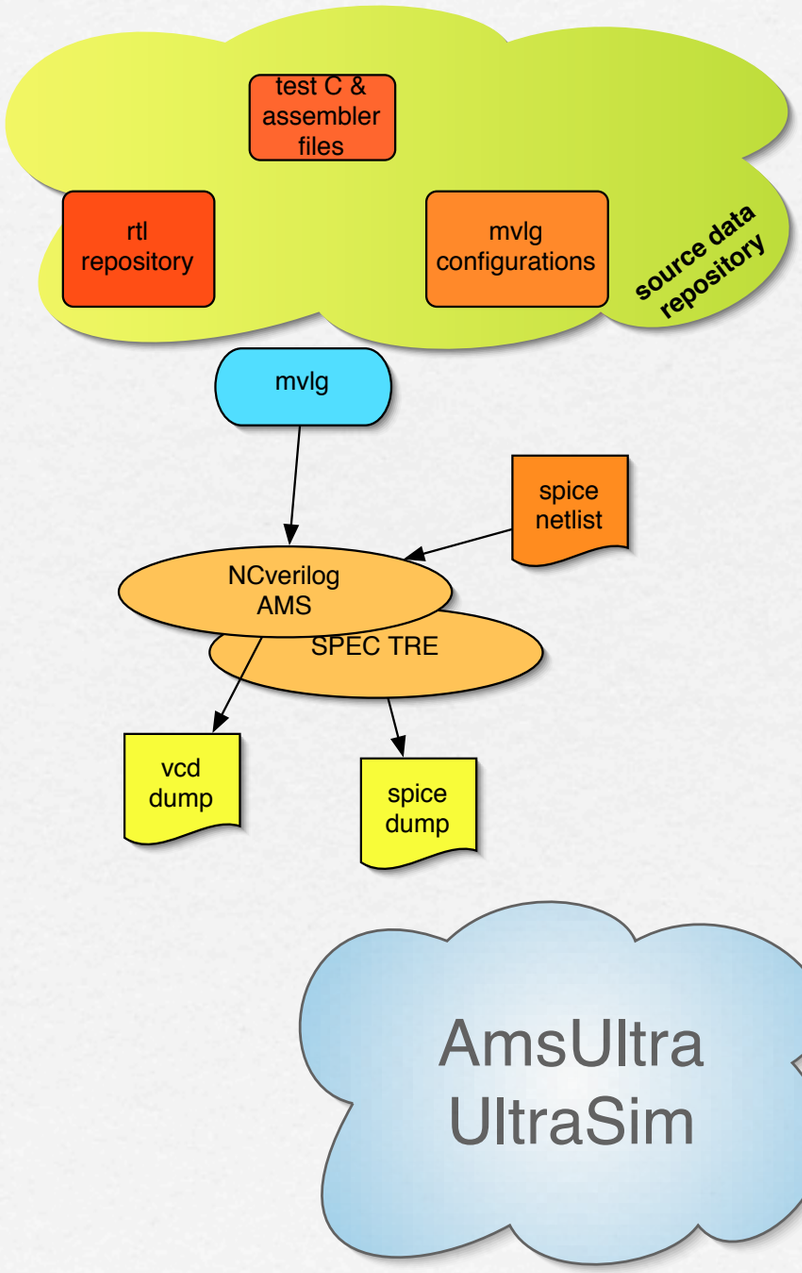
FPGA validation



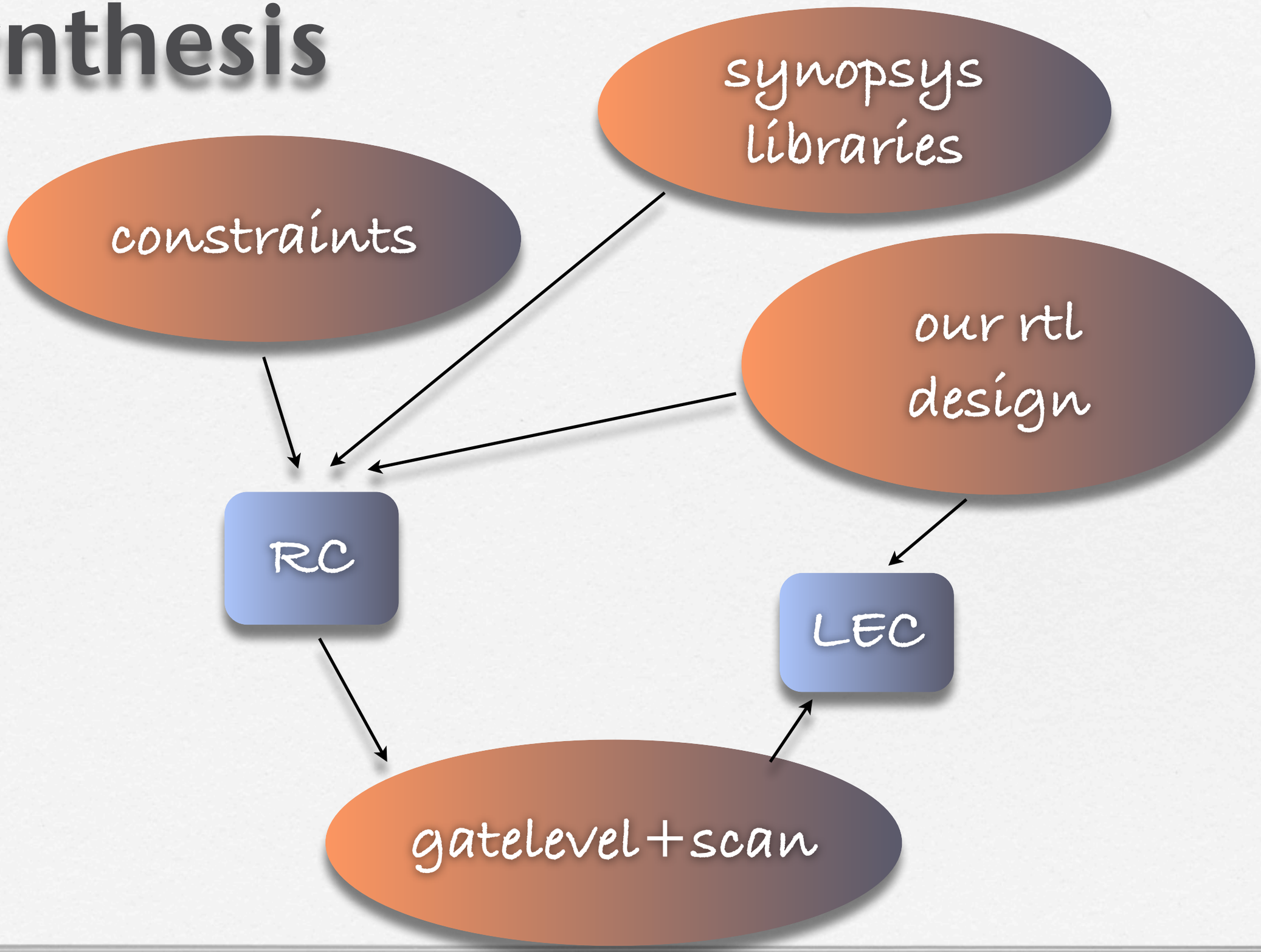


Mixed signal validation

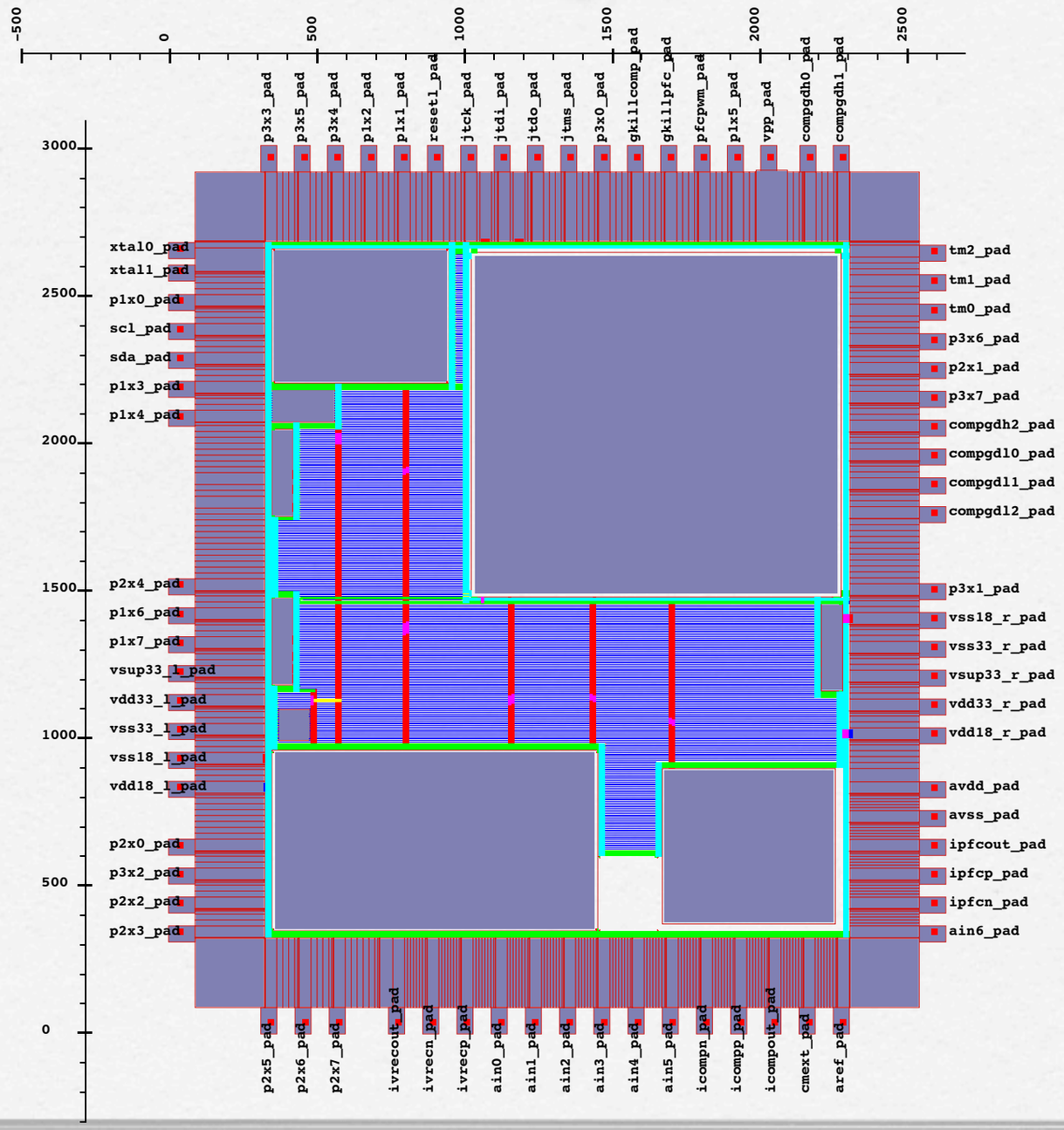
- One approach: write "digital" models for analog IP.
- Can hide mis-understanding of analog modules spec.
- better: Fast spice (UltraSim).
- Not useful for external analog IP.
- FPGA validation doesnt help here.
- Spice-like simulations use "Virtual Tester" approach.



Synthesis


synopsys libraries
constraints
our rtl design
RC
LEC
gatelevel+scan

Floorplan



* hard macros:
  ram, otp ..
* IO cells
* IO pads
* power/ground grid

Place & Route

technology

constraint

netlist

libs

lefs

floorplan

place design

reorder scan

opt design

clock tree

detail route

add fillers

opt design

metal fill

gds

netlist

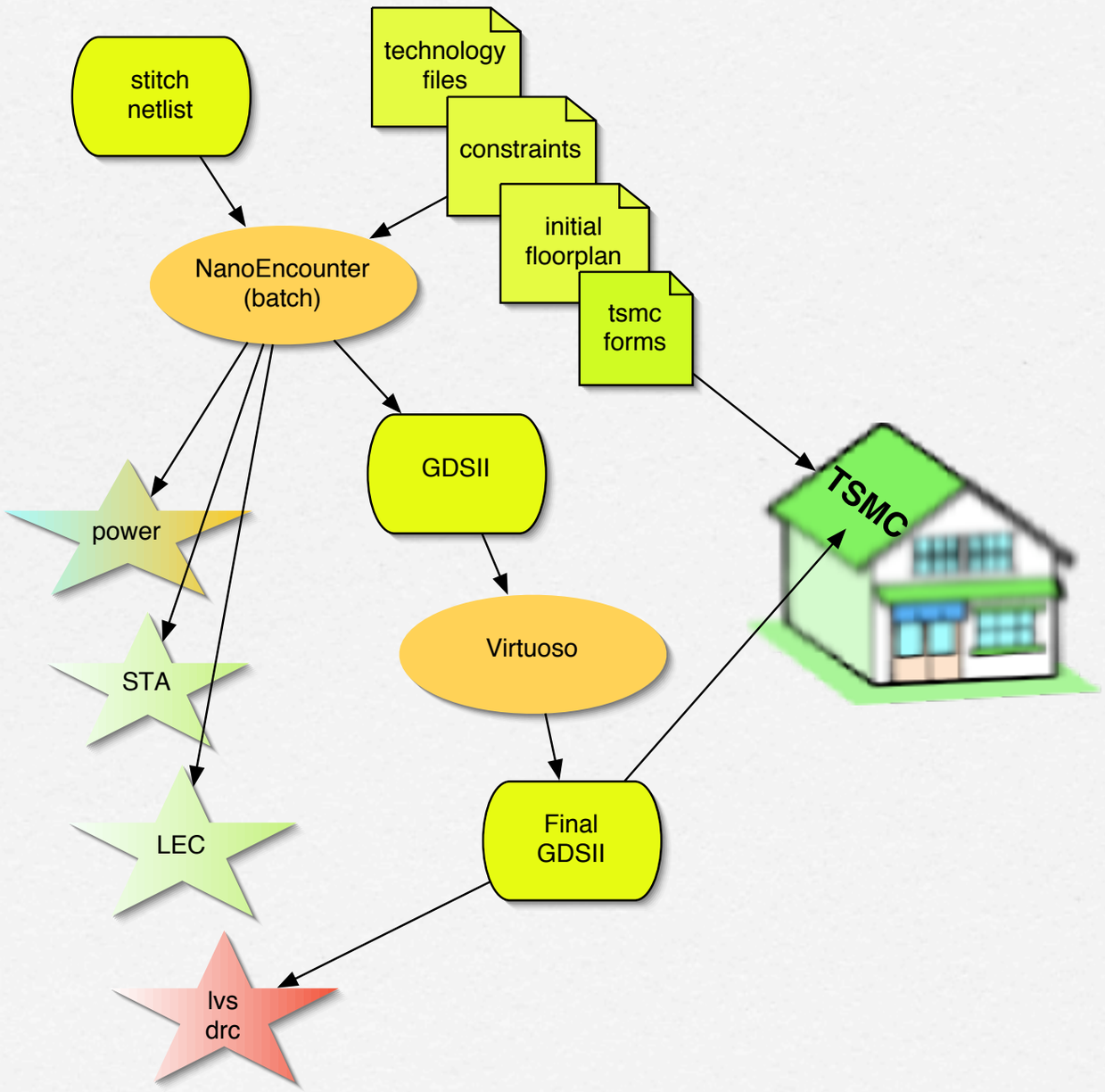
sdf

parasitics

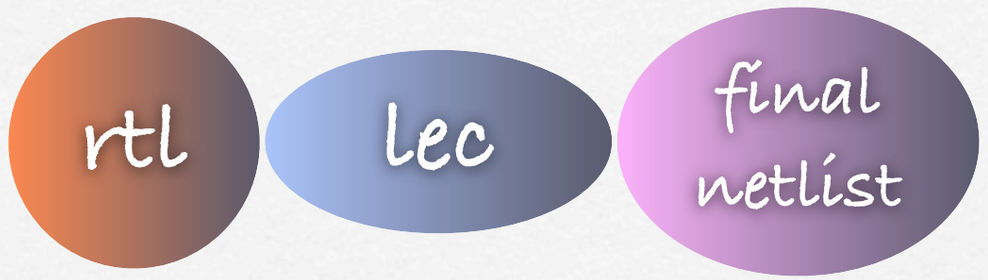
Full gds for tapeout

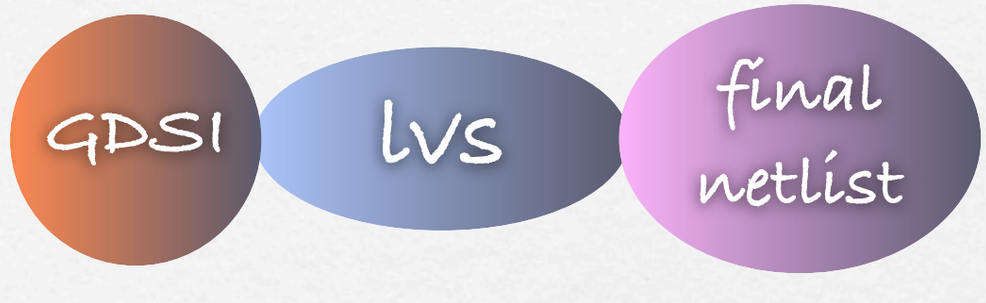
- Encounter (FE) produces flat gds file, without the insides of standard cells and macros. This is because all cells are present to FE just by LEF.
- For tapeout we need full gds, including cells and macros.
- It is done, either through Virtuoso or my script.
- Similar thing happens with final netlist. The netlist includes only instances of standard cells, not the transistors inside. For LVS we need full spice.

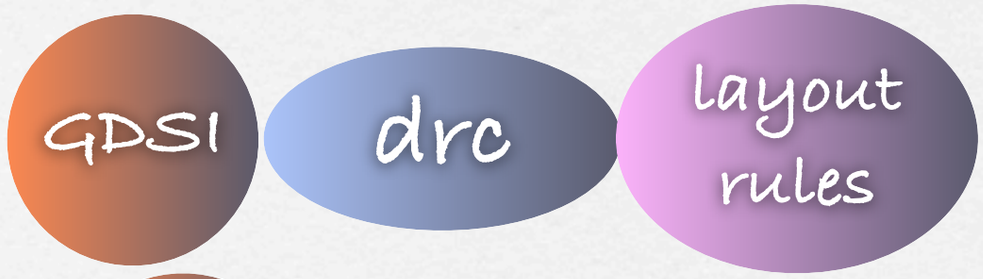
Final checks

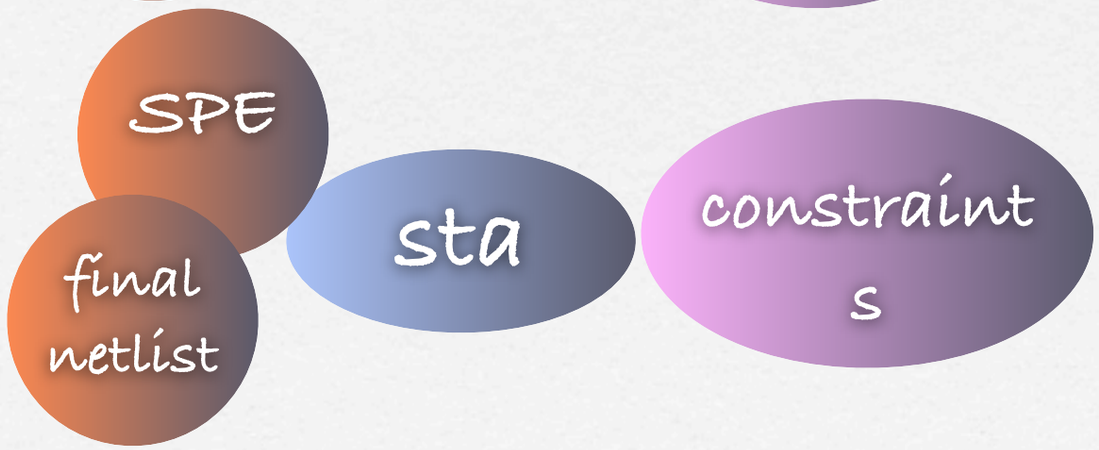


compares:









Scan test

Final netlist

setup files

Test Encounter

% Coverage+

pattern

adapt to tester

Virtual Tester

python

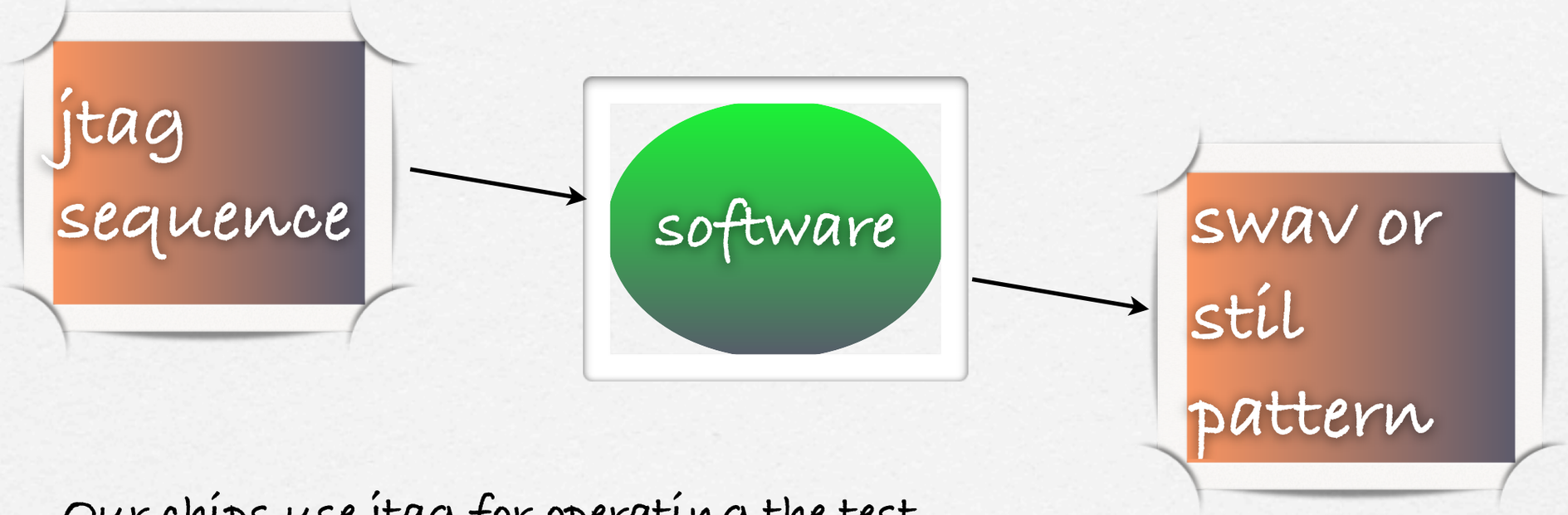
bridge

NCverilo

pattern file

Final netlist

Digital pattern tests



Our chips use jtag for operating the test modes.

<u>Digital (non scan) tests:</u>
bists
clocks/pll
IO in / IO drive
functional at speed

External IP

- TSMC IO lib,

  TSMC (Artisan) standard cells.

  TSMC (Artisan) ram generators.

  OTP or Flash macros.

  Nordic ADC.

- analog subsystem from Pavia

Library is made out of :

actual mask data — gds11

spice netlist for LVS — lvs spice

cell footprint for PGR — lef

function, timing, power for synthesis — liberty

function for simulation — verilog for sim

function model for atpg — verilog for atpg

IO Cells

IO comes from TSMC standard IO library.
most of IO cells are Input/Output (like this one)
there are few PDIDGZ (input only cells)
additional cells:

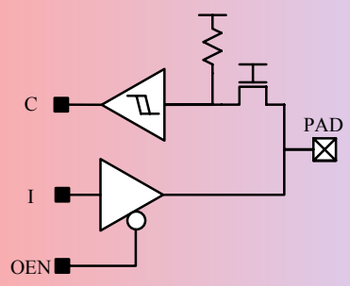
- analog IO
- supply cells
- crystal osc
- bond pad cells (not part of IO cells)

TPZ973GV
TSMC 0.18um
Standard I/O Library

Databook

8.61 PDU16SDGZ

Tri-State Output Pad with Schmitt Trigger Inp



Truth Table

INPUT			OUTPUT	
OEN	I	PAD	PAD	C
0	0	-	0	0
0	1	-	1	1
1	0/1	0	-	0
1	0/1	1	-	1
1	0/1	Z	-	1

Cell Information

	Value	Unit
Pad Number	1	-

Leakage Power

	Value	Unit
VDD	5.5621	nW
VD33	5.0918	nW

Pin Capacitance

	Value	Unit
I	0.0567	pF
OEN	0.0562	pF
PAD	2.2896	pF

TSMC Standard I/O *TPZ973GV* Databook

Design Dimension	Physical Dimension
I/O Height	*185.0*μm
I/O Width	*30.0*μm

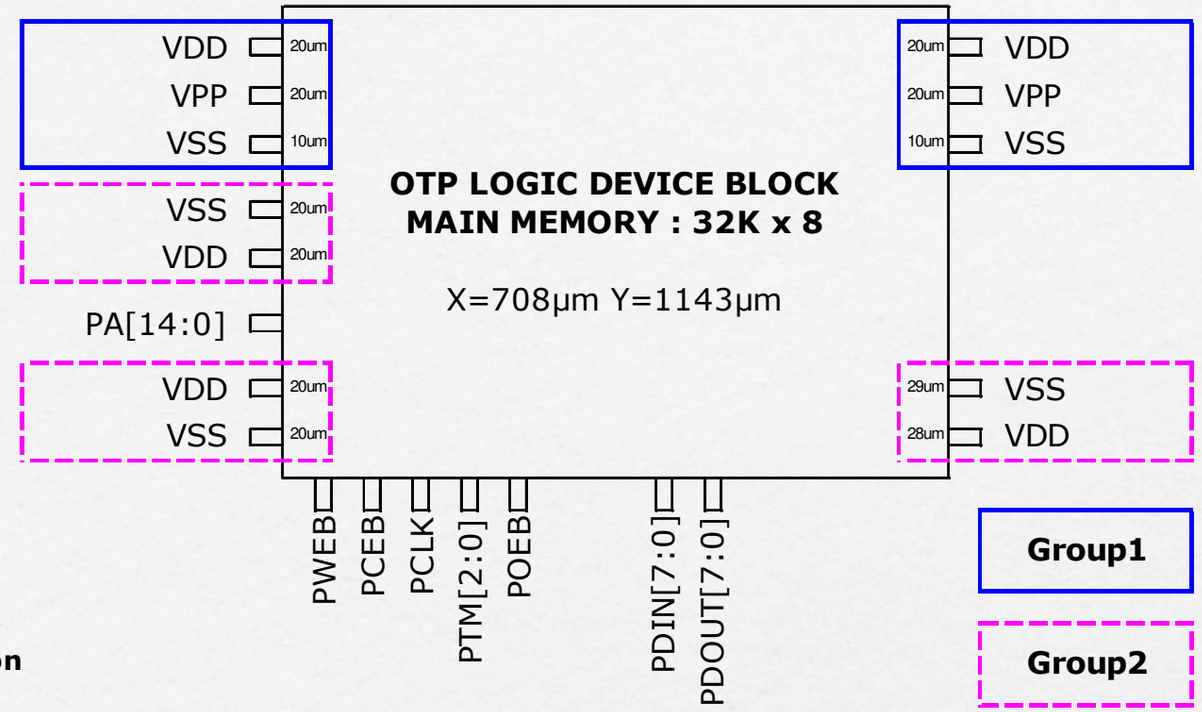
Table 2.1: Recommended Operating Conditions

Parameter		Min.	Nom.	Max.	Units
V_{DD}	Pre-Driver Voltage	*1.62*	*1.8*	*1.98*	V
V_{DDPST}	Post-Driver Voltage	*3.0*	*3.3*	*3.6*	V
T_J	Junction Temperature	*-40*	*25*	*125*	°C
V_{IMAX}	Maximum Input Voltage			*5.5*	V

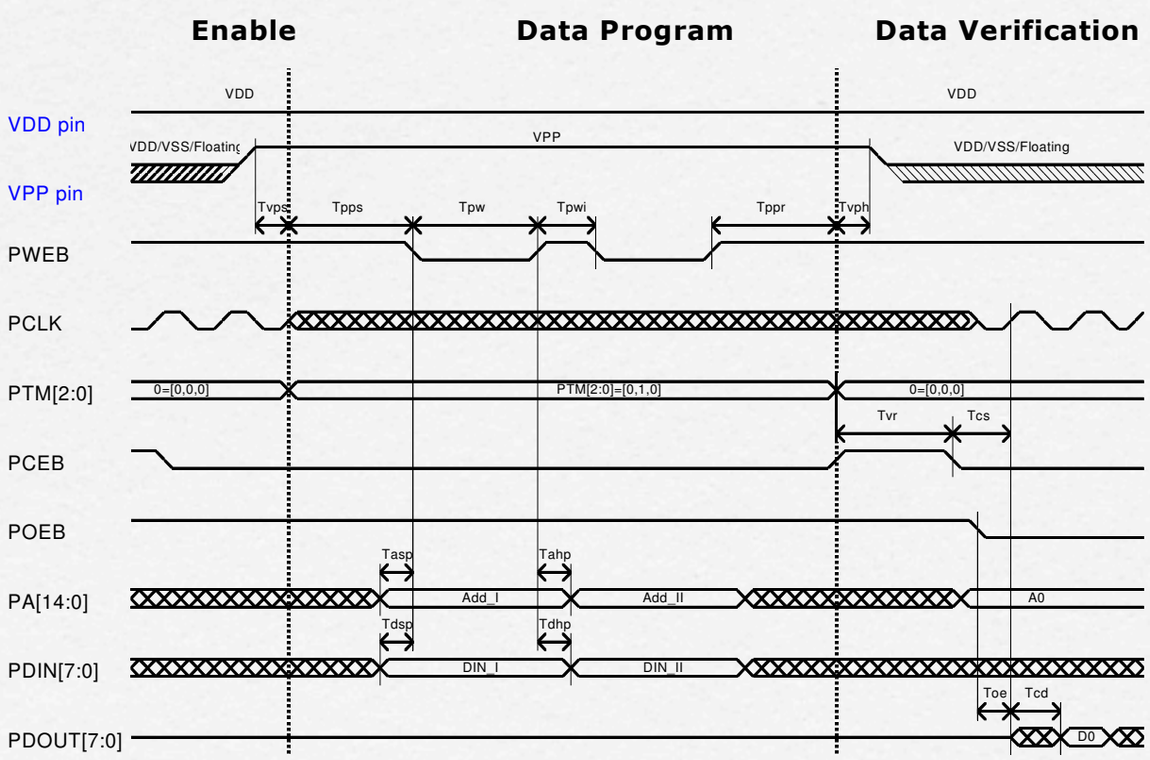
Propagation Delay

	Group1	Group2	Group3
Timing Arc	**(< 50.0000)pf**	**(50.0000-120.0000)pf**	**(> 120.0000)pf**
I_PAD_T_{PHL}	2.7360+0.0311*Cload	2.8520+0.0290*Cload	2.9230+0.0283*Cload
I_PAD_T_{PLH}	2.3890+0.0311*Cload	2.4480+0.0300*Cload	2.4680+0.0298*Cload
Timing Arc	**(< 50.0000)pf**	**(50.0000-120.0000)pf**	**(> 120.0000)pf**
OEN_PAD_T_{PHZ}	5.9190	5.9190	5.9190
OEN_PAD_T_{PLZ}	1.7550	1.7480+0.0001*Cload	1.7560
OEN_PAD_T_{PZH}	2.4290+0.0311*Cload	2.4890+0.0300*Cload	2.5100+0.0298*Cload
OEN_PAD_T_{PZL}	2.4480+0.0314*Cload	2.5750+0.0291*Cload	2.6560+0.0283*Cload
Timing Arc	**(< 0.0300)pf**	**(0.0300-0.3000)pf**	**(> 0.3000)pf**
PAD_C_T_{PHL}	1.5145+0.6500*Cload	1.5200+0.5000*Cload	1.5335+0.4150*Cload
PAD_C_T_{PLH}	1.8680+0.5000*Cload	1.8720+0.4000*Cload	1.8785+0.3550*Cload

OTP



Program Cycle



VDD=1.62V~1.98V, VPP=6.5V~7V, VSS=0V