Assignment - delay bitstream

In this assignment you will create a module which receives input: **din** and **dly**[**11:0**] and gives out **dout** - which mirrors **din** with a delay of **dly** clocks. **dout** should follow **din** after reset, and only once the delay has passed, it should follow the delayed version of **din**.

- Assume that the delay value is stable during the run. It may be 0, in that case **dout** == **din**.
- Assume there is a limited number of changes in **din** during delay - no more than 8.

Notice that the delay can be up to ~4k clocks.
hint: naive implementation is valid, but not very efficient. Think on how to reduce hardware needed.

Example:

dly = 1

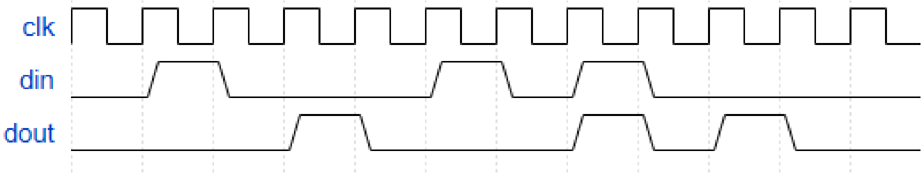
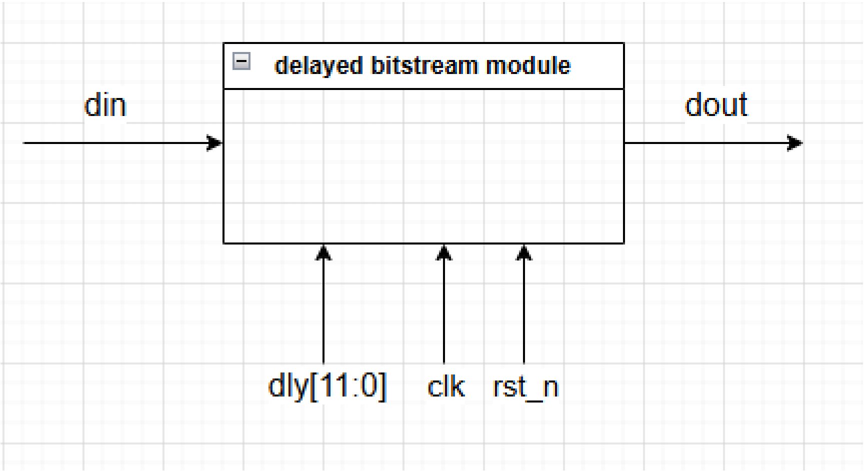


Diagram:



Here is a headstart:

```
module delayed_bitstream(
    input clk
    ,input rst_n
    ,input din
    ,input [11:0] dly
    ,output dout
);
```