# Details of the ARM Architecture

John Doe

Studienstiftung
des deutschen Volkes

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### Abstract

The ARM processor architecture made the staggering success and influence of mobile communication technologies on one's everyday life in the recent years possible. In the vast majority of smartphones, tablets and other embedded devices an ARM-powered chip is built-in. Yet this brand is nearly unknown outside the corresponding tech communities.

This paper illuminates the technical details and properties of this architecture while explaining some basics of processor design and examines later the reasons of the ingenious design for its huge success in mobile device markets. After a look on economical aspects, current developments regarding the ARM architecture will be discussed, as well as an excursus on alternative processor designs.

# Contents

**1 Introduction 3**

**2 Technical Design 3**

2.1 RISC vs. CISC . . . . . 3

2.2 Register Set . . . . . 4

2.3 Instruction Set . . . . . 4

2.3.1 ARM-specific Features . . . . . 4

2.3.2 Thumb Instructions . . . . . 4

2.4 Pipeline . . . . . 5

**3 Practical Issues 5**

3.1 Power Consumption . . . . . 5

3.2 Heat Dissipation . . . . . 6

**4 Markets and Success 6**

**5 Alternatives and Outlook 8**

5.1 64-bit ARM Architecture . . . . . 8

5.2 Mill Architecture . . . . . 8

# 1 Introduction

A computer architecture or processor design specifies the buildings blocks of a processor, like the executions units, the register bank and eventually the instruction set, and how these components work together. ARM is incorporating the Reduced Instruction Set Computing (RISC) principle.

The development began in 1985 at the UK-based company Acorn as "**A**corn **R**ISC **M**achine", later the subsidary was outsourced and renamed to "Advanced RISC Machines Ltd."
Noteworthy is the distribution model of ARM. The company itself does not produce any chips, they are only licensing their technologies to fabricators and providing additional support and tools for their customers. Thus, there is a very broad scope of processors using the ARM instruction set with very diverse properties and abilities. These CPUs are used mainly in all kinds of embedded systems due to their low power consumption, scalability and price sensitivity.

In the recent years, ARM got especially famous during the boom of smartphones and tablets, leading to a share of approx. 90 % at smartphones. As of 2014 there were approx. 50 billion ARM chips produced thus far, but in 2015 alone 15 billion chips , what shows the immense growth and significance of this architecture.

# 2 Technical Design

## 2.1 RISC vs. CISC

The underlying design principle of the ARM architecture is called "Reduced Instruction Set Computing" (RISC) and was first mentioned in the 1980s. The basic idea is to use an instuction set, that includes only the most elementary and simplest instructions and whose executions take only a single cycle. This leads generally to a simpler and less bloated hardware design.

This principle was in contrast to the development of processors at the time, which focused to implement further instructions and features, improving performance and facilitating programming on the processor. This design is retrospectively called "Complex Instruction Set Computing" (CISC).

One implication of RISC is that the reduced hardware complexity due to the simple design has to be compensated by more complex and mighty compilers. The idea is that compilers are much more suitable for optimizing and improving than a hard-wired processor design.
On the other side a CISC processor is able of executing more complex instructions in hardware, that need to be synthesized out of basic operations in a RISC processors. This shall provide a better performance compared to RISC processors.

The four major design rules of RISC are:

1. **Instructions:** Only basic instructions, complicated operations synthesized by elementary instructions, fixed length of instruction codes

2. **Pipelines:** Instructions always decoded in one pipeline stage, no need for microprograms

3. **Registers:** Larger, general-purpose register set. Serves as fast memory store

4. **Load/Store architecture:** Processor operates only on registers. Load and Store instructions access external memory

## 2.2 Register Set

The register set in a classic 32-bit ARM architecture consists of 16 registers in total, that can store a 32-bit word. Most registers are free to use for the programmer, except for three registers that are critical for the processor's work. These are:

- r13 as stack pointer, designates stack memory frame
- r14 as link register, contains the return address for subroutines
- r15 as program counter, contains the address of the next instruction

Additionally there exists the "Current Program Status Register" (CPSR), which cannot be accessed directly. The CPSR contains data about the processor's current status, e.g. the current operating mode or interrupts, and information about possible overflows or other incidents during the execution of an instruction.

## 2.3 Instruction Set

The ARM architecture differs in some points from a strict RISC implementation by providing extra functionality useful for embedded applications. The basis of the instruction set is built by the load/store instructions, arithmetic and logical operations and a variety of branch instructions. But the ARM architecture provides ways for more efficiency without much more technical effort and disregarding the RISC design principle.

### 2.3.1 ARM-specific Features

One feature are conditional branches. Thereby an instruction will only be executed, if the simple condition, set by condition flags in the instruction code, is satisfied. The advantage in comparison with classic, dedicated branch instructions is, that the pipeline has not to be flushed, if the condition fails, and thus leads to more efficient performance.

The inline barrel shifter works in a similar way. This hardware unit preprocesses an incoming value from the register before it is piped to the arithmetic logical unit, where the actual instruction is executed. Thus it can save an extra instruction. The barrel shifter is able to shift the 32-bit pattern by a given number of bit positions or rotate the pattern. This operation is often necessary in certain cryptographic algorithms and can therefore improve performance, especially in certain applications of embedded systems.

Furthermore there are instructions, that alternatively could take more than one cycle computation time. For instance ARM provides load/store instructions that can process multiple registers at once, what occurs often at accesses of data arrays. This enhances the speed of load/stores due to the fact, that sequential memory access is faster than a number of single accesses, and shrinks the memory size of programs.

### 2.3.2 Thumb Instructions

Another feature of the ARM architecture, that is especially addressed to embedded systems, is the Thumb instruction set. This instruction set represents a subset of the original instruction set with the most commonly used instructions, but the codes need only a length of 16-bits instead of 32-bits. The usage of Thumb instructions can shrink the code up to 30 % and is thus especially suitable for

systems with a limited amount of memory, as price sensitive embedded devices.
On the other hand the performance is lacking, because certain features like conditional branches are only available with the 32-bit set.

## 2.4 Pipeline

The processor pipeline can be imagined as a conveyor belt in a factory, in which a product will be transported from one step to another. The same happens with the processing of an instruction in a CPU. By dividing the processing pipeline into substages the throughput of instructions will be increased while using relatively low clock rates. The pipeline in the first ARM designs up to ARM7 was very simply made of 3 stages: Fetch - Decode - Execute.
In the fetch stage, the next instruction is loaded from the memory according to the address stored in the program counter. After that the instruction bit pattern will be examined in the decode stage. Eventually the instruction will be executed in the respective functional units.
In further versions of the architecure more and more stages - like a seperate write stage, in which memory accesses are performed - were incorporated, what expanded the capabilities of the cores. The newest ARM Cortex cores, that are used in recent high-end smartphones, use pipelines with up to 14 stages and even implement more elaborate techniques as superscalarity und out-of-order execution, that were in the past characteristic features solely to CISC processors. Superscalarity means dividing the pipeline and allow parallel execution of independent instructions, like integer and float operations. Thereby the throughput of instructions is increased substantially. Out-of-order execution tackles idle times in the pipeline by letting instructions execute before instructions, that shall actually be processed afore, but have to wait for certain events. This requires a sophisticated logic, that can predict the dependencies between consecutive instructions.

These examples show, that the classical distinction between RISC and CISC processors blurs the more it has been developing. Modern ARM processors are able of elaborate computing techniques and high-end CISC CPUs support reduced instruction sets. Nevertheless the differences are immanent, as considered in the next chapters.

# 3 Practical Issues

There are some reasons, which make the ARM architecture particularly suitable for the use in mobile devices und thus made the success in the smartphone market possible. As already mentioned, the RISC design principle and its focus on simplicity and efficiency takes a big part in this suitability.

## 3.1 Power Consumption

The power consumption of an processor is - besides the clock frequency - mainly determined by the amount of transistors, because a transistor can be depicted as some kind of electric capacitor and the charging of a capacitor, respectively the switching of a transistor, requires energy.
Thus the RISC property of the ARM architecture has an heavy influence on the power consumption:

**Less complex processor design ⇒ less transistors ⇒ less power consumption!**

Nevertheless, ARM processors are still performant and capable of computing complex tasks, but the lean architecture is more efficient than classic CISC processors. This is somewhat illustrated in the following table. Of course, the comparison between a high performance Intel CISC CPU and an ARM processor is not fair regarding the performance and capability, but it shows the difference in magnitude of the complexity and the resulting power consumption quite impressively.

| | |
|---|---|
| ARM Cortex-A9 | Intel Core i7-760 |
| 26 Million Transistors | 731 Million Transistors |
| 0.5 - 1.9 W | 130 W (TDP) |

However, there are plenty of other RISC architectures, that are efficient either, so this does not explain, why specifically the ARM architecture is preferred by companies producing mobile devices. Another key advantage lies in the distribution model of ARM.

The company developing the architecture, ARM Limited, only licenses the processor design as intellectual property (IP) to semicondutor fabricators, who are producing the actual chips. This means that the chip companies are able to adapt the IP cores for specific purposes and melt the ARM core with additional peripherical hardware, like sensors, radios, graphics and audio units. This concept is called "System-on-a-Chip" (SoC). By using only required and purpose-tailored components, the power consumption can be further reduced.

### 3.2 Heat Dissipation

Generally heat dissipation is not that much a problem in mobile or embedded devices since their power consumption is relatively low as explained before. Nevertheless there is a risk of hot spots, that might occur particularly during longer computation times. This affects especially embedded devices as they are usually designed to run nonstop. Another problem is to spread the heat in such compact cases.

In order to solve this problem in smartphones, Fujitsu introduced in 2015 ultra thin ($\approx 0.2$ mm) heat pipes, filled with a cooling liquid. As shown in Figure 1, the evaporator is placed onto the hot spot, usually the main SoC. The heat evaporates the liquid, so that it begins to flow to cooler areas, where it condenses again. Thus a circuit is established spreading the heat throughout the entire case of the device. This suffices to avoid overheating and collapsing the CPU at more demanding applications.

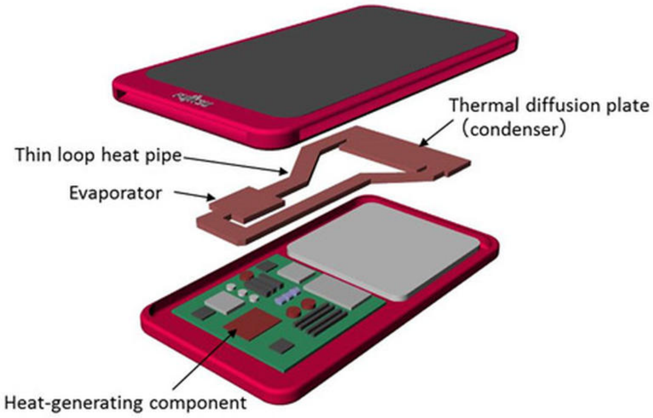
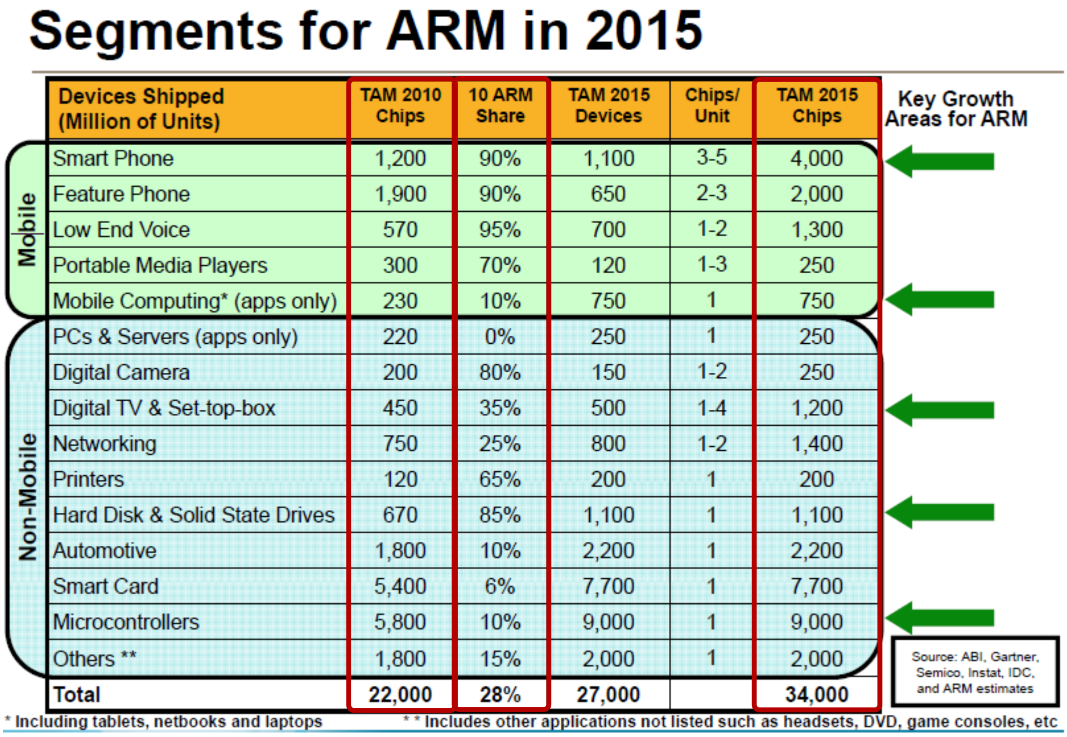


Figure 1: Liquid heat spreader in smartphones [1]

## 4 Markets and Success

The distribution model of the ARM architecture has an immediate influence on its broad success, as already explained. ARM is providing a common platform for hardware, that can occur in a broad variety of forms, shown in Figure 2. Astonishing is dominant market share in certain fields, like all kinds of mobile phones, but also digital cameras and mass storage drives. Of course, the smartphone and tablet market is recently the most profitable market (Figure 3), since the traditional PC market, mainly using CISC CPUs, is stagnating and the trend is moving towards the mobile devices, that are powered by ARM processors with an share of about 90%.



## Segments for ARM in 2015

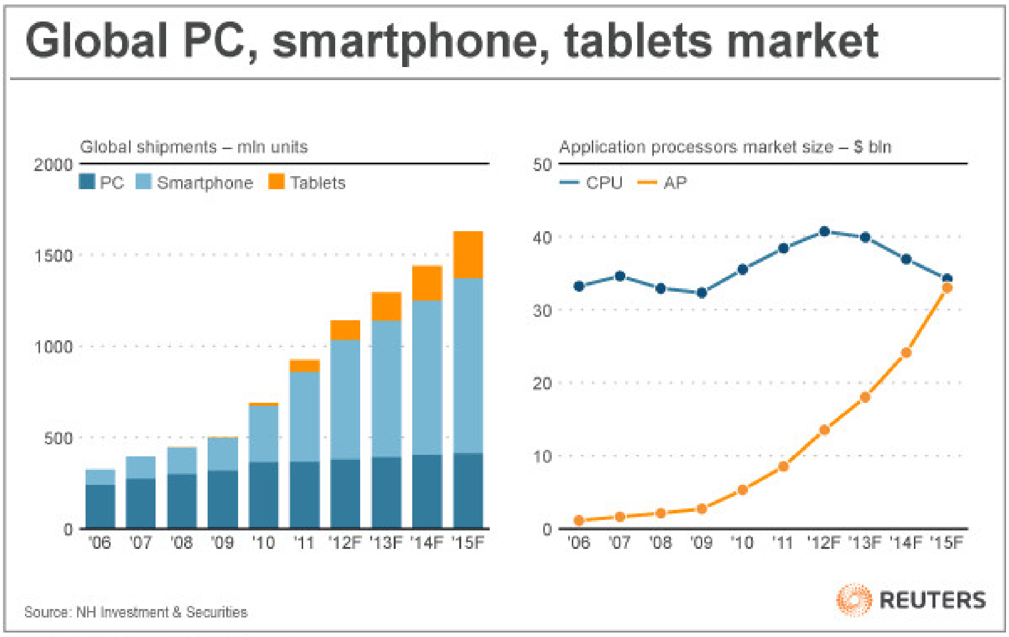
| | Devices Shipped (Million of Units) | TAM 2010 Chips | 10 ARM Share | TAM 2015 Devices | Chips/ Unit | TAM 2015 Chips | Key Growth Areas for ARM |
|---|---|---|---|---|---|---|---|
| Mobile | Smart Phone | 1,200 | 90% | 1,100 | 3-5 | 4,000 | ← |
| | Feature Phone | 1,900 | 90% | 650 | 2-3 | 2,000 | |
| | Low End Voice | 570 | 95% | 700 | 1-2 | 1,300 | |
| | Portable Media Players | 300 | 70% | 120 | 1-3 | 250 | |
| | Mobile Computing* (apps only) | 230 | 10% | 750 | 1 | 750 | ← |
| Non-Mobile | PCs & Servers (apps only) | 220 | 0% | 250 | 1 | 250 | |
| | Digital Camera | 200 | 80% | 150 | 1-2 | 250 | |
| | Digital TV & Set-top-box | 450 | 35% | 500 | 1-4 | 1,200 | ← |
| | Networking | 750 | 25% | 800 | 1-2 | 1,400 | |
| | Printers | 120 | 65% | 200 | 1 | 200 | |
| | Hard Disk & Solid State Drives | 670 | 85% | 1,100 | 1 | 1,100 | ← |
| | Automotive | 1,800 | 10% | 2,200 | 1 | 2,200 | |
| | Smart Card | 5,400 | 6% | 7,700 | 1 | 7,700 | |
| | Microcontrollers | 5,800 | 10% | 9,000 | 1 | 9,000 | ← |
| | Others ** | 1,800 | 15% | 2,000 | 1 | 2,000 | Source: ABI, Gartner, Semico, Instat, IDC, and ARM estimates |
| | **Total** | **22,000** | **28%** | **27,000** | | **34,000** | |

* Including tablets, netbooks and laptops

* * Includes other applications not listed such as headsets, DVD, game consoles, etc

Figure 2: Markets and Shares of ARM processors [2]

Looking at the total amount of chips produced, it is remarkable, that by far the most number of ARM chips are implemented in smart cards and microcontrollers. This is also the area with the highest estimated growth in the future, what is strongly connected to the development of the Internet of Things (IoT). Thus the ARM architecture has, providing highly efficient, simple chips, an immediate influence in this development.



Source: NH Investment & Securities

Reuters graphic/Christine Chan 20/06/12

Figure 3: Competition in the PC, smartphone and tablet market [3]

# 5 Alternatives and Outlook

## 5.1 64-bit ARM Architecture

The most recent milestone in the development of the ARM architecture was the release of a 64-bit version. All the time 32-bit addresses as used in the first ARM releases were absolutely sufficent for the embedded systems, in which ARM processors were applied mainly. But by now the most powerful smartphones were reaching the famous 3.5 GB main memory limit, caused by the use of 32-bit addresses. This made a new development necessary.

So in 2013, the ARM Cortex-A50 was released and the first ARM core to incorporate a 64-bit architecture. Thereby the number of registers was increased to 31 instead of 15 general purpose registers. The first consumer device to implement the A50 core was the Apple A7 SoC, which was designed for the iPhone 5S.

## 5.2 Mill Architecture

When searching for alternative processor architectures, the "Mill architecture" seems to be the most interesting and radical approach. The concept tackles the disadvantages of random access registers, that they are used in nearly every common architecture. It is based on the claim, that 80% of register values are accessed only once, what undermines the benefit of a random access register bank. So the idea of the Mill architecture is a "register belt", in which a new value can only be placed in front of the former values. Register contents that exceed the maximal amount of memory cells vanish. An operation needs to access register values by relative adressing as shown in Figure 5.2. The result of the operation is then again put at the beginning of the belt and pushes the older values' positions.

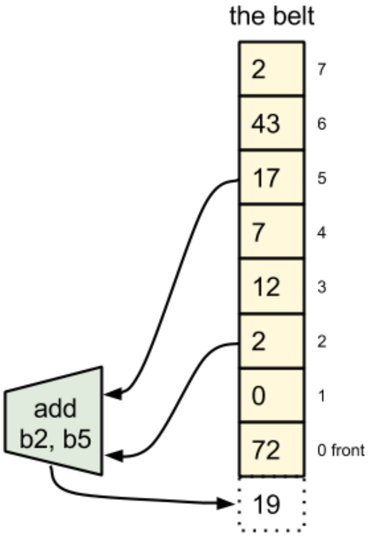


Figure 4: Depiction of the register's belt operating mode in the Mill architecture [4]

This architecture shall improve performance due to less register accesses and a simpler hardware, since sequential memory access is easier. But the belt concept brings huge problems regarding programming the processor. Assembly code would be hard to read and write, because of relative addressing, that changes depending on the order and number of instructions before. Even if most applications are not programmed in low-level languages, compilers could be error-prone and hard to create. Besides, the only company following this approach, Mill Computing, Inc., was yet not able to present a working prototype using this architecture.

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