## GPUs, Co-Processors, ASICs, and FPGAs

Sommerakademie in Leysin AG 2 – Effizientes Rechnen

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### Outline

1 Challenges to HPC

Functioning of a regular CPU Limits of Moore's Law Problems with general purpose processors Need for Heterogeneous Architectures

- 2 Co-Processors Intel Xeon Phi GPUs
- 3 ASICs
- 4 FPGAs

Reconfigurable Computing Applications

# Functioning of a CPU

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- Fetch instructions
- Decode instructions
- Fetch operands
- Execute instruction

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- ⇒ Single Instruction Single Data (SISD)

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- Performance only increases by 40%
- Approaching physical limits
- ⇒ Increasing speed/number of cores not sufficient

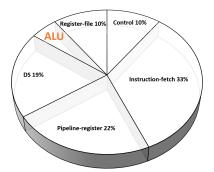
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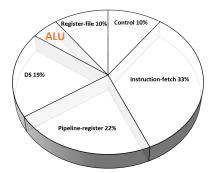
## Problems with general purpose processors

General Purpose ⇒ Control Unit Overhead



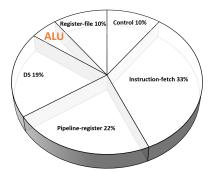
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## Problems with general purpose processors

- General Purpose ⇒ Control Unit Overhead
- High power demand, supply costs are exploding
- Low parallelism
- HPC: often a Single Instruction is executed on multiple Data (SIMD) ⇒ CPU has to fetch and decode for each operation



## Need for Heterogeneous Architectures

Alternatives

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#### **Alternatives**

- Multi-Core CPUs
- Co-Processors
- Hardware Accelerators
  - ASICs
  - FPGAs

Heterogeneous Architectures are crucial for further increasing performance in HPC

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### Definition

- Specialized processor to handle related tasks
  - floating point arithmetic
  - graphics processing
  - encryption
  - etc.

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- Specialized processor to handle related tasks
  - floating point arithmetic
  - graphics processing
  - encryption
  - etc.
- Often bound to a family of processors
- · Aim to increase performance and lower energy demand

#### Examples:

- Apple M7
- 80387 (FPU)

Intel Xeon Phi

#### Intel Xeon Phi

- Coprocessor for Intel Xeon processors
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- Highly parallel vector computations
- Vector capabilities / SIMD ⇒ 3 teraFLOPS (floating-point)
- Specifications
  - Up to 72 cores
  - 16GB on-chip memory
  - 215W power consumption

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Originally accelerators for 3D-Applications
 ⇒ Today: General Purpose computing features

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- Originally accelerators for 3D-Applications
   ⇒ Today: General Purpose computing features
- Communication to host via PCI-Express
- Highly parallel  $\mathsf{Grid} \Rightarrow \mathsf{Block} \Rightarrow \mathsf{Warp} \Rightarrow \mathsf{Thread}$
- Single Instruction Multiple Data
  - $\Rightarrow$  Applications with many floating point operations benefit most

#### Problems with GPUs

- High power consumption
- Difficulties of parallelization
- Relatively low performance gains

1 Challenges to HPC

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Reconfigurable Computing Applications

### **ASICs**

### Application Specific Integrated Circuits

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  - $\rightarrow$  Functionality cannot be changed after fabrication

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#### Applications

- Bitcoin mining
- Car: Anti-lock, airbag
- Kitchen & Home Appliances

#### ASICs: Pros and Cons

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- Low power consumption

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#### Cons

- High development and production cost for low quantities
   High quantities actually make ASICs cheaper than FPGAs
- No versatility, cannot be updated after production

Challenges to HPC

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- FPGAs Reconfigurable Computing Applications

#### **FPGA**

#### Field Programmable Gate Array

Reconfigurable circuits used in HPC

- Configurable Logic Blocks as Gates
- LUT-based, select a boolean function (e.g. or)
  - $\Rightarrow$  Saving configuration with SRAM or antifuse
- CLB connected through configurable wiring

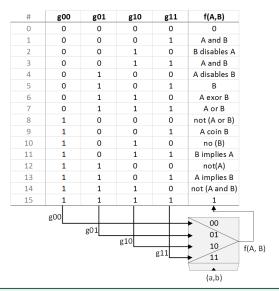
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#### Field Programmable Gate Array

#### Reconfigurable circuits used in HPC

- Configurable Logic Blocks as Gates
- LUT-based, select a boolean function (e.g. or)
  - ⇒ Saving configuration with SRAM or antifuse
- CLB connected through configurable wiring
- Combined with host CPU (e.g. integrated ARM-Processors) for general purpose processing and boot-up, configuration and I/O
- Manufacturers: Altera, Xilinx

# Configurable Logic Blocks (LUT)



## Reconfigurable Computing

Circuits, that can be configured with programming

- Hardware-Description-Languages (VHDL)
   ⇒ configware & flowware
- Reconfiguration possible at runtime

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Circuits, that can be configured with programming

- Hardware-Description-Languages (VHDL)
  - ⇒ configware & flowware
- Reconfiguration possible at runtime
- ⇒ Slower, larger, less power-efficient than ASICs or microprocessors, but:

Superior to microprocessors  $\equiv$  Reconfigurable Computing Paradox

## **Applications**

Can be used in small projects because of low cost

- Encryption/Decryption
- Pattern Matching

Large number of memory accesses, often present in scientific problems promise huge improvements

Speedup factors of over 1000 possible

 $\Rightarrow$  FPGAs are used in 70% of all embedded devices



Thank you!