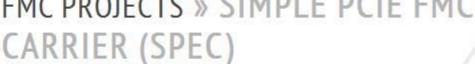
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» S



A simple 4-lane PCIe carrier for FPGA Mezzanine Cards (VITA 57). It has memory and clocking resources and supports the White Rabbit timing and control network.

- Detailed project information
- · Subprojects: Software support for the SPEC board
- · Status: Beta
- Licence: CERN OHL