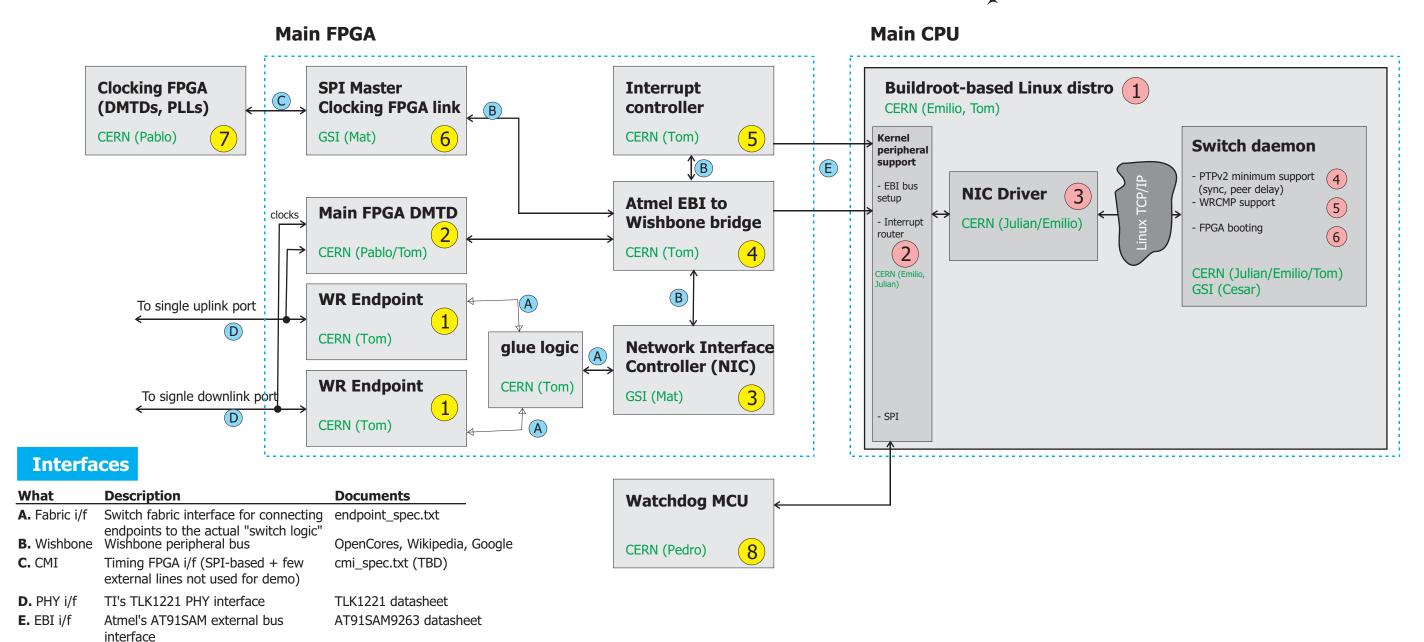
White Rabbit Switch - The Evil Masterplan



HW Tasks

What	Responsible	Description	Documents
1. WR Endpoint	Tom	Partially 802.1x compliant MAC implementing Ethernet framing/deframing, timestamping and WR-specific extensions	endpoint_spec.txt
2. Main FPGA DMTD	Pablo, Tom	Multichannel DMTD-based phase detector with Wishbone interface for measuring shifs between reference and recovered clocks	TBD
3. Internal NIC	Mat	Network interface controller with packet buffering.	internal_nic_spec.txt
4. EBI to WB bridge	Tom, Mat (?)	Simple bridge between Atmel EBI and Wishbone	-
5. Interrupt controller	Tom, Mat (?)	Interrupt multiplexer/controller	TBD
6. SPI Master	Mat	SPI Master for clocking FPGA communication	TBD
7. Clocking FPGA	A Pablo	PLL for generating DMTD clock and PLL for phase shifter + clock input selection	TBD
8.Watchdog	Pedro	Watchdog MCU firmware for booting the card, voltage/current monitoring and i2c access	TBD

SW Tasks

SW Tasks				
What	Responsible	Description	Documents	
1. Buildroot	Emilio, Tom	Create SW design environment based on buildroot	-	
2. Peripheral support	Emilio, Julian	EBI, SSC, SPI, GPIO and FPGA interrupt controller patches for Linux kernel (board support)	TBD	
3. NIC driver	Emilio, Julian	Network interface controller with packet buffering.	internal_nic_spec.txt	
4. PTPv2 deamor	nCesar	Minimal implementation of PTPv2 daemon: sync and peer delay messages.	ptp_daemon_spec.txt TBD	
5. WRCMP daemon	Emilio, Tom Julian, Pedro	Link initialization and delay reporting using WRCMP	TBD	
6. FPGA booting	Tom	FPGA bootloader program	www.altera.com	