# The White Rabbit Project

## Technical introduction and status report

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# Outline

# BE-CO-HT mission

## Provide HW kit for equipment groups at CERN

Based on carriers (VME64x, PCIe...) and FMC (VITA 57) mezzanines.

## Act as knowledge hub for hardware design

FPGA designs based on Wishbone bus, ADC, DAC, TDC, fine delay generators...

## Provide low-level software support for the HW kit

Linux device drivers and libraries, production testing environment...

## Design and operate CERN's General Machine Timing system

Based on the HW and SW technologies the section develops. We eat our own dog food!

# Why we use Open Hardware

## Get a design just the way we want it

We fully specify the design.

## Peer review

Get your design reviewed by experts all around the world, including companies!

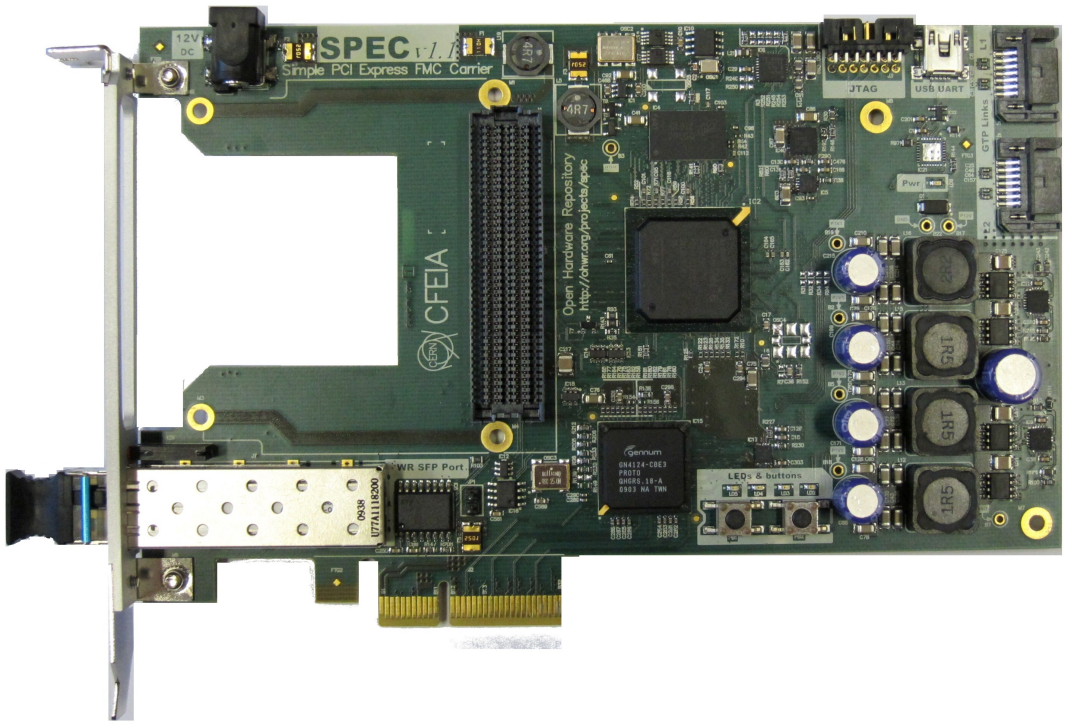
## Design re-use

When it's Open, people are more likely to re-use it.

## Healthier relationship with companies

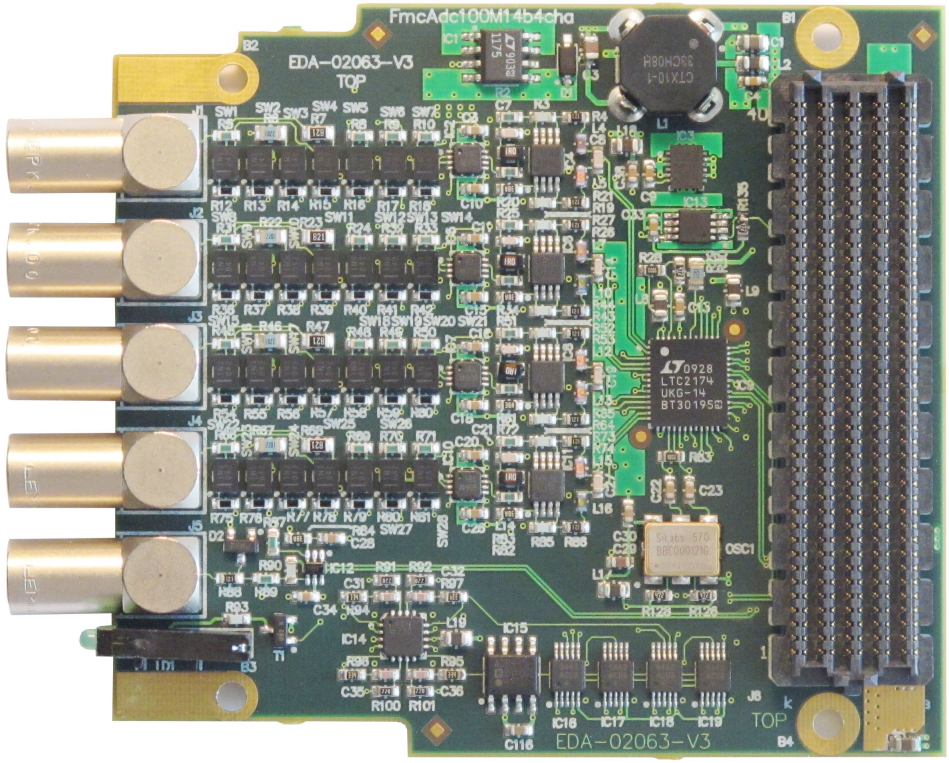
No vendor-locked situations. Companies selected solely on the basis of technical excellence, good support and price.

# Example of a carrier: the SPEC board




- Low-cost PCI-Express Carrier
- Spartan-6 FPGA (XC6SLX45T), 256 MB DDR3 RAM
- White Rabbit Ethernet port

# Example of a mezzanine: 4-channel 100MS/s ADC

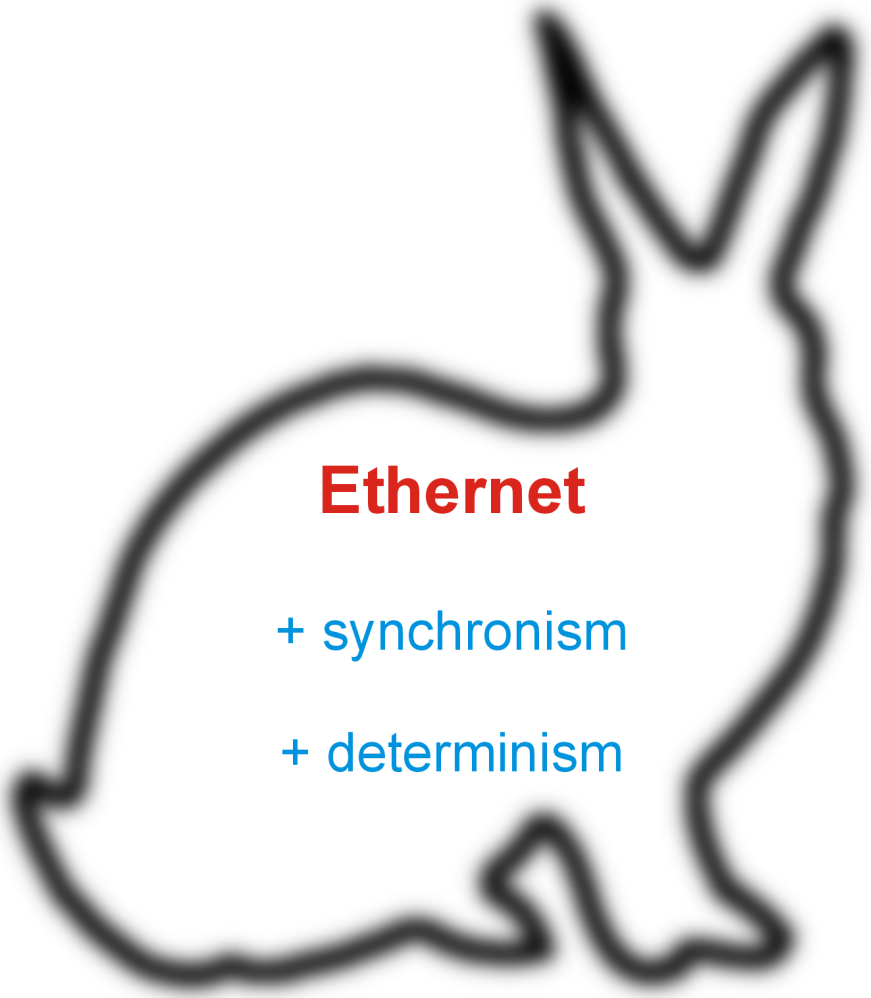



- 105 MSa/s, 14 bits (11.7 ENOB)
- 3 input ranges ($\pm 5V$, $\pm 0.5V$, $\pm 50mV$)
- Flexible triggering: (external, internal or via White Rabbit)

# Development model

- Developed in the frame of CERN's (and GSI's) renovation projects.
- Open source design done in collaboration with industry.
- Commercial production and support.

# What is White Rabbit?



# What is White Rabbit?

An **extension** to **Ethernet** which provides:

- **Synchronous mode** (Sync-E) - common clock for physical layer in entire network, allowing for precise time and frequency transfer.
- **Deterministic routing** latency - a guarantee that packet transmission delay between two stations will never exceed a certain boundary.

# Design goals

## Precision

1 ns time synchronization accuracy, 20 ps jitter

## Range

10 km fiber links

## Scalability

Up to 2000 nodes

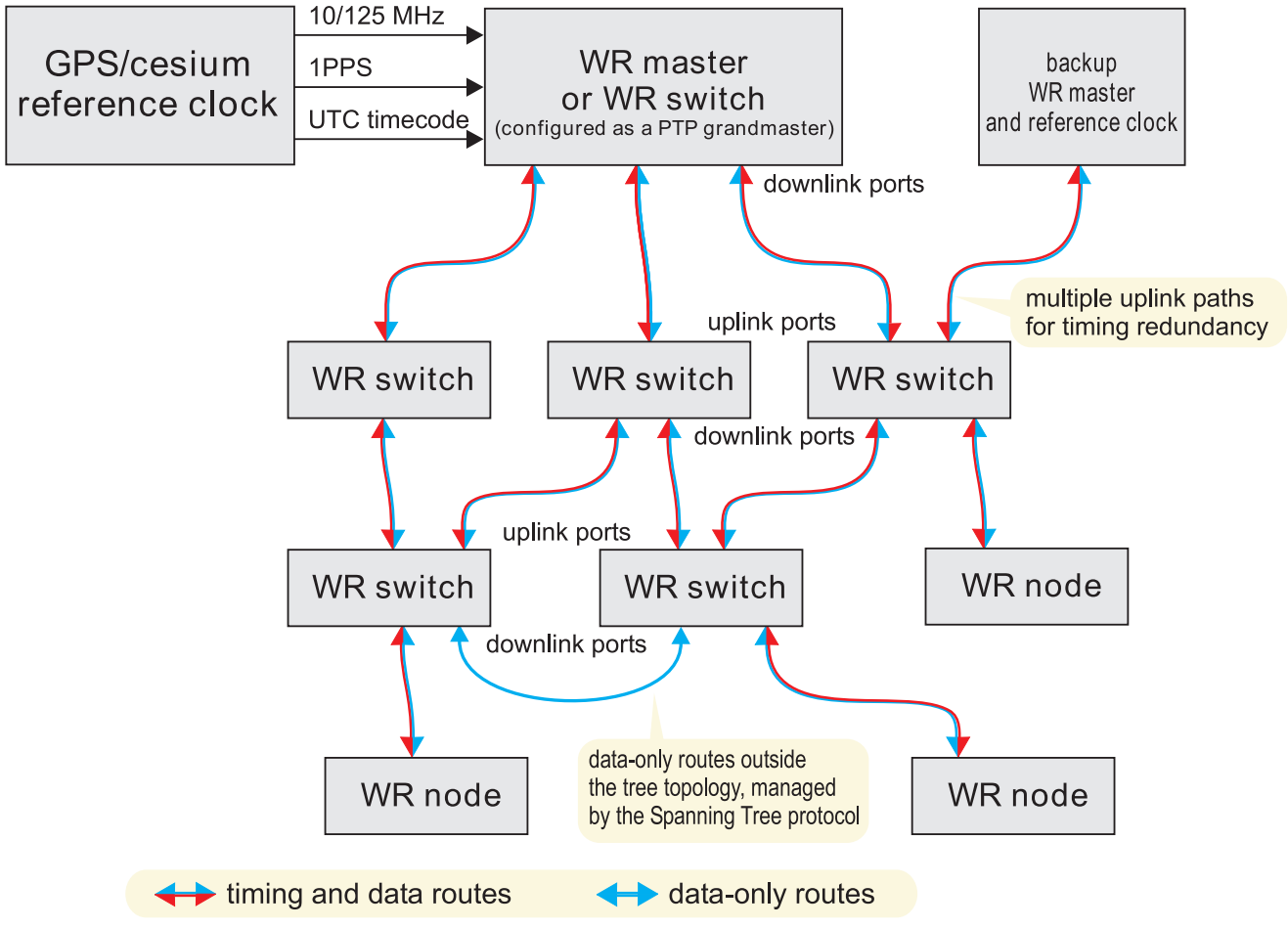
# Outline

# Technologies used in White Rabbit

Sub-nanosecond synchonization in WR is achieved by using the following three technologies together:

- Precision Time Protocol (IEEE1588)
- Synchronous Ethernet
- DMTD phase tracking

# Network topology



# PTP Protocol (IEEE1588)

## PTP

Synchronizes local clock with the master clock by measuring and compensating the delay introduced by the link.

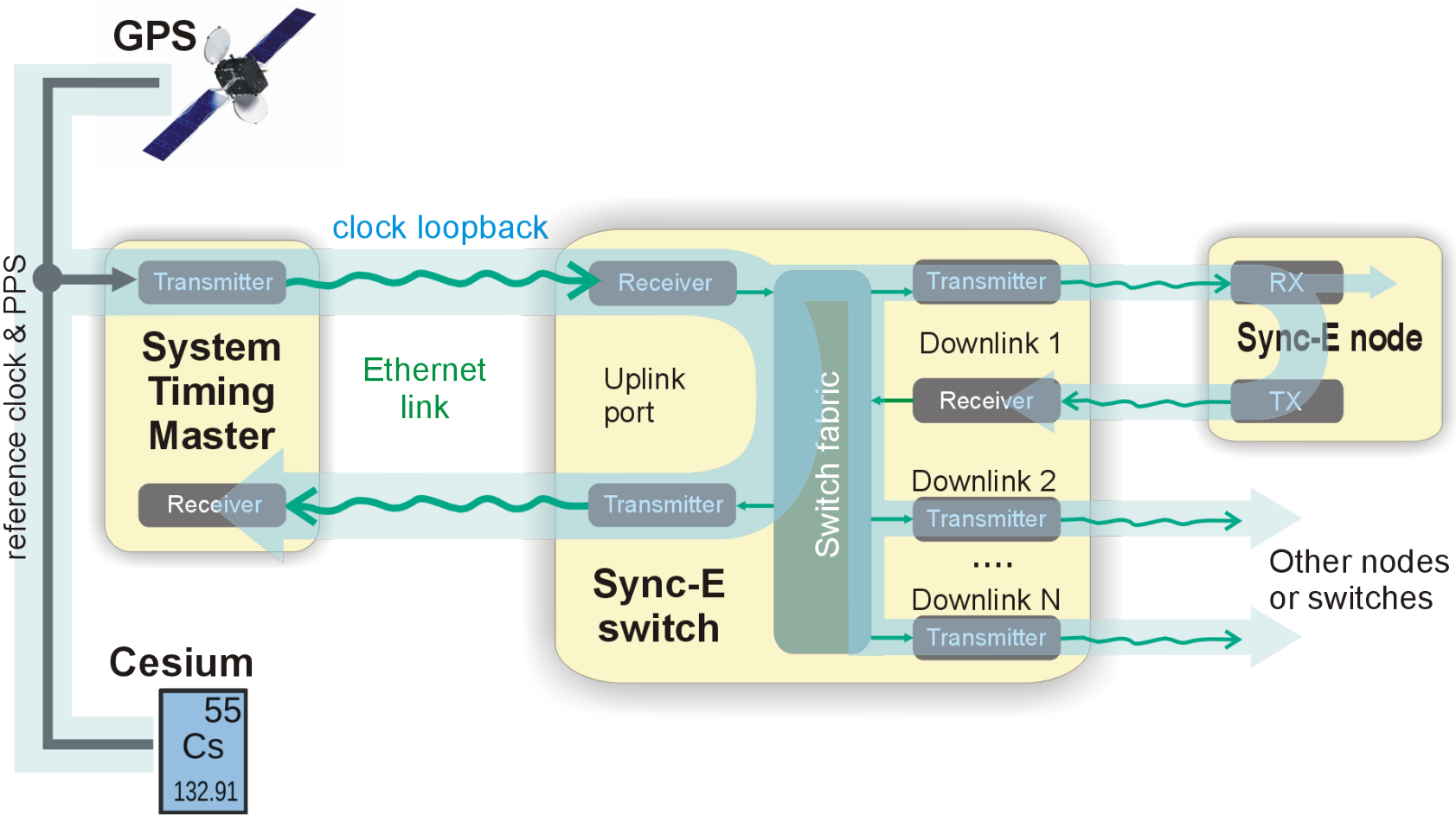
## Packet timestamping

Link delay is measured by exchanging packets with precise hardware transmit/receive timestamps.

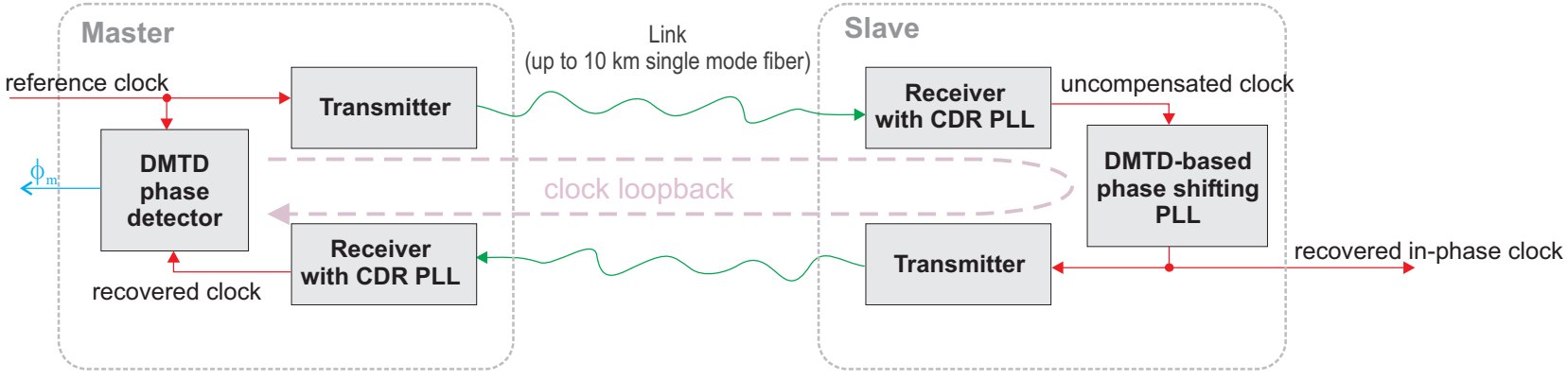
# Disadvantages of traditional PTP

- All nodes have free-running oscillators.
- Frequency drift has to be continously compensated, causing lots of network traffic.
- That doesn't go well with determinism...

# Synchronous Ethernet

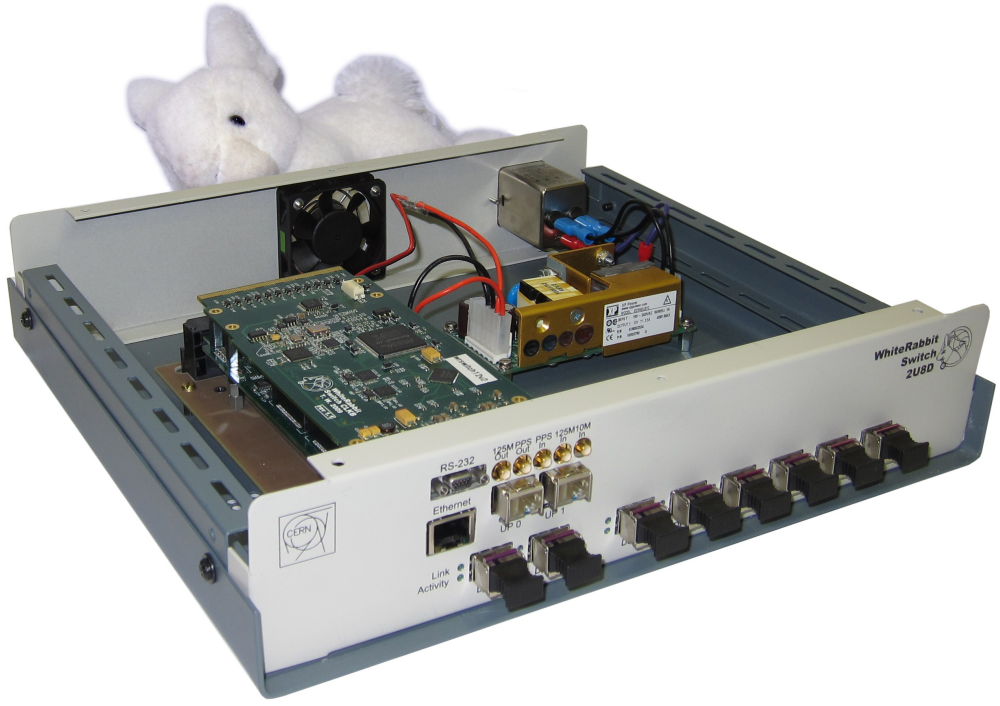


# Phase tracking




- Monitor phase of bounced-back clock continuously.
- Phase-locked loop in the slave follows the phase changes measured by the master.

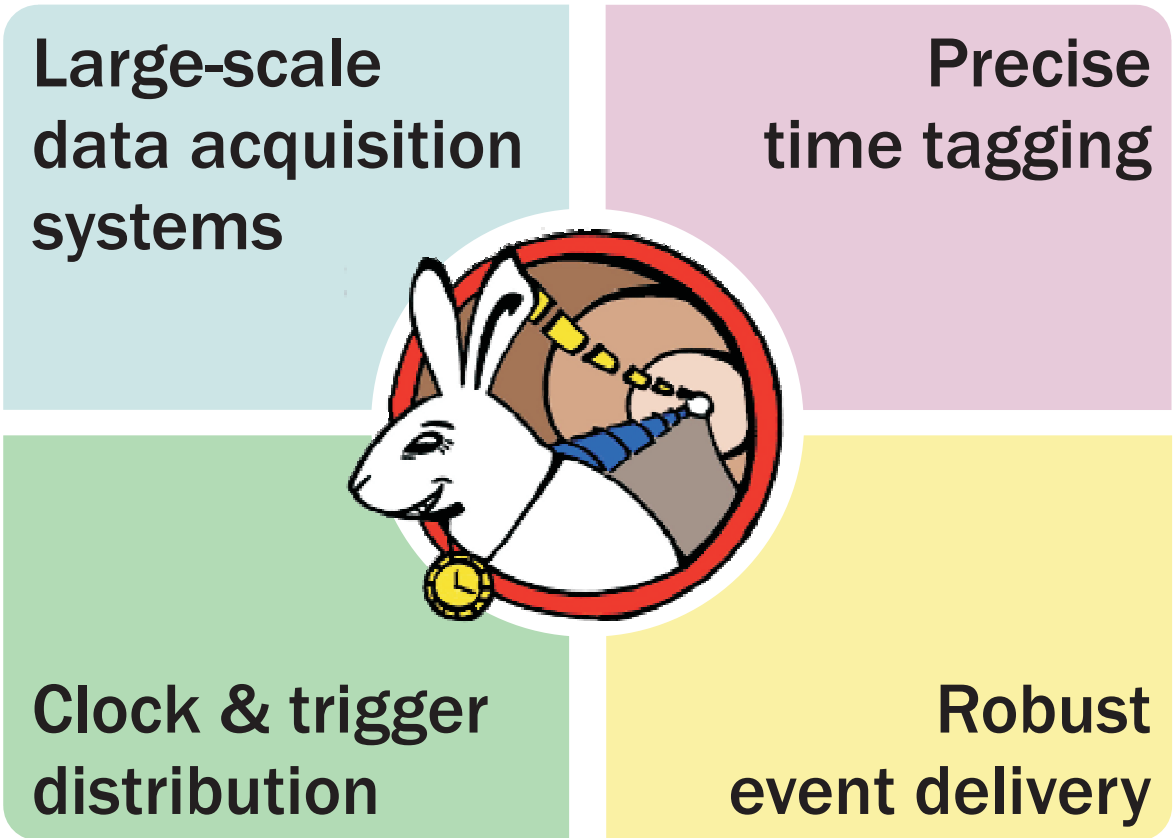
# White Rabbit Switch



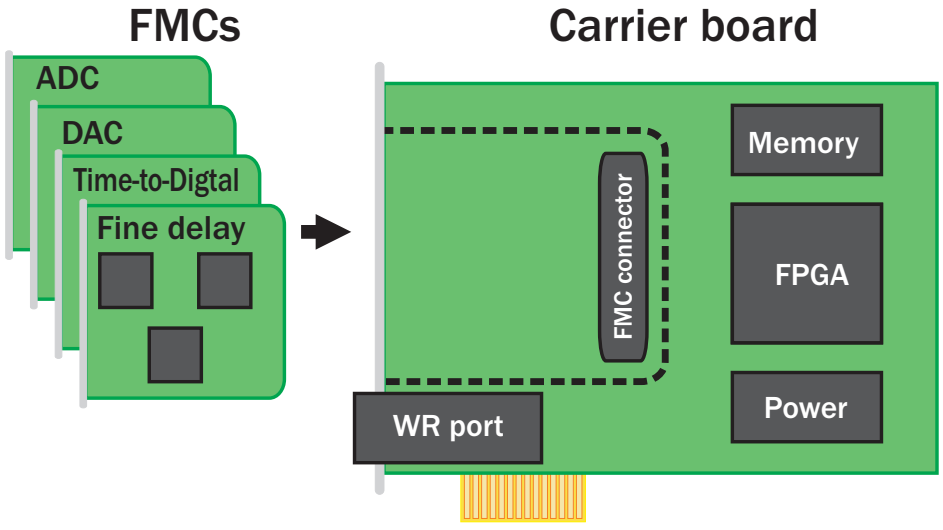

- Central element of WR network
- Fully custom design, done from scratch at CERN
- Ten 1000Base-X ports, may drive 10+ km of SM fiber
- 200 ps synchronization accuracy

# Outline

# Possible applications of White Rabbit



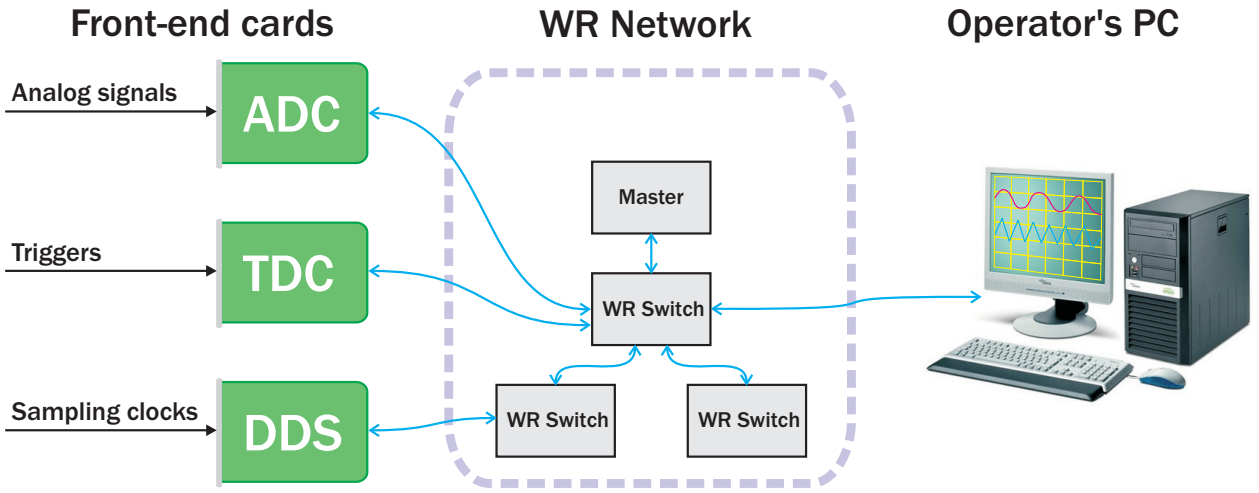
# WR in CERN's BE-CO-HT Hardware Kit




## CERN's BE-CO-HT FMC-based Hardware Kit:

- FMCs (FPGA Mezzanine Cards) with ADCs, DACs, TDCs, fine delays, digital I/O.
- Carrier boards in PCI-Express, VME and uTCA formats.
- All carriers are equipped with a White Rabbit port.

# Distributed oscilloscope




- Common clock: no skew between ADCs
- Ability to sample with different clocks via Distributed DDS
- External triggers can be time tagged with a TDC and used to reconstruct the original time base in the operator's PC

# Outline

# WR Switch development status

## Switch hardware

- Working and debugged V2 hardware prototype
- Tested on 10-km fiber links
- Interoperates with standard Ethernet gear

## Switch software

- Done the Hardware Abstraction Layer and PTP daemon
- Sub-nanosecond accuracy over PTP has been achieved
- Verified interoperability with other PTP devices on ISPCS 2010 Plug Fest

# Already achieved...

## According to ISPCS Plug Fest results ...

**... White Rabbit is the most accurate PTP implementation in the world!**

# Foreseen milestones

## WR Switch

- Basic functionality of HDL and software achieved, code cleanup underway
- V3 prototype (18 ports): Q4 2011
- Commercial product: Q2 2012
  Estimated COTS price: ∼2500€

## WR Ecosystem commercial availability

- PCIe carrier available now, VME Q2 2012
- WR timing node in VME and PCIe: Q2 2012
- Mezzanines: Full set of cards Q2 2012

# Summary

## A deterministic timing and data link

- 1 ns accuracy and 20 ps jitter
- 10 km fiber links
- Up to 2000 nodes

## A successful **open collaboration**

- Fully open development
- Involving institutes and companies
- Full system commercially available mid-2012

For more information,
http://www.ohwr.org/projects/white-rabbit/wiki