

The White Rabbit Project

Technical introduction and status report

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BE-CO Hardware and Timing section
CERN

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Outline

Origin of the name



Oh dear! Oh dear! I shall be too late!
The White Rabbit in charge of real time

Development model

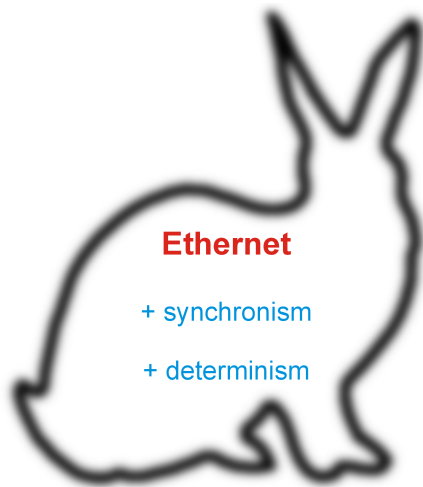
- Developed in the frame of ACCOR project
- Open source design done in collaboration with industry
- Commercial production and support

Why White Rabbit?

General Machine Timing limitations

- Low speed (500 kbps)
- Lack of bidirectional communication
- Complicated maintenance

What is White Rabbit?



What is White Rabbit?

An **extension** to **Ethernet** which provides:

- **Synchronous mode** (Sync-E) - common clock for physical layer in entire network, allowing for precise time and frequency transfer.
- **Deterministic routing** latency - a guarantee that packet transmission delay between two stations will never exceed a certain boundary.

Design goals

Scalability

Up to 2000 nodes.

Range

10 km fiber links.

Precision

1 ns time synchronization accuracy, 20 ps jitter.

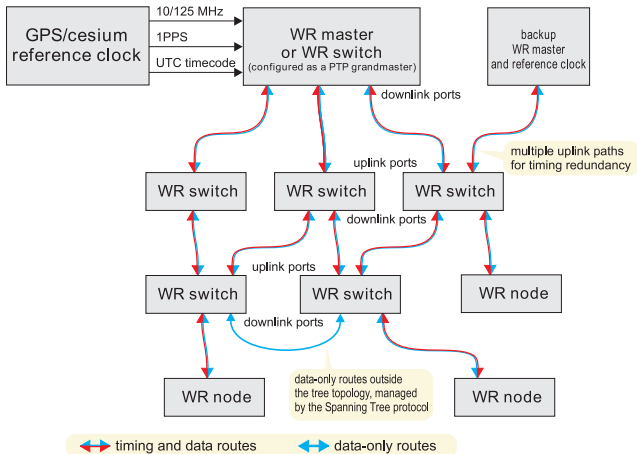
Outline

Technologies used in White Rabbit

Sub-nanosecond synchronization in WR is achieved by using the following three technologies together:

- Precision Time Protocol (IEEE1588)
- Synchronous Ethernet
- DMTD phase tracking

Network topology



PTP Protocol (IEEE1588)

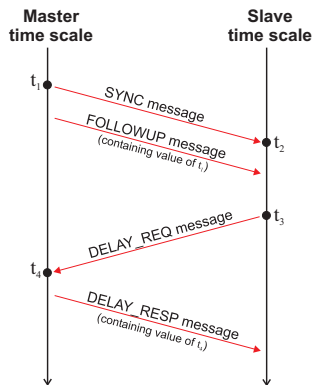
PTP

Synchronizes local clock with the master clock by measuring and compensating the delay introduced by the link.

Packet timestamping

Link delay is measured by exchanging packets with precise hardware transmit/receipt timestamps

PTP Protocol (IEEE1588)



Having values of $t_1...t_4$, slave can:

- calculate one-way link delay:
$$\delta_{ms} = \frac{(t_4 - t_1) - (t_3 - t_2)}{2}$$
- syntonize its clock rate with the master by tracking the value of $t_2 - t_1$
- compute clock offset:
$$offset = t_2 - t_1 + \delta_{ms}$$

Disadvantages of traditional PTP

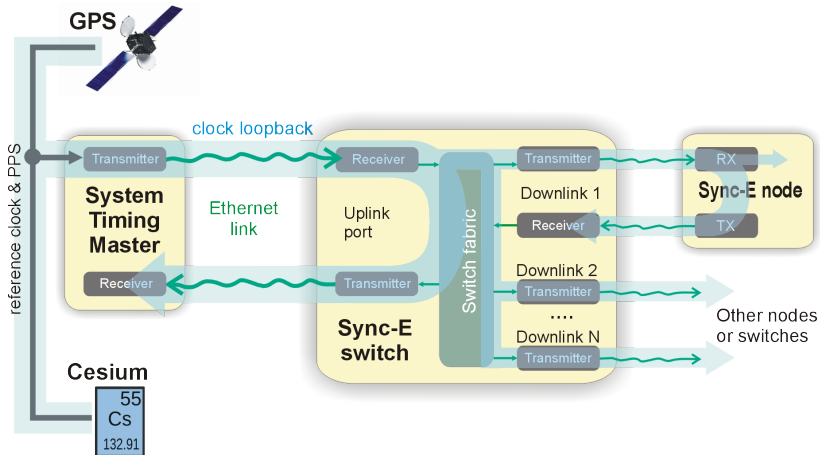
- All nodes have free-running oscillators
- Frequency drift has to be continuously compensated, causing lots of network traffic
- That doesn't go well with determinism...

Synchronous Ethernet

Common clock for the entire network

- All network nodes use the same physical layer clock, generated by the System Timing Master
- Clock is encoded in the Ethernet carrier and recovered by the receiver chip (PHY).
- PTP is used only for compensating clock offset.
- Having the same clock frequency everywhere enables phase detector technology as the means of measuring time.

Synchronous Ethernet



Phase tracking

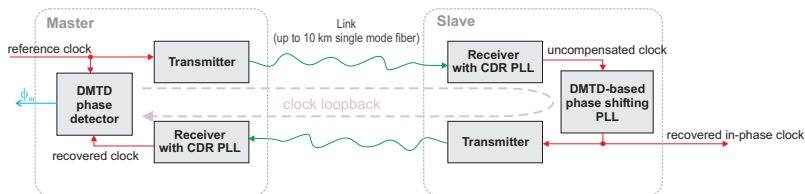
Plain PTP

PTP alone is not enough if we want very good accuracy, because of the granularity of the timestamps.

Solution

Measure the phase shift between transmit and receive clock on the master side, taking the advantage of Synchronous Ethernet.

Phase tracking



- Monitor phase of bounced-back clock continuously
- Phase-locked loop in the slave follows the phase changes measured by the master

White Rabbit Switch

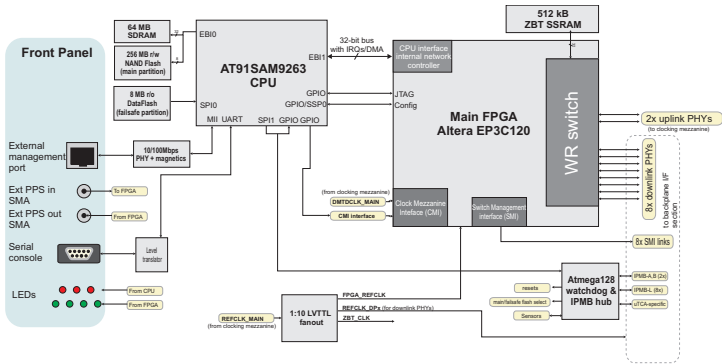


- Central element of WR network
- Fully custom design, designed from scratch
- 10 1000Base-LX ports, capable of driving 10 km of SM fiber
- 200 ps synchronization accuracy

White Rabbit Switch

- Designed in microTCA MCH (Management Carrier Hub) format.
- Multi-PCB design: base board with main big FPGA and CPU and Clocking Mezzanine, which handles the timing.
- Can work in standalone mode (without a microTCA crate) via mini-backplane.

Switch block diagram - main part



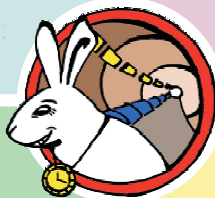
- System FPGA handles all packet processing
- CPU implements PTP stack and management functions (SNMP, Spanning Tree)

Outline

Possible applications of White Rabbit

**Large-scale
data acquisition
systems**

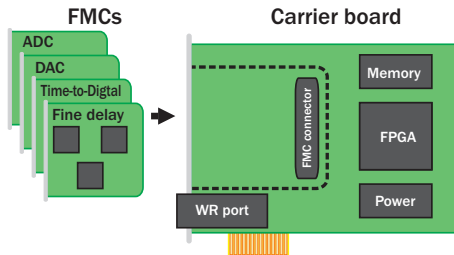
**Precise
time tagging**



**Clock & trigger
distribution**

**Robust
event delivery**

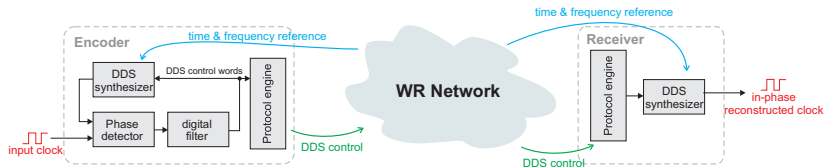
WR in Co-HT's Hardware Kit



Co-HT FMC-based Hardware Kit:

- FMCs (FPGA Mezzanine Cards) with ADCs, DACs, TDCs, fine delays, digital I/O
- Carrier boards in PCI-Express, VME and uTCA formats
- All carriers are equipped with a White Rabbit port

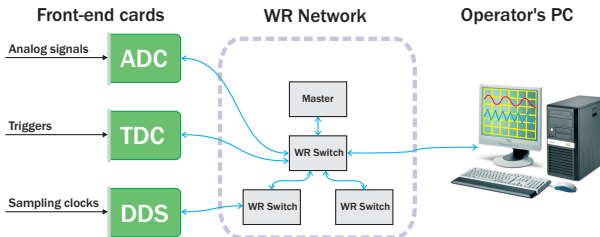
Ethernet Clock distribution a.k.a. Distributed DDS



Distributed Direct Digital Synthesis

- Replaces dozens of cables with a single fiber
- Works over big distances without degrading signal quality
- Can provide various clocks (TTC, RF, bunch clock) with a single, standardized link

Distributed oscilloscope



- Common clock in the entire network: no skew between ADCs
- Ability to sample with different clocks via Distributed DDS
- External triggers can be time tagged with a TDC and used to reconstruct the original time base in the Operator's PC.

Outline

WR Switch development status

Switch hardware

- Working and debugged V2 hardware prototype
- Tested on 10-km fiber links
- Interoperates with standard Ethernet gear

Switch software

- Done the Hardware Abstraction Layer and PTP daemon
- Sub-nanosecond accuracy over PTP has been achieved
- Verified interoperability with other PTP devices on ISPCS 2010 Plug Fest

Already achieved...

According to ISPCS Plug Fest results ...

**... White Rabbit is the most accurate PTP implementation
in the world!**

CERN - White Rabbit developers

T. Wlostowski

- HDL development
- Further improvements in the synchronization performance
- Co-design of V3 Switch hardware with the industrial partners

M. Lipinski

- Development of fault-proof event delivery protocol
- PTP stack support
- HDL development

External contributors

GSI Darmstadt

- Fieldbus protocol development, working on reliability
- HDL development

Alessandro Rubini (GNUDD)

- Main software developer
- Device drivers
- Embedded Linux support

Integrasys

- Development of switch management software
- IEEE802.x compatibility testing

Seven Solutions

- Co-design of V3 switch hardware (technical spec available mid-November)
- Prototype production and testing

Elproma (not confirmed yet)

- Commercial WR OEM modules and time servers

Foreseen milestones

WR Switch

- Full basic functionality of HDL and software: mid-December 2010
- V3 prototype: Q3 2011
- Commercial product: Q1 2012

WR Ecosystem

- FMC Carriers: VME version prototype done, PCIe available at the end of November
- WR timing node: Q2 2012
- Mezzanines: Full set of cards available Q4 2011

Summary

- A data link fulfilling all our needs in **synchronization** and **determinism**.
- A successful **collaboration** including institutes and companies.
- Full system available at the **middle of 2012**