

The White Rabbit Project

Technical introduction and status report

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November 7, 2011

Outline

1 Introduction

2 Technology overview

- Precision Time Protocol (IEEE1588)
- Synchronous Ethernet
- Phase tracking
- White Rabbit Switch

3 Applications

- WR in CERN's BE-CO-HT Hardware Kit

4 Planning

- Current status
- Development plans for 2011

BE-CO-HT mission

Provide HW kit for equipment groups at CERN

Based on carriers (VME64x, PCIe...) and FMC (VITA 57) mezzanines.

Act as knowledge hub for hardware design

FPGA designs based on Wishbone bus, ADC, DAC, TDC, fine delay generators...

Provide low-level software support for the HW kit

Linux device drivers and libraries, production testing environment...

Design and operate CERN's General Machine Timing system

Based on the HW and SW technologies the section develops.
We eat our own dog food!

Why we use Open Hardware

Get a design just the way we want it

We fully specify the design.

Peer review

Get your design reviewed by experts all around the world, including companies!

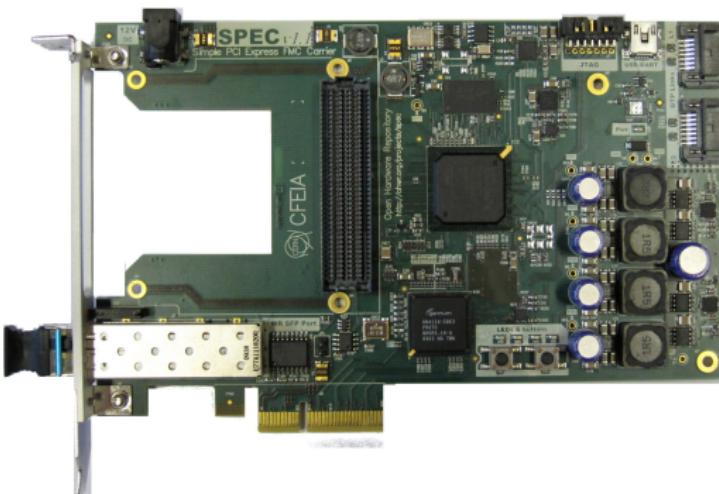
Design re-use

When it's Open, people are more likely to re-use it.

Healthier relationship with companies

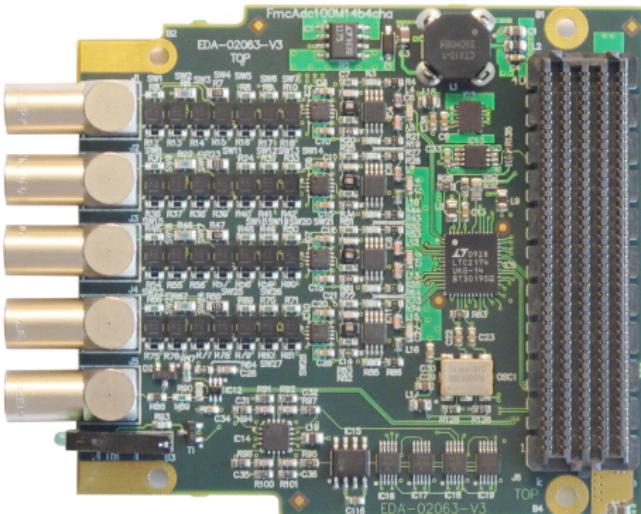
No vendor-locked situations. Companies selected solely on the basis of technical excellence, good support and price.

Example of a carrier: the SPEC board



- Low-cost PCI-Express Carrier
- Spartan-6 FPGA (XC6SLX45T), 256 MB DDR3 RAM
- White Rabbit Ethernet port

Example of a mezzanine: 4-channel 100MS/s ADC



- 105 MSa/s, 14 bits (11.7 ENOB)
- 3 input ranges (10 V, 1 V, 100 mV)
- Flexible triggering: (external, internal or via White Rabbit)

What's in a name?

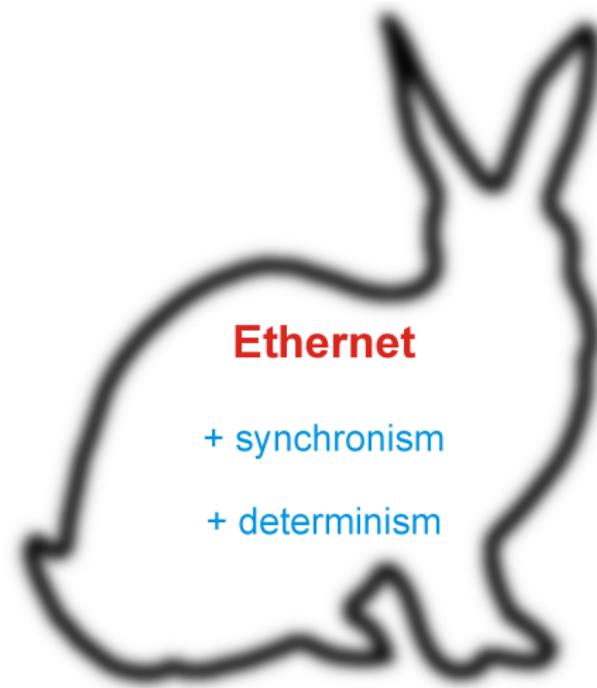


Oh dear! Oh dear! I shall be too late!

Development model

- Developed in the frame of CERN's (and GSI's) renovation projects.
- Open source design done in collaboration with industry.
- Commercial production and support.

What is White Rabbit?



What is White Rabbit?

An **extension** to **Ethernet** which provides:

- **Synchronous mode** (Sync-E) - common clock for physical layer in entire network, allowing for precise time and frequency transfer.
- **Deterministic routing** latency - a guarantee that packet transmission delay between two stations will never exceed a certain boundary.

Design goals

Scalability

Up to 2000 nodes.

Range

10 km fiber links.

Precision

1 ns time synchronization accuracy, 20 ps jitter.

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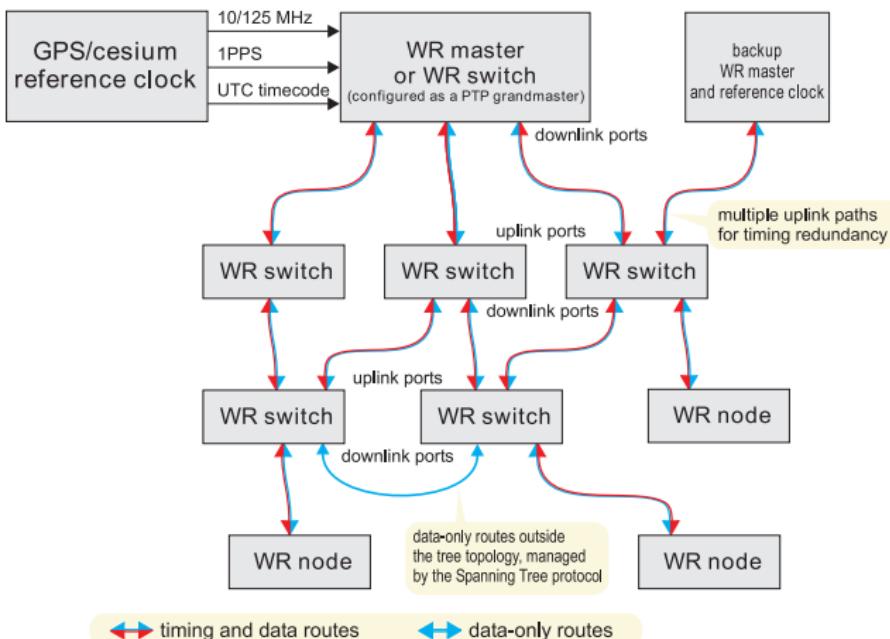
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Technologies used in White Rabbit

Sub-nanosecond synchronization in WR is achieved by using the following three technologies together:

- Precision Time Protocol (IEEE1588).
- Synchronous Ethernet.
- DMTD phase tracking.

Network topology



PTP Protocol (IEEE1588)

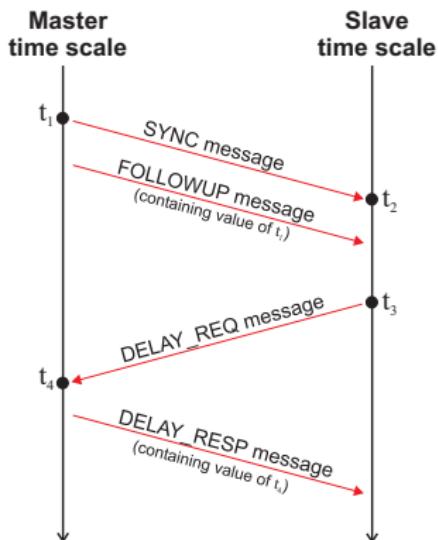
PTP

Synchronizes local clock with the master clock by measuring and compensating the delay introduced by the link.

Packet timestamping

Link delay is measured by exchanging packets with precise hardware transmit/receipt timestamps.

PTP Protocol (IEEE1588)



Having values of $t_1 \dots t_4$, slave can:

- calculate one-way link delay:

$$\delta_{ms} = \frac{(t_4 - t_1) - (t_3 - t_2)}{2}$$
- syntonize its clock rate with the master by tracking the value of $t_2 - t_1$
- compute clock offset:

$$\text{offset} = t_2 - t_1 + \delta_{ms}$$

Disadvantages of traditional PTP

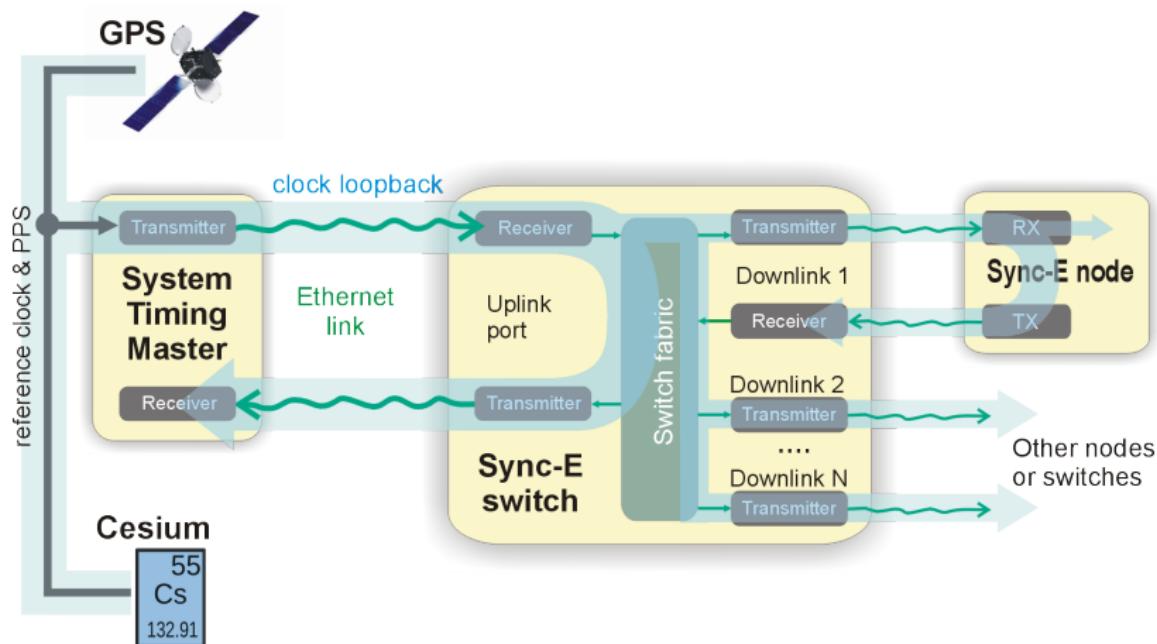
- All nodes have free-running oscillators.
- Frequency drift has to be continuously compensated, causing lots of network traffic.
- That doesn't go well with determinism...

Synchronous Ethernet

Common clock for the entire network

- All network nodes use the same physical layer clock, generated by the System Timing Master.
- Clock is encoded in the Ethernet carrier and recovered by the receiver chip (PHY).
- PTP is used only for compensating clock offset.
- Having the same clock frequency everywhere enables phase detector technology as the means of measuring time.

Synchronous Ethernet



Phase tracking

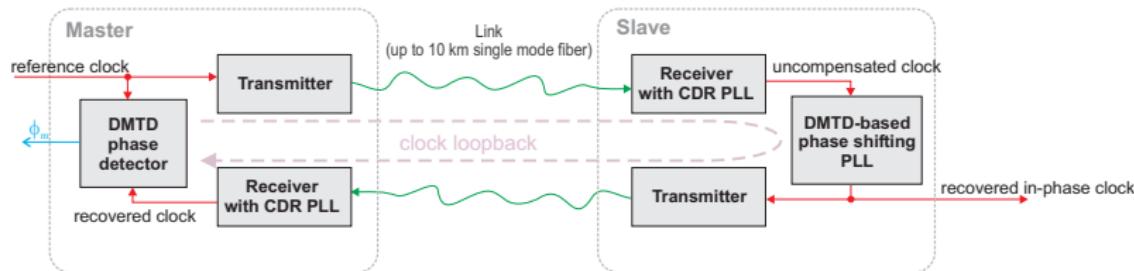
Plain PTP

PTP alone is not enough if we want very good accuracy, because of the granularity of the timestamps.

Solution

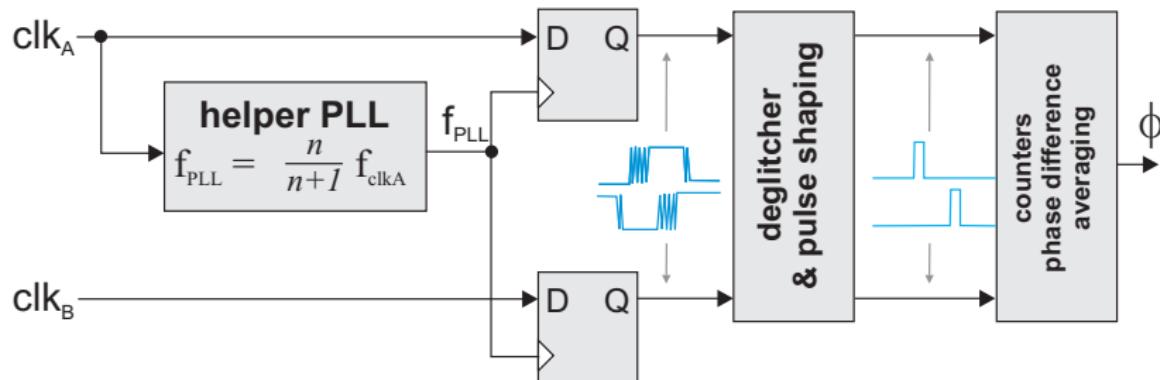
Measure the phase shift between transmit and receive clock on the master side, taking the advantage of Synchronous Ethernet.

Phase tracking



- Monitor phase of bounced-back clock continuously.
- Phase-locked loop in the slave follows the phase changes measured by the master.

Digital Dual Mixer Time Domain (DMTD) phase detector



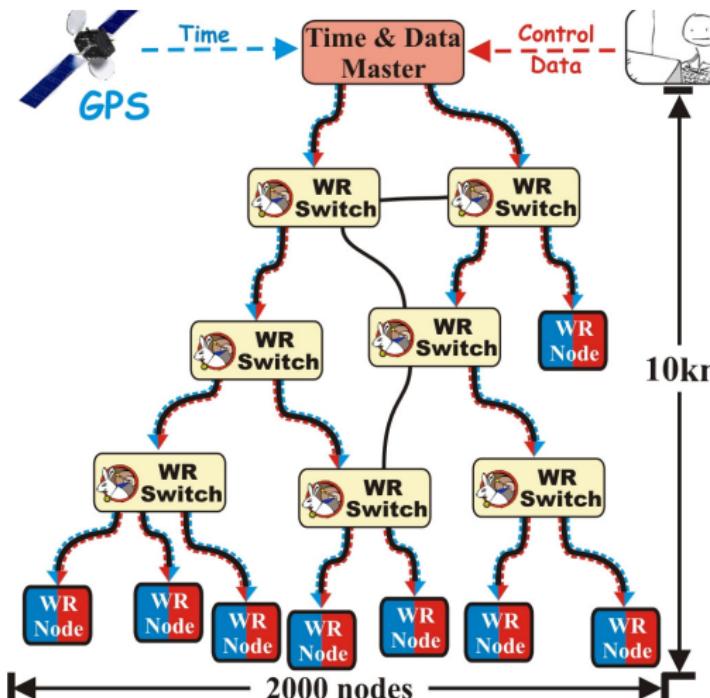
- Fully digital, so fully linear
- In a loop, it becomes a linear phase shifter
- Can handle multiple channels without need for extra hardware

What is Robustness in WR?

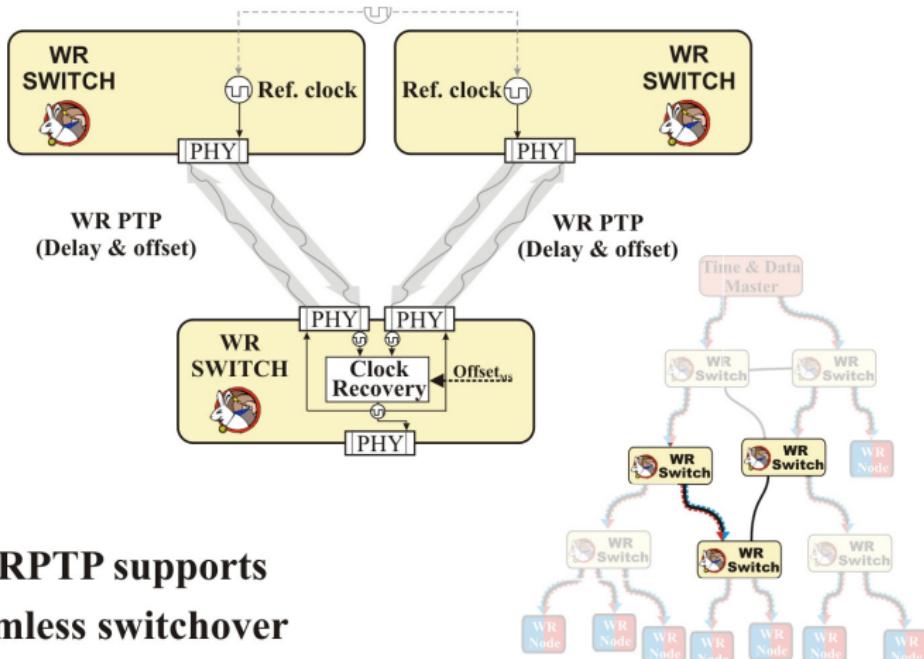
Robustness

preventing degradation of parameters in abnormal circumstances

- Sub-nanosecond time synchronization
- Deterministic Control Data delivery



Synchronization redundancy support



White Rabbit Switch

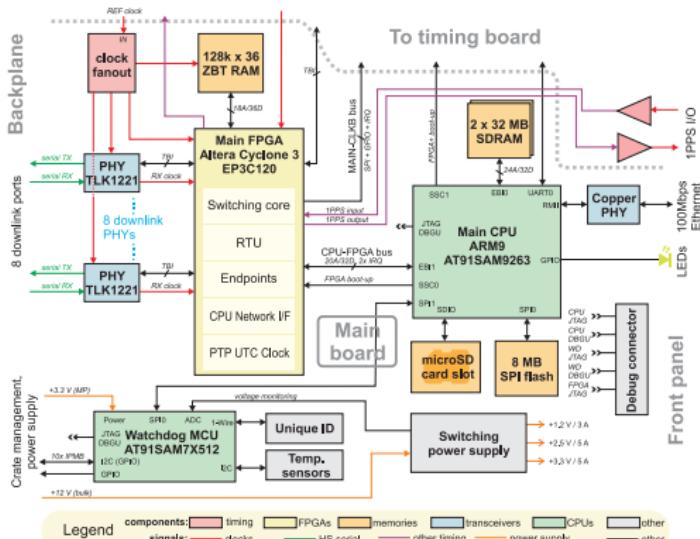


- Central element of WR network.
- Fully custom design, done from scratch at CERN.
- 10 1000Base-X ports, capable of driving 10+ km of SM fiber.
- 200 ps synchronization accuracy.

White Rabbit Switch

- Designed in microTCA MCH (Management Carrier Hub) format.
- Multi-PCB design: base board with main big FPGA and CPU and Clocking Mezzanine, which handles the timing.
- Can work in standalone mode (without a microTCA crate) via mini-backplane.

Switch block diagram - main part



- System FPGA handles all packet processing.
- CPU implements PTP stack and management functions (SNMP, Spanning Tree).

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Possible applications of White Rabbit

**Large-scale
data acquisition
systems**

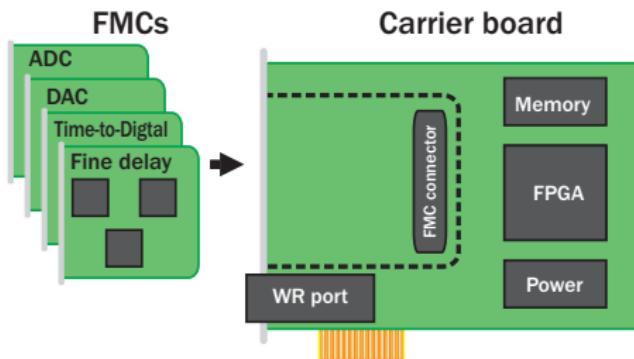
**Precise
time tagging**

**Clock & trigger
distribution**

**Robust
event delivery**



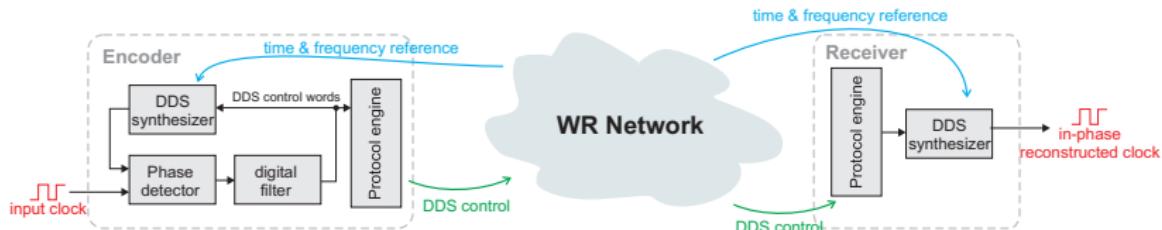
WR in CERN's BE-CO-HT Hardware Kit



CERN's BE-CO-HT FMC-based Hardware Kit:

- FMCs (FPGA Mezzanine Cards) with ADCs, DACs, TDCs, fine delays, digital I/O.
- Carrier boards in PCI-Express, VME and uTCA formats.
- All carriers are equipped with a White Rabbit port.

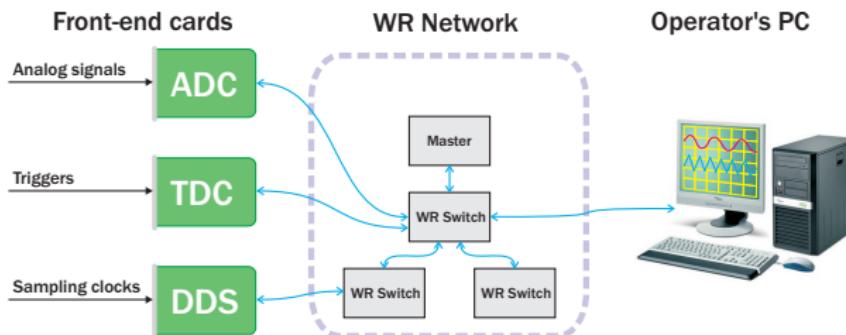
Ethernet Clock distribution a.k.a. Distributed DDS



Distributed Direct Digital Synthesis

- Replaces dozens of cables with a single fiber.
- Works over big distances without degrading signal quality.
- Can provide various clocks (TTC, RF, bunch clock) with a single, standarized link.

Distributed oscilloscope



- Common clock in the entire network: no skew between ADCs.
- Ability to sample with different clocks via Distributed DDS.
- External triggers can be time tagged with a TDC and used to reconstruct the original time base in the operator's PC.

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WR Switch development status

Switch hardware

- Working and debugged V2 hardware prototype.
- Tested on 10-km fiber links.
- Interoperates with standard Ethernet gear.

Switch software

- Done the Hardware Abstraction Layer and PTP daemon.
- Sub-nanosecond accuracy over PTP has been achieved.
- Verified interoperability with other PTP devices on ISPCS 2010 Plug Fest.

Already achieved...

According to ISPCS Plug Fest results ...

**... White Rabbit is the most accurate PTP implementation
in the world!**

Foreseen milestones

WR Switch

- Full basic functionality of HDL and software already achieved, code cleanup underway.
- V3 prototype: Q4 2011.
- Commercial product: Q2 2012.

WR Ecosystem

- FMC Carriers: PCIe commercially available now, VME Q2 2012.
- WR timing node in VME and PCIe: commercially available Q2 2012.
- Mezzanines: Full set of cards commercially available Q2 2012.

Summary

- A data link fulfilling all our needs in **synchronization** and **determinism**.
- A successful **collaboration** including institutes and companies.
- Full system commercially available **mid-2012**.

For more information, visit
<http://www.ohwr.org/projects/white-rabbit/wiki>