TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC4093BP, TC4093BF, TC4093BFN

TC4093B QUAD 2-INPUT NAND SCHMITT TRIGGERS

The TC4093B is a quad 2-input NAND gate having Schmitt trigger function for all the input terminals.

Since the circuit threshold voltage varies with rising time and falling time of the input waveform (V_P and V_N), this gate can be used for a wide variety of applications to line receivers, waveform shaping.

Astable multivibrators, monosatable multivibrators, etc.

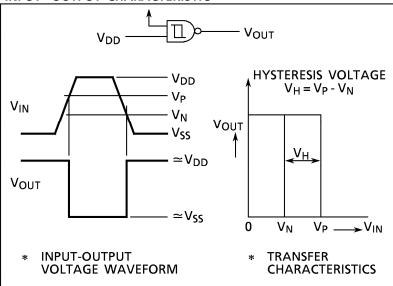
In addition to regular NAND gates.

As the TC4093B and the TC4011B are identical in pin assignment, they are compatible each other.

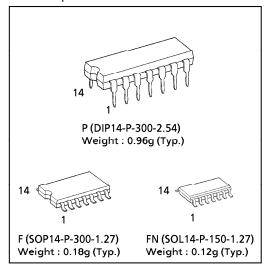
MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	$V_{SS} - 0.5 \sim V_{SS} + 20$	٧
Input Voltage	V _{IN}	$V_{SS} - 0.5 \sim V_{DD} + 0.5$	٧
Output Voltage	V _{OUT}	$V_{SS} - 0.5 \sim V_{DD} + 0.5$	٧
DC Input Current	I _{IN}	± 10	mA
Power Dissipation	P _D	300 (DIP) / 180 (SOIC)	mW
Operating Temperature Range	T _{opr}	- 40~85	°C
Storage Temperature Range	T _{stg}	- 65∼150	°C

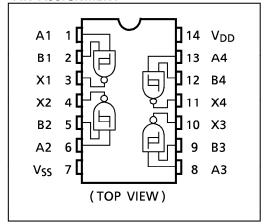
INPUT - OUTPUT CHARACTERISTIC



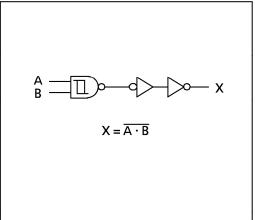
(Note) The JEDEC SOP (FN) is not available in Japan.



PIN ASSIGNMENT



LOGIC DIAGRAM



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RECOMMENDED OPERATING CONDITIONS ($V_{SS} = 0V$)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
DC Supply Voltage	V _{DD}		3	_	18	V
Input Voltage	V _{IN}		0	_	V_{DD}	V

STATIC ELECTRICAL CHARACTERISTICS (V_{SS} = 0V)

CHARACTERISTIC		SYM-	TEST CONDITION	(V)	– 40°C		25°C			85°C		UNIT
СПАКА	ACTERISTIC BOL		TEST CONDITION		MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	UNIT
High-Lev Output \		V _{OH}	$ I_{OUT} < 1\mu A$ $V_{IN} = V_{SS}, V_{DD}$	5 10 15	4.95 9.95 14.95		4.95 9.95 14.95	5.00 10.00 15.00		4.95 9.95 14.95	_ _ _	V
Low-Level Output Voltage		V _{OL}	$\begin{vmatrix} I_{OUT} < 1\mu A \\ V_{IN} = V_{DD} \end{vmatrix}$	5 10 15		0.05 0.05 0.05		0.00 0.00 0.00	0.05 0.05 0.05		0.05 0.05 0.05	V
Output I Current	High	Іон	$V_{OH} = 4.6V$ $V_{OH} = 2.5V$ $V_{OH} = 9.5V$ $V_{OH} = 13.5V$ $V_{IN} = V_{SS}, V_{DD}$	5 5 10 15	- 0.61 - 2.50 - 1.50 - 4.00		- 0.51 - 2.10 - 1.30 - 3.40	- 1.0 - 4.0 - 2.2 - 9.0		- 0.42 - 1.70 - 1.10 - 2.80	_	- mA
Output Low Current		I _{OL}	$V_{OL} = 0.4V$ $V_{OL} = 0.5V$ $V_{OL} = 1.5V$ $V_{IN} = V_{DD}$	5 10 15	0.61 1.5 4.0		0.51 1.30 3.40	1.5 3.8 15.0		0.42 1.10 2.80		
High Threshold Voltage		V _P	$V_{OUT} = 0.5V, 4.5V$ $V_{OUT} = 1.0V, 9.0V$ $V_{OUT} = 1.5V, 13.5V$	5 10 15			2.05 4.10 6.20	2.8 5.3 7.8	3.55 7.00 10.40		_ _ _	
Low Thro	eshold	V _N	$V_{OUT} = 0.5V, 4.5V$ $V_{OUT} = 1.0V, 9.0V$ $V_{OUT} = 1.5V, 13.5V$	5 10 15		_ _ _	1.5 3.2 4.8	2.3 4.5 6.6	3.15 6.30 9.30	_ _ _	_ _ _	v
Hysteresis Voltage		V _H		5 10 15	_ _ _	_ _ _	0.20 0.30 0.45	0.5 0.8 1.2	0.85 1.40 1.90	_ _ _	_ _ _	
Input	"H" Level	I _{IH}	V _{IH} = 18V	18	_	0.1	_	10 ⁻⁵	0.1	_	1.0	μΑ
Quiescen Current	"L" Level	I _{IL}	$V_{IL} = 0V$ $V_{IN} = V_{SS}, V_{DD} *$	18 5 10 15		- 0.1 1 2 4	_ _ _	0.001 0.002 0.004	1 2 4	_ _ _	7.5 15.0 30.0	μA

^{*} All valid input combinations.

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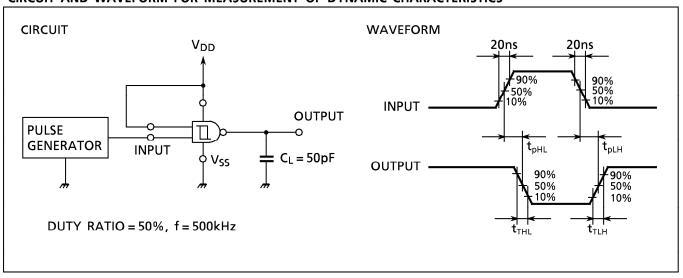
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DYNAMIC ELECTRICAL CHARACTERISTICS (Ta = 25°C, Vss = 0V, C_L = 50_PF)

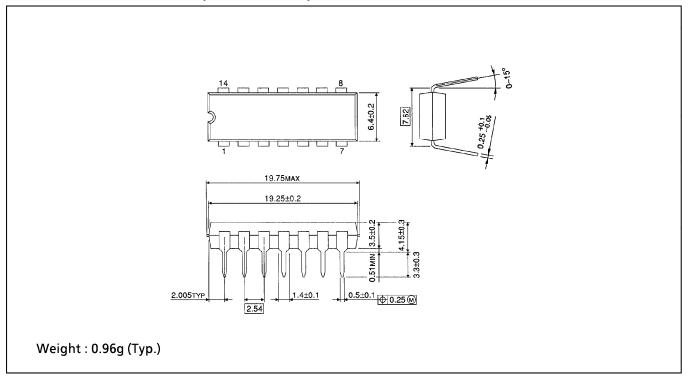
CHARACTERISTIC	SYMBOL	TEST CONDITION	V _{DD} (V)	MIN.	TYP.	MAX.	UNIT
Output Transition Time			5	_	80	200	
	t _{TLH}		10	<u> </u>	50	100	
(Low to High)			15	<u> </u>	40	80	ns
Output Transition Time (High to Low)			5	_	80	200] '' `
	t _{THL}		10	_	50	100	
			15	<u>—</u>	40	80	
Propagation Delay Time			5	_	130	260	
	t _{pLH}		10	_	60	120	ns
	t _{pHL}		15	_	40	80	
Input Capacitance	C _{IN}			_	5	7.5	pF

CIRCUIT AND WAVEFORM FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS



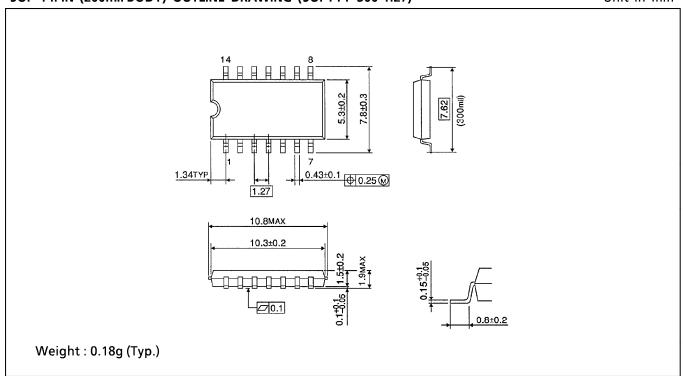
DIP 14PIN OUTLINE DRAWING (DIP14-P-300-2.54)

Unit in mm



SOP 14PIN (200mil BODY) OUTLINE DRAWING (SOP14-P-300-1.27)

Unit in mm



SOP 14PIN (150mil BODY) OUTLINE DRAWING (SOL14-P-150 -1.27)

Unit in mm

