

## REFERENCES

- [1] J. S. Hall, "An Electroid Switching Model for Reversible Computer Architectures," in *Physics of Computation Workshop*. Dallas Texas: Citeseer, Oct 1992.
- [2] S. Younis and T. Knight, "Asymptotically Zero Energy Split-Level Charge Recovery Logic," in *Int. Wkshp. on Low Power Design*, 1994, pp. 177–182.
- [3] M. P. Frank, R. W. Brocato, B. D. Tierney, N. A. Missert, and A. H. Hsia, "Reversible Computing with Fast, Fully Static, Fully Adiabatic CMOS," in *2020 International Conference on Rebooting Computing (ICRC)*. IEEE, Piscataway, New Jersey, USA, 2020, pp. 1–8.
- [4] M. P. Frank, R. W. Brocato, T. M. Conte, A. H. Hsia, A. Jain, N. A. Missert, K. Shukla, and B. D. Tierney, "Special Session: Exploring the Ultimate Limits of Adiabatic Circuits," in *2020 IEEE 38th International Conference on Computer Design (ICCD)*. IEEE, Piscataway, New Jersey, USA, 2020, pp. 21–24.
- [5] J. E. Smith and G. S. Sohi, "The microarchitecture of superscalar processors," *Proceedings of the IEEE*, vol. 83, no. 12, pp. 1609–1624, 1995.
- [6] T.-Y. Yeh and Y. N. Patt, "Alternative implementations of two-level adaptive branch prediction," *ACM SIGARCH Computer Architecture News*, vol. 20, no. 2, pp. 124–134, 1992.
- [7] S. McFarling, "Combining branch predictors," Vol. 49. TN-36, Digital Western Research Laboratory, Tech. Rep., 1993.
- [8] T. Austin, D. Burger, M. Franklin, S. Breach, and K. Skadron. (1998) The simplescalar architectural research tool set, version 2.0. [Online]. Available: <https://pages.cs.wisc.edu/~mscalar/simplescalar.html>
- [9] M. P. Frank, B. Tierney, and R. Lewis, "Stretching the thermodynamic limits of hpc efficiency," 2023, <https://www.sandia.gov/news/publications/hpc-annual-reports/article/stretching-the-thermodynamic-limits-of-hpc-efficiency/> [Accessed: (05/27/2024)].
- [10] B. Hoefflinger, "ITRS: The International Technology Roadmap for Semiconductors," in *Chips 2020: a guide to the future of nanoelectronics*. Springer, 2011, pp. 161–174.
- [11] C. J. Vieri, "Reversible Computer Engineering and Architecture," Ph.D. dissertation, Massachusetts Institute of Technology, Dept. of Electrical Engineering and Computer Science, 1999.
- [12] M. P. Frank and T. F. Knight Jr, "Reversibility for efficient computing," Ph.D. dissertation, Massachusetts Institute of Technology, Dept. of Electrical Engineering and Computer Science, 1999.
- [13] R. Landauer, "Irreversibility and Heat Generation in the Computing Process," *IBM Journal of Research and Development*, vol. 5, no. 3, pp. 183–191, 1961.
- [14] C. H. Bennett, "Logical Reversibility of Computation," *IBM Journal of Research and Development*, vol. 17, no. 6, pp. 525–532, 1973.
- [15] E. F. Fredkin and T. Toffoli, "Design Principles for Achieving High-Performance Submicron Digital Technologies," in *Collision-based Computing*. Springer, Salmon Tower Building, New York, New York, USA, 2002, pp. 27–46.
- [16] C. H. Bennett, "The Thermodynamics of Computation—A Review," *International Journal of Theoretical Physics*, vol. 21, pp. 905–940, 1982.
- [17] C. H. Bennett and R. Landauer, "The Fundamental Physical Limits of Computation," *Scientific American*, vol. 253, no. 1, pp. 48–57, 1985.
- [18] C. H. Bennett, "Time/space Trade-offs for Reversible Computation," *SIAM Journal on Computing*, vol. 18, no. 4, pp. 766–776, 1989.
- [19] J. S. Hall, "A Reversible Instruction Set Architecture and Algorithms," in *Proceedings Workshop on Physics and Computation*. IEEE, Piscataway, New Jersey, USA, 1994, pp. 128–134.
- [20] C. J. Vieri, "Pendulum—A Reversible Computer Architecture," Ph.D. dissertation, Massachusetts Institute of Technology, Dept. of Electrical Engineering and Computer Science, 1995.
- [21] Y. Shen and M. Ferdman, "Temporal stream branch predictor," in *Championship Branch Prediction Program*, June 2014.
- [22] B. Gregg. (2024) MBP\_FARS. [Online]. Available: [https://github.com/greggbyr/MBP\\_FARS.git](https://github.com/greggbyr/MBP_FARS.git)