

# Benchtop linear power supply: design, construction and characterisation

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## Abstract

This document describes the design, simulation, construction and characterisation of a versatile general purpose benchtop linear power supply. Functionality is greatly enhanced by the incorporation of current limiting and the digital control of the supply parameters and, therefore, feature in the design. This is work in progress, results are documented as they are obtained.

## LPS features, characteristics and design goals

### Power supply features

Although a power supply can be considered as performing a single function; provide an appropriate and constant voltage to a load irrespective of any time dependent current requirements, additional features greatly increase its versatility. A general purpose benchtop power supply must have two supplies at a minimum to allow for the powering of split-rail analog circuits. The addition of a third, lower voltage supply is useful for powering mixed analog and digital circuits. Current limiting is indispensable for R&D purposes to minimise circuit destruction under fault conditions. A constant current mode has many applications beyond circuit protection. Digitally controlling and monitoring the power supply voltage, load current and current limit enhances its functionality. For example, microcontroller routines can be written for battery charging applications or circuit and component I-V characterisation.

The upper supply voltage and current capability must be chosen. Increasing the voltage and current capability extends the usability of the supply, all-be-it with diminishing returns. However, an increase of the voltage capability comes with increasing thermal dissipation management and transformer size costs. An upper voltage of about 35 V and a continuous current capability of 4 A are tentatively chosen. A list of the chosen power supply features include:

- Two independent and electrically isolated voltage adjustable channels with a 35V and 4A capability.
- A third adjustable lower-voltage channel intended for the powering of digital circuits, also electrically isolated.
- Analog constant current and digital shutdown protection modes on all channels.
- Digital control of the voltage and current limit.
- Load current and voltage readout.
- Computer USB interface for data logging.

A single user interface board shall communicate with the 3 power boards and handle all user interface and data logging tasks. A description of the third, lower voltage supply is given after that of the main supplies.

### LPS analog characteristics

All power supplies exhibit nonideal behaviour. The following are commonly specified to describe power supply quality,

- Noise and ripple
- Load regulation
- Transient response

## Noise

Power supply noise may adversely influence the performance characteristics of some circuit classes and must be explicitly considered. Two types of noise are present on the output of a power supply; wideband and ripple. Wideband noise is the result of fundamental physical mechanisms such as resistor thermal noise and can be minimised, but not eliminated. A number of mechanisms may contribute to output ripple including a poor PCB layout. Certainly, output voltage ripple will occur due to a combination of input ripple along with the pass transistor early voltage and the finite loop gain at the ripple frequency. Integrated over the frequency band 10 Hz-100 kHz a total output noise voltage of 50  $\mu$ V<sub>RMS</sub> is a low noise figure for a linear power supply and is chosen as the maximum specification limit.

## Load regulation

Load regulation indicates the degree of dependence that the output voltage has on the static load current and is defined by the equation,

$$\% \text{ Load regulation} = 100\% \frac{\Delta V_{\text{out}}}{V_{\text{out}}} \frac{I_{\text{max}}}{\Delta I_{\text{load}}} \quad (1)$$

Load regulation is dependence on the DC loop gain and is likely to be insignificant.

## Transient response

Sudden changes in load current result in transient fluctuations of the supply voltage. When designing a power supply great attention must be given to its transient behaviour. Transient behaviour indicates the degree of stability of the power supply, which must be ensured for all expected load conditions. In addition, excessive ringing of the output voltage in response to sudden changes of load current can be considered as load induced noise.

## Current limit response time

The response time of the current limit should be sufficiently short to minimise circuit destruction. However, the supply output capacitance will limit the effectiveness of a fast response due to the stored charge.

## Power board analog design

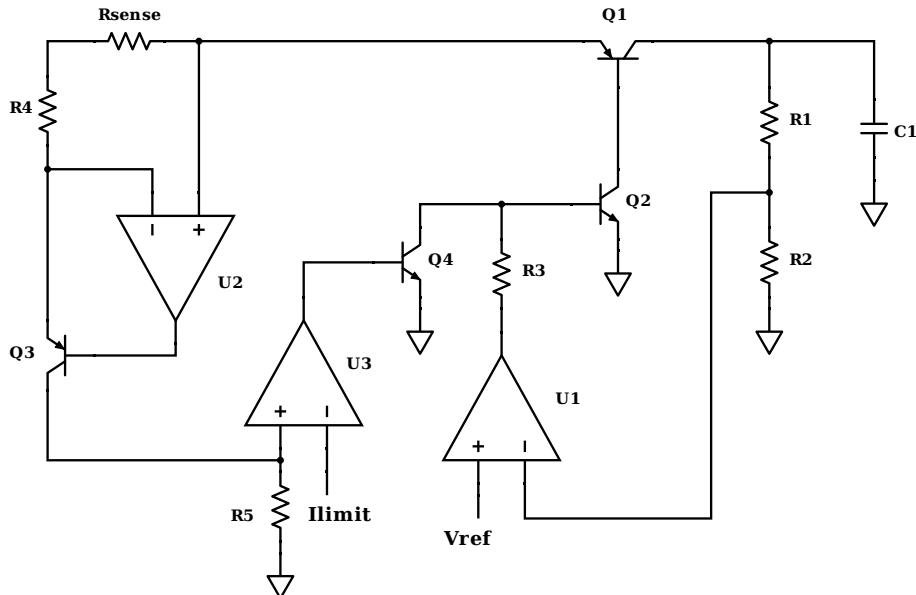


Figure 1: Simplified topology of the constant voltage and constant current control loops.

The simplified proposed topology of the constant voltage (CV) and constant current (CC) control loops is shown in figure 1. Opamps are an ideal choice for central use in the control loops since low cost and high performance options are available.

## Opamp requirements

Given the topology some approximate opamp specification requirements can now be determined.

### Noise

The wideband output voltage noise of the CV loop is ultimately limited by the input noise of the opamp, U1 (of figure 1). Reference voltage noise and thermal noise of the feedback resistors (R1 and R2) also contribute to the voltage noise. Reference voltage noise can be filtered, although, filtering low-frequency noise might be cumbersome. Within the frequency band 10 Hz-100 kHz a total output noise voltage of  $50 \mu V_{\text{RMS}}$  is a low noise figure for a linear power supply and is chosen as the maximum specification limit. If noise is dominated by the opamp voltage noise its density,  $e_n$ , must be less than,

$$e_n(U1) < \frac{50 \mu V}{\sqrt{10^5 - 10}} \frac{R2}{R1 + R2} = \frac{R2}{R1 + R2} \times 158 nV_{\text{RMS}}/\sqrt{\text{Hz}} \quad (2)$$

Feedback resistance (R1 and R2) will contribute to the output noise by the inherent thermal noise of the resistors and through opamp noise current which ultimately must be considered.

The output current noise of the constant current loop is limited by the input voltage noise of U2 and U3. The magnitude of the noise contribution from U2 is inversely proportional to the resistance of  $R_{\text{sense}}$ ,

$$I_{\text{noise}} = \frac{e_n(U2)}{R_{\text{sense}}} \quad (3)$$

The contribution of U3 to the current noise of the constant current loop is given by,

$$e_n(U3) \frac{I_{\text{max}}}{V_{-\text{max}}} \quad (4)$$

where  $I_{\text{max}}$  is the maximum constant current, and  $V_{-\text{max}}$  is the voltage on the inverting input of U3 that corresponds to the maximum current. It is likely that Eq. 3 will be greater than Eq. 4 since  $R_{\text{sense}}$  must be significantly smaller than  $1\Omega$ .

### Transient response

The transient behaviour (and associated stability) of the CV loop in response to sudden changes of load current is determined by the loop gain and phase as a function of frequency. A necessary condition for stability is a loop gain of less than unity at frequencies where the phase delay is 360 degrees. Output capacitance (C1) is required for high-frequency stability. C1 results in a decreasing loop gain with increasing frequency. The equivalent series resistance of C1 also has a critical impact upon circuit stability, at higher frequencies ESR makes C1 appear resistive and therefore improves the phase margin. Ultimately, the response time of the CV loop is limited by the bandwidth of the pass transistor, Q1. Therefore, it appears that there is little advantage to using a very high-speed opamp for U1. On the other hand, U2 can be of relatively high speed such that the U2, Q3 and R4 combination form a tight local feedback loop with little phase delay with respect to the entire CC feedback loop. Ideally U2 has an input common mode range that includes its positive supply voltage, otherwise an additional supply voltage greater than  $V_{\text{in}}$  is required.

Opamp, U3, requires the smallest bandwidth since the CC loop does not have a mechanism to reduce loop gain with frequency that is equivalent to C1 of the CV loop.

## SPICE simulations

The schematic of the constant voltage analog section of the linear power supply as simulated using LTspice is shown in figure 2. After running many simulations and considering the circuit dynamics the LT6233 opamp has been chosen. The LT6233 has a very low voltage noise, a gain-bandwidth product that is sufficient for a fast transient response and a phase delay that allows for good stability. To capture some of the realistic characteristics of the output capacitance a SPICE model of a  $100 \mu F$  Rubycon aluminium polymer capacitor (50PZF100M10X9) was incorporated into the simulations. Inductances have also been included to represent pass transistor wiring.

## Circuit description

The CV control loop is a negative feedback circuit and its dynamic behaviour can be understood in terms of the loop gain,  $A(s)$ , and phase delay,  $\phi(s)$ , as a function of frequency. A necessary condition for stability is a loop gain of less than unity at the frequencies where the phase delay is 360 degrees. An understanding of the behaviour of the CV loop is aided by small signal transfer function calculations of the transistor network shown in Fig. 3, the results of which are shown in Fig. 4.

## Constant voltage loop

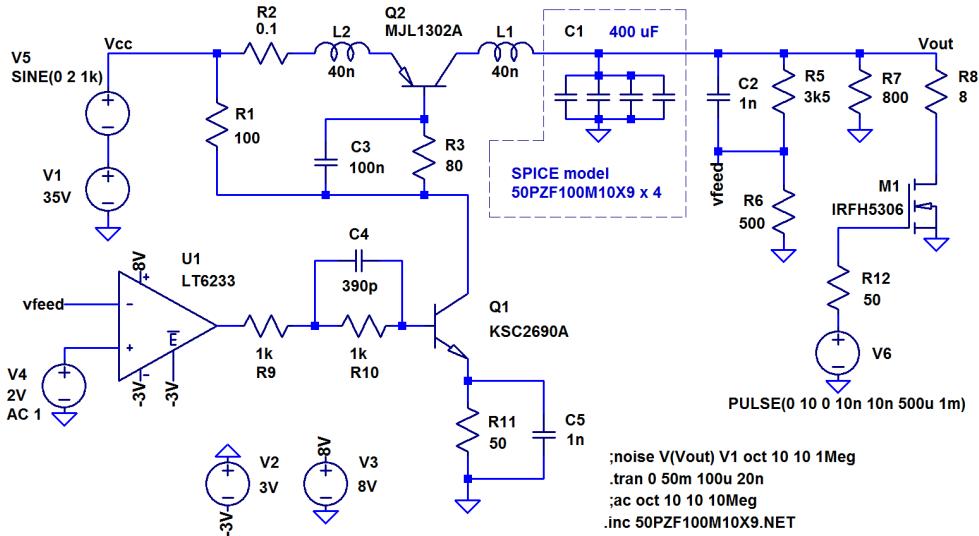


Figure 2: Schematic diagram of the constant voltage control loop as simulated by LTspice.

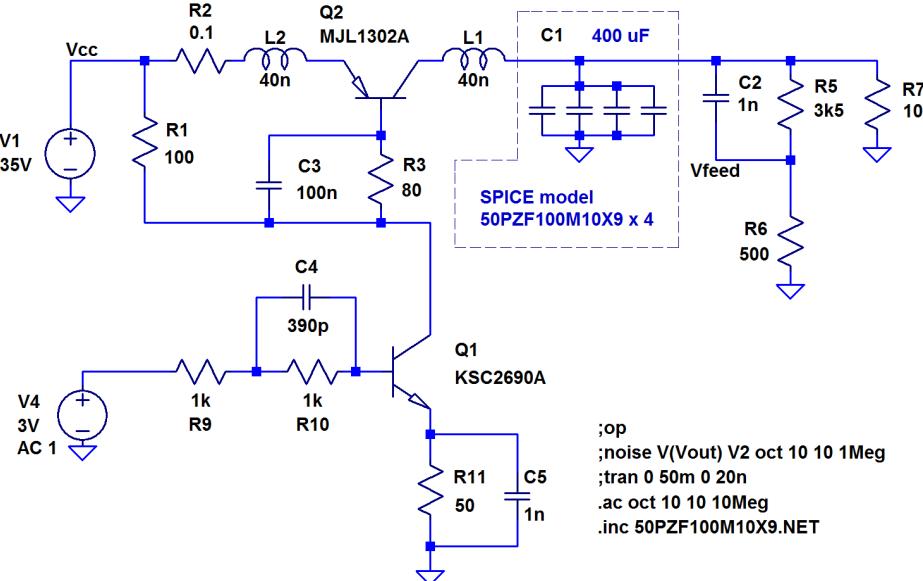


Figure 3: Schematic diagram of the transistor network as simulated by LTspice.

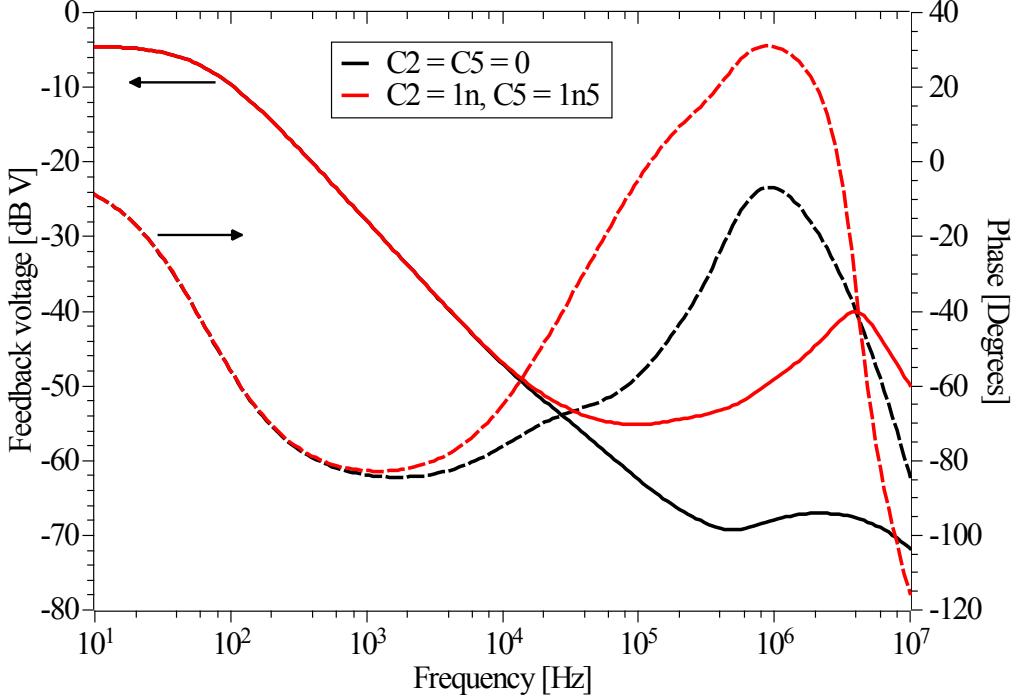


Figure 4: Small signal AC transfer function of the transistor network of the schematic shown in Fig. 3. V4 is the small signal input and Vfeed is the output.

At low frequencies the phase delay of the transistor network is minimal because the resistive load, R7, and output capacitance, C1, combination appears resistive. The phase then begins to decrease towards  $-90^\circ$  as the output appears capacitive. At frequencies greater than 2 kHz the phase increases as the ESR and ESL of the output capacitors make the output appear resistive once again. For frequencies greater than about 1 MHz the phase decreases again due to the bandwidth limits of Q1 and Q2. C2 and C5 play the most critical role, they provide a phase lead around the 5 kHz to 50 kHz band, without which, the additional phase delay of the LT6233 opamp results in a marginal phase margin and ringing of the pass transistor in response to sudden changes in load current. The phase delay of the opamp at the lower frequencies where the phase delay of the transistor network approaches  $90^\circ$  clearly has a critical impact upon circuit stability. The LT6233 opamp has a phase delay sufficiently less than  $90^\circ$  within this critical frequency band. A higher-frequency oscillation may result if the loop gain does not decrease sufficiently for frequencies greater than a few MHz. Circuit simulations suggest that there are no high-frequency oscillations, however, if the actual circuit displays high-frequency instabilities then C5 can be removed since it has a strong impact upon loop gain at high-frequency, but only makes a small contribution to the low-frequency stability. Figure 6 is a plot of the calculated pass transistor collector current in response to a step change of the load current for the optimised component values as shown in Fig. 2 and for  $C_2 = 100 \text{ pF}$ . The importance of the phase lead created by C2 is evident. The possible influence of an input voltage ripple was simulated by adding a  $4 \text{ V}_{p-p}$  1 kHz sinewave (V5) to the 35 V input source (V1). The output voltage ripple was  $25 \mu\text{V}_{p-p}$  for a load current of 1 A and negligible for a load current of 10 mA.

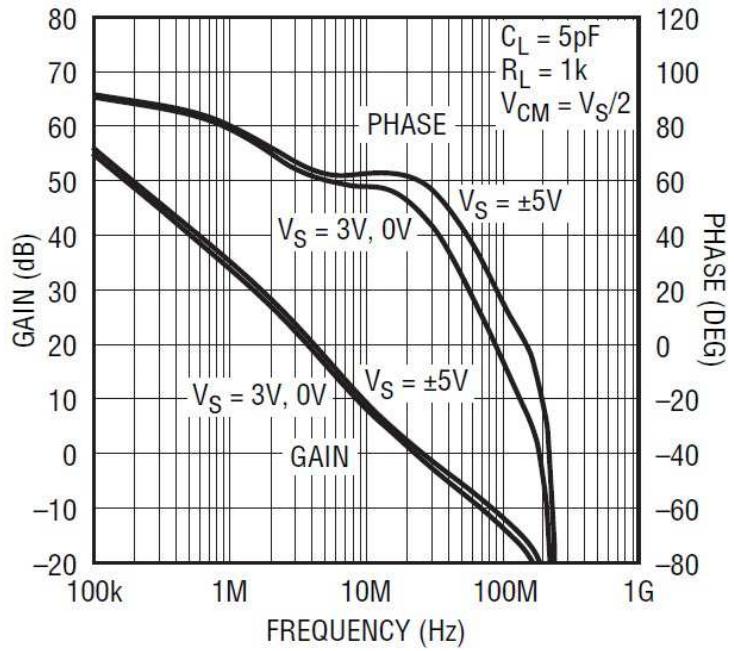


Figure 5: Open-loop gain and phase of the LT6233 opamp.

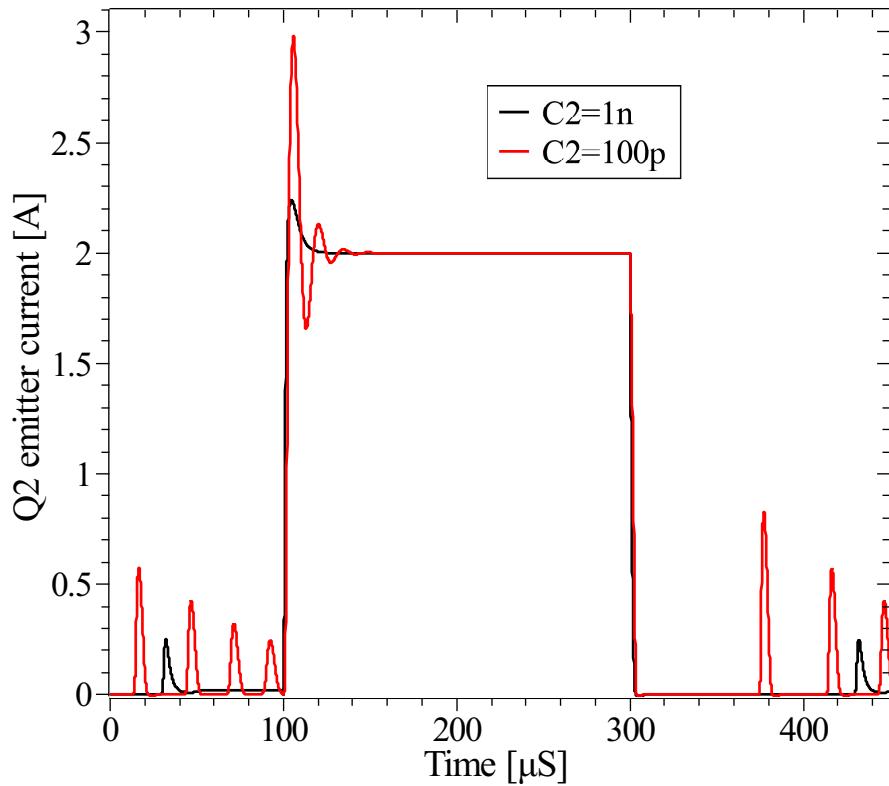


Figure 6: Simulated constant voltage loop response to a step increase of load current from 20 mA to 2 A.

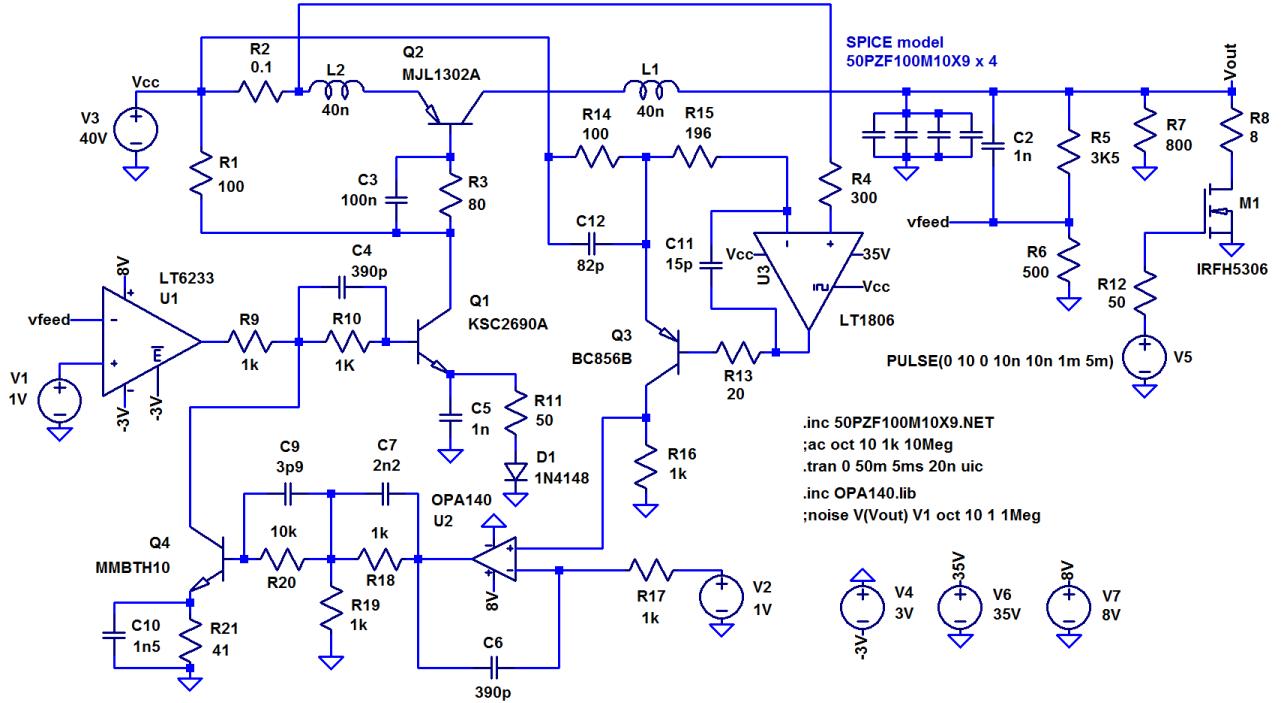


Figure 7: Schematic diagram of the CV and CC control loops as simulated by LTspice.

The full simulation schematic of the combined CV and CC control loops is shown in Fig. 7. Although the CC and CV loops share circuitry the CC loop is compatible with optimal CV loop component values, or thereabouts. The LT1806 opamp senses the voltage across R2 and together with R14, R16 and Q2 produces a voltage across R16 in proportion to the emitter current of Q2,  $V_{R16} = I_{E,Q2}$ . LT1806 has a relatively large gain-bandwidth product of about 325 MHz such that the voltage across R16 has little phase delay in response to the emitter current of Q2 at the frequencies of importance to the entire CC feedback loop. C12 produces a phase lead to assist in stability of the loop, while C11 ensures high-frequency stability of the LT1806 opamp. The OPA140 opamp compares the voltage across R16 to the current limit setting voltage. When  $V_{R16}$  becomes greater than the current limiting voltage the MMBTH10 transistor starts to conduct and draw current away from the base of Q1. C7, C9 and C10 provide a phase-lead. R17 and C6 reduces the loop gain at higher frequencies. The net effect is a loop gain of less than unity at the frequencies where the phase delay is greater than  $360^\circ$ . The OPA140 opamp has an important property: There are no protection diodes connected between the inputs and large differential voltages are permissible without input current draw. This property is important since it permits a large current limit setting voltage to be present on the inverting input of U2 without interfering with the voltage across R16. Fig. 8 displays the response of the CC circuit to a step increase of load current with current limiting set to 0.5 A. The time taken to limit current is  $2 \mu\text{s}$  with a settling time of about  $15 \mu\text{s}$ .

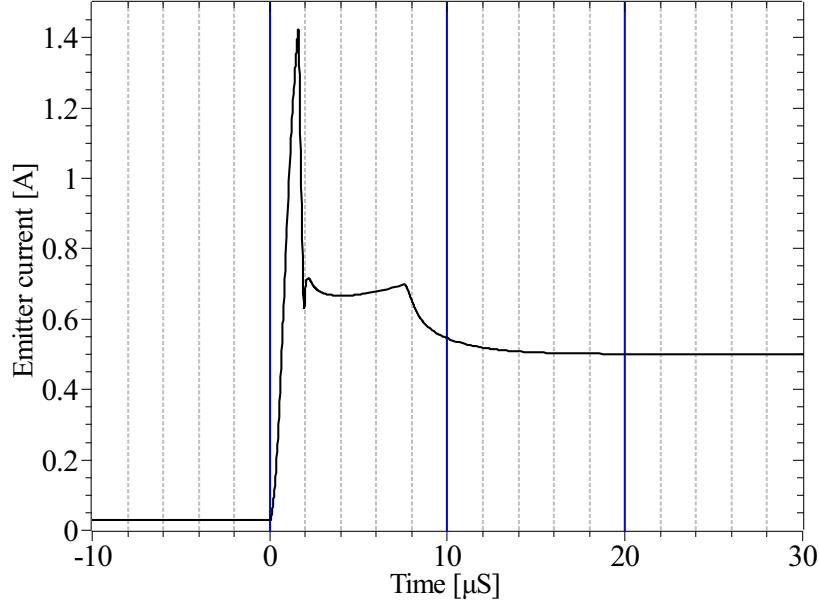


Figure 8: Simulated constant current loop response to a step increase of load current.

## Analog prototype board

The analog sections of the power board were prototyped and characterised. The prototype schematic diagram and PCB layout are shown in figures 10 - 12. The prototype schematic closely matches the SPICE simulation circuit, with the addition of opamp and reference voltage power circuitry. The prototype board was populated and characterised with the component values as shown in the schematic diagram. Careful consideration has (and must) be given to the PCB layout in order for the circuit to behave as intended. A substandard layout will degrade performance from optimal. The PCB layout can have an impact upon the following LPS characteristics in particular,

- Voltage regulation
- Ripple
- Excessive transient ringing / stability issues

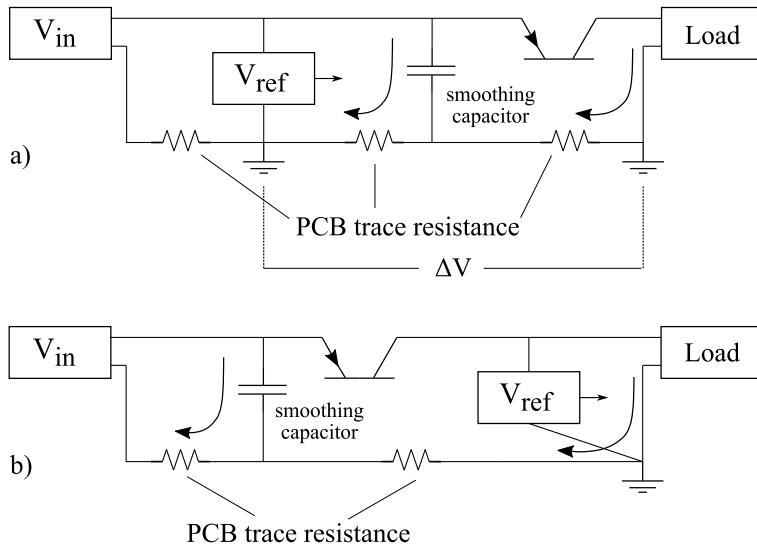


Figure 9: Diagram of a) poor PCB layout resulting in excess ripple due to current loops and b) the strategy used to minimise excess ripple.

Ground current loops can result in ripple and degraded voltage regulation as demonstrated in Fig. 9. Fortunately, the effects of ground current loops are easily minimised by following two strategies. All large currents, namely those associated with the input, filtering capacitors and the output load are isolated from the control loops. In addition, the point at which the control loops derive their ground potential is taken at the output connector. Optimising the PCB layout in regards to transient response is a little bit more complicated. Consideration must be given to the effects of PCB parasitic capacitance, capacitive coupling and electromagnetic coupling. Parasitic capacitance can degrade phase margin and therefore stability and capacitive and magnetic coupling can result in unintentional feedback which can lead to stability issues. Minimising the size of large current loops and providing a good ground plane for the sensitive analog sections can be very effective at reducing the effects of electromagnetic coupling.

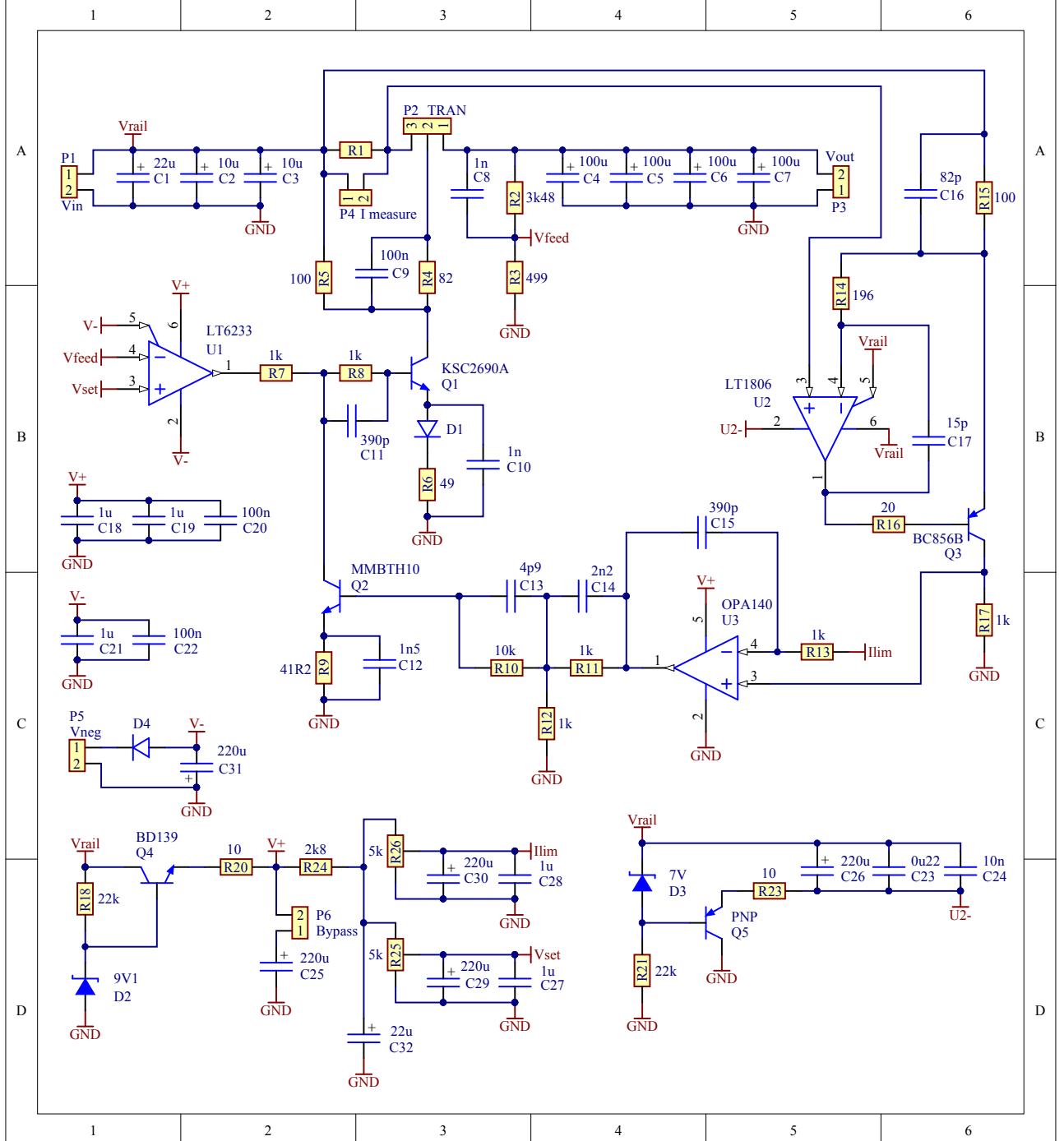


Figure 10: Schematic diagram of the analog prototype board.

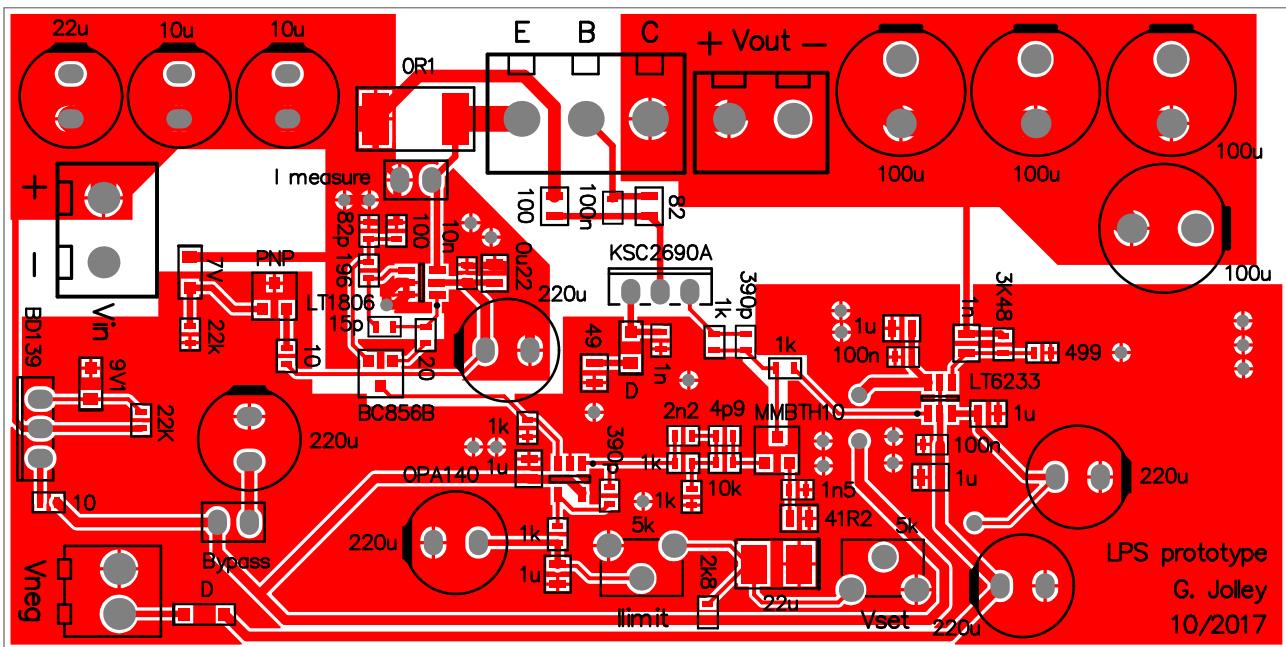


Figure 11: PCB top copper layer of the analog prototype board.

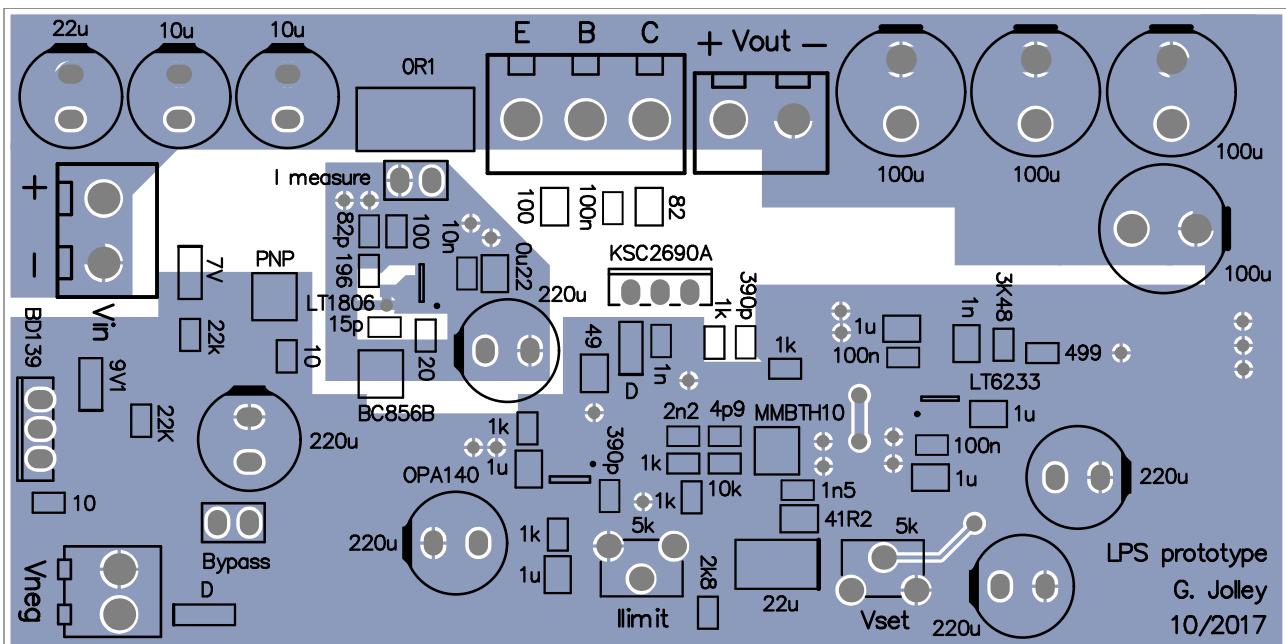


Figure 12: PCB bottom copper layer of the analog prototype board.

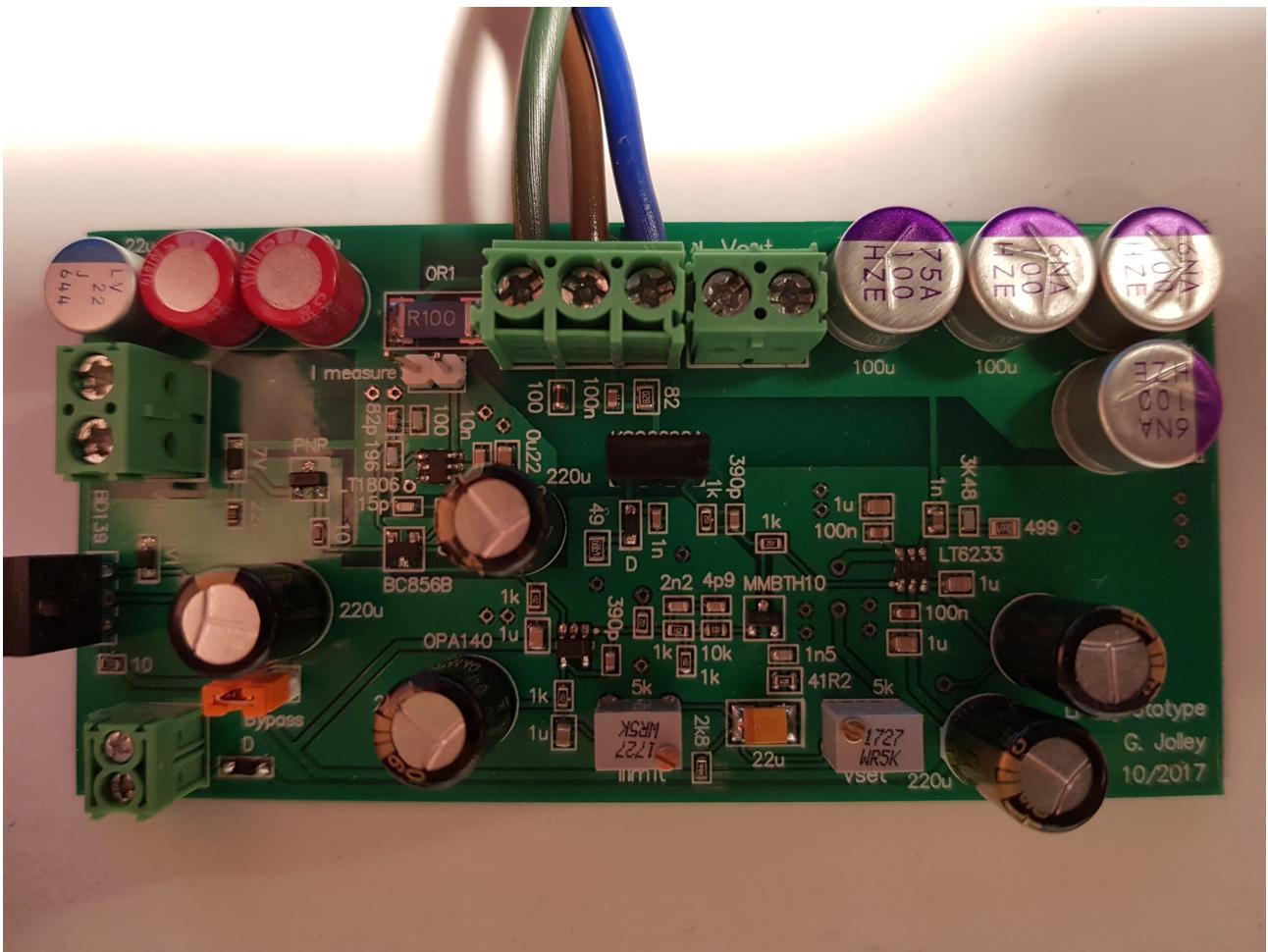


Figure 13: Constructed prototype board.

## Prototype baord characterisation

### Transient response

To measure the transient response of the CV mode to a rapidly changing load current a circuit switching a  $10\ \Omega$  load resistor by MOSFET with rise and fall times of the order of  $20\text{ nS}$  was placed across the output. The pass transistor emitter current was captured by an oscilloscope measuring the voltage across the  $0.1\ \Omega$  sense resistor. The measured transient response agrees well with simulation showing a rise time of about  $2\ \mu\text{s}$ , an overshoot of 15% and no ringing. In a similar manner the response of the CC loop was obtained. The current limit was set to  $0.5\text{ A}$  and a resistive load was switched on and off, results shown in figure 15. Initially, in response to the sudden load increase, the pass transistor current overshoots to  $0.74\text{ A}$  due a the time delay associated with the CC mode circuit. The response of the CC loop is rapid with a current overshoot lasting only  $6\ \mu\text{s}$ .

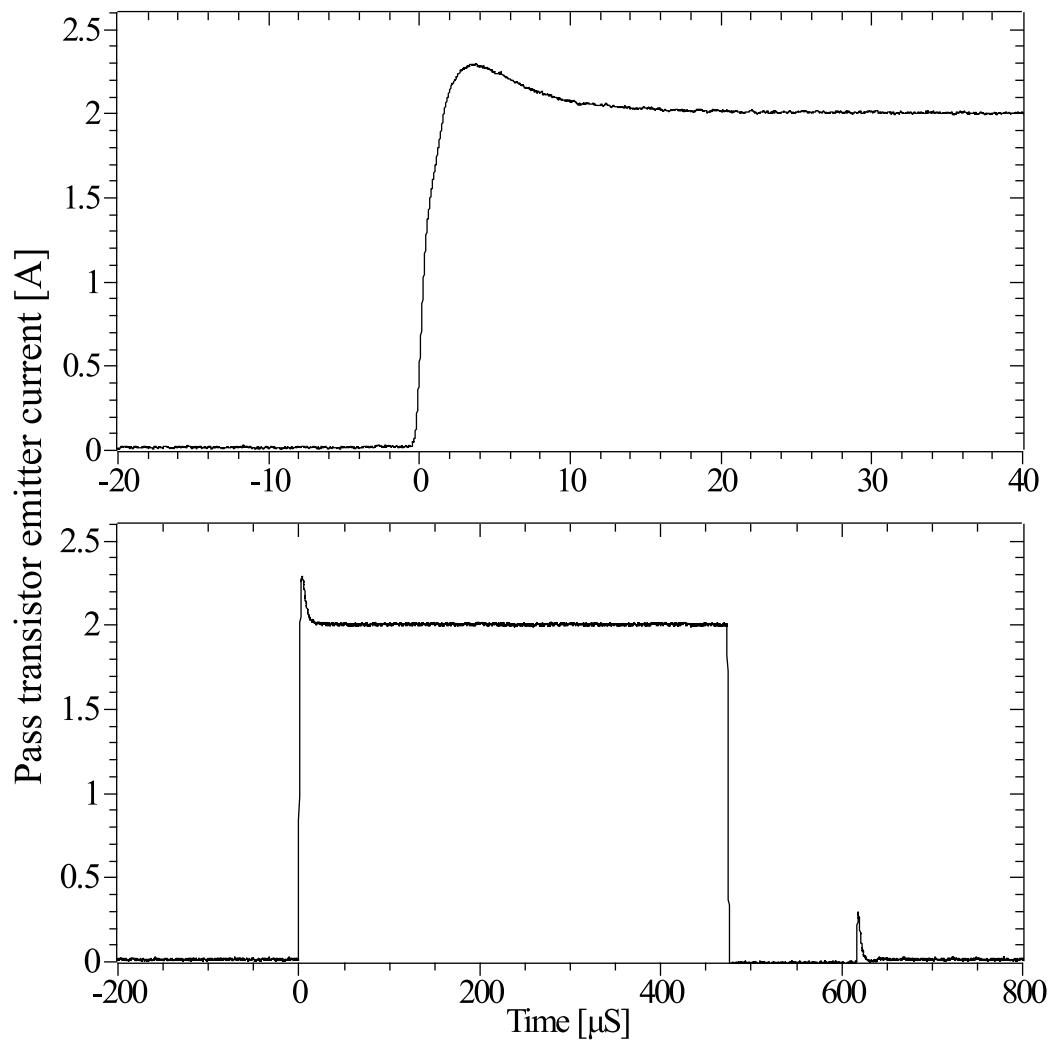


Figure 14: Measured constant voltage loop response to a step increase of load current from 20 mA to 2 A.

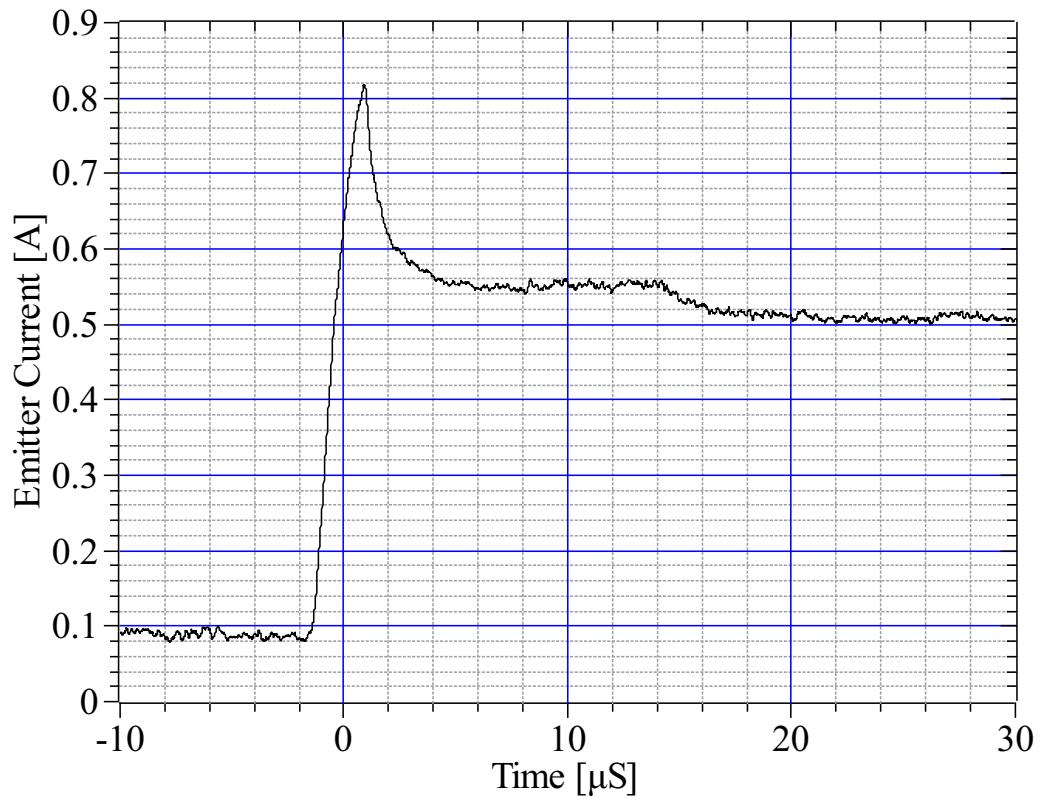


Figure 15: Measured constant current loop response to a step increase of load current.

## Noise

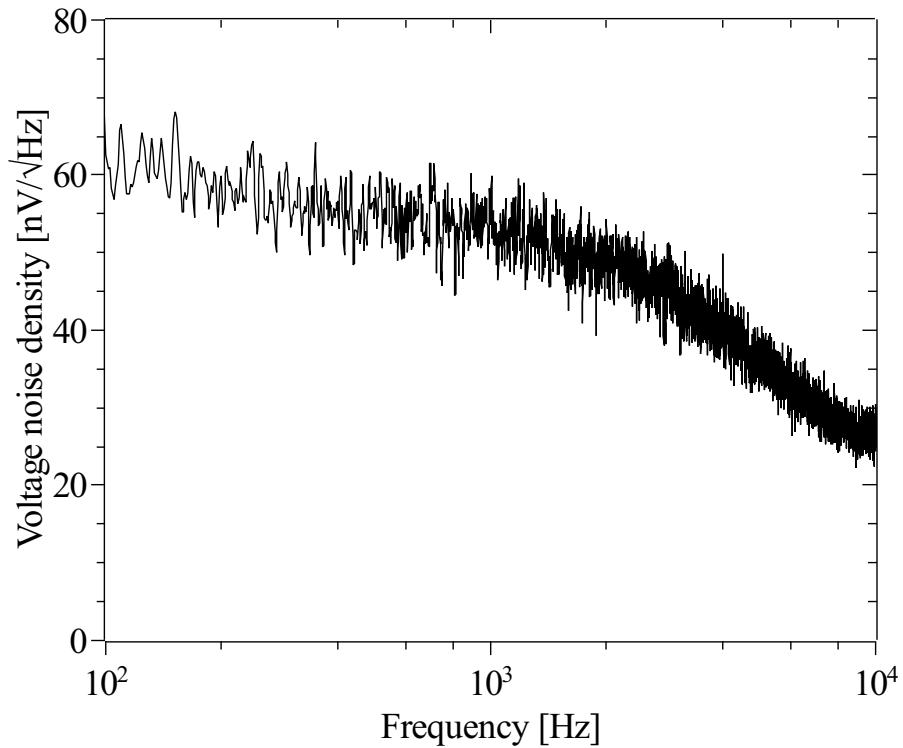


Figure 16: Output voltage noise spectrum.

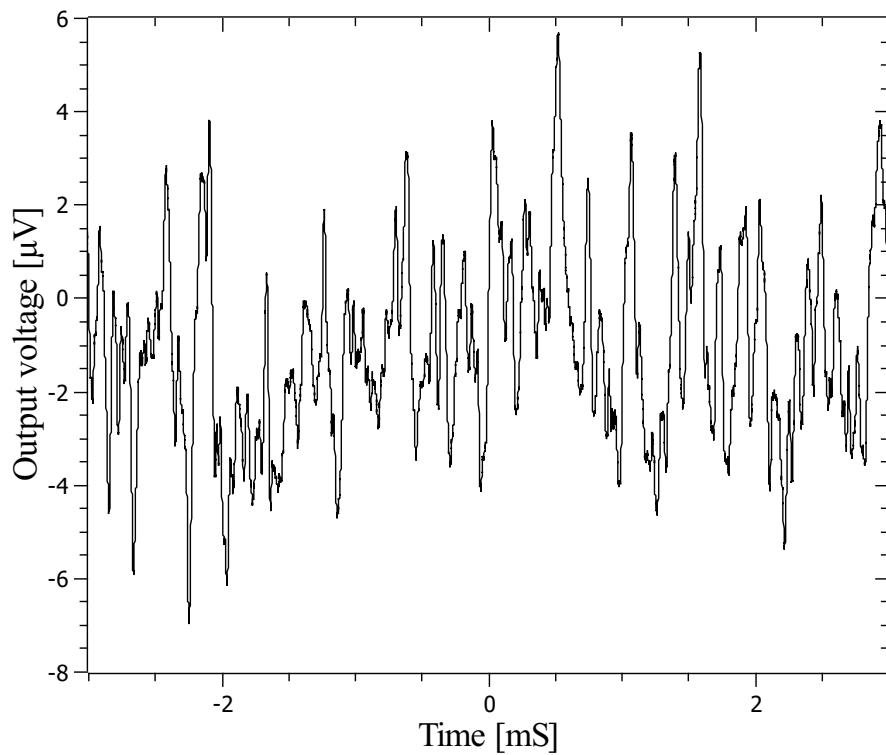


Figure 17: Output voltage noise within the 10-10 kHz band.

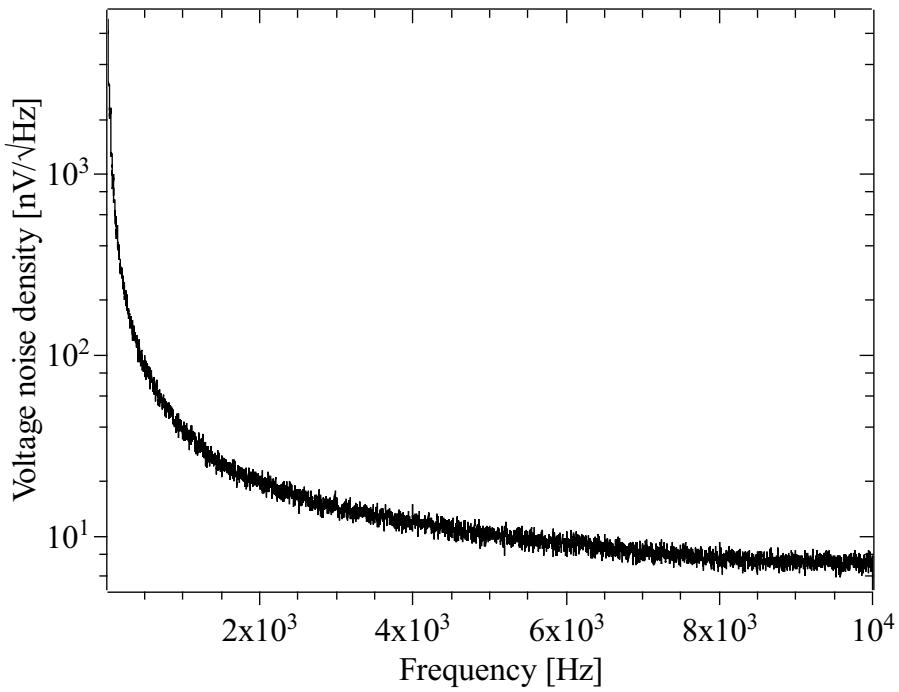


Figure 18: Output voltage noise spectrum within the 10-10 kHz band under constant current mode.

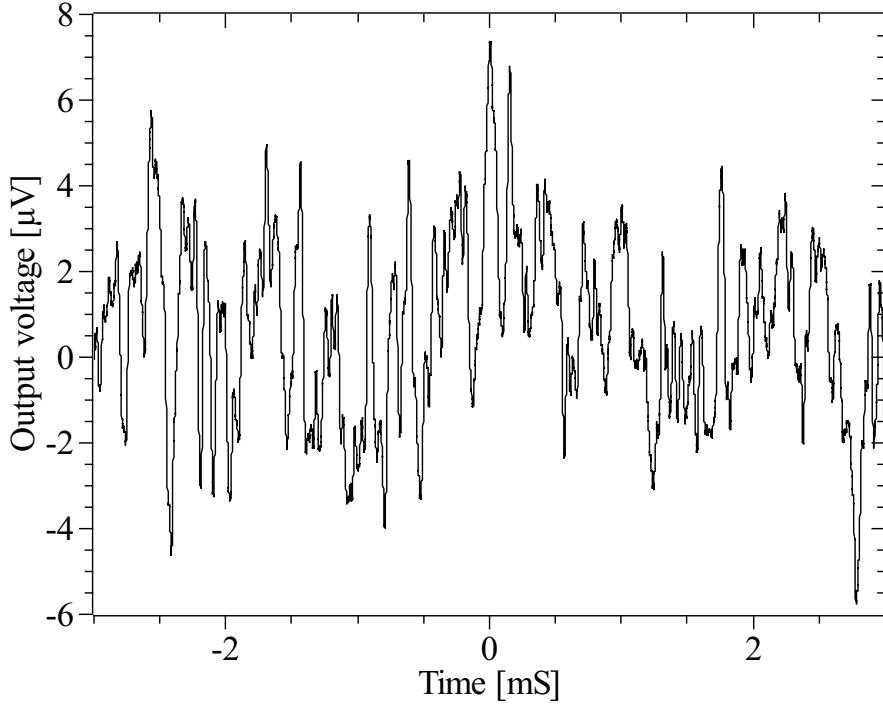


Figure 19: Output voltage noise within the 10-10 kHz band under constant current mode.

Those sources which significantly contribute to the output voltage noise are well known and the magnitude of the noise is easily calculated. In CV mode the noise sources are:

- The voltage and current input referred noise of opamp U1
- The thermal noise of feedback resistors R2 and R3 and potentiometer R25

Noise sources within the feedback loop have minimal impact upon the output noise since the negative feedback loop minimises their influence. Referring to figure 10, the output voltage noise density at frequencies greater than about 1 kHz, such that R25 has little effect and the LT6233 is within its flat band noise region is calculated to be,

$$\frac{R_2 + R_3}{R_3} \left[ e_n^2 + I_n^2 \left( \frac{R_2 R_3}{R_2 + R_3} \right)^2 + 4k_B T \frac{R_2 R_3}{R_2 + R_3} \right]^{1/2} \quad (5)$$

$$8 \left[ (1.9 \times 10^{-9})^2 + (7.8 \times 10^{-13} \times 438)^2 + 438 \times 4 \times 1.38 \times 10^{-23} \times 300 \right]^{1/2} \text{ V}/\sqrt{\text{Hz}} \quad (6)$$

$$= 26.5 \text{ nV}/\sqrt{\text{Hz}} \quad (7)$$

This value is very much less than the upper specification limit of  $158 \text{ nV}/\sqrt{\text{Hz}}$ . The voltage and current noise of the LT6233 opamp increases for frequencies less than 1 kHz and 100 Hz respectively.

### Spectrum analysis result

The power supply noise within the 20 - 10 kHz band was measured by connecting the output up to a low-noise amplifier with a gain of 80 dB. Output noise of the CV mode was captured in the frequency and time-domain, the results of which are shown in figures 16 and 17. This result can be compared with the LTspice result shown in figure 20. There is very good agreement between the calculated, and simulated noise values. However, the measured noise spectrum is a little larger than expected for frequencies less than about 5 kHz.

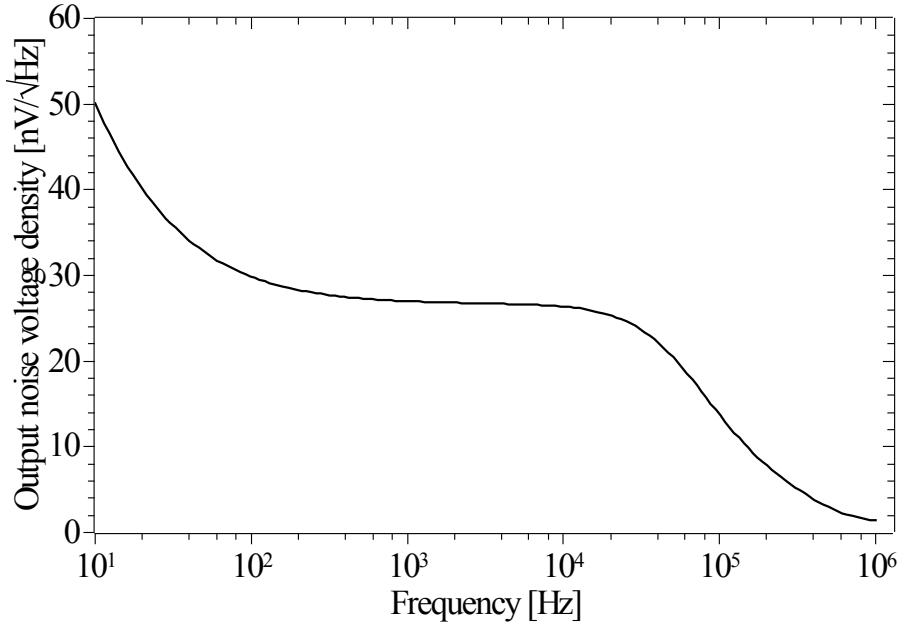


Figure 20: Simulated output voltage noise spectrum of the CV loop.

## Digital control and final schematics

The digital control aspects of the LPS power board are summarised as follows,

- DACs set the output voltage and current limit
- ADCs read the output voltage and load current
- A microcontroller communicates with the DACs, ADCs and control board

The schematic diagrams of the complete power board are shown in figures 21-23 and the PCB layout is shown in figures 24 and 25. Figure 21 displays the main CV and CC circuitry which closely follows the prototype board aside from some additional features including,

- Split-rail input voltage and associated switching circuitry
- Over current digital shutdown

The split-rail input reduces the thermal dissipation of the pass transistor by only switching to the higher rail voltage for higher output voltages. Polymer electrolytic capacitors C5-C7 provide a low impedance at higher frequency with the intention of minimising the size of the current loop between the power supply input and output. The voltage across R10 which is in proportion to the pass transistor emitter current is buffered by U4 and low-pass filtered by a selectable RC time constant. The filtered signal is applied to the non-inverting input of comparator U5 which drives a latch to shutdown transistor Q5 under load current fault conditions.

A MAX6126 provides a 4.096 V reference which is noise filtered and applied to the DACs and ADCs. The DACs (LTC2641) have an unbuffered output and are chosen for their low output voltage noise. However, the DAC output is noise filtered since it's noise specification is several times larger than opamps U1 and U3.

## Final Characterisation

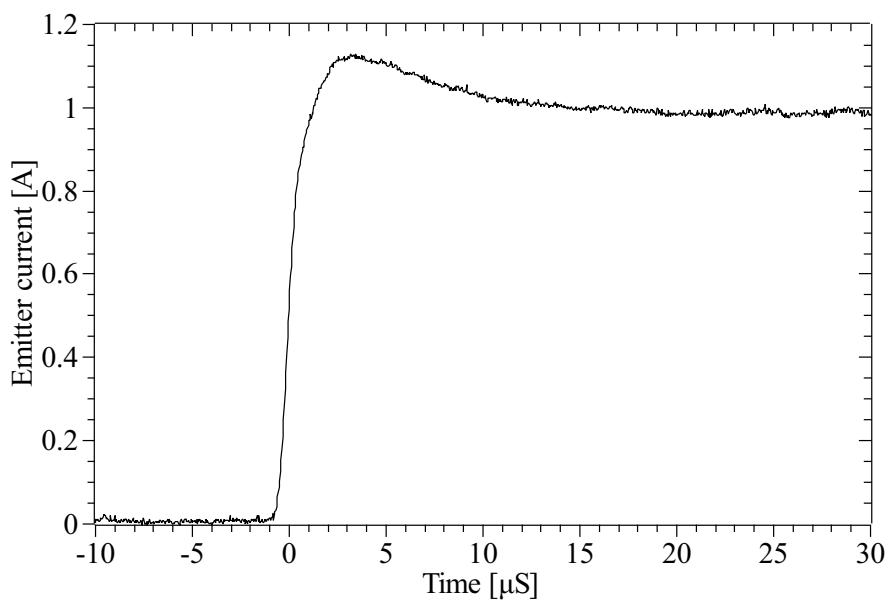


Figure 26: Final CV characterisation.

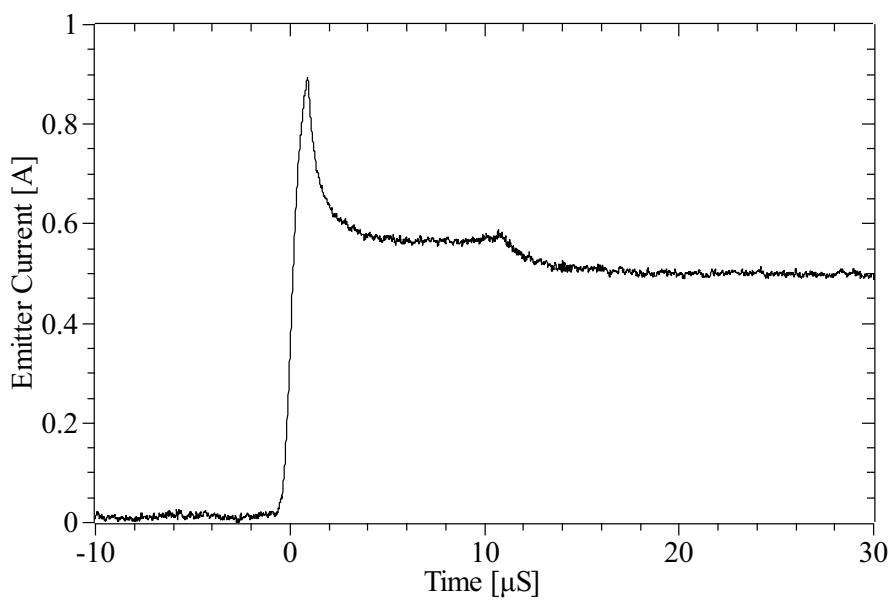
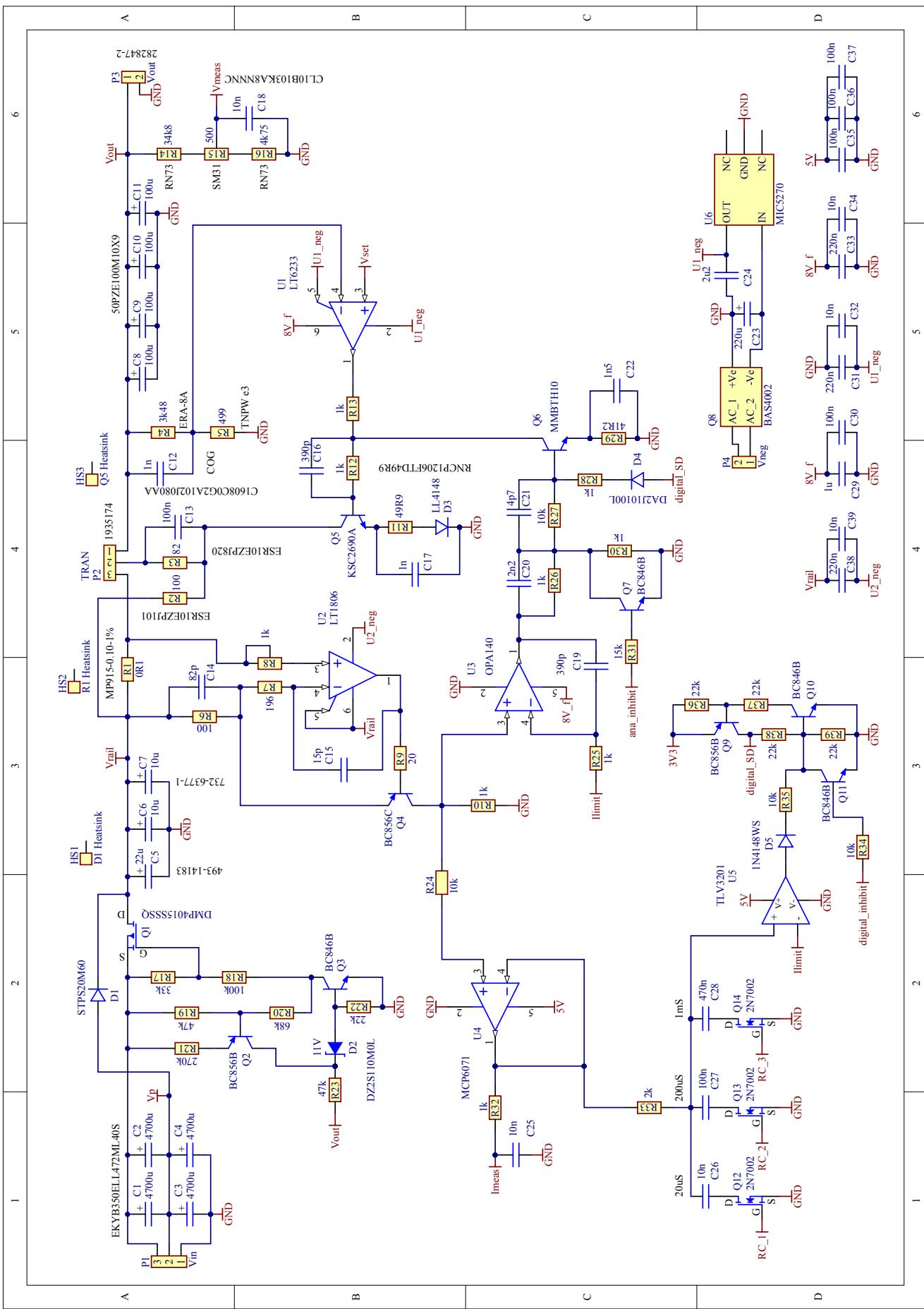


Figure 27: Final CC characterisation.

Figure 21: Power



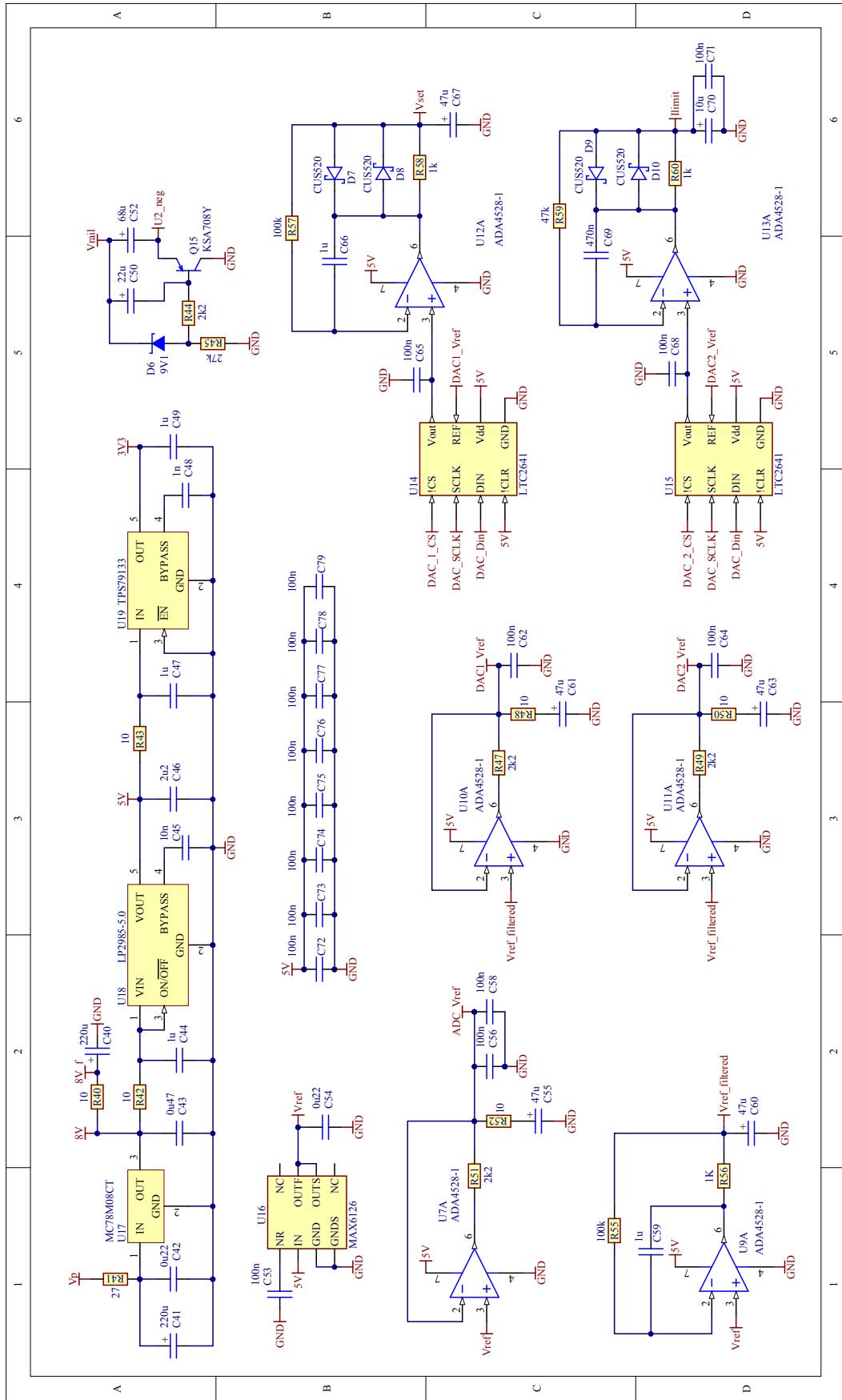


Figure 22: Power

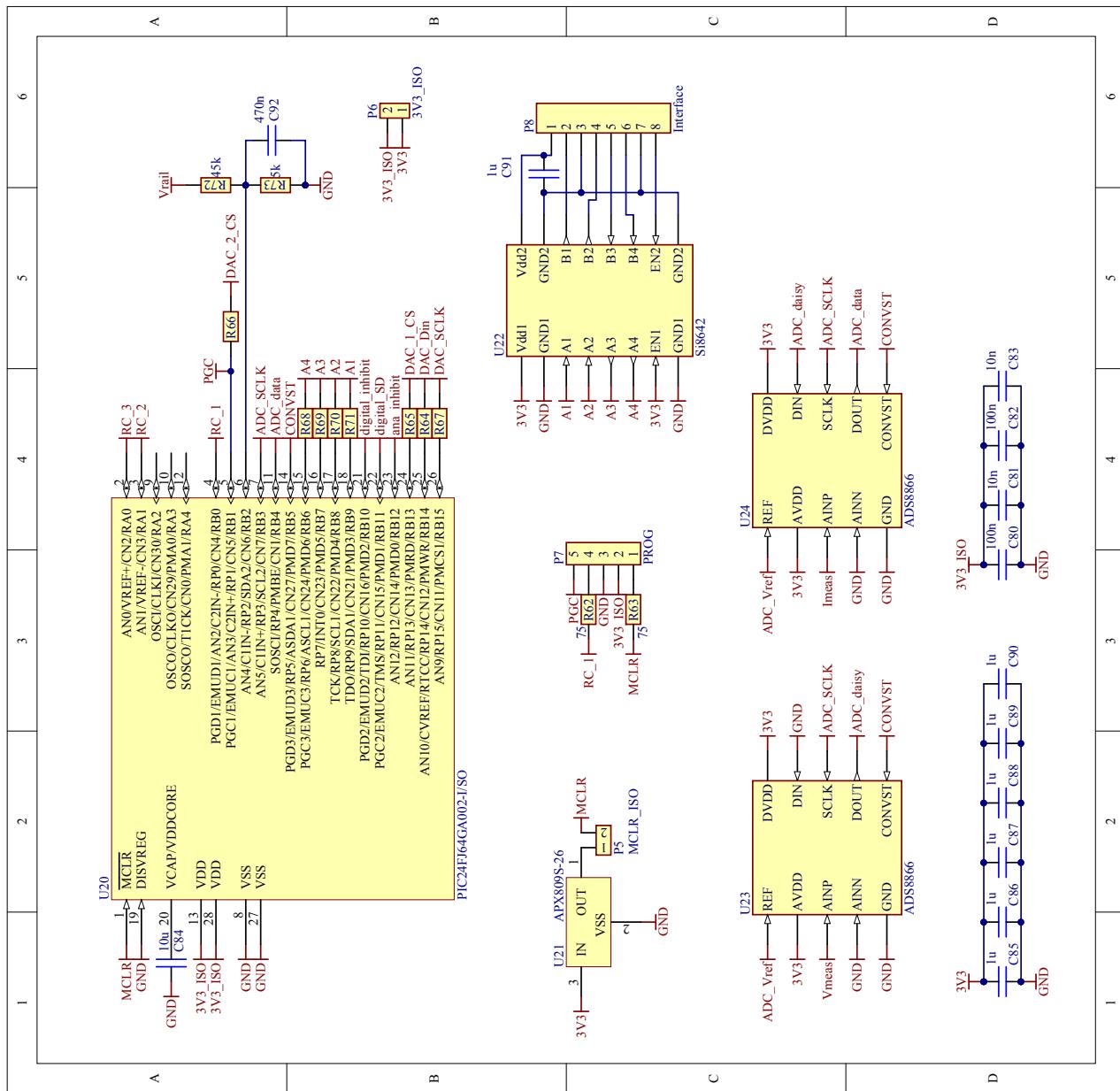


Figure 23: Power

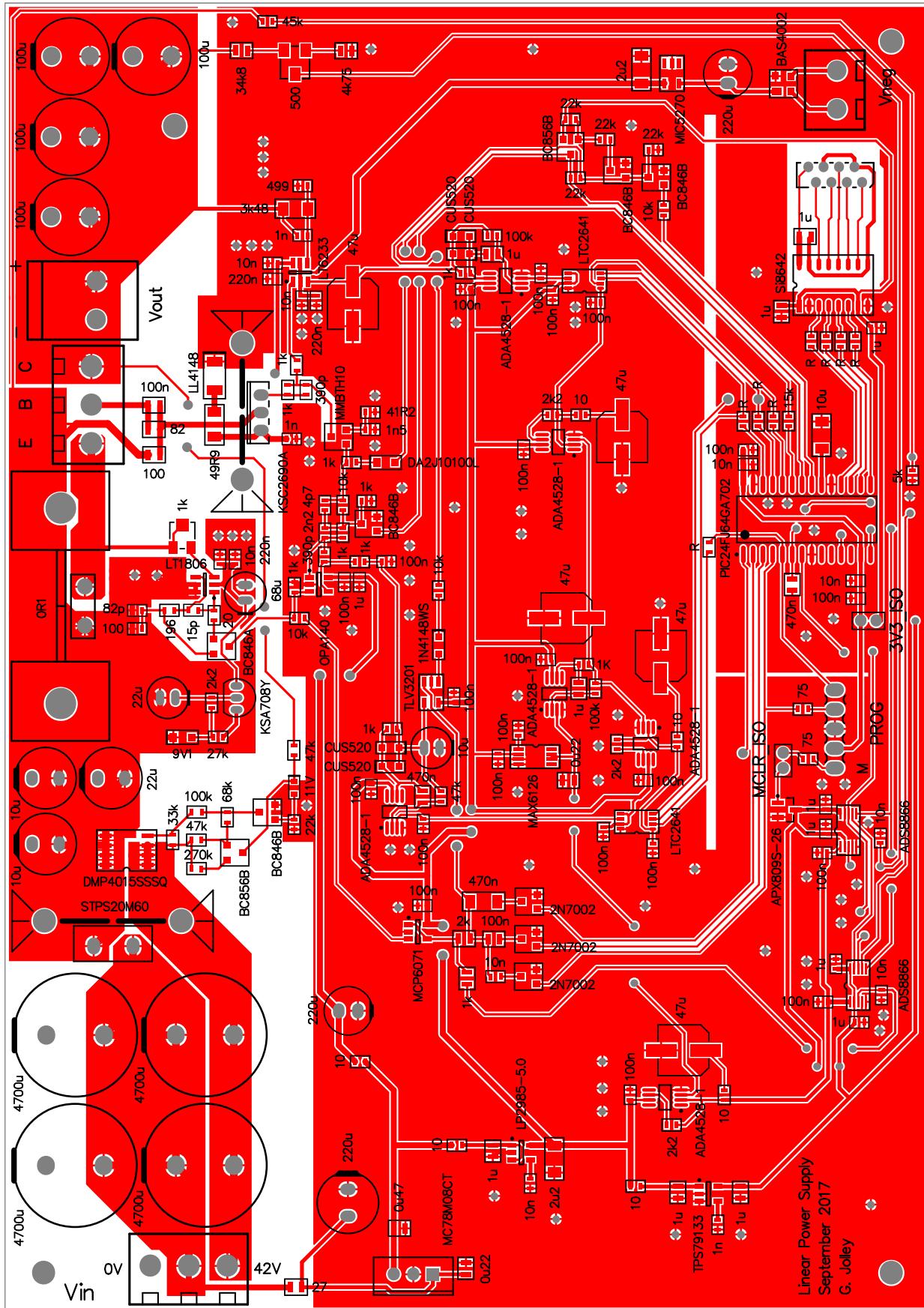


Figure 24: Power

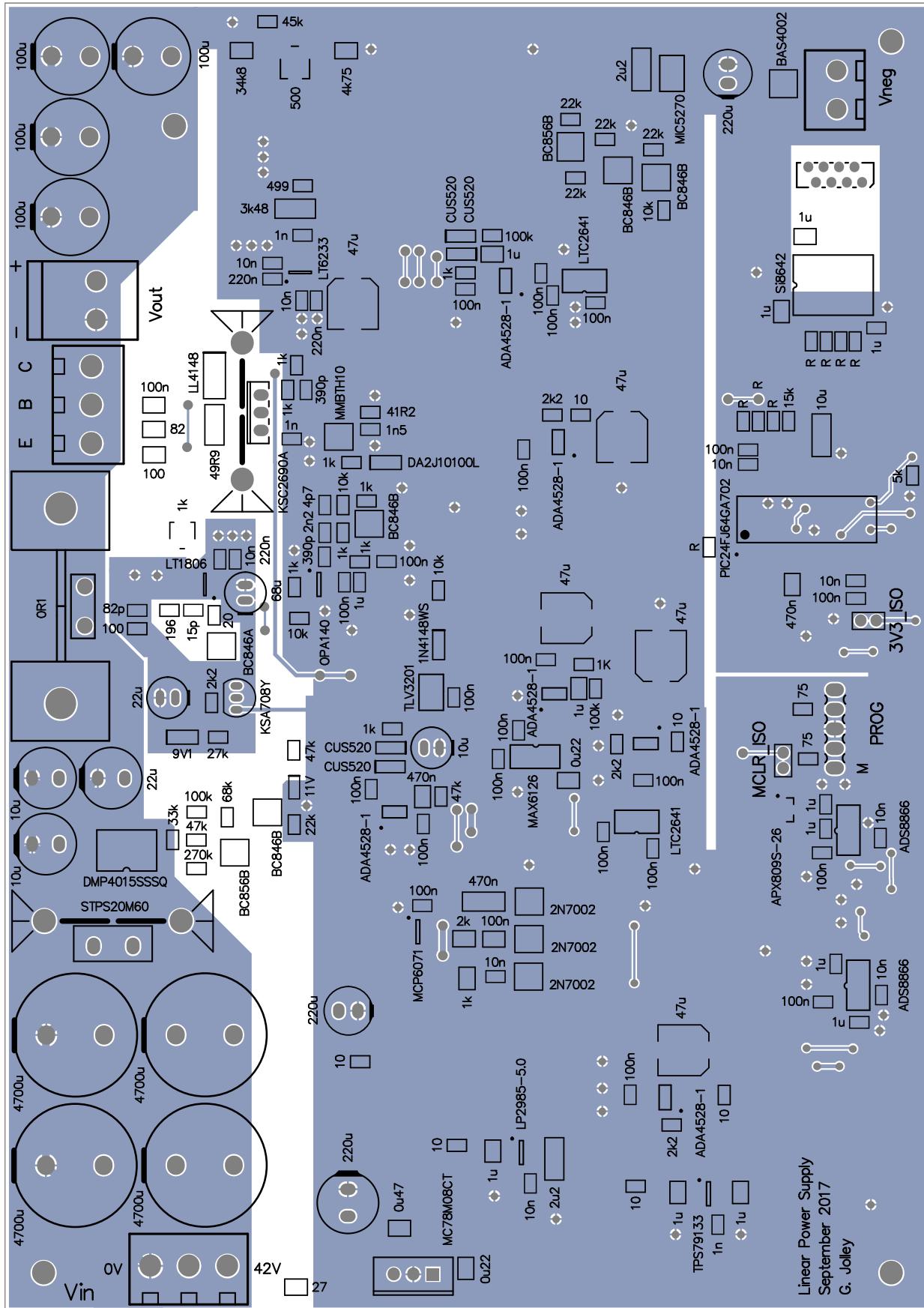


Figure 25: Power