Final Exam Project Advanced Power Electronics

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Task 1

In this task, we should design and specified all the parameter of given a synchronous buck converter, as shown in Figure 1, thus it could meet the specified ripple current and could keep the performance within load variation scenarios.

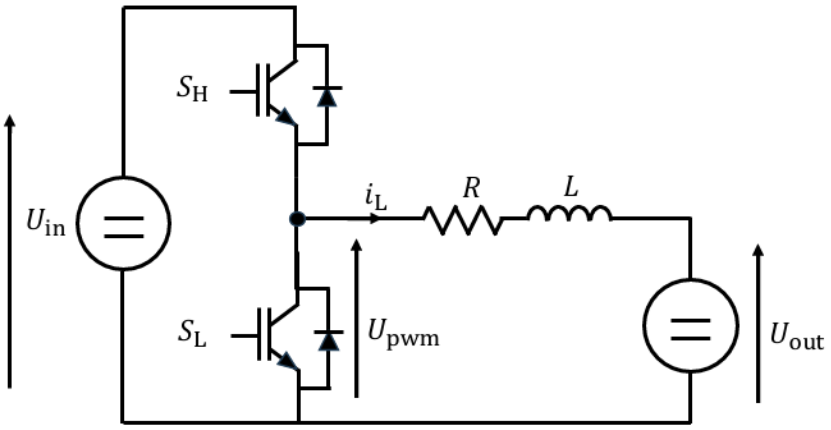

Figure 1 Synchronous Buck Converter

1.1 Operation range of topology

There are four quadrant operation of a converter, as shown in Figure 2. Operation in Quadrant I give positive voltage and positive current, usually for motoring or forward power flow. Operation in Quadrant II give positive voltage and negative current (acting as a load), thus could be used to perform regenerative braking and reverse power flow. In Quadrant III, converter give negative voltage and negative current, thus could perform reverse motoring. In Quadrant IV, converter give negative voltage and positive current, thus could be used to perform reverse braking. The synchronous buck converter operates only in a **single quadrant** (quadrant I: positive voltage and positive current) as a step-down power source. The output voltage is always positive and lower than the input voltage, while the current flows from the converter to the load (it acts as a power source).

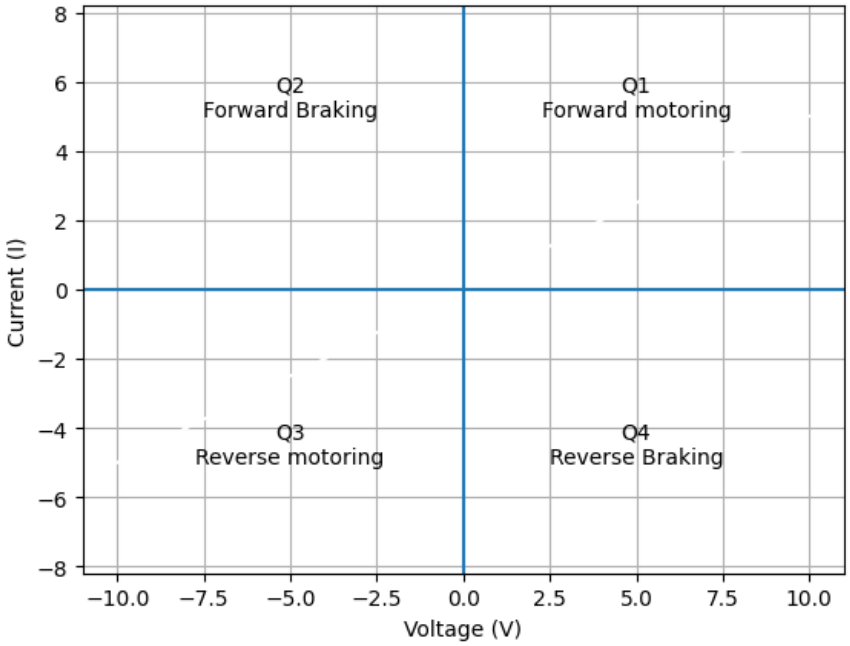

Figure 2 Four-Quadrant Operation of Converter

1.2 Steady-state duty cycle required

For a synchronous buck converter that operates in continuous conduction mode (CCM) and have a perfect efficiency, the duty cycle (d) is just simply ratio between output voltage (V_{out}) and input voltage (V_{in}), as given in (1).

$$d = \frac{V_{out}}{V_{in}} \tag{1}$$

1.3 PWM and Inductor Voltage waveform

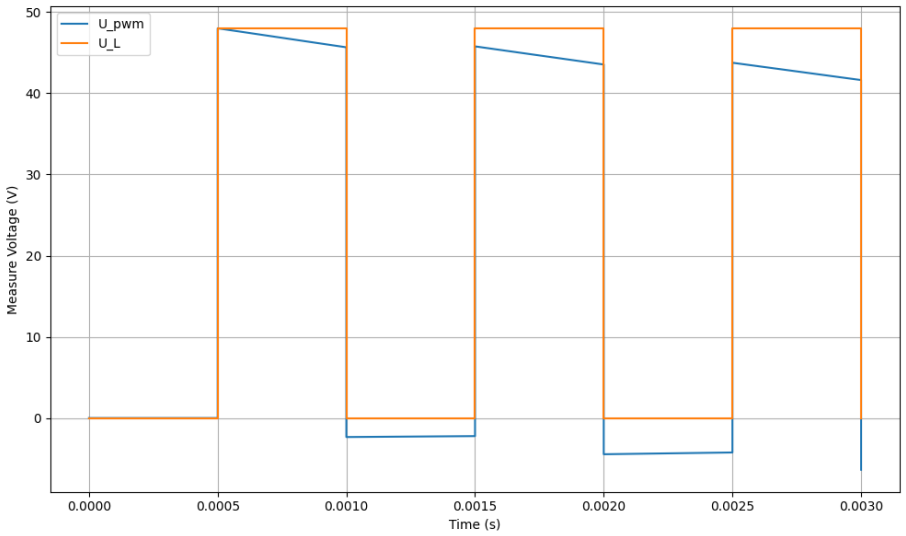

Figure 3 PWM and Inductor Voltage Waveform over three switching cycles

1.4 Relation between voltage and current ripple in inductor

In steady-state, these two quantities are linked by the fundamental principle of Inductor Volt-Second Balance. The voltage across an inductor (v_L) and the change in its current (i_L) are related by Faraday's Law of Induction:

$$v_L(t) = L\frac{di_L(t)}{dt} \tag{2}$$

From this formula, we can see that the instantaneous voltage determines the slope of the inductor current. Then, the inductor ripple current (Δi_L) is the result of applying a specific voltage across the inductor for a specific duration of time.

In steady-state operation, the average voltage across the inductor over a full switching period (T_s) must be zero. This is known as the Inductor Volt-Second Balance.

$$\langle v_L \rangle = \frac{1}{T_s}\int_0^{T_s} v_L(t)dt = 0 \tag{3}$$

If the average voltage were not zero, the current would increase or decrease indefinitely every cycle, meaning the converter would not be in a "steady" state.

1.5 Design system with customized ripple

In this section, we want to discuss about the ripple in the inductor current and what is the mathematical expression that determine inductor ripple current. In the end of this section, we want to design the converter with customized ripple by determine the right inductance value.

1.5.1 Expression of current ripple

The ripple current is calculated by observing the inductor voltage during the two main switching intervals:

- **Interval 1: Switch ON (Duration DT_s)**
  The inductor is connected between V_{in} and V_{out}.
- Inductor Voltage: $v_{L,on} = V_{in} - V_{out}$
- The current rises with a positive slope:

$$\Delta i_L = \frac{V_{in} - V_{out}}{L} \cdot DT_s \tag{4}$$

- **Interval 2: Switch OFF (Duration $(1-D)T_s$)**
  The inductor is connected between Ground and V_{out}.
- Inductor Voltage: $v_{L,off} = -V_{out}$

- The current falls with a negative slope:

$$\Delta i_L = \frac{V_{out}}{L} \cdot (1 - D)T_s \tag{5}$$

Because the net change in current over one cycle is zero, the "area" of the positive voltage rectangle must exactly equal the "area" of the negative voltage rectangle.

1.5.2 Minimum inductance

From (4) and (5), we could determine the value of inductance to achieve our desired ripple current. The inductance value of L could be determined by rearrange (5) into (6).

$$L = \frac{V_{out}}{\Delta i_L} \cdot (1 - D)T_s \tag{5}$$

$$L = \frac{D * V_{in}}{\Delta i_L} \cdot \frac{(1 - D)}{fw} \tag{6}$$

Let we use these parameter:

V_in = 48 V

fw = 1000 Hz

D = 0.5

R_1 = 0.1 Ω

$\mathrm{R_{Load}}$ = 1000 Ω

To achieve ripple current of 5%, means that the $\Delta i_L = (\mathrm{V_{out}}/(\mathrm{R_{Load}} + \mathrm{R_1})) * 5\%$, then the value of L could be determined by (7). The result is a big inductance, because the switching frequency is relatively low. Once we use high switching frequency, we can minimize the value of inductor.

$$L = \frac{D * V_{in}}{(\mathrm{V_{out}}/(\mathrm{R_{Load}} + \mathrm{R_1})) * 5\%,} \cdot \frac{(1 - D)}{fw} = 10\ H \tag{7}$$

1.5.3 Inductor current waveform

Since we want the ripple current is 5% of its nominal value, then the $\Delta i_L = 1.2\ x\ 10^{-3}\ A$. Figure 4 shows us about the inductor current waveform. In Figure 5, seen that using the calculated inductance value, the ripple is 5%.

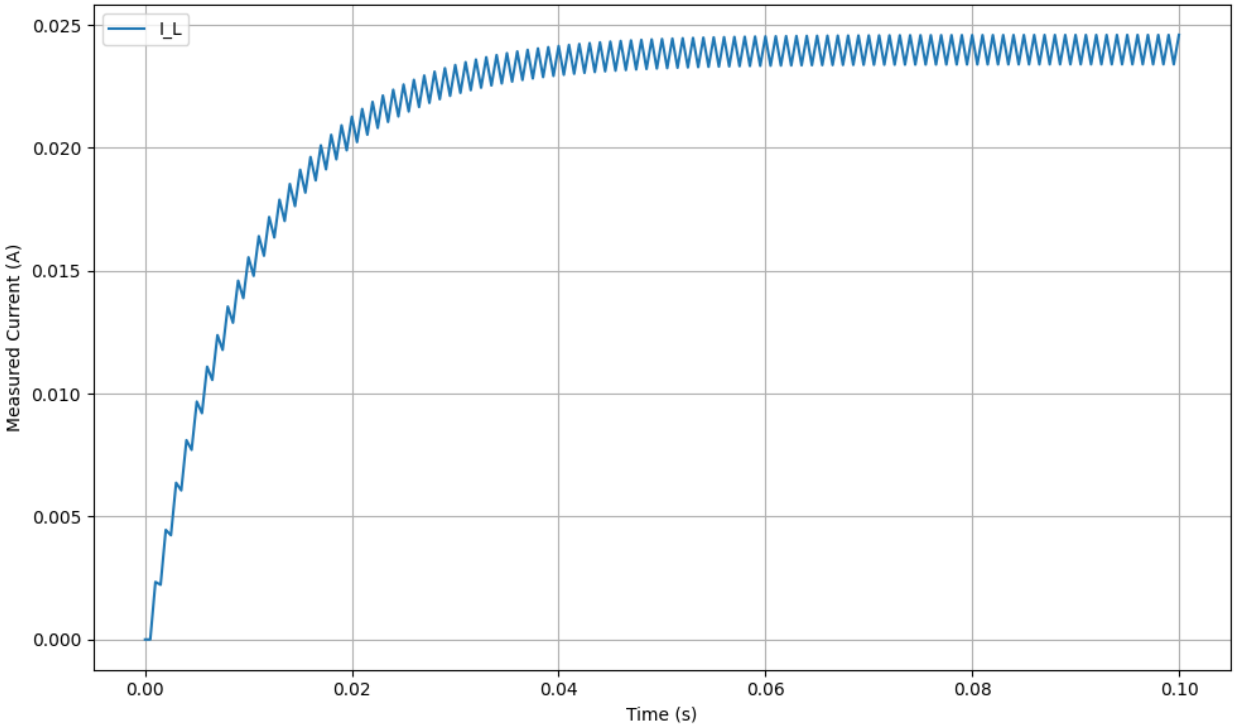

Figure 4 Inductor Current Waveform

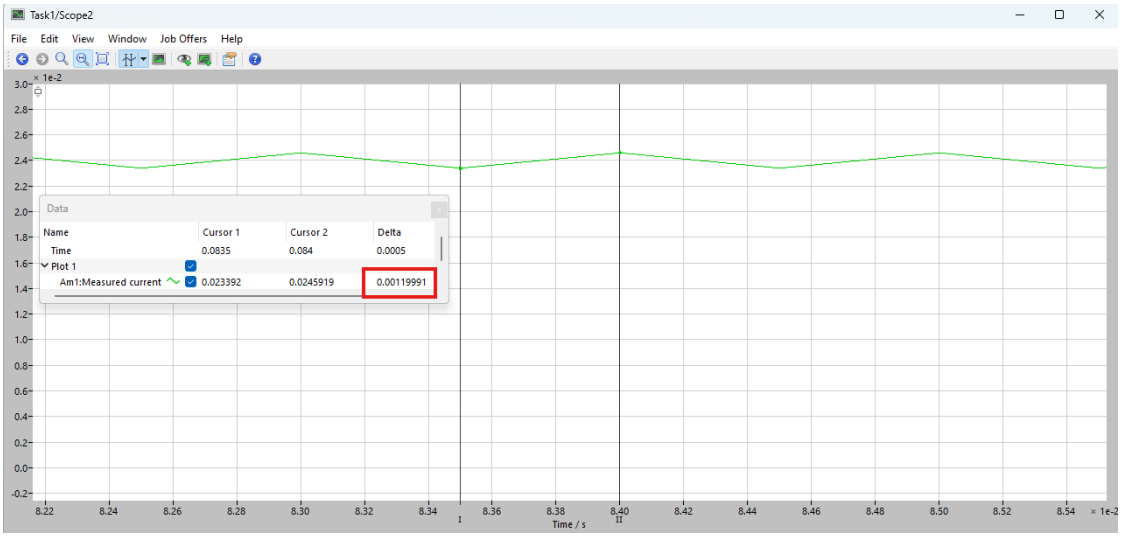

Figure 5 Ripple Current of Inductor

1.5.4 Operating condition of the system during load variation

Continous conduction mode is rely so much with comparison between average load current (I_{out}) and half of the inductor ripple current $\left(\frac{\Delta i_L}{2}\right)$. Converter is said to still in CCM Condition when $I_{out} > \frac{\Delta i_L}{2}$. If the load current I_{out} drops below half of the ripple current, the inductor current will hit zero before the next switching cycle begins, causing the converter to enter Discontinuous Conduction Mode (DCM). In Figure 4 and Figure 5, it is seen that $I_{out} > \frac{\Delta i_L}{2}$ when the load is in 100% of its nominal load. Similiarly, in Figure 6 and Figure 7, it is seen that $I_{out} > \frac{\Delta i_L}{2}$ when the load is in 75% of its nominal load. Also, in Figure 4 and Figure 5, it is seen that $I_{out} > \frac{\Delta i_L}{2}$ when the load is in 25% of its nominal load. So, with the variation of load, converter is still in the CCM mode.

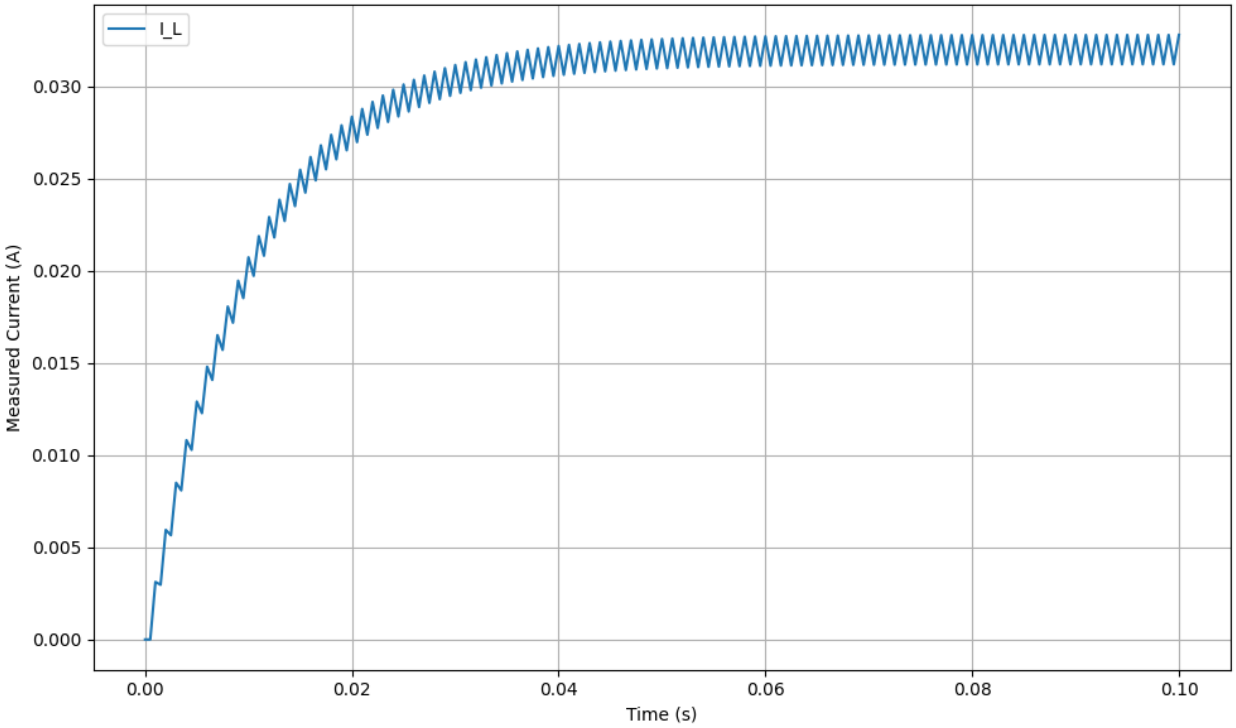

Figure 6 Inductor Current Waveform in 75% Load

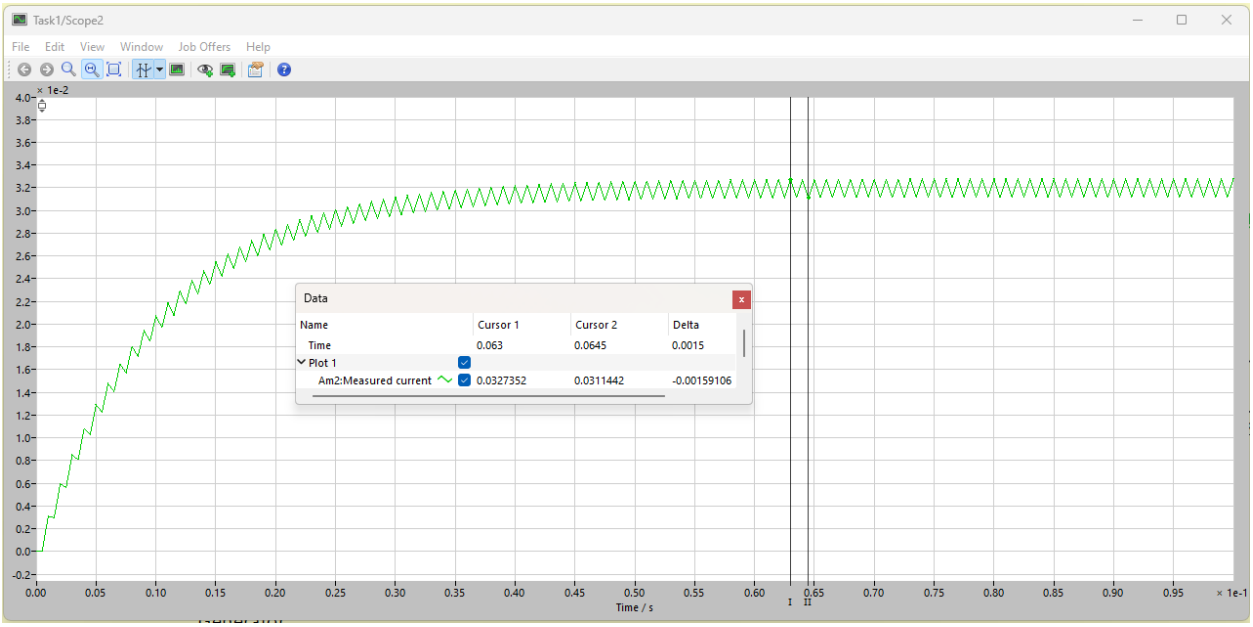

Figure 7 Ripple Current of Inductor in 75% Load

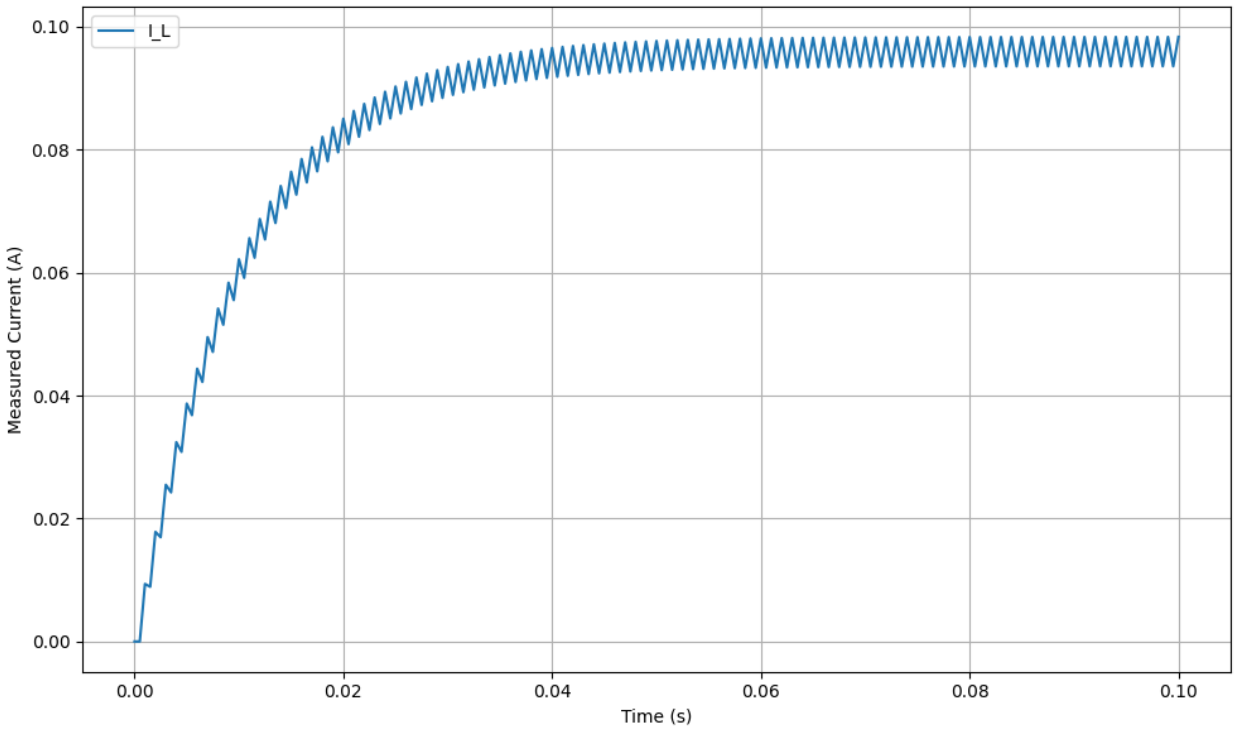

Figure 8 Inductor Current Waveform in 25% Load

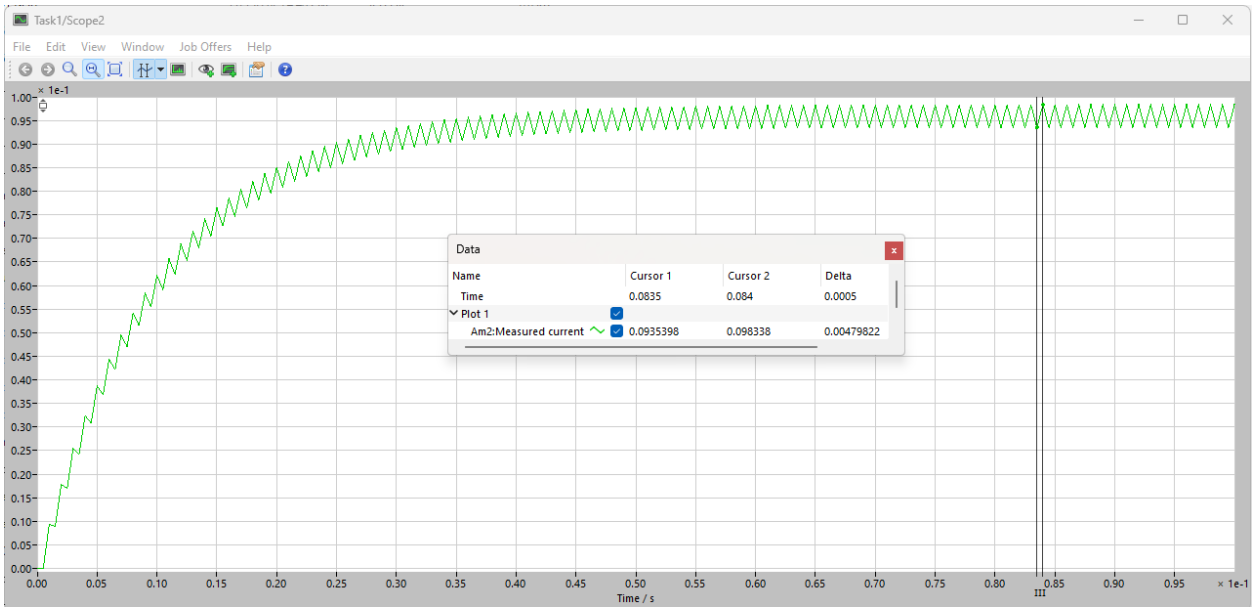

Figure 9 Ripple Current of Inductor in 25% Load

Task 2

In this task, a three phase inverter was designed using sinusoidal pulse-width modulation (SPWM). Second-order filter also designed to improve the output quality of inverter. The inverter using topology as seen in Figure 10.

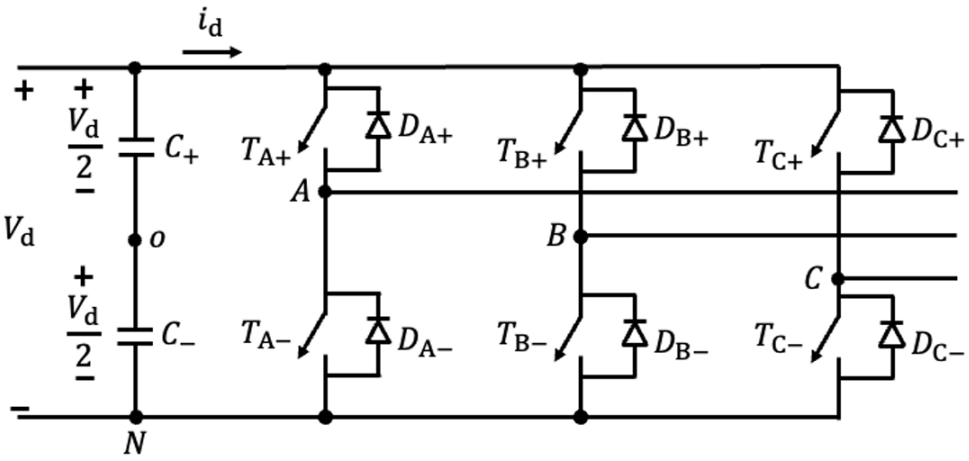

Figure 10 Three Phase Inverter Topology

2.1 Switching and Output Voltage Waveform using SPWM

Figure 11 show us the control and carrier signal waveform. The control signal waveform is sinusoidal with frequency of 50 Hz and amplitude of 1. Control signal a, b, and c have 120^0 of phase difference between each signal. Then we can also see the carrier signal, which is a triangular wave with duty cycle of 0.5, frequency of 1 kHz, and amplitude of 1. With this configuration, the modulation index, m_a, would be also 1.

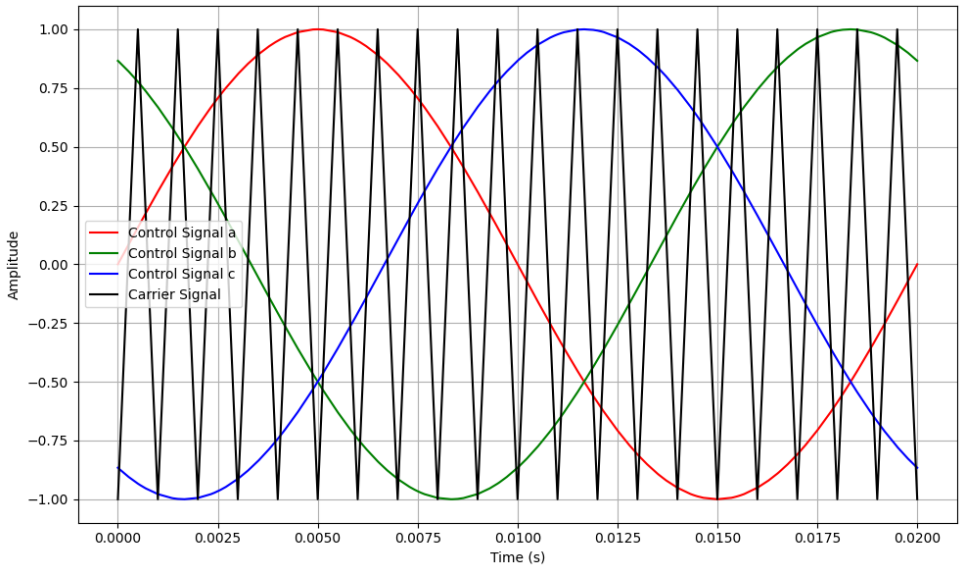

Figure 11 Control and Carrier Signal of SPWM

Meanwhile, in Figure 12, we can see the modulation signal waveform for phase a, b, and c respectively. This signal is generated by comparing the control signal with carrier signal using comparator. This modulation signal is used to switch the upper leg IGBT. While, in Figure 13, we can see the complimentary signal which generated by ‘not’-ing the modulation signal form Figure 12. This signal is used to switch the lower leg IGBT, so it guarantee that upper and lower leg is operates in complimentary ways.

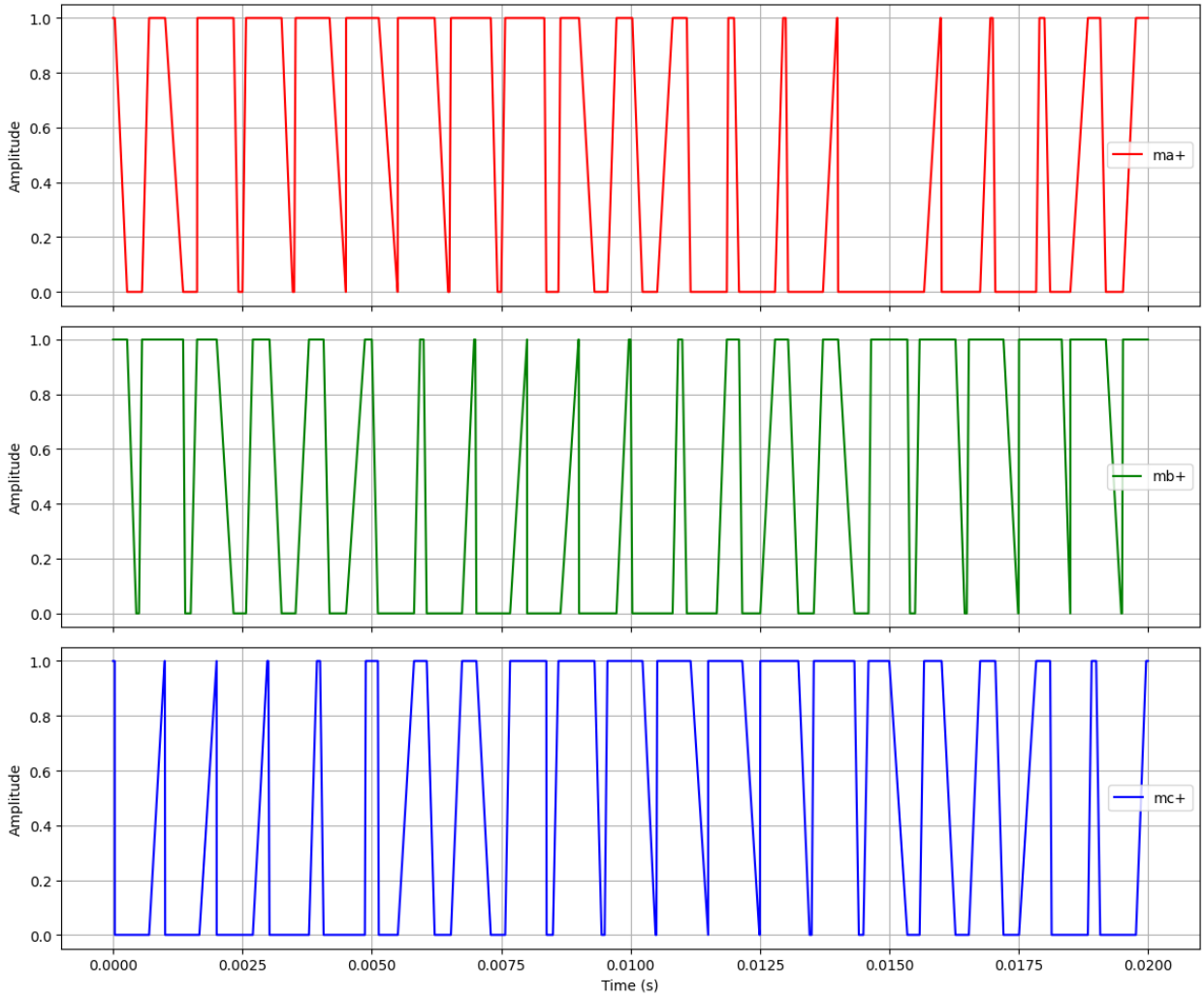

Figure 12 Index Modulation for Upper Switch

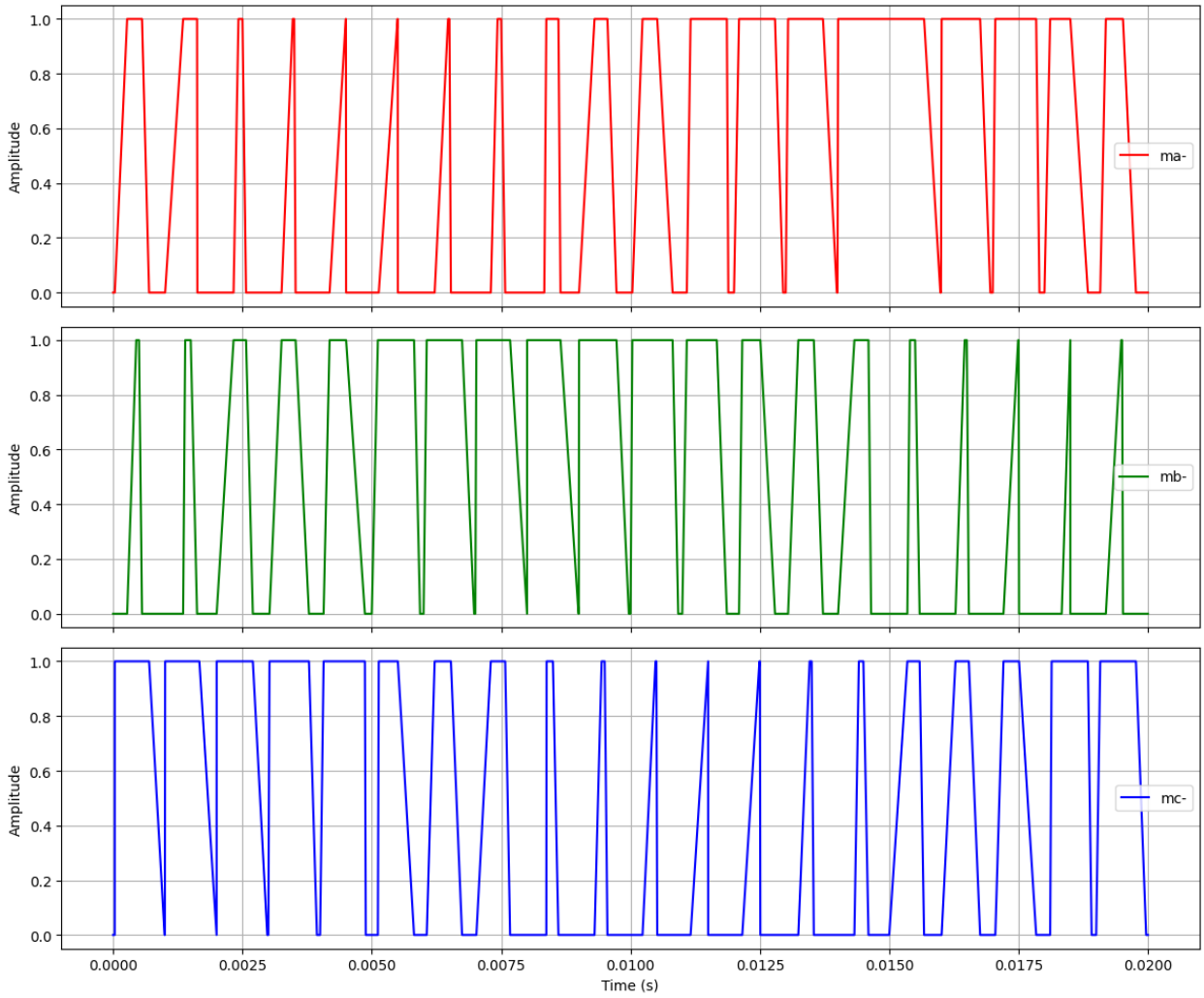

Figure 13 Index Modulation (Complimentary) for Lower Switch

2.2 Time-Domain Waveform of The Output Voltage

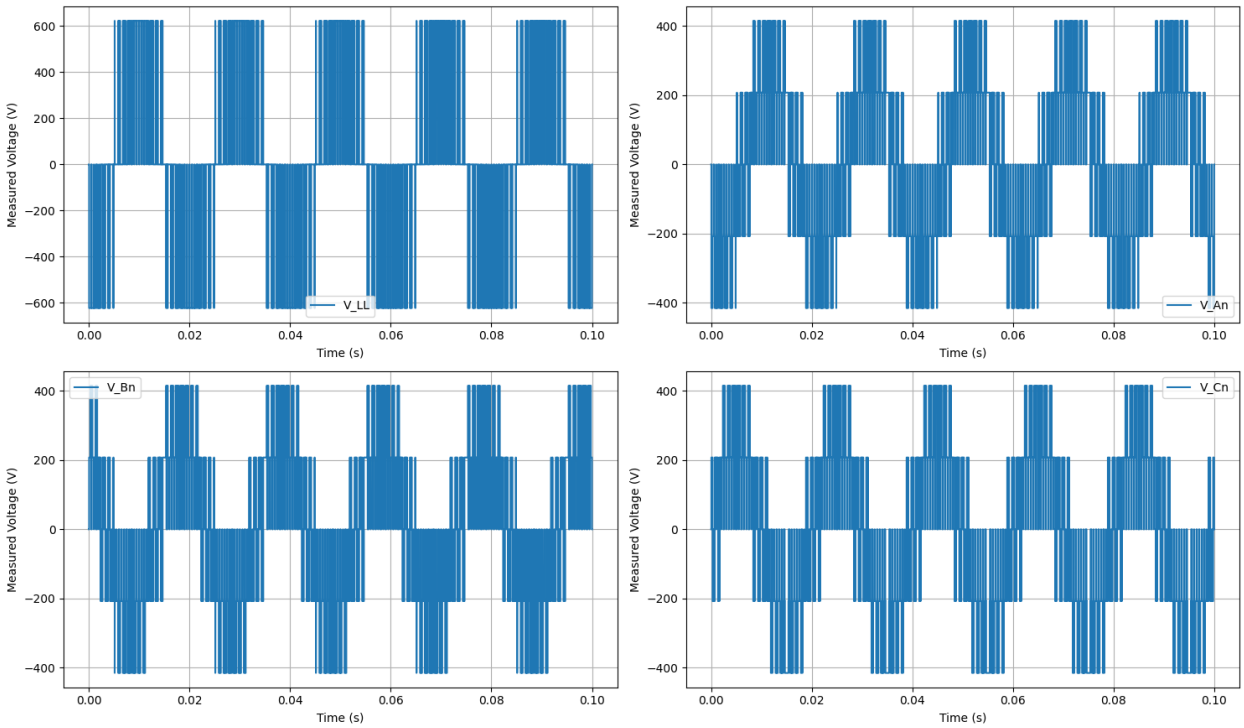

Figure 14 Time Domain Output Voltage (V_LL, V_AN, V_BN, and V_CN, respectively) Waveform using ma=1

2.3 Frequency-Domain Representation using FFT

Using FFT, we could see the frequency domain of output voltage signal, as seen in Figure 15. We could determine that the fundamental component is in 50 Hz and the dominant harmonic switching frequency are in the 800 Hz (small) and 900 Hz (rather big).

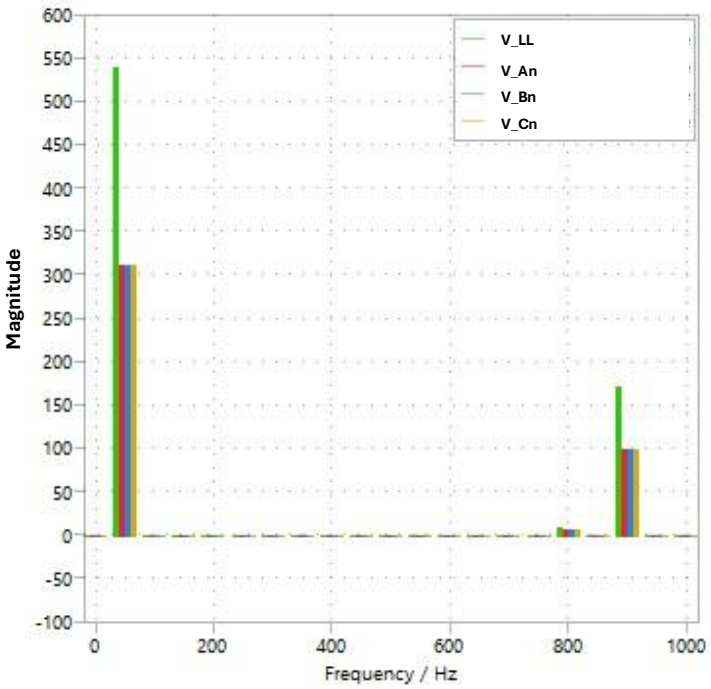

Figure 15 Frequency Domain Representation of Output Waveform

2.4 Designing Second Order Filter

Because we already know which frequency contains fundamental signal and which contains the harmonic, we could define which range of frequency that we want to keep and to cut. To cut the unwanted frequency, we would design a second-order filter using inductor and capacitor component.

2.4.1 Specification of the Filter

Of course we want to keep the 50 Hz but we want to cut the >800 Hz. By rule of thumb, the cutoff frequency is selected at least 2 times of the fundamental frequency, so the fundamental signal is not attenuated or experiencing phase shift. So, we choose cutoff frequency of 100 Hz. This could make the THD so small, but it need a big capacitance or inductance, so the hardware would rather big. For the calculation, we can refer to (8). Using that, we got $LC = 2.53 \times 10^{-6}$. We could select C = 22 uF and L = 115.1 mH. We choose the capacitor value because it just common in the market and could make the inductor smaller.

$$f_c = \frac{1}{2\pi\sqrt{LC}} \tag{8}$$

2.4.2 Output Quality Improvement

To give the idea about output quality improvement the, Figure 16 and Figure 17 shows output voltage waveform after LC filter. Figure 16 shows the line to neutral voltage which is low in harmonics and the peak value is meet our wanted voltage. $V_{LN} = 220\sqrt{2}$ V, which is around 311 V. Meanwhile, Figure 17 shows us the line to line voltage waveform after filter. It also low in harmonics and have peak value as designed, which is $V_{LL} = 380\sqrt{2}$ V (around 537 V). So, both figure has shows us about the quality improvement after using LC filter, which is reducing the harmonics to the output.

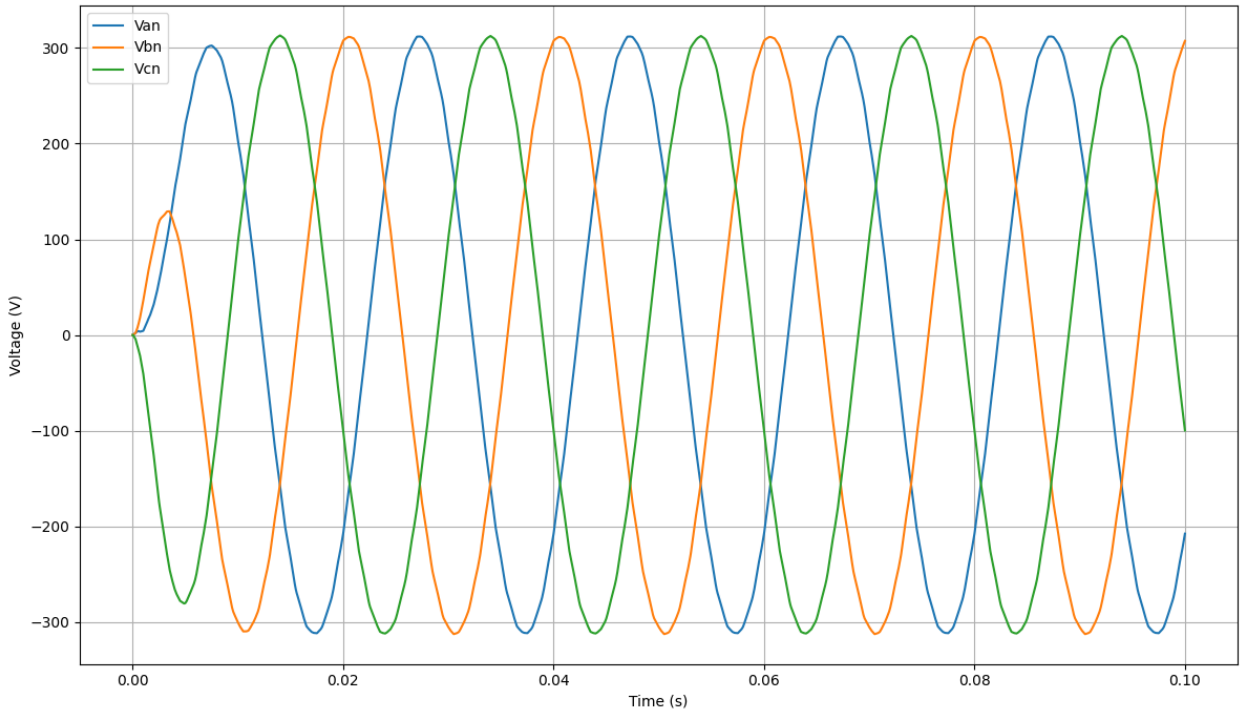

Figure 16 Voltage (Line to Neutral) Output Waveform After Using LC Filter

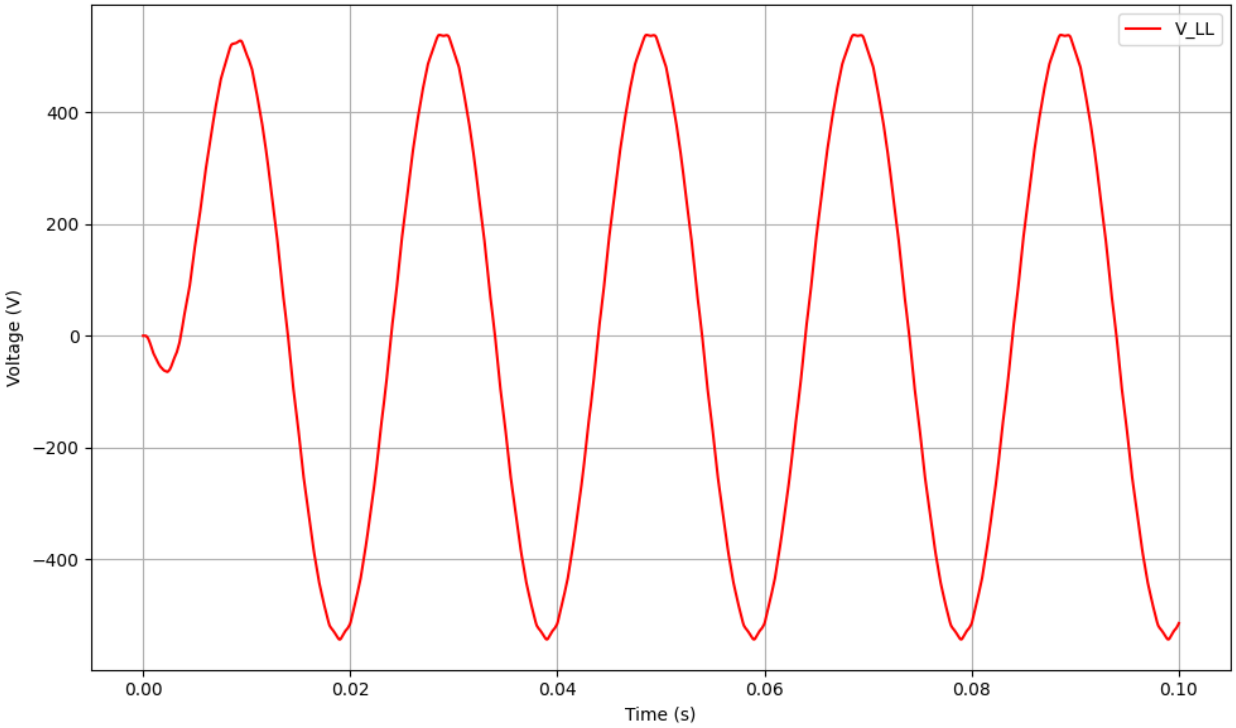

Figure 17 Voltage (Line to Line) Output Waveform After Using LC Filter

Task 3

In this task, we design a grid-following three-phase voltage source inverter. The inverter is connected to the grid thus need phase-locked loop (PLL) to synchronize with the grid. Inverter would inject controlled active and reactive power to the grid.

3.1 Current Tracking Performance

To analyze the current tracking performance, a step reference for the Id and Iq are given at t=0.1 s. The reference given for Iq is 5 A, while for Id is 20 A. Figure 18 shows us that the current could tracking the reference and thus could inject power as requested.

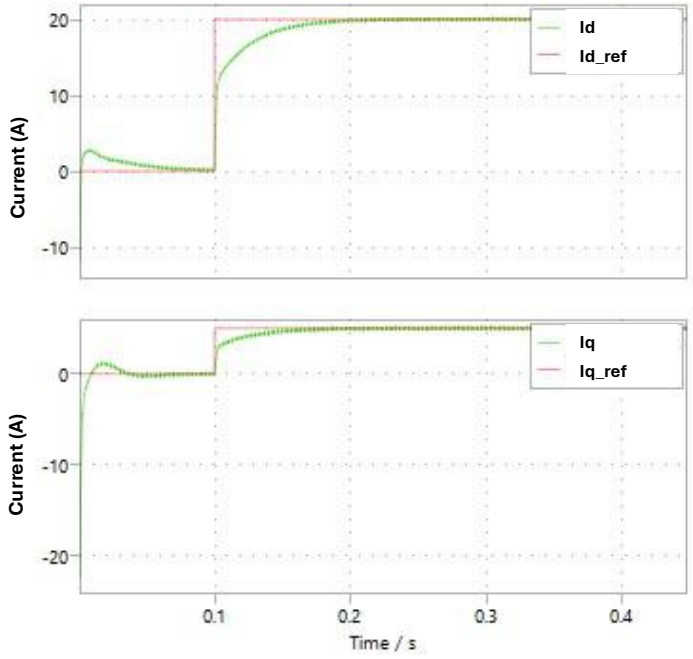

Figure 18 Current Tracking Performance

3.2 Steady-State Current Ripple

Figure 19 shows us the ripple current when steady-state achieved. As we can see, the ripple is 0.318 A, which is very small, around 1.6% from its peak value.

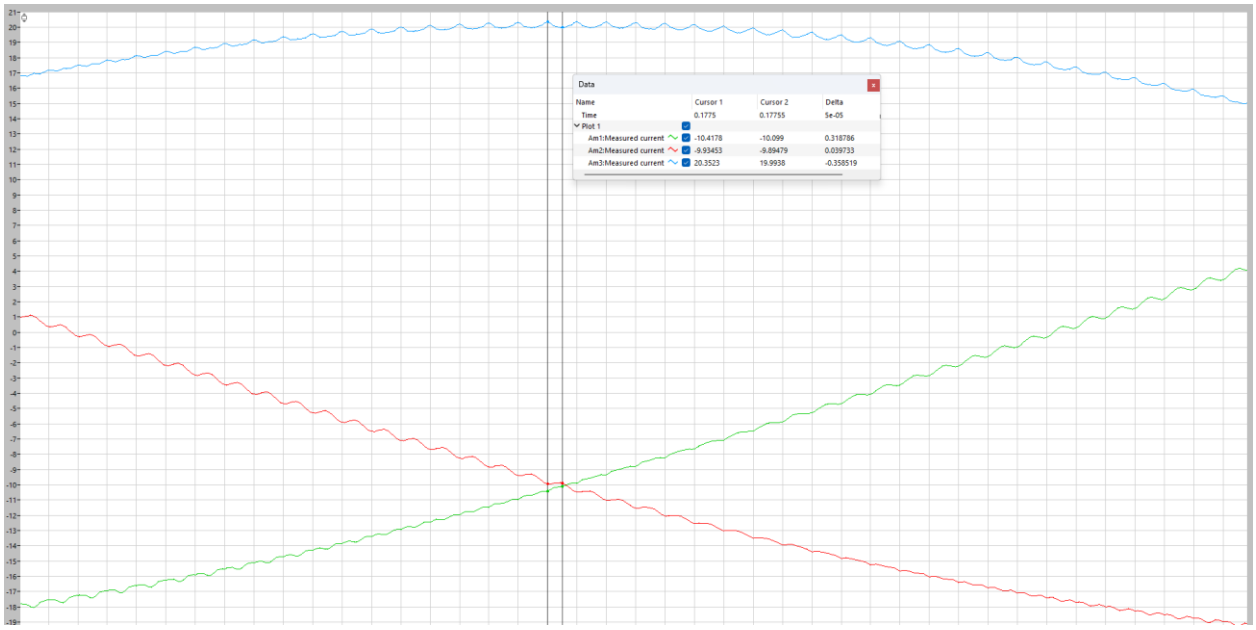

Figure 19 Steady-State Current Ripple

3.3 Closed-Loop Response to a Load Step

To analyze the closed loop response to a load step of the inverter, we use a step load at t=0.5 from 50% to 100% of the nominal load. As you can see in Figure 20, that the output current is success to stable again after load changes. From figure 21, we could agree that the reason it still stable is because the PI controller could give a response such as the Id and Iq current still could follow the reference, thus make the system stable after load changes.

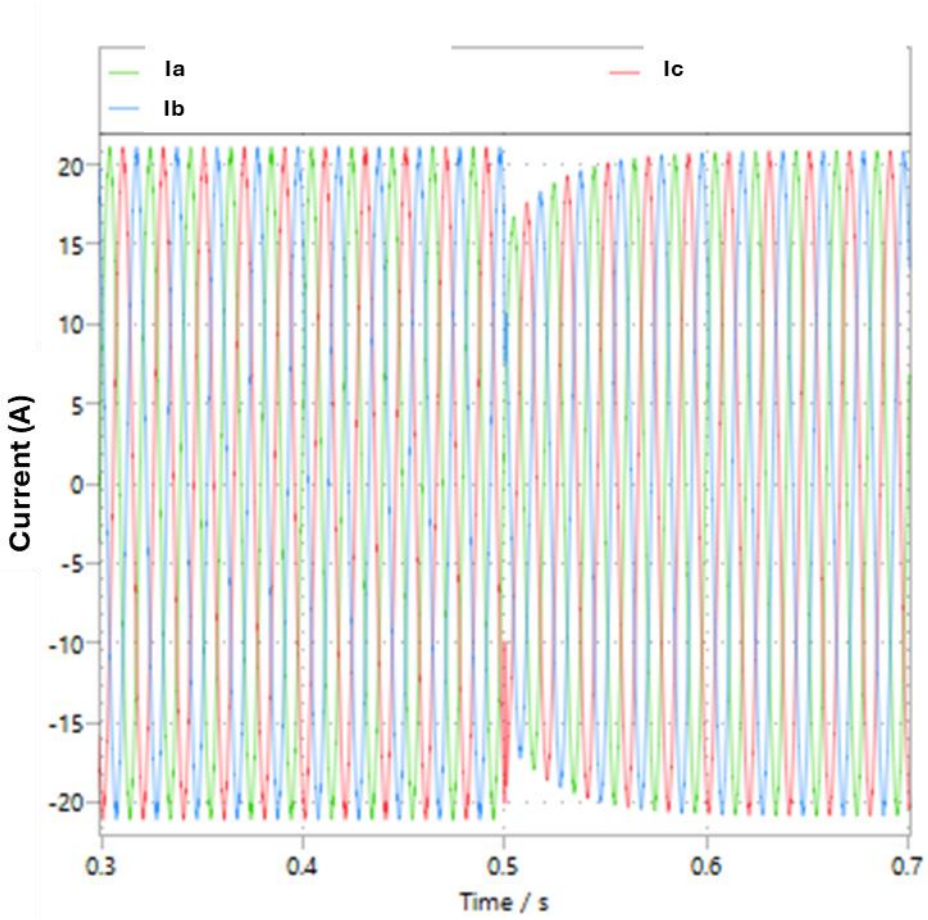

Figure 20 Output Voltage Waveform after Load Step at t=0.5 s

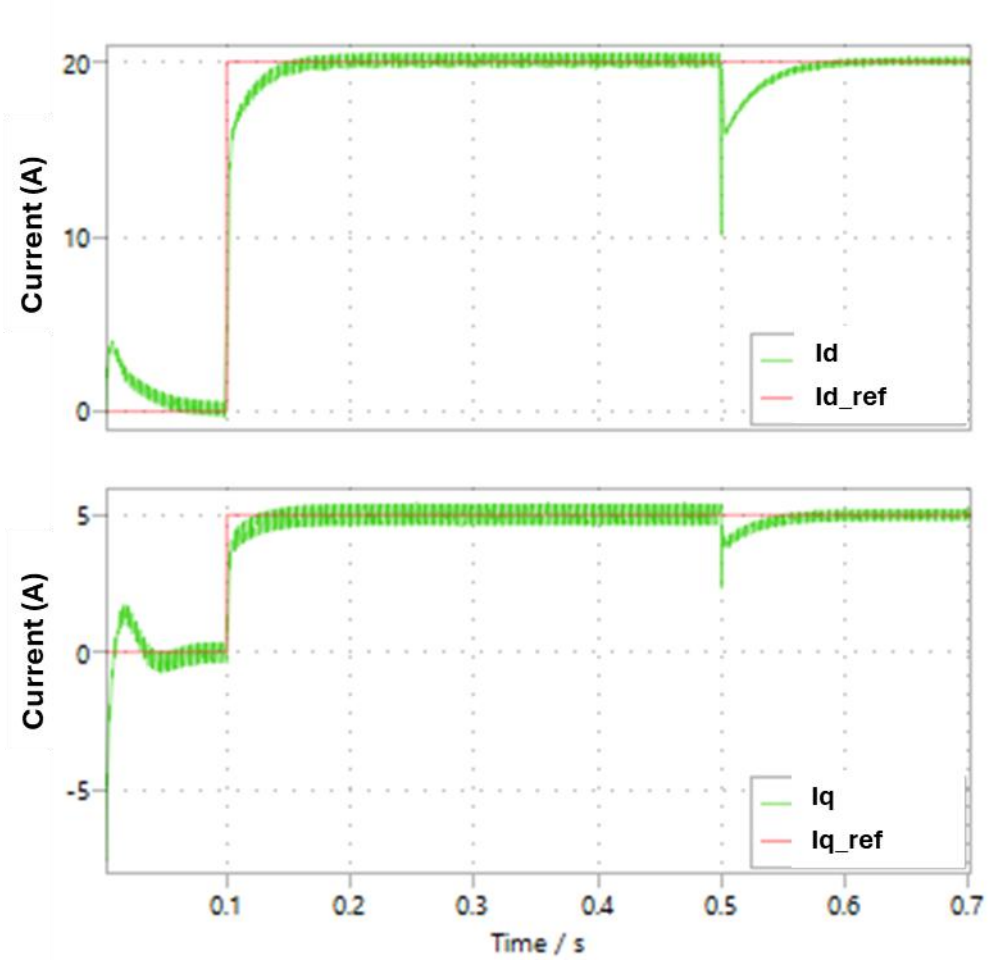

Figure 21 Closed Loop Response of Id and Iq after Load Step at t=0.5 s

3.4 Inverter Operation at Different Power Factor

As we can see at Figure 22, the operation of inverter is analyzed in different power factor. Figure 22 (a) is at unity, (b) is at leading, and (c) is at lagging. Unity is achieved by only using resistor as load, leading achieved by using capacitor as load, and lagging achieved by using inductor as load. As we can see, the inverter could operates normally in unity and leading power factor, but then not stable at lagging power factor.

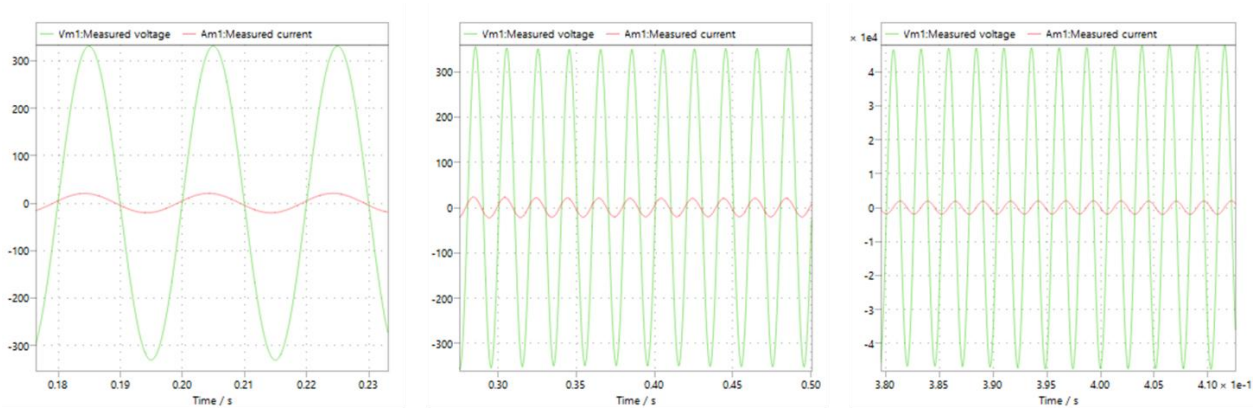

Figure 22 Inverter Operation at Different Power Factor