Lab 1:
Digital Logic Devices

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This lab focused on the exploration of the equipment and familiarizing ourselves with the gates and their functions in the lab. Our primary tasks were to build circuits using Inverters, NAND gates, NOR gates and XOR gates, then test them using our Oscilloscope or multimeter. This lab was completed entirely in UWBB-220.
The following equipment was used to complete this lab:
Keithley 2110 multimeter
Keithley 2230-30-1 power supply
Tektronix AFG3022B arbitrary function generator
Tektronix MSO3012 dual channel oscilloscope
Tektronix DMM4020 5-½ Digit Multimeter

Note: Procedures 1 through 3 were informational and contained no work to be completed. These procedures have been omitted for this reason.

Procedure 4
Procedure 4, regardless of the gate, had the same diagram that we were to construct. The diagram can be found below in Figure 4.1.

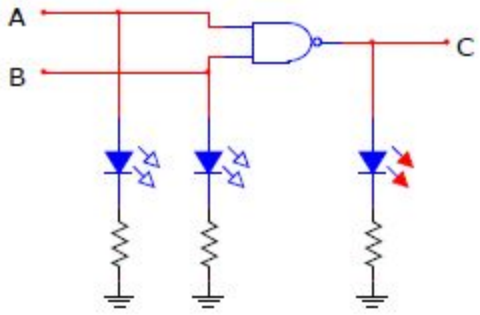


Figure 4.1: Diagram of the circuit to be built for parts 4.1, 4.2, and 4.3. Inputs are labeled as **A** and **B** while the output is labeled **C**.

In order to vary the inputs as was required for each of the sections, we used a 5 volt DC source from the Keithley power supply and assumed that to be a 1 in our truth table, and in order to obtain a 0, we connected the pin to ground.

4.1 - 7400 NAND Gate

A	B	C
1	1	0
1	0	1
0	1	1
0	0	1

Figure 4.2: Truth table of our 7400 NAND gate where 1 indicates LED on, 0 indicates LED off.

4.2 - 7402 NOR Gate

A	B	C
1	1	0
1	0	0
0	1	0
0	0	1

Figure 4.3: Truth table of our 7402 NOR gate where 1 indicates LED on, 0 indicates LED off.

4.3 7486 XOR Gate

A	B	C
1	1	0
1	0	1
0	1	1
0	0	0

Figure 4.4: Truth table of our 7486 XOR gate where 1 indicates LED on, 0 indicates LED off.

4.4 Latch

For this section we are to construct a latch using the provided diagram that is

reproduced below in figure 4.5. After construction of the latch we observe the outcome when shorting two separate input points to ground.

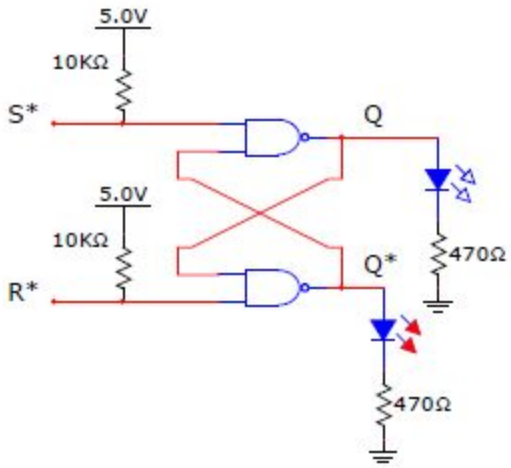


Figure 4.5: Circuit diagram for our latch. S* and R* are points that are alternated shorting to ground.

When we alternate the short between S* and R* the opposite diode would light, while the diode connected to the close gate would go dark. The diodes would alternate lighting depending on which input you were shorting.

4.5 Active low versus active high

For this part we are to construct the circuits given below in figure 4.6 using two separate NAND gates.

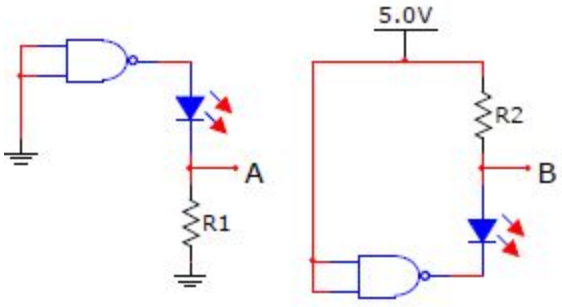


Figure 4.6: Active low versus active high circuit diagrams.

The table below has our recorded resistor and voltage values.

Item	Value
R1	468Ω
R2	468Ω
A	2.82 Volts
B	2.15 Volts
Voltage Source	5 Volts

Figure 4.7: Table of our values for the Active low versus active high circuit.

4.6 Analysis

1.) Below in figure 4.8 is our design for a NOR function using one NAND gate and 3 inverters.

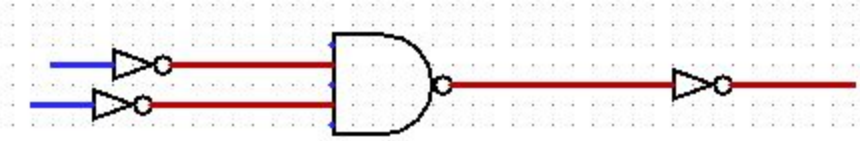


Figure 4.8: A design of a NOR function using one NAND gate and three inverters.

2.)

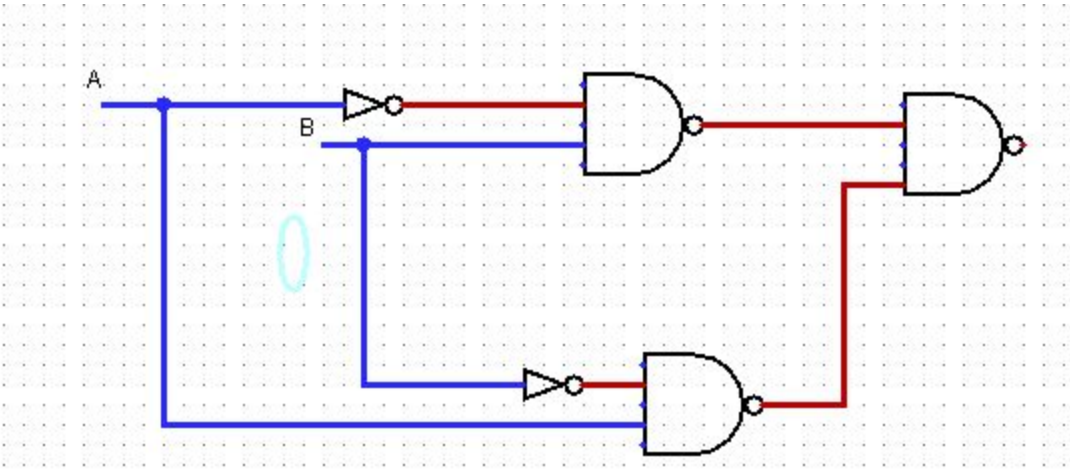


Figure 4.9: A design of an XOR function using three NAND gates and two inverters with inputs **A** and **B**.

3.) If a square wave is fed into the input when one is tied to high. The output will be 0 when the square wave is at its peak and the output will be 1 when the square wave goes to zero.
4.) A latch takes the output of one gate and sends it as an input to the other gate. As a result, only one of the gates can output a 1 at any given time. Inputting 1 and 1 into a NAND gate results in a 0 output. Having the inputs S* and R* allow you to short at that location. This allows you to actively change the input to a 0 instead of a 1, and thus change the output of each gate respectively.
5.) The LED's appeared to be the same brightness in the active low and active high circuits.
6.) VR1 = VA = 2.82 volts
VR2 = 5.0 - VB = 2.85 volts
Current through resistor 1 = 2.82/468 = 6.03mA
Current through resistor 2 = 2.85/468 = 6.09mA

Procedure 5
For procedure 5 we are discovering the electrical characteristics of a real inverter. We will be measuring:

- Output voltages for various inputs
- The input voltage level at which the inverter switches
- How many nanoseconds it takes for a change on the input to cause a change in the output
- How many nanoseconds it takes for the output to change from low to high and high to low.

5.1 TTL logic levels
Using the diagram in figure 5.1 we took measurements to fill the table below in figure 5.2.

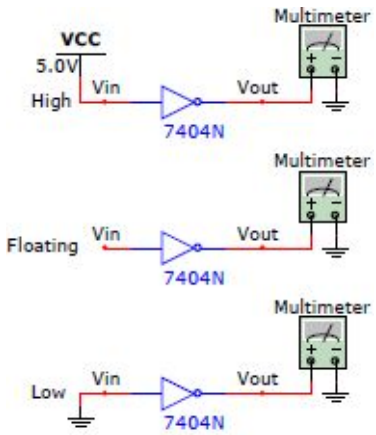


Figure 5.1: Diagram for measurements

Input Type	Vin	Vout
High	5 V	3.5 mV
Floating	0 V	5 Volts
Low	0 V	5 Volts

Figure 5.2: Measurements obtained using our inverter gate on 7404N

5.2 Switching threshold

For 5.2 we needed the function generator set up to drive an inverter input. The function generator was set with the following configuration: a triangle wave with 5.0 Vpp, with a +2.5 V offset at 1KHz. Below in figure 5.3 is the diagram we followed to construct our circuit.

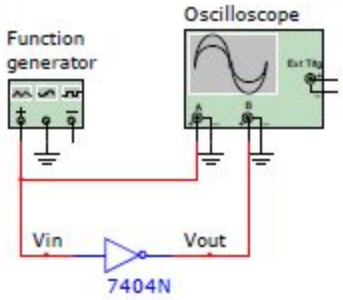


Figure 5.3: Circuit diagram for section the switching threshold.

Figure 5.4 has an oscilloscope screenshot with both our Vin and Vout measured.

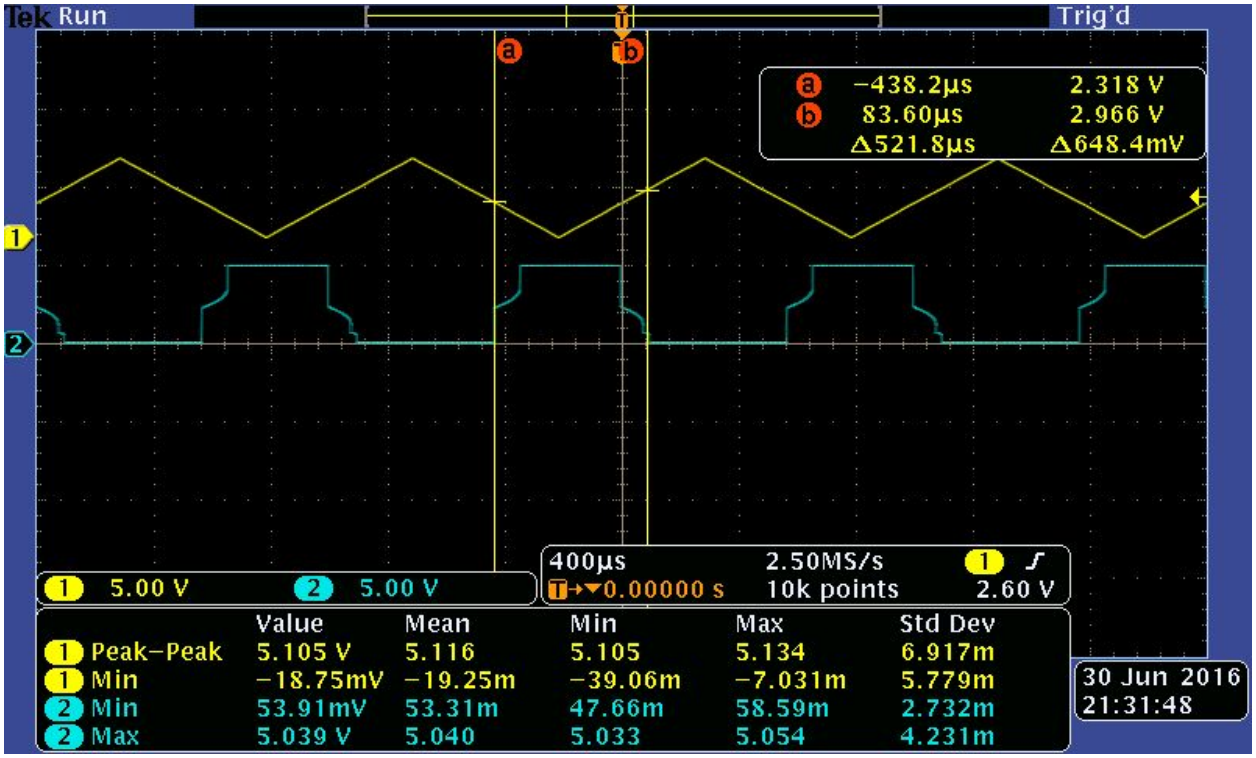


Figure 5.4: Screenshot of triangle wave input from function generator (yellow) and output wave (blue) from oscilloscope.

5.3 Transient response

For section 5.3 we set our function generator to have the following settings: Vin = 5.0 Vpp with a +2.5 Volt offset as a square wave with frequency of 1MHz. We then used the oscilloscope to collect the t_{PHL}, t_{PLH}, t_{FALL}, and t_{RISE} times. These screenshots are displayed in figures 5.5, 5.6, 5.7 and 5.8.

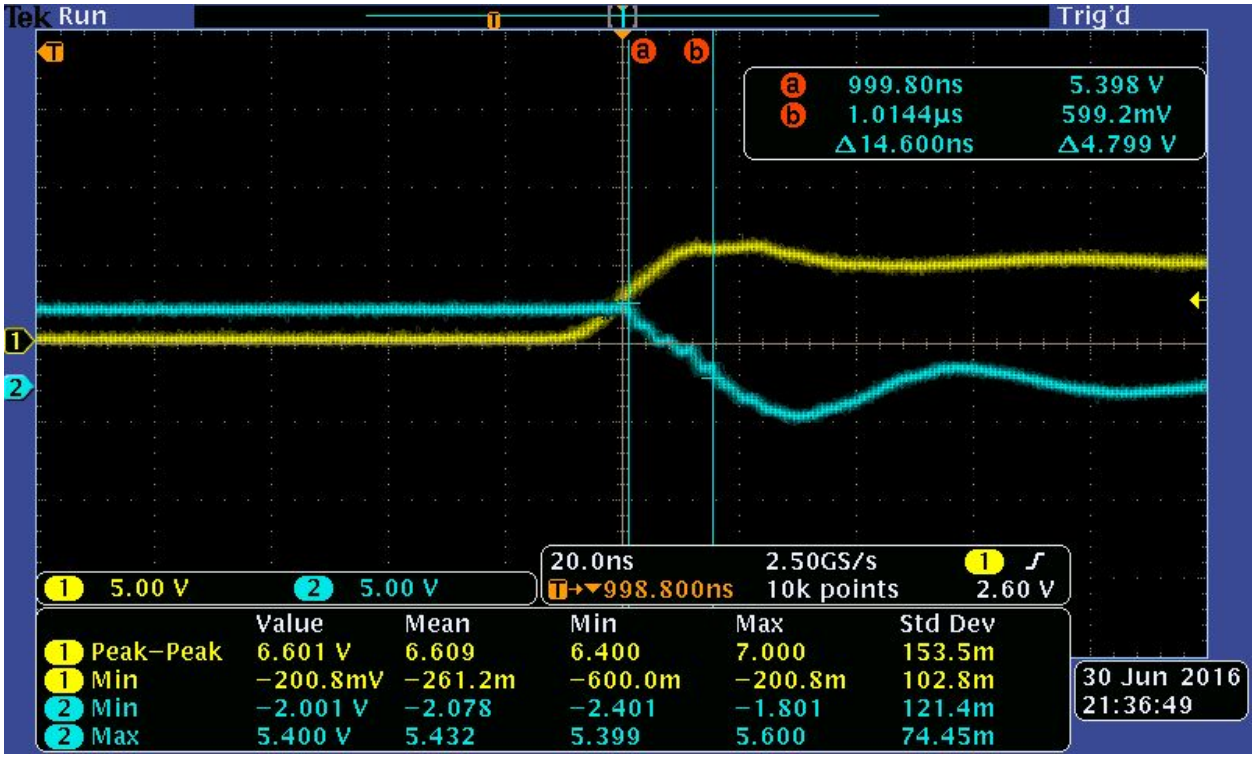


Figure 5.5: Screenshot from oscilloscope displaying t_{PHL}.

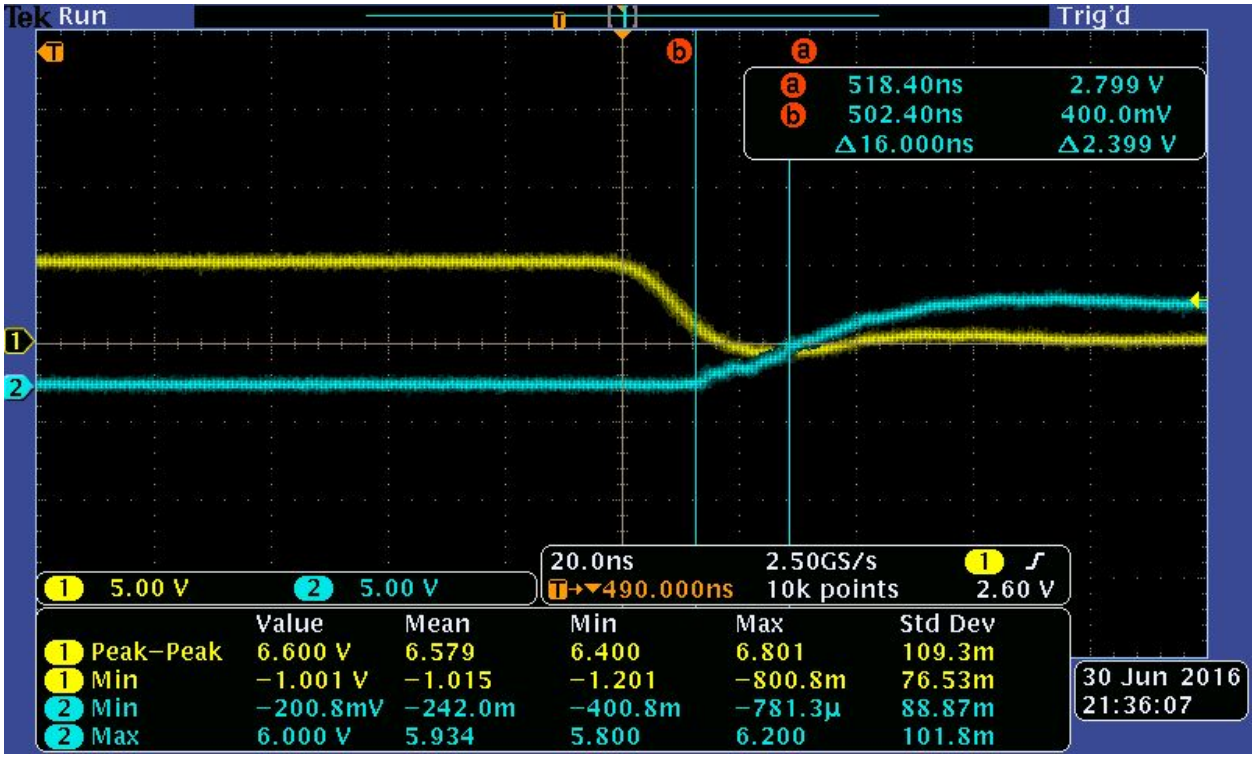


Figure 5.6: Screenshot from oscilloscope displaying t_{PLH}.

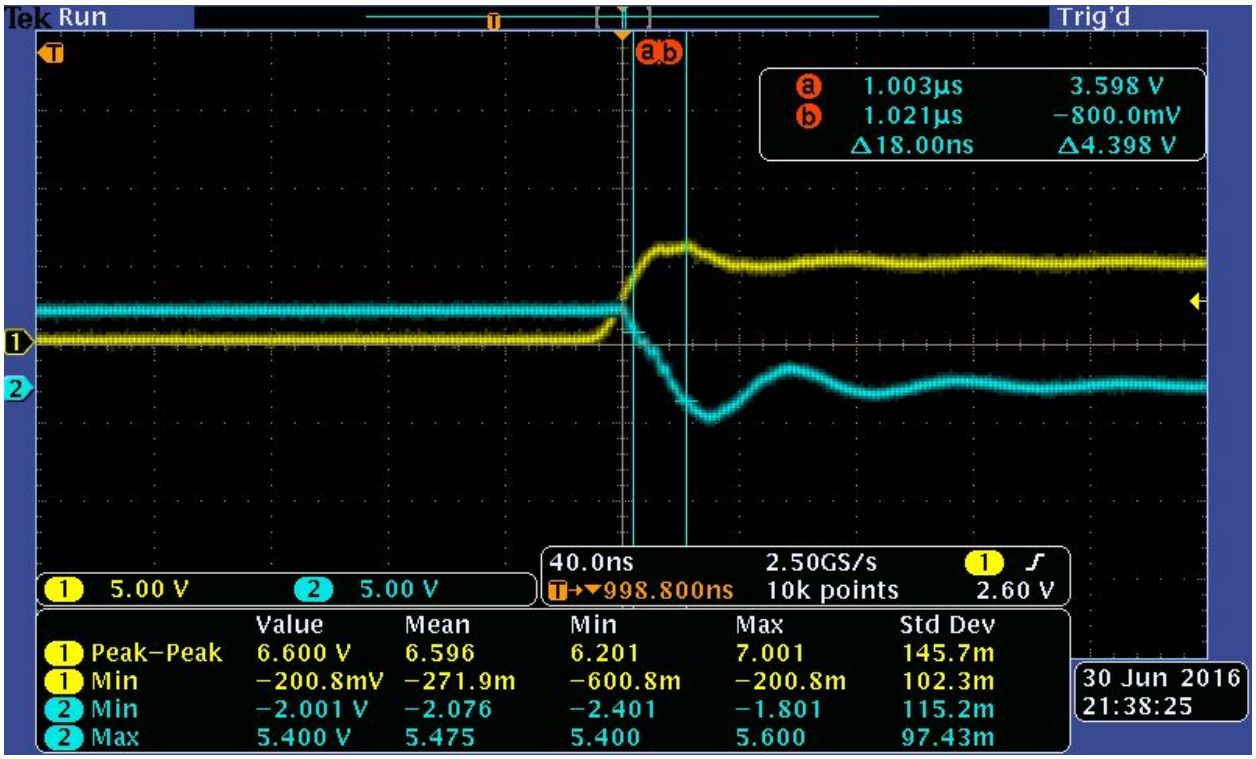


Figure 5.7: Screenshot from oscilloscope displaying t_{FALL}.

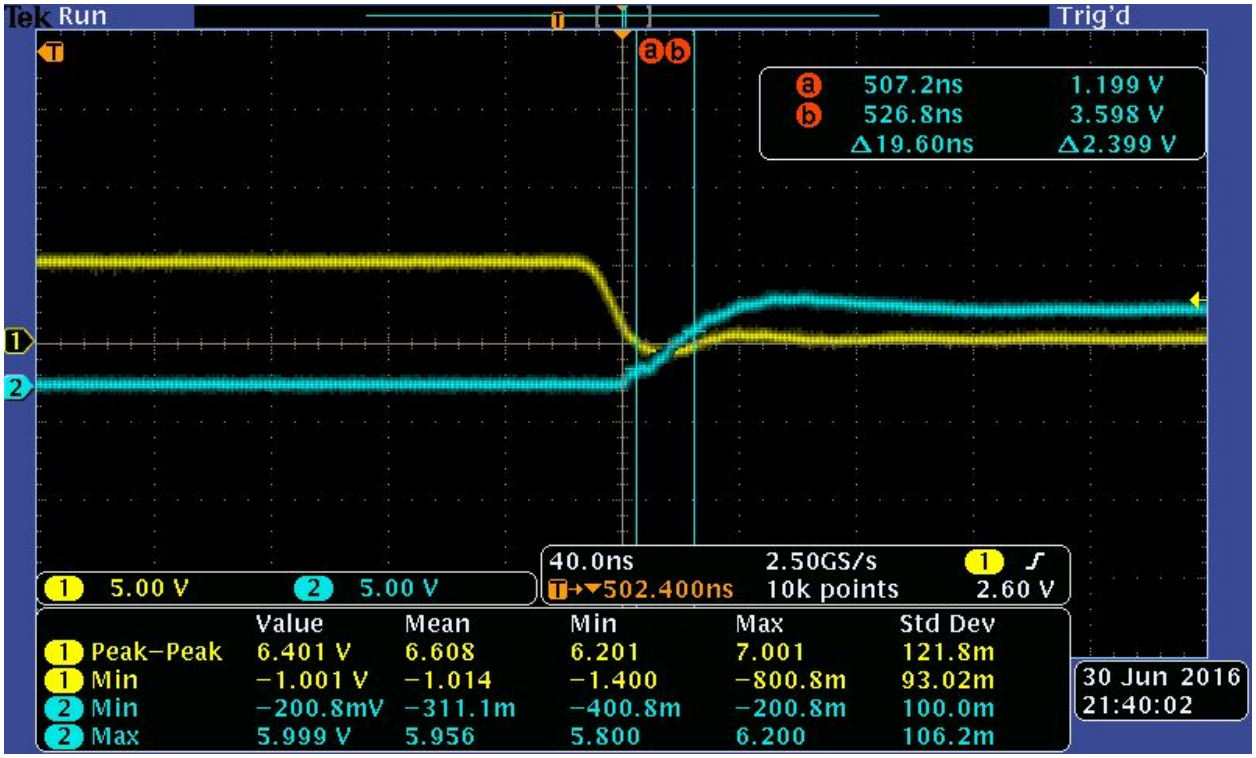


Figure 5.8: Screenshot from oscilloscope displaying t_{RISE}.

5.4 Analysis

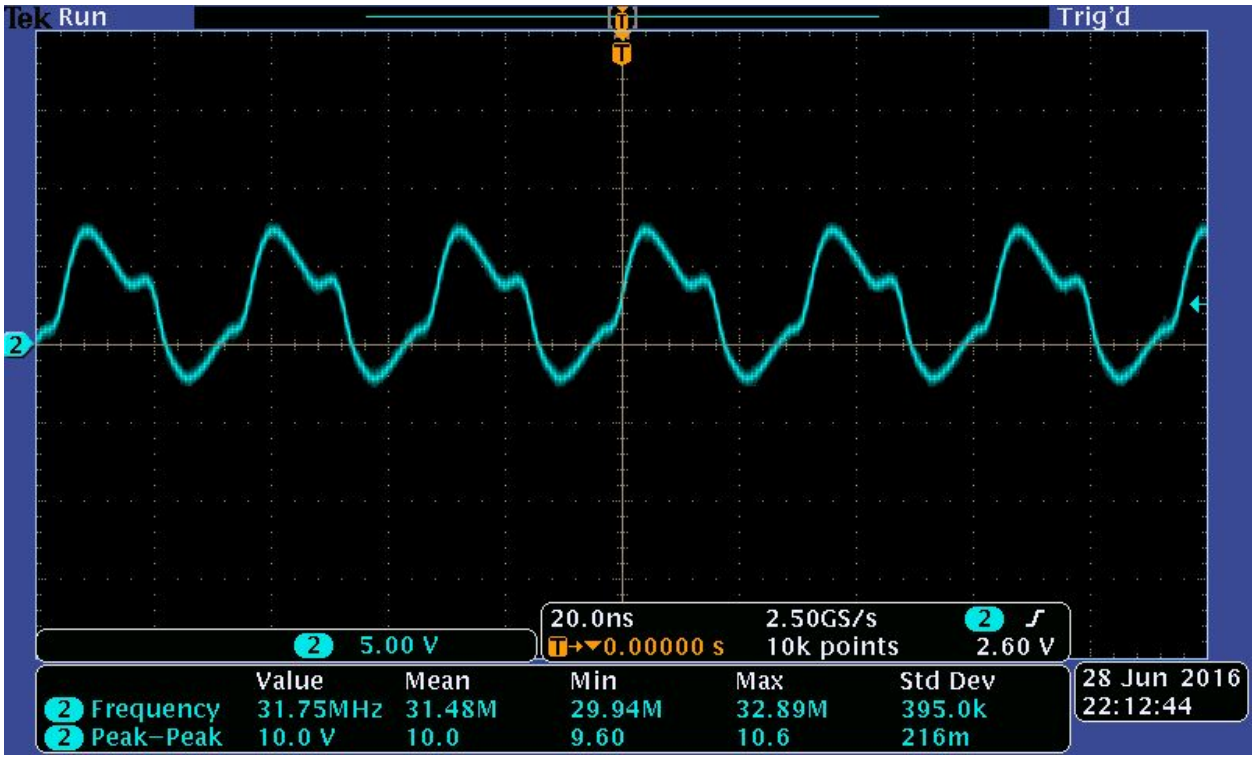
1.) In the switching threshold, the measured values was approximately 521micro-seconds and the margin between the high and low output level was around 14.6 nanoseconds.

2) When the system was driven by a triangle wave the output was not a symmetric square wave because there were values between .8V -2.0V when the inverter did not know whether it should invert the signal.

3)The TTL device is equally fast from switching from high-to-low as it is from low-to-high. Our measurements were 2 nanoseconds apart from high to low and low to high and what could be the difference is due to human errors in the specific measurement of where the marks are set.

6 Ring Oscillator

6.2 Measurements

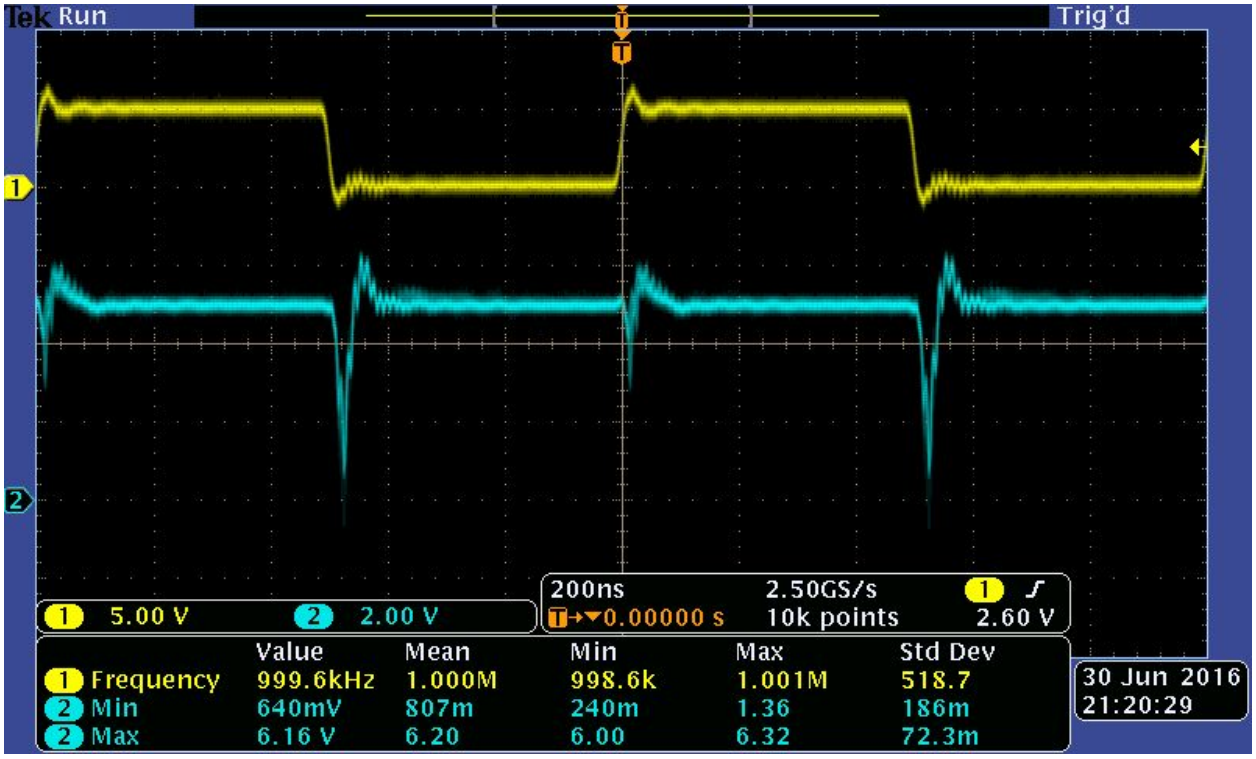


6.3: Analysis

1)The ring oscillator works but constantly inverting the signal. This circuit does not need an input is because the result would be the same due to the fact that depending on where the circuit initially starts, the low values would be inverted to high and while being inverted to the high signal it gets inverted back to low. In an endless cycle of inverting the the values from low to high and high to low.

2) The output frequency and the shape of the waveform to the propagation rise and fall time is correlated to each other. With the output frequency being 31.75MHz it is similar to 1/(16 nanoseconds) which is approximately 62.5MHz which is double the frequency. The single inverter has less time delay when being inverted only once compared to the ring oscillator which goes through multiple inverters before forming a wave form.

7. **Hazards**



7.2 **Analysis**

1)The expected output value for when Vin is high is high and for Vin is low is also high. When Vin changes from 1 to 0 and 0 to 1 the Vout should not change because the input for NAND gate will change from 1 & 0 to 0 & 1 which will output 1 regardless.

2) I observe the fact that the output signal tries to go down to low which is a downwards spike.

3) The output spiked down due to the fact that Vin for one of the inputs has to pass through two gates which causes a momentary delay when reaching the output NAND gate. At that momentary delay the output will put out a 0 because the logic would be 0&0 and 1&1 which quickly gets switched to 1&0 and 0&1 so the output becomes high again.

4) I believe this is called a hazard is due to the fact the output would look right when drawn out, but in real life there would be a obstacles such as the delay which would output a different than anticipated which results in the wrong logic.