***KL85***

***Multiple-Resonant Switched Capacitor Converter***

**Test Chip Manual**

*BCD110AP technology*

Advanced IC & Technology Sensitive IPs Design

Smart Power & High Voltage Competence Center

Front-end Technology and Manufacturing - FTM R&D

STMicroelectronics S.r.l.

Castelletto – Italy

Revision 0.1

The purpose of this document is to describe content and control instructions ofKL85AA chip included in HI13AA multi-chip in BCD110AP technology, which integrates a Multiple-Resonant Switched Capacitor Converter (MuReSCC), including

* Comparator
* 13MHz clock
* Comparator
* Phase generator with programmable delays
* Drivers
* Output stage

Additional cells are included to allow proper biasing

* Bandgap voltage reference
* PTAT and ZTAT current reference

The used back-end option is 4M2X1UNIPDPI (4 Metals, NiPd Pads with PI). The used front-end option is DTI, with both 1.8V and 5V Gate Oxides.

REVISION HISTORY

|  |  |  |  |
| --- | --- | --- | --- |
| **Revision** | **Authors** | **Release** | **Notes** |
| 0.1 | Alessandro Nicolosi | June 2024 | Document Creation |

TECHNOLOGY AND OPERATING CONDITIONS

|  |  |
| --- | --- |
| **Name** | **Version** |
| PDK\_STM\_BCD110AP | 3.1.a-00 |
| MACROCELLS\_ESD\_BCD110AP | 1.2-00 |
| BCD110AP\_SC\_13d5T\_CORE\_OD50 | 3.0-00 |
| BCD110AP\_SC\_12T\_CORE\_H | 3.0-00 |
| BCD110AP\_SC\_13d5TGO2\_SHIFTJI\_H\_OD50 | 3.0-00 |
| BCD110AP\_IO\_SFISO\_GPIO\_1V8\_5V\_OD50\_4M2X1UNIPDPI | 1.0 |

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# KL85 Overview

EXT\_REF\_SNS\_INT\_REF

OSC\_VCTRL

SEL\_INT\_REF

RESET

VBATT\_COMP

VDD\_IO

GND\_IO

SENSE\_CMP\_OUT

SEL\_OPEN\_LOOP

V1V8

SENSE\_OSC\_CLK

SEL\_CLK

## PADRing

The external access (on wafer) to the testchip is shown in Figure 4‑1:

48 47 46 45 44 43 42 41 40 39 38 37



ADT\_D4

VBATT\_PWR

VS1

VOUT

VOUT\_SENSE

VS3

GND

VDD\_IO

GND\_IO

VBATT\_DRV

VG4

VG3

EXT\_CLK

DT\_D0

DT\_D1

DT\_D2

DT\_D3

DT\_D4

VDD\_IO

GND\_IO

ADT\_D0

ADT\_D1

ADT\_D2

ADT\_D3

36

35

34

33

32

31

30

29

28

27

26

25

13 14 15 16 17 18 19 20 21 22 23 24

1

2

3

4

5

6

7

8

9

10

11

12

VBATT

IPTAT\_SENSE

IZTAT\_SENSE

DRIVE\_G1

DRIVE\_G2

GND\_IO

VDD\_IO

DRIVE\_G3

DRIVE\_G4

SEL\_DRIVING

VG1

VG2

Figure 4‑1 KL85 Padring and Pinout

In the following table the 48 PADs of the KL85 and their coordinates are reported. All dimensions are provided at **CAD level (pre-shrink**). To get coordinates at silicon level, you need to apply the optical shrink factor (8%).

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Pin count** | **Name** | **Type** | **Description** | **X** | **Y** |
| 1 | VBATT | SUPPLY | Main input voltage supply for bandgap and current reference |  |  |
| 2 | IPTAT\_SENSE | ANALOG | Sensing of internal PTAT current reference |  |  |
| 3 | IZTAT\_SENSE | ANALOG | Sensing of internal ZTAT current reference |  |  |
| 4 | DRIVE\_G1 | DIG IN | Direct command for driver 1 |  |  |
| 5 | DRIVE\_G2 | DIG IN | Direct command for driver 2 |  |  |
| 6 | GND\_IO | GROUND | Ground for IOs |  |  |
| 7 | VDD\_IO | SUPPLY | Voltage supply for IOs |  |  |
| 8 | DRIVE\_G3 | DIG IN | Direct command for driver 3 |  |  |
| 9 | DRIVE\_G4 | DIG IN | Direct command for driver 4 |  |  |
| 10 | SEL\_DRIVING | DIG IN | Selector between internal/external commands for drivers |  |  |
| 11 | VG1 | DIG OUT | Pre-driver output 1 |  |  |
| 12 | VG2 | DIG OUT | Pre-driver output 2 |  |  |
| 13 | VG3 | DIG OUT | Pre-driver output 3 |  |  |
| 14 | VG4 | DIG OUT | Pre-driver output 4 |  |  |
| 15 | VBATT\_DRV | SUPPLY | Main input voltage supply for drivers |  |  |
| 16 | GND\_IO | GROUND | Ground for IOs |  |  |
| 17 | VDD\_IO | SUPPLY | Voltage supply for IOs |  |  |
| 18 | GND | GROUND | Analog and power and substrate ground |  |  |
| 19 | VS3 | ANALOG | Intermediate output voltage 3 |  |  |
| 20 | VOUT\_SENSE | ANALOG | Sensing of the output voltage |  |  |
| 21 | VOUT | ANALOG | Output voltage |  |  |
| 22 | VS1 | ANALOG | Intermediate output voltage 1 |  |  |
| 23 | VBATT\_PWR | SUPPLY | Main input voltage supply for output stage |  |  |
| 24 | ADT\_D4 | DIG IN | Additional dead time bit 4 |  |  |
| 25 | ADT\_D3 | DIG IN | Additional dead time bit 3 |  |  |
| 26 | ADT\_D2 | DIG IN | Additional dead time bit 2 |  |  |
| 27 | ADT\_D1 | DIG IN | Additional dead time bit 1 |  |  |
| 28 | ADT\_D0 | DIG IN | Additional dead time bit 0 |  |  |
| 29 | GND\_IO | GROUND | Ground for IOs |  |  |
| 30 | VDD\_IO | SUPPLY | Voltage supply for IOs |  |  |
| 31 | DT\_D4 | DIG IN | Dead time bit 4 |  |  |
| 32 | DT\_D3 | DIG IN | Dead time bit 3 |  |  |
| 33 | DT\_D2 | DIG IN | Dead time bit 2 |  |  |
| 34 | DT\_D1 | DIG IN | Dead time bit 1 |  |  |
| 35 | DT\_D0 | DIG IN | Dead time bit 0 |  |  |
| 36 | EXT\_CLK | DIG IN | External clock |  |  |
| 37 | SEL\_CLK | DIG IN | Selector between internal and external clock |  |  |
| 38 | SENSE\_OSC\_CLK | DIG OUT | Oscillator output |  |  |
| 39 | V1V8 | SUPPLY | Input voltage supply for 1.8V Circuits |  |  |
| 40 | SEL\_OPEN\_LOOP | DIG IN | Selector between closed and open loop regulation |  |  |
| 41 | SENSE\_CMP\_OUT | DIG OUT | Comparator output |  |  |
| 42 | GND\_IO | GROUND | Ground for IOs |  |  |
| 43 | VDD\_IO | SUPPLY | Voltage supply for IOs |  |  |
| 44 | VBATT\_COMP | SUPPLY | Main input voltage supply for comparator |  |  |
| 45 | RESET | DIG IN | Digital global reset (active low) |  |  |
| 46 | SEL\_INT\_REF | DIG IN | Reference Selector |  |  |
| 47 | OSC\_VCTRL | ANALOG | Oscillator control voltage |  |  |
| 48 | EXT\_REF\_SNS\_INT\_REF | ANALOG | External reference to bypass internal bandgap or sensing of internal reference |  |  |

Table 4‑1 KL85 Pin list