Objective

- Familiarization with Input-Output I-V relationship of MOS transistors through measured characteristic data.
- To know practical values of device model parameters

Components

- MOSFET
- Breadboard
- Resistors 1kΩ
- Potentiometers 10kΩ and 4kΩ range
- Connecting wires

Circuit Diagram

Observation Table

0.1 Id versus V_{DS} for Vgs=7.8V

Vds(V)	Id(mA)
1.53	12.02
1.78	12.01
1.97	11.83
2.14	11.54
2.24	11.29
2.31	11.05
2.36	10.88
2.45	10.54
2.55	10.13
2.63	9.78
2.7	9.38
2.77	9.04
2.81	8.86
2.87	8.57
2.91	8.19
2.98	7.81
3	7.67
3.06	7.27
3.11	6.98
3.17	6.55
3.22	6.14
3.3	5.64
3.4	4.99
3.43	4.57
3.51	4.11
3.61	3.83
3.59	3.46
3.64	2.94
3.69	2.6
3.74	2.08
3.78	1.7
3.85	1.22
3.94	0.99
4.1	0.8
4.88	0.54
5.86	0.41
6.3	0.38

0.2 Id versus V_{DS} for Vgs=9.7V

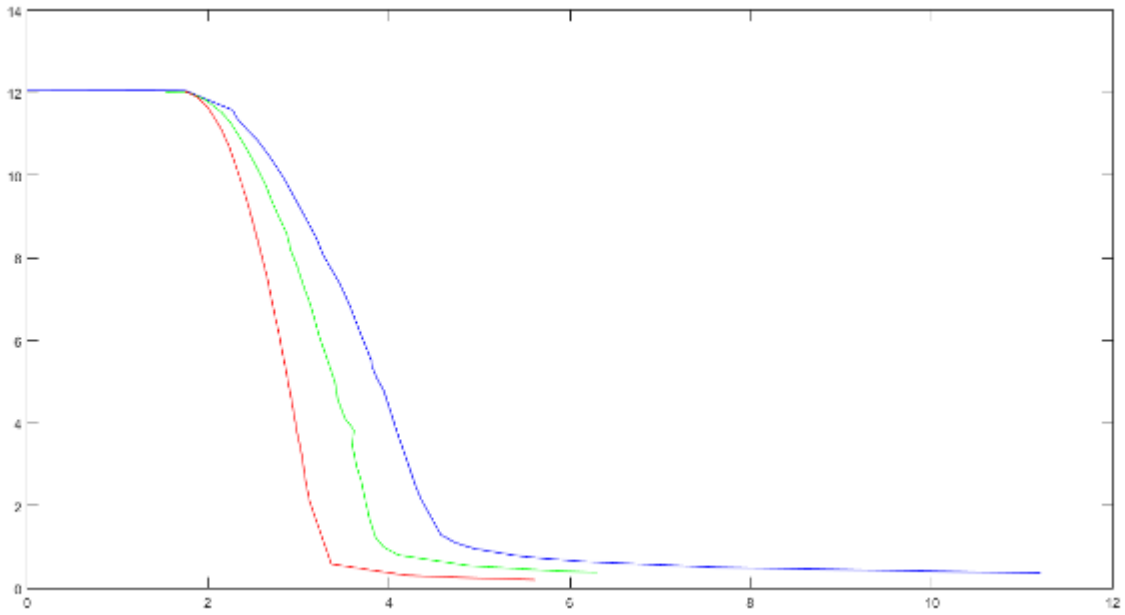
Vds(V)	Id(mA)
0.0	12.06
1.33	12.07
1.74	12.06
2.27	11.58
2.31	11.4
2.42	11.13
2.54	10.86
2.67	10.48
2.83	9.95
3.03	9.15
3.19	8.5
3.27	8.07
3.45	7.39
3.56	6.86
3.68	6.18
3.8	5.53
3.81	5.37
3.86	5.1
3.94	4.78
4.07	3.89
4.11	3.63
4.19	3.13
4.29	2.48
4.35	2.16
4.57	1.29
4.73	1.1
4.93	0.96
5.42	0.78
5.69	0.72
6.15	0.64
7.63	0.5
10.14	0.4
11.2	0.36

0.3 Id versus V_{GS} for Vds=6V

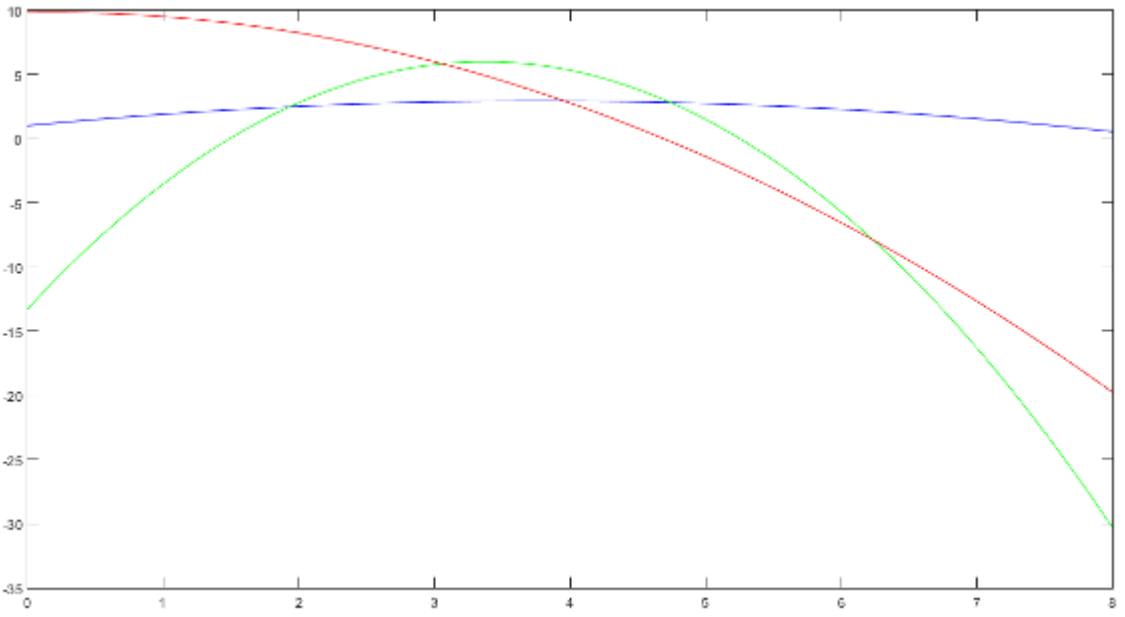
Vds(V)	Id(mA)
1.74	12.04
1.88	11.9
2.0	11.63
2.14	11.13
2.23	10.69
2.28	10.38
2.37	9.79
2.44	9.29
2.51	8.71
2.58	8.13
2.61	7.87
2.65	7.52
2.68	7.18
2.74	6.55
2.78	6.17
2.82	5.69
2.86	5.27
2.88	5.0
2.91	4.68
2.95	4.17
2.98	3.78
3.03	3.25
3.08	2.52
3.12	2.09
3.36	0.58
4.17	0.31
4.45	0.28
4.83	0.25
5.61	0.2

Plots

Plot of $V_{OUT} vs V_{IN}$



Gain versus



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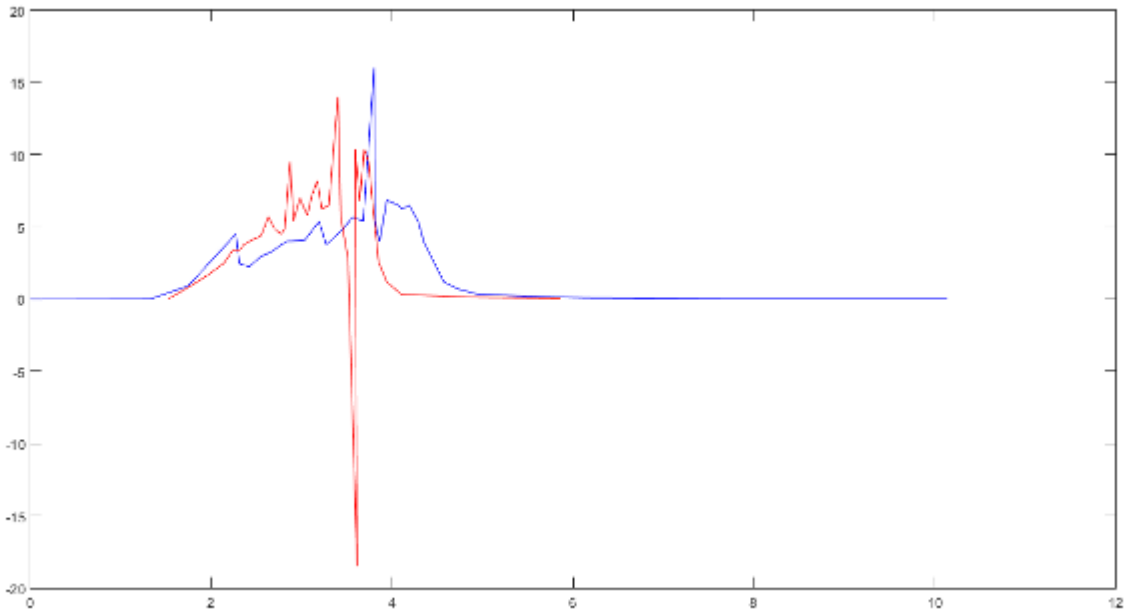
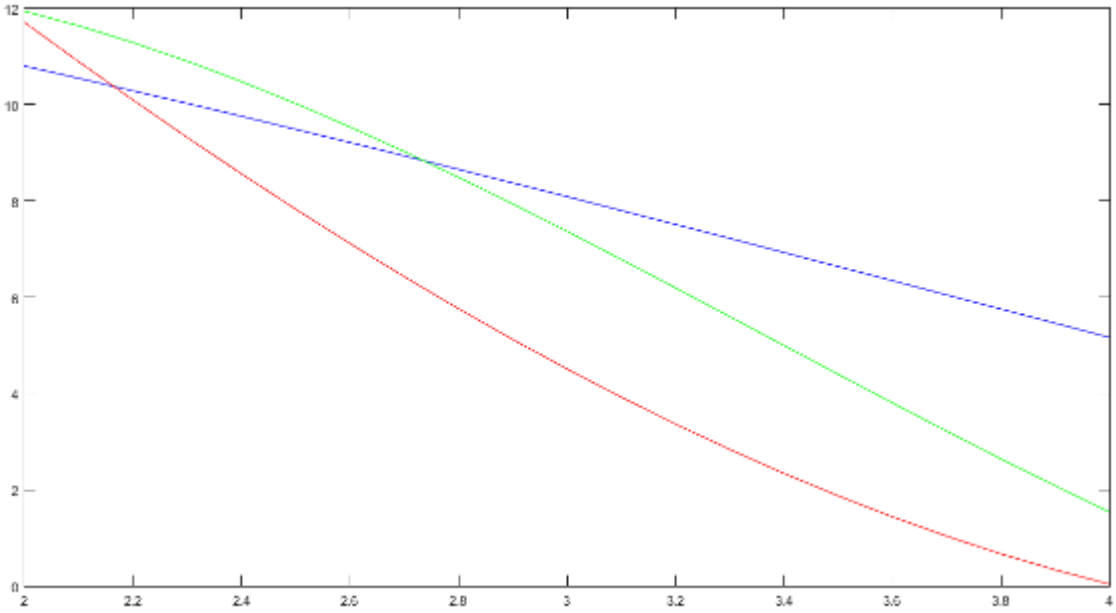
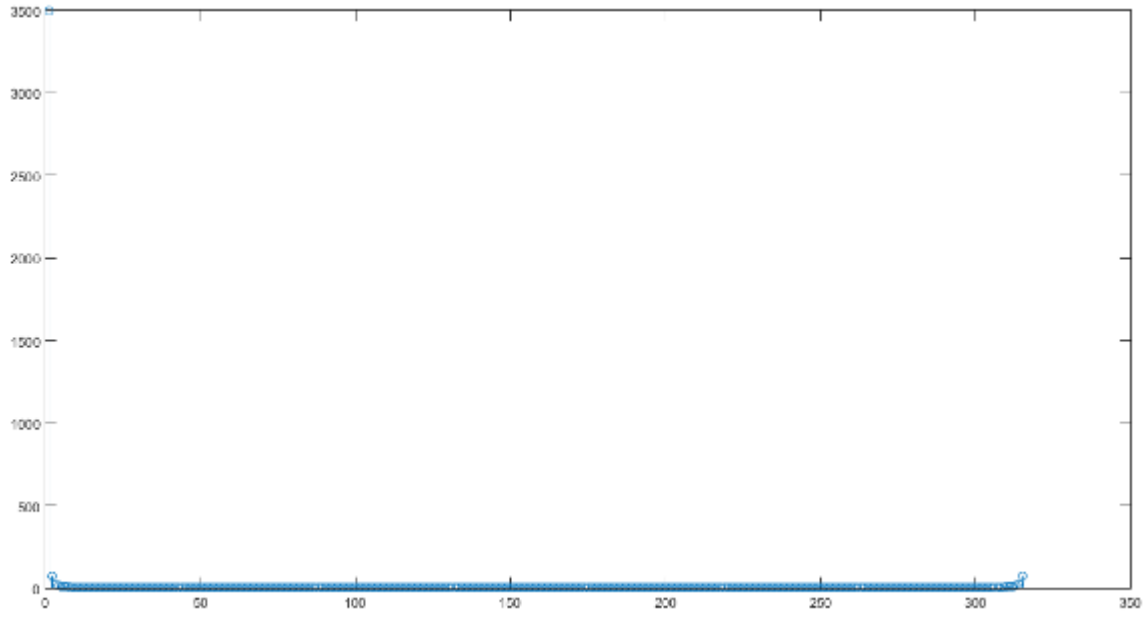


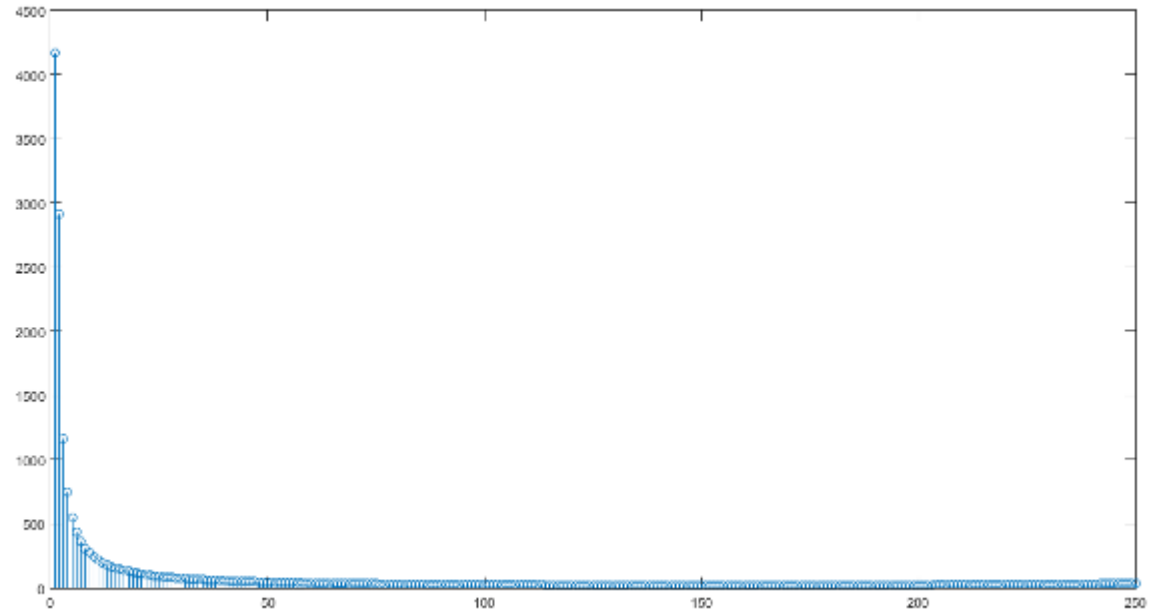
Gain versus


12
10
8
6
4
2
0
2
2.2
2.4
2.6
2.8
3
3.2
3.4
3.6
3.8
4

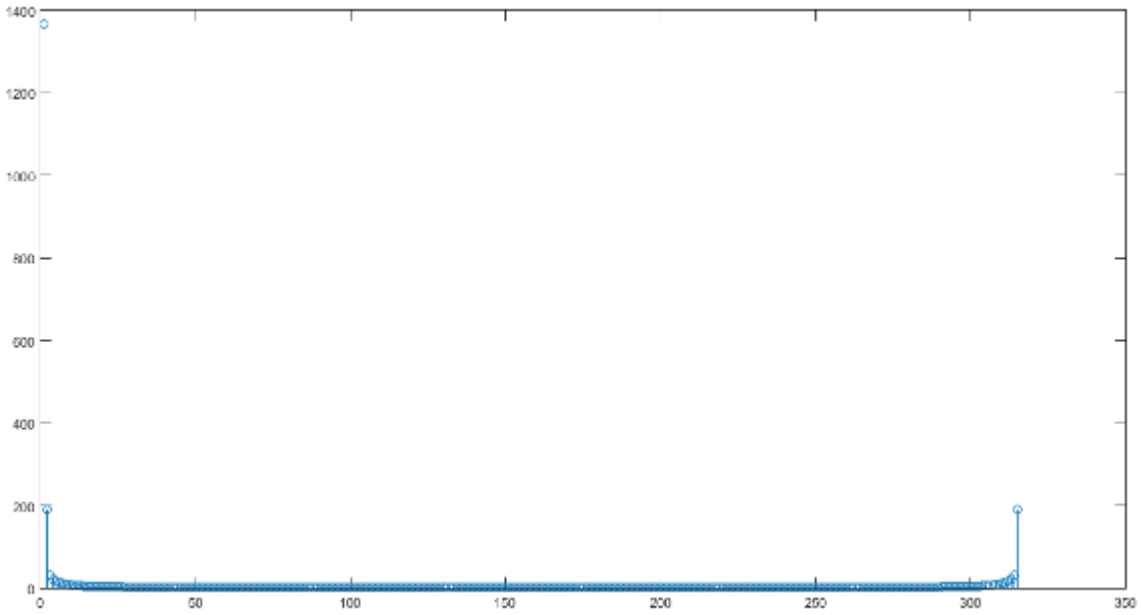
Gain versus


3500
3000
2500
2000
1500
1000
500
0
0
50
100
150
200
250
300
350

Gain versus



Gain versus



Results

THD values for

K_1^2	$\lambda(V^{-1})$	$g_d(mS)$
-9.59	0.104	0.72
-220.49	$4.5x10^{-3}$	$9.4x10^{-3}$
-358.19	$2.79x10^{-3}$	0.017

Large signal parameters from Id vs Vds plot

$V_{th}(V)$	k	$g_m(m\Omega)$
4.14	2.25	2.25

Discussion

14EC10043

From the characteristics we could observe that in the output characteristics as Vds increases the Id increases upto the transition point.

After the transition the curve didnt remain perfectly horizontal as expected and this due to the channel width modulation effect.

While measuring Id with respect to Vgs we must keep Vds constant in our experiment we must adjust the value of drain resistance to keep Vds constant it was found roughly constant

14EC10049

In the graph id vs Vds the nonzero slope even after in the saturation region gives the value of Va which is a negative value this non zero slope is due to the channel effect this is also known as channel length modulation

The additional resistance kept in the circuit other than the potentiometer is to avoid burning of transistor due to high drain current.

While do id vs Vgs we have to measure the value at constant Vds but in our experiment we can observe Vds decreasing this can be adjusted every time as precise as possible as the potentiometer range is not wide we can adjust upto some extent only. Chat Conversation End