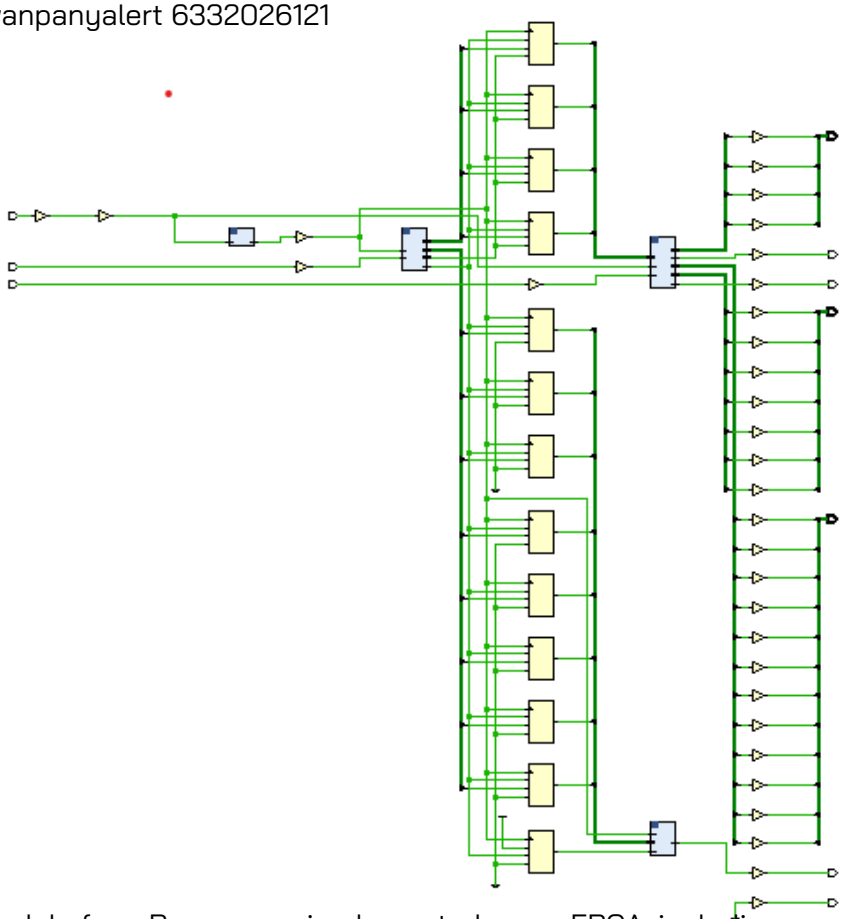
Kanawat Vilasri 6430001121, Paramaa Sawanpanyalert 6332026121

Pong Game Design

System schema



Modular design description

1. **Control module**
    a. **pong_top.v**: the top-level module for a Pong game implemented on an FPGA, including animated graphics, text displays, and timer.
    b. **pong_animated.v**: handles the animation and game logic, including movable bars controlled by player inputs, a bouncing ball, and detection of misses by players. In addition, the display color is shown based on game status, where is in progress or stopped.
2. **Display module**
    a. **Vga_core.v:** generates control signals for VGA display, including horizontal and vertical sync signals, pixel positions, and an on/off signal. It uses clock division to synchronize with a 25MHz clock, making it suitable for VGA applications.
    b. **Pong_text.v**: creates the text display for various elements in a Pong game spending on the game state and pixel coordinates.
    c. **Font_rom.v:** font directory used for displaying in our ping pon game
    d. **HexTo7Segment.v**: decodes 4-bit hexadecimal to 7-segment representing each digit
    e. **QuadSevenSeg.v**: controls multiplexer of 4 4-bit hexadecimal inputs to 4-digit 7-segment display. The digit and input selection are controlled by a state machine.
    f. **ClockDiv.v**: producing a clock signal at half frequency by dividing input clock frequency by 2
    g. **Timer.v**: acts as a 2-second timer, used during the resting period before restarting the game
3. **Serial/USB module (UART)**
    a. **Baudrate_gen.v**: generate baud signal at a maximum of 325 clock cycles, every toggling, and be configurated to achieve a baud rate of 9600 at 100 MHz clock
    b. **Transmitter.v**: receives 8-bit input data, an enable signal, and a clock signal through *din* line serially, transmits it via the *dout* line, and sends the flag when the transmission is accomplished.
    c. **Receiver.v**: reconstructs serial input (din) and the clock signal (clk) to 8-bit data (dout) and sets the received flag when the entire data frame is received. Moreover, the counting variable will track the bit positioning during the reception.