Transimpedance Amplifier (TIA) Design and PCB Implementation

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1 Transimpedance Amplifier (TIA) Design

1.1 Overview

A transimpedance amplifier (TIA) was designed using the previously implemented differential amplifier to convert input photocurrent into a proportional output voltage. The design targeted a transimpedance gain of 66 dBΩ, an output voltage swing of 1V, and robust performance in the presence of a 100 pF photodiode capacitance. The TIA utilized on-chip PDK resistors and was optimized for linearity, bandwidth, and stability. The design methodology was supported by both small-signal analysis and transient simulations, ensuring compatibility with practical optical front-end applications.

1.2 Design Specifications

- **Target Gain:** 66 dBΩ ($R_f \approx 2$ kΩ)
- **Output Swing:** 1 V
- **Photodiode Capacitance (C_{pd}):** 100 pF
- **Core Amplifier:** Differential amplifier with current mirror load

1.3 Design Considerations and Calculations

The core function of the TIA is governed by the feedback resistor R_f, which determines the gain:

$$V_{out} = -I_{in}R_f \quad \Rightarrow \quad R_f = \frac{V_{out,max}}{I_{in,max}} \tag{1}$$

The bandwidth is dominantly limited by the large photodiode capacitance at the input node:

$$f_{-3dB} = \frac{1}{2\pi R_f C_{pd}} \tag{2}$$

To ensure signal integrity under the high C_{pd} load, a high-gain, wide-bandwidth differential amplifier was employed. Special care was taken to ensure the output swing remained within the linear region of the amplifier to avoid clipping due to saturation.

1.4 Performance Summary

The transimpedance amplifier was designed using a feedback resistor from the PDK to achieve the target gain. The circuit provides a 1V output swing while driving a 100 pF photodiode capacitance. The key simulation results are summarized below:

- **Feedback Resistor (R_f):** 2.05 kΩ (PDK poly resistor)
- **Transimpedance Gain:** 66.26 dBΩ (≈2056.56 V/A)
- **Output Swing:** 0.90 V
- **Bandwidth (f_{-3dB}):** 2.26 MHz
- **Operating Region:** Strong Inversion, Saturation
- **Linearity:** Verified (no output clipping)

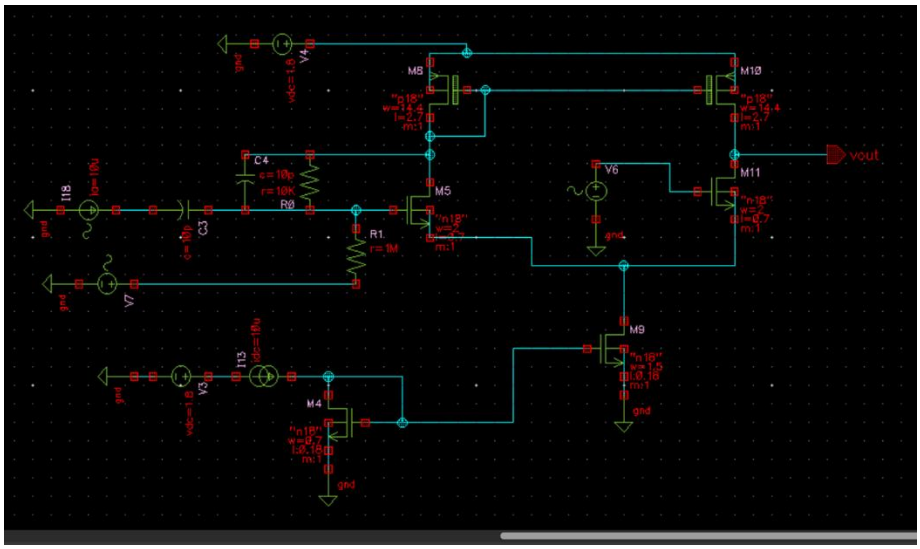

Figure 1 Schematic of the transimpedance amplifier

1.5 PVT Corner Analysis

The robustness of the design was verified across Process, Voltage, and Temperature (PVT) variations. Table 1 summarizes the gain stability under these conditions.

Table 1: PVT Analysis of Transimpedance Amplifier (TIA)

Process Corner	**Supply Voltage (V_{DD})**	**Temp (°C)**	**Gain (dBΩ)**
Nominal Condition			
TT	1.8 V	27	66.0
Varying V_{DD} (at Temp = 27°C, Process = TT)			
TT	1.6 V	27	56.2
TT	1.7 V	27	72.31
TT	1.9 V	27	57.61
TT	2.0 V	27	55.27
Varying Temperature (at V_{DD} = 1.8V, Process = TT)			
TT	1.8 V	-40	77.5
TT	1.8 V	0	69.52
TT	1.8 V	50	64.27
TT	1.8 V	85	60.19

Process Corners (at Nominal V_{DD} and Temp)			
SS	1.8 V	27	64.7
FF	1.8 V	27	58.1

Figure 2:Response of TIA showing Transimpedance Gain and Bandwidth.

2 PCB Design and Implementation

2.1 Overview

A printed circuit board (PCB) was designed in Altium Designer to facilitate hardware testing of the TIA. The layout includes an IC socket for modular testing of different TIA implementations and provisions for connecting a photodiode emulator or external current source.

2.2 Design Features

To replicate the behavior of a real optical front-end, the PCB incorporates:

- **Photodiode Emulator:** Additional components such as load resistors and variable capacitors (C_{pd}) to simulate the photodiode model.
- **IC Socket:** Allows for easy swapping of the fabricated chip without soldering.
- **Bias Control:** Provisions for stable biasing of the TIA core.

2.3 Altium Design Elements

The design process utilized the following key features of Altium Designer:

1. **Schematic Design:** Placement and logical connection of resistors, capacitors, and connectors.
2. **Component Placement:** Optimized arrangement to minimize trace lengths and signal interference.
3. **Routing:** Careful routing of signal paths to ensure integrity.
4. **Polygon Pour:** Used to create solid Ground (GND) and Power (VDD) planes for noise reduction and better thermal dissipation.

5. **Layer Stack:** A standard 2-layer board configuration was defined with a mechanical outline.

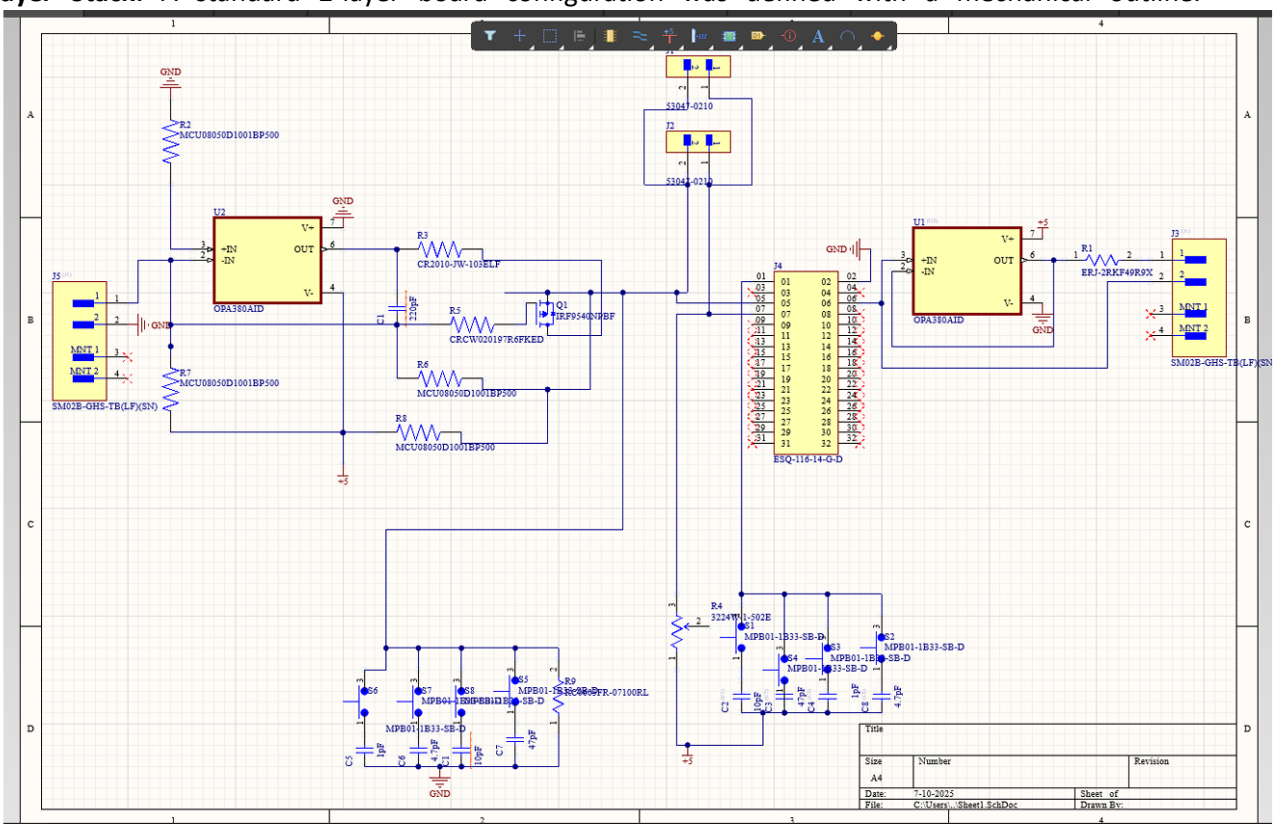

Figure 3 Schematic with photodiode emulator, bias control, feedback, and MCU interface.

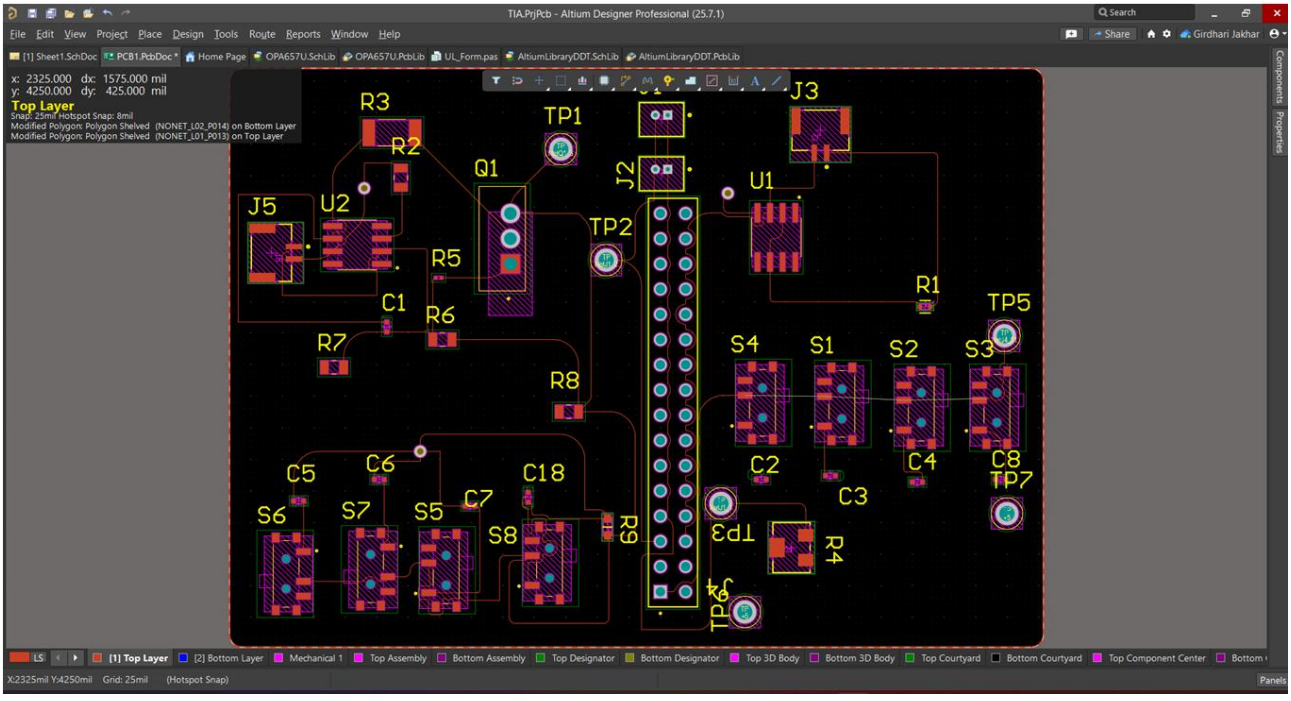

Figure 4 :2D top view of the PCB layout highlighting component placement

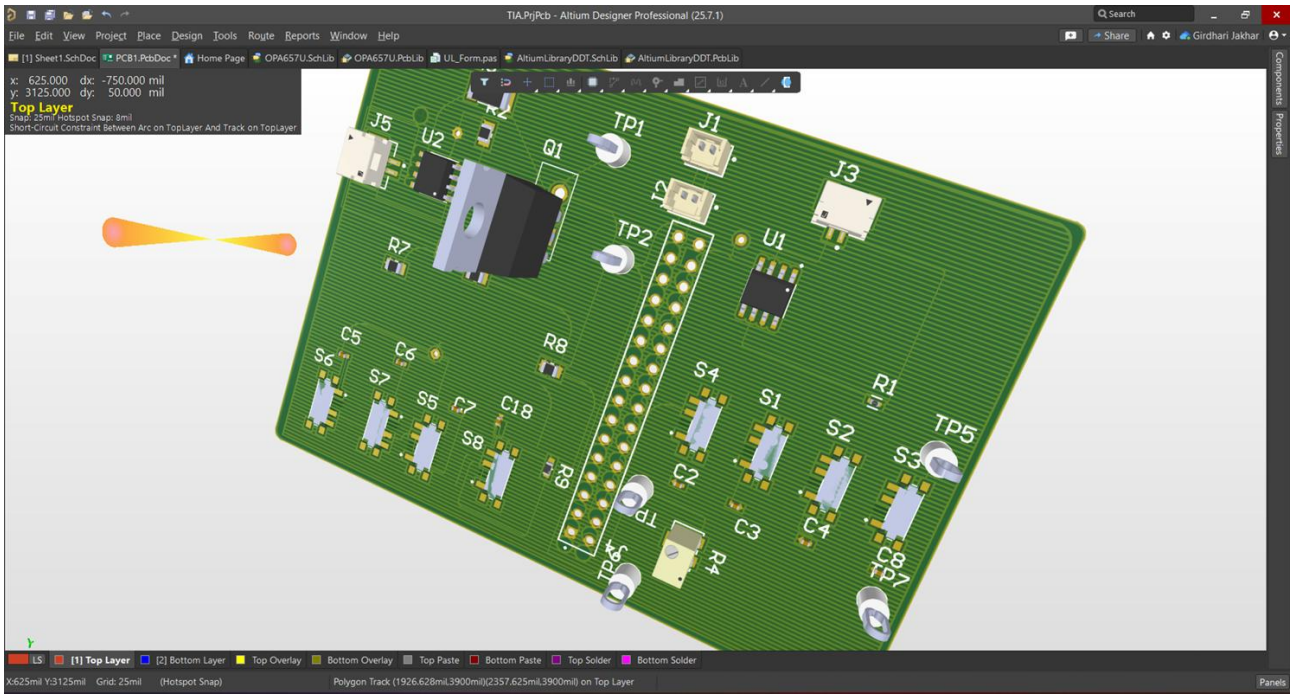

Figure5: 3D top view of the assembled PCB showing ICs, capacitors, connectors, and test points.