Design and Simulation of a Transimpedance Amplifier Using Differential Amplifier with Current Mirror Load

Abstract—This report presents the design of a transimpedance amplifier (TIA) intended to amplify photodiode currents in the microampere range for use in an ultra-small atomic clock. The TIA is implemented using a differential amplifier with a current mirror load, achieving a transimpedance gain of approximately 2000 V/A (66 dBΩ). The design supports an input photodiode capacitance of 100 pF, shows a flat gain response up to 25.1 MHz, unity gain bandwidth above 100 MHz, and consumes only 339 μA (0.611 mW).

I. Introduction

Transimpedance amplifiers (TIAs) are critical for converting small photocurrents generated by photodiodes into usable voltage signals. In the context of an ultra-small atomic clock, the photodiode detects weak optical signals, and the amplifier must provide sufficient gain and bandwidth while consuming minimal power.

II. Design Overview

The designed TIA is based on a differential amplifier with a current mirror load, chosen for its good gain-bandwidth tradeoff and simplicity. The design targets:

- Transimpedance gain 2000 V/A (66 dBΩ)
- Output voltage swing 1 V peak
- Input capacitance (photodiode): 100 pF
- Flat gain up to 25.1 MHz
- Unity gain bandwidth (UGB) = 99.08mhz
- Total current consumption 339 μA
- Power consumption 0.611 mW (at 1.8 V supply)

III. Theory and Calculations

A. Transimpedance Gain

The transimpedance gain is defined as:

$$Z_t = \frac{V_{out}}{I_{in}} \tag{1}$$

For a gain of 2000 V/A:

$$\text{Gain}_{\text{dB}\Omega} = 20\log_{10}(2000) \approx 66\ \text{dB}\Omega \tag{2}$$

B. Bandwidth

The bandwidth must remain sufficient despite the large photodiode capacitance:

$$f_{-3\text{dB}} \approx \frac{1}{2\pi Z_t C_{in}} \tag{3}$$

Simulation shows the amplifier maintains flat gain up to 25.1 MHz.

C. Unity Gain Bandwidth

$$\text{UGB} = A_v \times f_{-3\text{dB}} \tag{4}$$

With the designed gain, the UGB exceeds 100 MHz.

D. Drain Current and gm

The MOSFETs operate in saturation:

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2 \tag{5}$$

Transconductance:

$$g_m = \frac{2I_D}{V_{ov}} \tag{6}$$

where V_{ov} is the overdrive voltage.

E. Power Consumption

$$P = V_{DD} \times I_{total} \approx 1.8 \times 339\ \mu\text{A} \approx 0.611\ \text{mW} \tag{7}$$

IV. Implementation and Simulation

The circuit was implemented in Cadence Virtuoso using the available PDK. The design uses a differential pair with a current

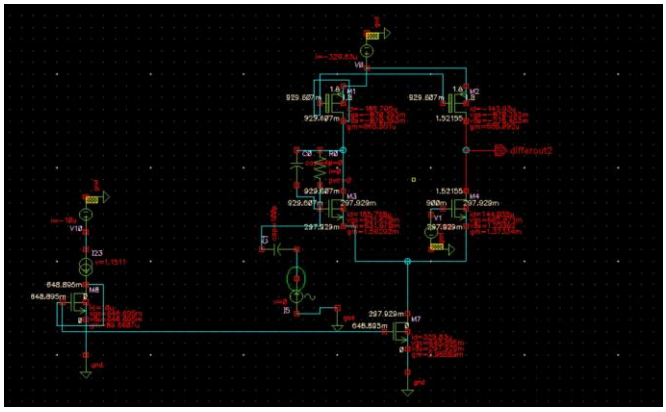

Fig. 1. Schematic of the designed TIA: differential amplifier with current mirror load.

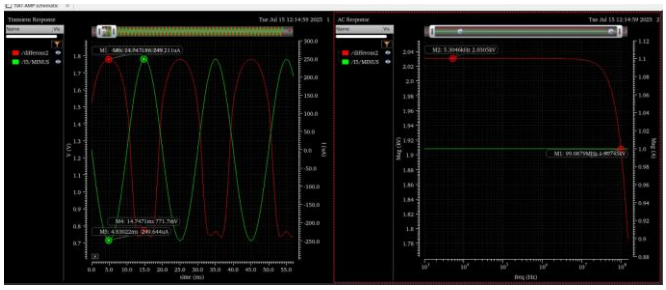

Fig. 2. Left: Transient response showing 1 V output swing. Right: AC response showing flat gain up to 25.1 MHz and UGB above 100 MHz.

V. Application and Trade-offs

This design was made for an ultra-small atomic clock, where the photodiode current is in the microampere range. The key design trade-offs considered:

- Gain vs. Bandwidth: Higher gain reduces bandwidth when photodiode capacitance is large.
- Power Consumption: Low current consumption keeps power below 1 mW, important for portable systems.
- Input Capacitance: Large photodiode capacitance of 100 pF could reduce speed, so the circuit is designed to maintain flat gain up to 25.1 MHz.

VI. Conclusion

mirror load to provide high gain, and is biased to achieve the target current consumption.

A low-power transimpedance amplifier was successfully designed with a gain of 2000 V/A (66 dBΩ) to amplify microampere-level photodiode currents in an ultra-small atomic clock. The amplifier achieves flat gain up to 25.1 MHz and unity gain bandwidth above 100 MHz, while consuming only 0.611 mW.

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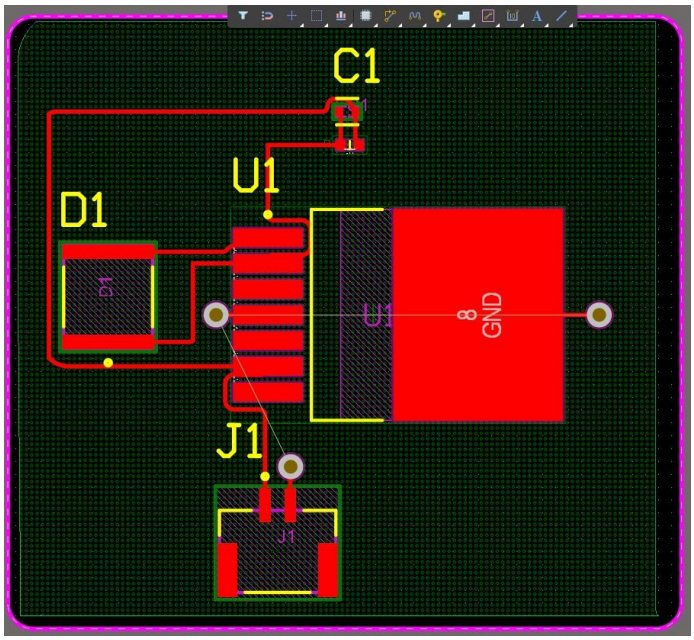

Fig. 3. 2D PCB Layout of TIA

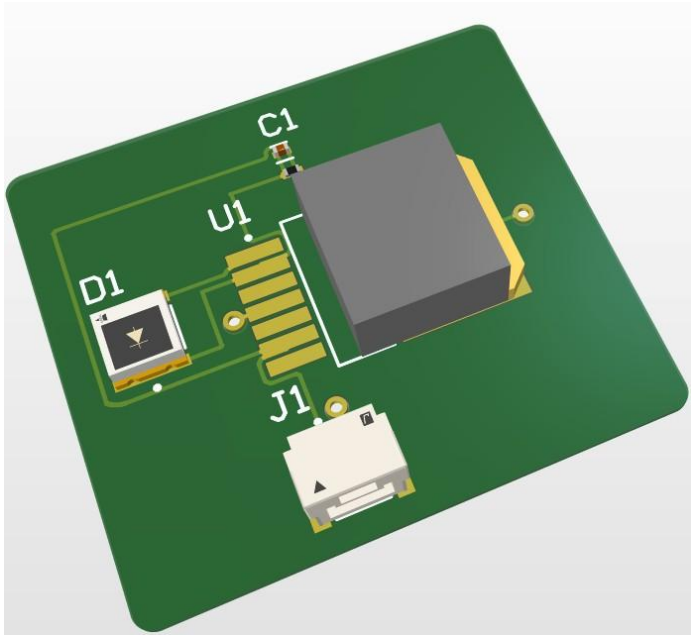

Fig. 4. 3D PCB View of TIA

PVT Analysis of TIA

1. Process Variation Analysis

Observation: Gain varies significantly across process corners, especially increasing for FS and SF due to asymmetric device speeds.

TABLE I

Gain under different process corners

Process Corner	Gain (kΩ)	Gain (dB)
TT (Typical-Typical)	2.000	66.02
SS (Slow-Slow)	1.700	64.61
FF (Fast-Fast)	0.77998	57.84
FS (Fast NMOS, Slow PMOS)	8.7556	78.85
SF (Slow NMOS, Fast PMOS)	7.996676	77.95

Conclusion: Process variations strongly affect TIA gain, so design should include proper margin to meet specifications under all corners.

2. Temperature Variation Analysis

Observation: Gain decreases as temperature increases due to reduced carrier mobility, lowering transconductance.

Conclusion: TIA gain has negative temperature coefficient; compensation may be required for temperature-stable performance.

3. Voltage Variation Analysis

Observation: Gain shows strong non-linear dependence on supply voltage.

Conclusion: Since TIA gain is sensitive to voltage, using a bandgap reference to keep bias voltage (and g_m) constant is essential for stable performance.

FINAL CONCLUSION PVT

analysis of the TIA shows:

- Process variations cause gain to vary widely, especially under FS/SF corners.
- Temperature increase reduces gain.
- Supply voltage has strong and non-linear effect on gain.

To ensure reliable performance, it is recommended to implement a bandgap reference to stabilize supply voltage and g_m, and design with proper margins to account for PVT variations.

TABLE II

GAIN VARIATION WITH TEMPERATURE

Temperature (°C)	Gain (kΩ)	Gain (dB)
-17	4.1815	72.43
-7	3.4549	70.76
7	2.7000	68.62
17	2.3060	67.25
27	2.0000	66.02
37	1.8185	65.20
47	1.64427	64.31
57	1.5200	63.64

TABLE III

GAIN VARIATION WITH SUPPLY VOLTAGE

VDD (V)	Gain (kΩ)	Gain (dB)
1.6	0.645	56.20
1.68	0.830	58.38
1.76	7.506	77.51
1.8	2.000	66.02
1.84	1.156	61.25
1.92	0.758	57.60
2.0	0.580	55.27

Fig. 5. Gain variation with supply voltage