PVT ANALYSIS AND COMPARISON OF 3 INVERTER AND 5 INVERTER RING VCO

Introduction

In this project, we designed and simulated a 3-inverter ring voltage-controlled oscillator (VCO) using SCL 180nm technology. The objective was to study how frequency depends on transistor sizing, process variation, supply voltage, and temperature (PVT analysis). We measured the delay of each inverter and observed how it affects the oscillation frequency.

Theory of Ring Oscillator

A ring oscillator is built from an odd number of inverters connected in a loop. The output of the last inverter feeds back to the input of the first inverter. Because of the odd number of inversions, the circuit cannot remain in a stable DC state, and oscillation occurs naturally.

For a ring oscillator with N stages, the fundamental oscillation frequency is:

$$f = \frac{1}{2N \cdot t_p}$$

where:

- t_p = propagation delay of a single inverter
- N = number of stages (odd)

Since $N = 3$ in this design, the frequency primarily depends on the inverter delay, which in turn depends on the transistor sizing and supply voltage.

The delay of each inverter can be approximated by:

$$t_p \approx k \cdot \frac{C_L \cdot V_{DD}}{I_{drive}}$$

where:

- C_L = load capacitance
- V_{DD} = supply voltage
- I_{drive} = average drive current of the transistors
- k = technology and design-dependent constant

By reducing C_L, increasing V_{DD}, or increasing transistor drive strength (by proper sizing), t_p can be reduced, leading to a higher oscillation frequency.

Process Corners Explained

In semiconductor manufacturing, process variations cause parameters like threshold voltage (V_{th}) and mobility (μ) to differ from their nominal values. To account for this, simulations are run under standard process corners:

- **TT (Typical-Typical):** Both NMOS and PMOS devices have nominal characteristics.
- **FF (Fast-Fast):** Both NMOS and PMOS are faster than nominal (lower V_{th}, higher mobility).
- **SS (Slow-Slow):** Both NMOS and PMOS are slower (higher V_{th}, lower mobility).
- **SF (Slow NMOS, Fast PMOS):** NMOS devices are slower, PMOS are faster.
- **FS (Fast NMOS, Slow PMOS):** NMOS devices are faster, PMOS are slower.

Fast process corners result in higher frequencies due to faster switching, while slow corners produce lower frequencies.

Design Details

- Technology: SCL 180nm
- Topology: 3-stage CMOS inverter ring oscillator
- PMOS: Width = 0.84μm, Length = 0.18μm
- NMOS: Width = 0.42μm, Length = 0.18μm

We calculated the inverter delay and simulated its effect on the oscillation frequency.

Delay Calculation

For the TT process at room temperature, the observed frequency was approximately:

$$f = 5.62454GHz$$

Since:

$$t_p = \frac{1}{2Nf}$$

with $N = 3$, we get:

$$t_p = \frac{1}{2 \times 3 \times 5.62454 \times 10^9} \approx 29.6ps$$

This delay matches the expected range for a 3-inverter ring oscillator in 180nm technology.

Simulation Results

1. Process Variation Analysis

Table 1: Frequency under different process corners

Process Corner	**Frequency (GHz)**
TT (Typical-Typical)	5.62454
SS (Slow-Slow)	4.23679
FF (Fast-Fast)	7.2218
FS (Fast NMOS, Slow PMOS)	5.33614
SF (Slow NMOS, Fast PMOS)	6.14481

Observation: Frequency increases at fast corners and decreases at slow corners.

2. Effect of Changing Transistor Dimensions

- Doubling length ($L = 0.36\mu$m): frequency reduced to 2.0053 GHz.
- Doubling width ($W_{PMOS} = 1.68\mu$m, $W_{NMOS} = 0.84\mu$m): frequency reduced to 1.96 GHz.

Reason: Larger transistors increase capacitance, which increases delay and lowers frequency.

3. Temperature Variation Analysis

Table 2: Frequency variation with temperature

Temperature (°C)	**Frequency (GHz)**
-50	6.37417
-40	6.26372
-30	6.16000
-20	6.05570
-10	5.96053
0	5.86573
10	5.77160
20	5.68428
30	5.59936
40	5.51740
50	5.43725
60	5.36086
70	5.28632
80	5.21406
90	5.14390
100	5.07671
150	4.77830

Observation: Frequency decreases as temperature increases because carrier mobility drops, increasing inverter delay.

4. Voltage Variation Analysis

Table 3: Frequency variation with supply voltage

VDD (V)	Frequency (GHz)
1.6	4.798
1.65	5.0146
1.7	5.22373
1.75	5.429
1.8	5.624
1.85	5.872
1.9	6.000
1.95	6.18
2.0	6.353

Observation: Frequency increases with VDD since higher supply voltage improves transistor drive strength, lowering delay.

Figures

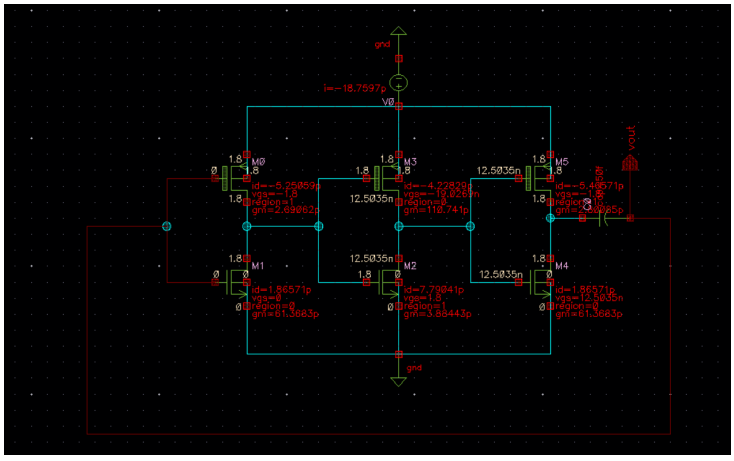

Figure 1: Schematic of the 3-inverter ring VCO

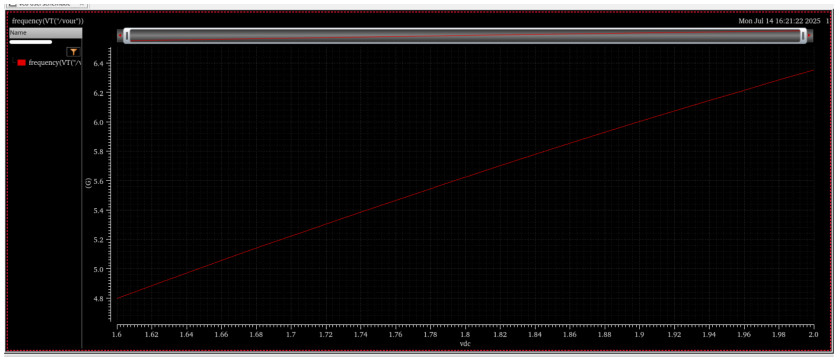

Figure 2: Graph showing frequency variation with supply voltage

Conclusion

The designed 3-inverter ring VCO achieved a nominal frequency of **5.624 GHz** at room temperature in the TT process.

- Frequency decreases with increased temperature.
- Frequency increases with higher VDD.
- Larger transistor sizes increase delay, lowering frequency.

PVT analysis confirms the importance of accounting for process, voltage, and temperature variations in robust VCO design.

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5-Inverter VCO: PVT Analysis

Process Variation

Table 4: Frequency variation under process corners

Process Corner	**Frequency (GHz)**
TT (Typical-Typical)	3.27
SS (Slow-Slow)	2.46
FF (Fast-Fast)	4.19

Conclusion: The frequency varies under different process corners, but 5-inverter VCO shows improved stability compared to 3-inverter VCO.

Temperature Variation Analysis

Table 5: Frequency variation with temperature

Temperature (°C)	**Frequency (GHz)**
-40	3.65229
-20	3.52830
0	3.41379
27	3.27110
50	3.15984
75	3.04802
100	2.94501
125	2.85084

Conclusion: As temperature increases, the oscillation frequency decreases due to reduced carrier mobility.

Voltage Variation Analysis

Table 6: Frequency variation with supply voltage

VDD (V)	**Frequency (GHz)**
1.62	2.8400
1.67	2.9685
1.72	3.0880
1.75	3.1580
1.82	3.3150
1.87	3.4200
1.92	3.5290
1.97	3.63072

Conclusion: Frequency shows a positive correlation with supply voltage; increasing VDD increases frequency.

Final Conclusion

By increasing the number of inverters from 3 to 5:

- Oscillation frequency decreases (from ≈5.6 GHz to ≈3.2 GHz).
- Stability to PVT variations improves significantly.

This demonstrates the trade-off between frequency and robustness in ring oscillator design.