Study of the Excess SEE in the Second Chip in a Series

Kathryn D. Huff

***Abstract*-This work investigates the cause of and solution to excess SEE (Single Event Effects) in the second chip in a series at the WNR (Weapons Neutron Research) ICE (Irradiation of Chips and Electronics) House facility. These calculations are made with the use of a nuclear interaction code (MCNPX: Monte Carlo N-Particle version X).**

I. Introduction

At high altitudes, and especially near the poles of the Earth where the magnetic fields attract charged particles from the cosmos, electronics suffer the effects of cosmic rays, neutron-rich particle showers created by the collisions of protons and gamma rays from space with the nuclei of atoms in our atmosphere. We now know these effects as Single Event Effects. When a neutron collides with the nucleus of an atom such as silicon, the ionization can cause enough of an imbalance in the silicon that an error can occur in the electronic system that has been bombarded with the cosmic rays [1]. It is now known that SEE can cause major problems for the electronics industries, avionics industries, and space programs internationally. So, at Los Alamos National Laboratory the LANSCE 3 (Los Alamos Neutron Science Center) group simulates cosmic rays to perform Single Event Effects research, and international companies like Hitachi, Infineon, Sony, Honeywell, Altera, and SAAB come to LANSCE 3 to test the reliability of their products with the spallation neutrons at the ICE House facility, and consult the experts in the field. Also, institutions such as Prairie View A&M and NASA come to test electronics and other materials such as spacesuit fabric and metal hydride shielding. The experimenters analyze the number and location of errors in their products and the LANSCE 3 physicists collaborate with them, providing the neutron flux for that experiment, so that an "errors per neutron" rate can be calculated.

During these experiments, a phenomenon was discovered in which the second chip of the series stacked in a row in line with the neutron beam suffered more SEE than the first. The underlying theory was that the neutron collisions with the silicon nuclei caused a shower of particles including high levels of some highly interactive particle, such as a proton. The purpose of this study is to investigate this phenomenon in a detailed manner from which a real solution can be reached. MCNPX was used to determine the flux and energy of the particles generated by the neutron interactions with the first chip, and the paths of these particles with respect to how they scatter away from the chips.

II. Monte Carlo Simulation

MCNPX is a general Monte Carlo N-Particle transport code that was used to measure the particle flux behind the first chip at varying distances. The chip model was derived from the model used by the team writing "SEU (Single Event Upset) Sensitivity of Bulk and SOI (Silicon on Insulator) Technologies to 14 MeV Neutrons". The chip is structured in three basic layers:

1) A .01 cm. polysilicon layer
2) A .125 cm. silicon dioxide (SiO_2) layer
3) A .365 cm. silicon layer

The chip modeled was a rectangular prism with a length of 5.08 cm., height of 5.08 cm., and width of .5 cm. [2]. This chip was centered on the X-axis along which was aligned the simulated neutron beam source characteristic of the ICE House beam. The flux and energy range of this source was defined by a histogram detailing a typical day of beam segmented into 51 energy bins from 0 to 810 MeV. With this information, the geometry, materials, densities, source, and desired measurements (tallies) were defined.

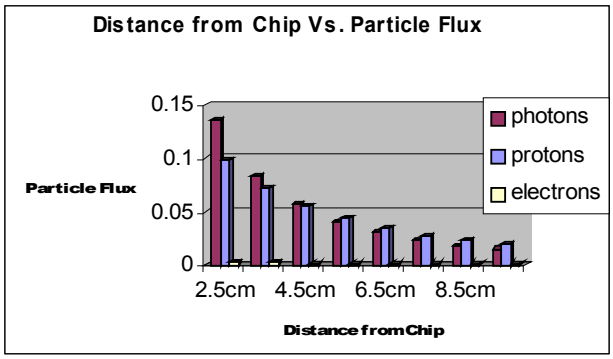

Fig. 1 Distance from Chip vs. Particle Flux (note: only 2.5 – 9.5 cm. shown for more detail)

In the first runs of MCNPX only the first 10 cm., in 10 segments of 1 cm. width each were measured to determine the particle or particles at fault in the errors incurred in the second chip, which is typically placed within a few centimeters of the first. In these calculations it was found that while photons, protons, and electrons were produced in high amounts, the photons and electrons scattered quickly out of the range of the solid angle of the second chip. However, the protons had a high

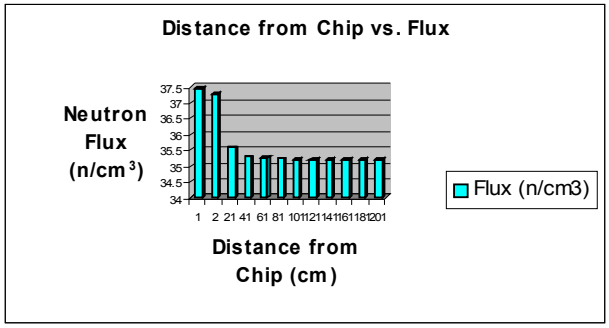

Fig. 2 Distance from Chip vs. Neutron Flux (note stabilization)

flux that scattered slowly, and from this it was determined that the protons cause the excess SEE.

These runs of MCNPX also determined that the neutron flux (fig. 2) drops in the first centimeter but then remains steady at a flux rate comparable to the original source. Note that the Y-axis scale is unimportant because it reflects the length of time spent running the MCNPX calculations. MCPX calculates these numbers by measuring the number of particles that pass through a cell and then dividing by the volume of the cell.

This data shows that spacing could be a viable option depending on the distance in which the neutron flux and energy range remains steady and the distance it takes for the proton flux to become very low. The proton level is determined by the sensitivity of electronics to proton flux. Therefore, the neutron and proton fluxes and

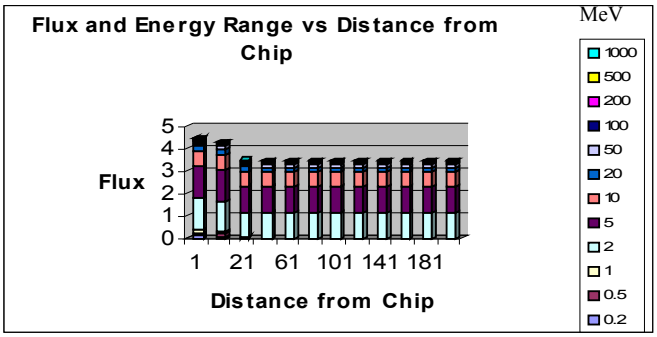

Fig. 3 Flux and Energy Range vs. Distance from chip (to two meters past the chip)

energies were measured again, but this time, the measurements were extended to a distance of 2 meters past the chip.

These results (fig. 3) showed that after about 15 cm. the neutron flux remains completely steady for the remainder of two meters.

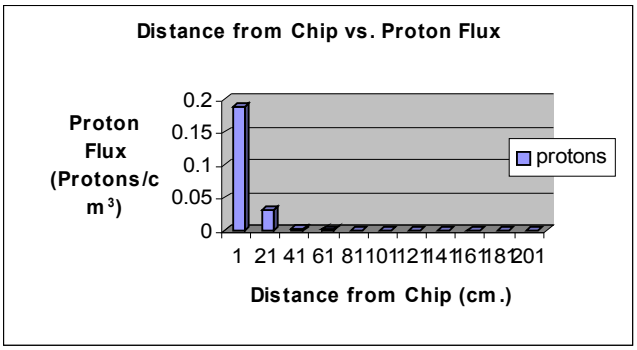

Fig. 4 Distance from Chip (cm.) vs. Proton Flux (Protons/cm^3)

The proton flux (fig. 4), however, drops significantly after 21 cm., and so, it can be determined that if the energy range of the protons at approximately 30 cm. past the chip is low, it would be feasible to use 30 cm. spacing. This would cause the entire set of chips, typically about 10, to stretch for 3 meters, which, while slightly awkward, is a realistic setup.

To determine the distance that would be best between each chip, information on the proton sensitivity of electronics is necessary. According to a study done by scientists at CERN and INFN led by F. Faccio, the proton SEU cross-section drops dramatically below 10 MeV [3]. Thus, if the proton energy range has a peak below 10 MeV, it is yet possible to solve this problem with spacing.

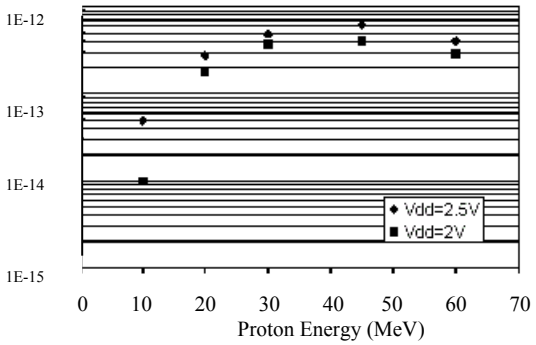

Fig. 5 : Proton Energy vs. SEU cross-section (σ[cm2/bit]) in an SRAM subject.
F. Faccio, K. Kloukinas, G. Magazzù, A. Marchioro, "SEU effects in registers and in a Dual-Ported Static RAM designed in a 0.25 µm CMOS technology for applications in the LHC", p. 5, http://lebwshop.home.cern.ch/lebwshop/LEB99_Book/Paperonly

Therefore, the energy range of the protons (fig. 6) was tallied, and it was discovered that the peak proton energy between 21 cm. and 41 cm. from the chip is less than 10 MeV. Also since there are far fewer protons in the higher energy ranges in that distance segment than at any closer to the chip, it is feasible that this will reduce the error rate caused by protons by a factor of at least 100.

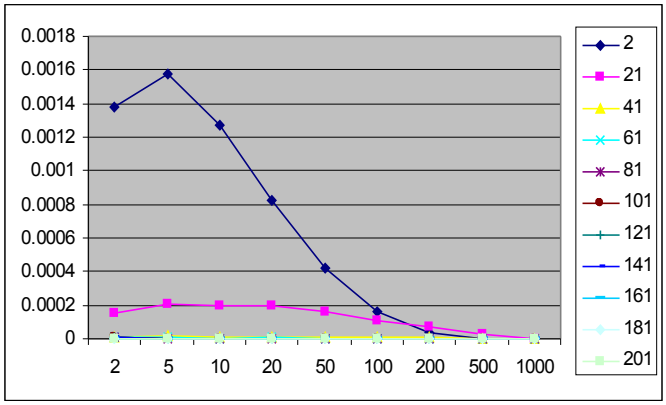

Fig. 6 Proton Energy vs. Flux (different colors indicate distances from chip)

III. Conclusion

This paper analyzes the particle shower resultant of neutron collisions with a silicon based chip bombarded with a neutron beam characteristic of the 30L ICE House

beam at the LANSCE 3 WNR facility at Los Alamos National Laboratory. In particular this paper has shown that:

- The high observed error rate in the second chip of the series can be attributed to protons in the particle shower produced by neutron-silicon interactions in the first chip.
- The neutron flux remains stable throughout the span of 2 meters past the silicon based chip in question, therefore allowing spacing of experimental chips up to that length.
- The proton flux lowers significantly after a length of approximately 30 cm., and so that has been determined as the most efficient spacing distance.

After reviewing all of the data and consulting other members of the LANSCE 3 staff, the conclusion was reached that a spacing of approximately 30 cm. between each chip will solve the problem.

References

[1] J. F. Ziegler, "Terrestrial Cosmic Ray Intensities," *IBM J. RES. DEVELOPMENT*, vol. 42 No. 1, pp. 117-126, Jan. 1998.

[2] Gasiot, Ferlet-Cavrois, Baggio, Roche, Flatresse, Guyot, Morel, Bersillon, and Pontcharra, "SEU Sensitivity of Bulk and SOI Technologies to 14-MeV Neutrons," *IEEE Transactions on Nuclear Science*, vol. 49, No. 6, p 3035, Dec 2002.

[3] F. Faccio, K. Kloukinas, G. Magazzù, A. Marchioro, "SEU effects in registers and in a Dual-Ported Static RAM designed in a 0.25 μm CMOS technology for applications in the LHC", p. 5, http://lebwshop.home.cern.ch/lebwshop/LEB99_Book/Paperonly/Faccio.pdf.