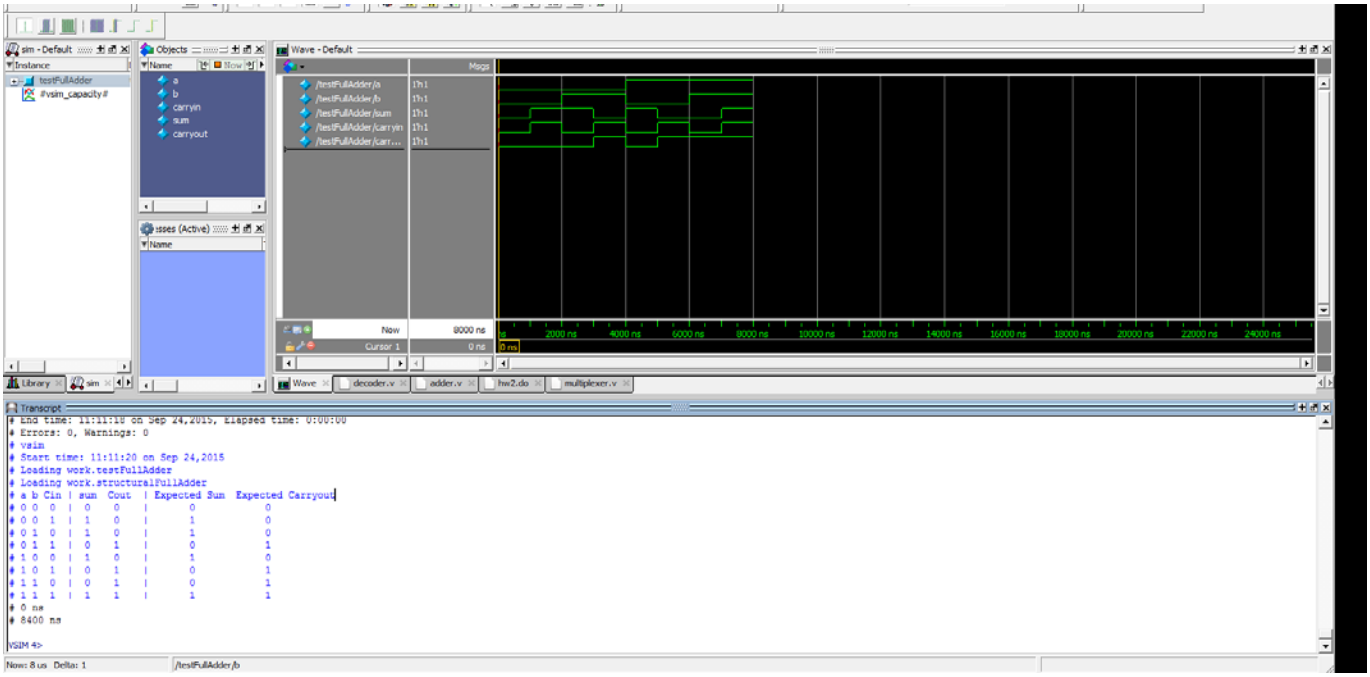
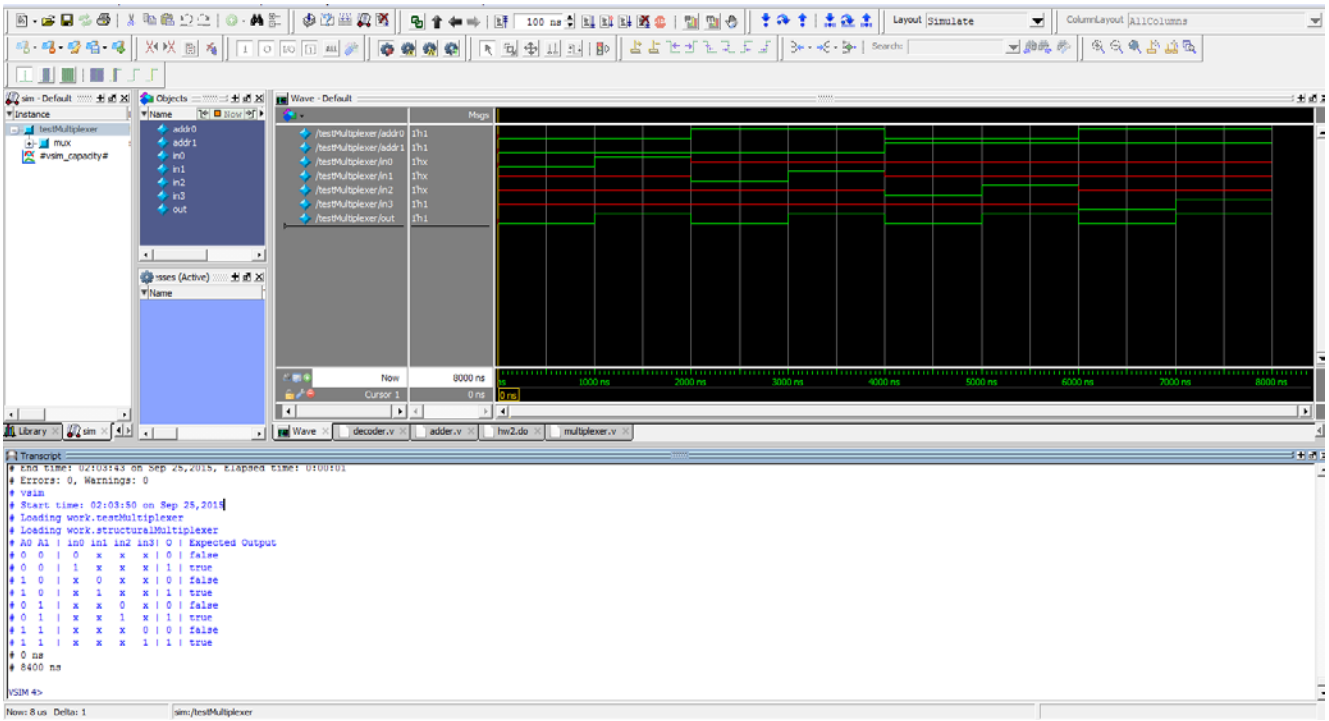
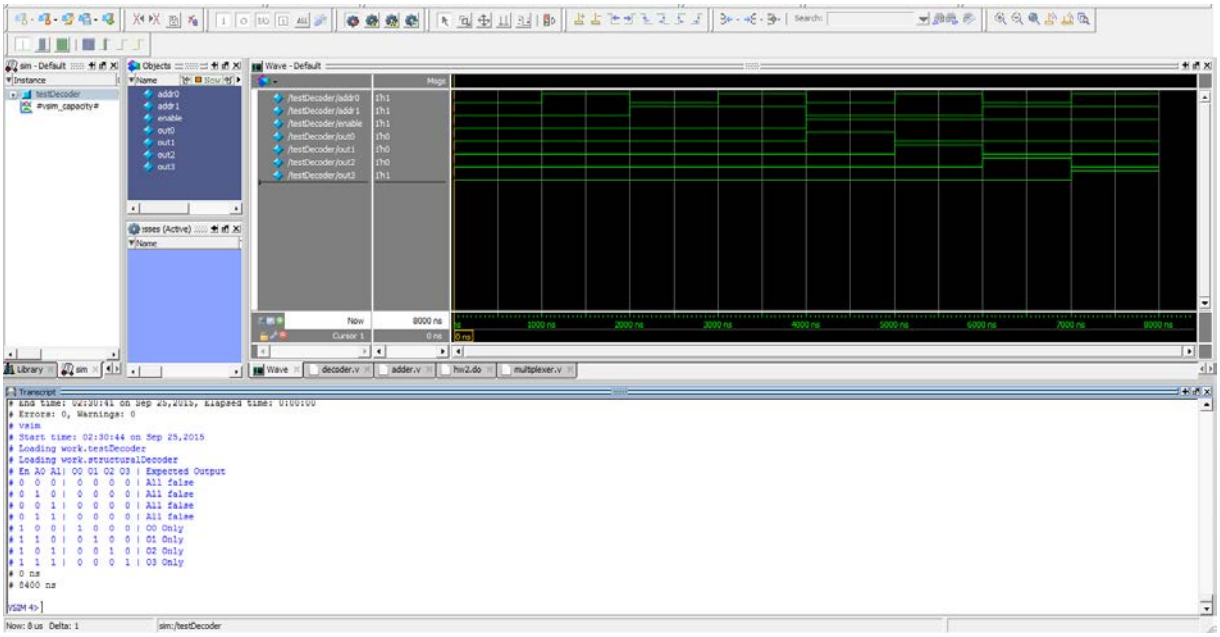

Wave - Default
Objects
sim - Default
Instance
testFullAdder
#vsim_capacity#
a
b
carryin
sum
carryout
/testFullAdder/a
/testFullAdder/b
/testFullAdder/sum
/testFullAdder/carryin
/testFullAdder/carr...
Now
8000 ns
Cursor 1
0 ns
Transcript
End time: 11:11:18 on Sep 24,2015, Elapsed time: 0:00:00
Errors: 0, Warnings: 0
vsim
Start time: 11:11:20 on Sep 24,2015
Loading work.testFullAdder
Loading work.structuralFullAdder
a b Cin | sum Cout | Expected Sum Expected Carryout
0 0 0 | 0 0 | 0 0
0 0 1 | 1 0 | 1 0
0 1 0 | 1 0 | 1 0
0 1 1 | 0 1 | 0 1
1 0 0 | 1 0 | 1 0
1 0 1 | 0 1 | 0 1
1 1 0 | 0 1 | 0 1
1 1 1 | 1 1 | 1 1
0 ns
8400 ns
VSIM 4>
Now: 8 us Delta: 1
/testFullAdder/b


Wave - Default
Objects
sim - Default
Instance
testMultiplexer
mux
#vsim_capacity#
addr0
addr1
in0
in1
in2
in3
out
/testMultiplexer/addr0
/testMultiplexer/addr1
/testMultiplexer/in0
/testMultiplexer/in1
/testMultiplexer/in2
/testMultiplexer/in3
/testMultiplexer/out
Now
8000 ns
Cursor 1
0 ns
Transcript
End time: 02:03:43 on Sep 25,2015, Elapsed time: 0:00:01
Errors: 0, Warnings: 0
vsim
Start time: 02:03:50 on Sep 25,2015
Loading work.testMultiplexer
Loading work.structuralMultiplexer
A0 A1 | in0 in1 in2 in3| O | Expected Output
0 0 | 0 x x x | 0 | false
0 0 | 1 x x x | 1 | true
1 0 | x 0 x x | 0 | false
1 0 | x 1 x x | 1 | true
0 1 | x x 0 x | 0 | false
0 1 | x x 1 x | 1 | true
1 1 | x x x 0 | 0 | false
1 1 | x x x 1 | 1 | true
0 ns
8400 ns
VSIM 4>
Now: 8 us Delta: 1
sim:/testMultiplexer


sim - Default
Instance
testDecoder
#vsim_capacity#
Objects
Name
addr0
addr1
enable
out0
out1
out2
out3
Wave - Default
Msgs
/testDecoder/addr0 1'h1
/testDecoder/addr1 1'h1
/testDecoder/enable 1'h1
/testDecoder/out0 1'h0
/testDecoder/out1 1'h0
/testDecoder/out2 1'h0
/testDecoder/out3 1'h1
Now 8000 ns
Cursor 1 0 ns
1000 ns
2000 ns
3000 ns
4000 ns
5000 ns
6000 ns
7000 ns
8000 ns
Library
sim
Wave
decoder.v
adder.v
hw2.do
multiplexer.v
Transcript
Start time: 02:30:44 on Sep 25,2015
Loading work.testDecoder
Loading work.structuralDecoder
En A0 A1| O0 O1 O2 O3 | Expected Output
0 0 0 | 0 0 0 0 | All false
0 1 0 | 0 0 0 0 | All false
0 0 1 | 0 0 0 0 | All false
0 1 1 | 0 0 0 0 | All false
1 0 0 | 1 0 0 0 | O0 Only
1 1 0 | 0 1 0 0 | O1 Only
1 0 1 | 0 0 1 0 | O2 Only
1 1 1 | 0 0 0 1 | O3 Only
0 ns
8400 ns
VSIM 4>
Now: 8 us Delta: 1
sim:/testDecoder