

Assignment 3: A SIK Pipeline Implementor's Notes  
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## **Abstract**

A pipelined design could best be created by initially designing a slow single-cycle implementation. The function units, data paths, and control signals defined for the single-cycle implementation could then be used in the pipelined version. It was mostly just a matter of carving the single-cycle design into appropriate pipeline stages. It required several modules which will be explained in further detail of this implementation note.

## **1. GENERAL APPROACH**

1. Begin by using the concept called Owner Computers. The concept was basically to use either module or at least an always block at least for each pipeline stage.
2. Defining an internal instruction set which basically is the second stage of the pipeline system. In this stage, the decode module would be created to decode the instruction that was passed through.
3. Use multithreading to flip back and forth between the threads with each clock cycle.
4. Structure the multithread. It is basically to decide which thread gets to go next (there are only two threads in our case). Then use Intel processors as an example to eliminate the even/odd pattern and let the thread that was not blocked use every cycle.
5. Use four stages design to avoid the register dependencies problem, which will

cause two more instructions, one from each thread, to simultaneously be in the register read cycle.

6. Set the Test instruction right in front of the JumpF or JumpT because Test instruction would set up the `toF` which will decide whether the jump instruction is taken or not.

## **2. ISSUE**

The code has several errors including syntax errors, misspelling, etc. The group had a hard time figuring the multithreading because it was our first time doing it. The idea of multithreading was not that. Another problem was to pick the code from last project since we have three different codes to pick it took a while for us to pick which would be the best.

