

A

B

C

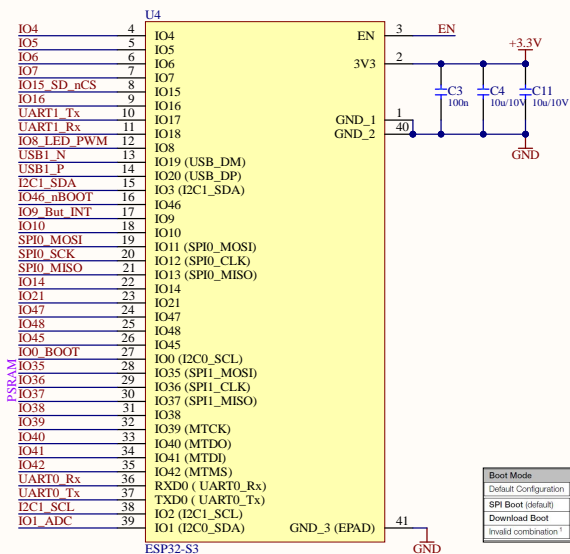
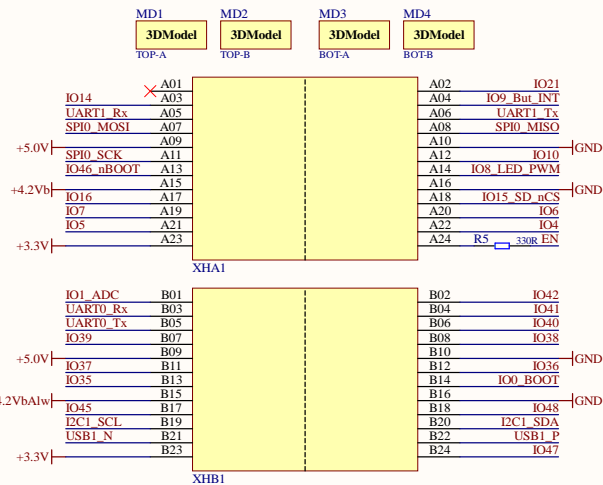
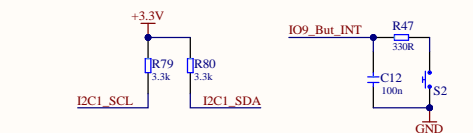
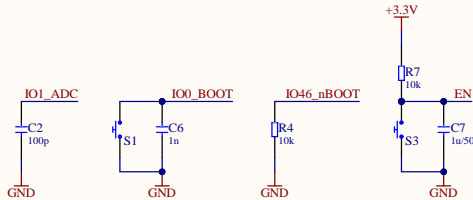
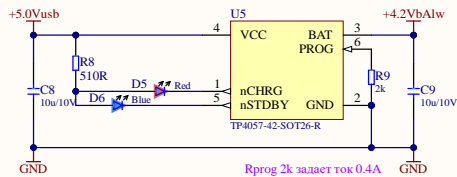
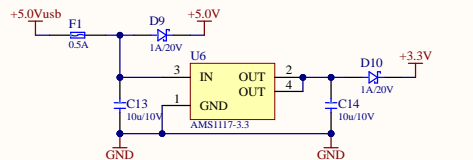
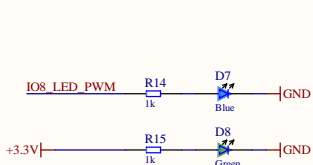
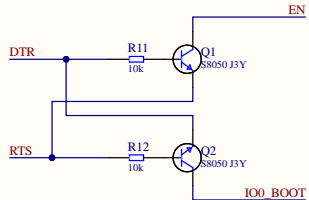
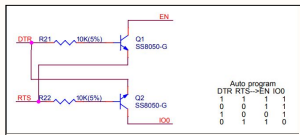
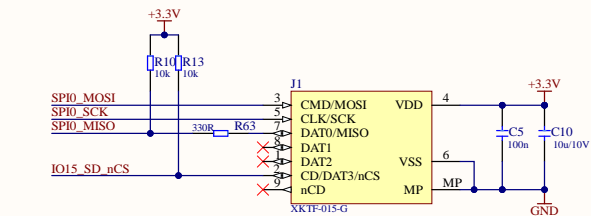
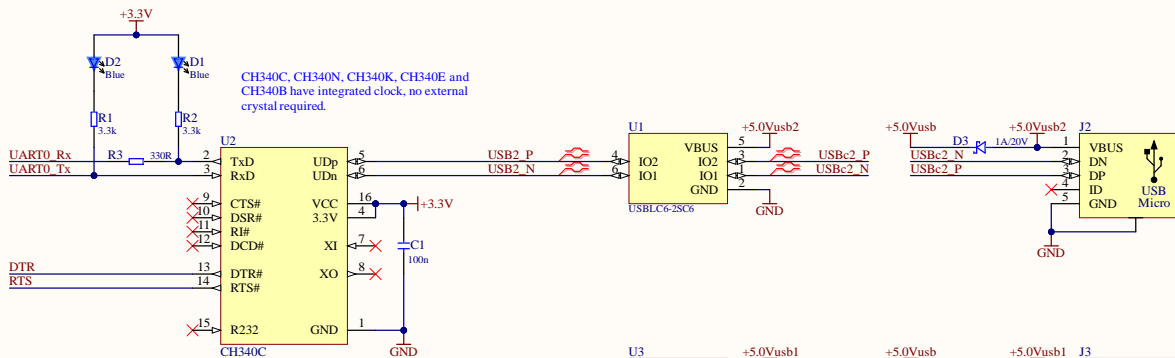
D

A

B

C

D



Chip boot mode- GPIO0 and GPIO46			
• VDD, SPI voltage- GPIO45			
• ROM messages printing- GPIO46			
• JTAG signal source- GPIO3			
Strapping Pin	Default Configuration	Bit Value	
GPIO0	Pull-up	1	
GPIO3	Floating	-	
GPIO45	Pull-down	0	
GPIO46	Pull-down	0	

EFUSE VDD, SPI FORCE	GPIO45	GPIO46	Voltage	VDD, SPI power source
0	0	Ignored	3.3 V	VDD3P3_RTC via Rpu
1	1	Ignored	1.8 V	Flash Voltage Regulator
1	Ignored	0	1.8 V	Flash Voltage Regulator
1	Ignored	1	3.3 V	VDD3P3_RTC via Rpu

GPIO0	GPIO3	JTAG Signal Source
0	0	Ignored
0	1	Ignored
1	0	Ignored
1	1	Ignored