CS/EEE/ENI F215

DIGITAL DESIGN

K.R.Anupama
BITS PILANI, KK BIRLA GOA CAMPUS

Q 1. Design a serial adder / subtractor that works with 4-bit data. A switch S_1 decides whether operation is addition or subtraction.

Q 2. Design a serial Excess-3 to BCD / BCD to Excess-3 converter. A switch S_1 decides what the conversion to be done is. (User input will always be BCD)

Q 3. Design a serial 2-bit complement generator using JK flip-flops and appropriate combinational gates. Data input is 4-bit serial and from LSB onwards and the circuit should return to initial state after 4-bit conversion has been completed.

Q 4. Design a circuit that generates one's complement / two's complement serially using shift registers and appropriate flip-flops. The input is given in parallel manner. Separate input and output registers are required.

Q 5. Design a circuit that does all possible 16 Boolean operations on two-bit data. There are four switches S_1-S_4 that select the appropriate Boolean operation.

Q 6. Design a circuit which generates even parity / odd parity serially. You have to use appropriate flip-flips and gates. A switch selects between even and odd parity.

Q 7. Design a divide by 100 ripple counter using flip-flips and appropriate number of gates.

Q 8. Design a parallel 8-bit adder / subtractor. A switch S_1 decides whether operation is addition or subtraction.

Q 9. Design a 4x4 memory from which data can be read / written. The 4x4 memory will have a 4-input data lines and 4-output lines and RD' / WR' control signals.

Q 10. Design a 16-bit signed comparator.

Q 11. Design a 4-bit logic unit that can do following operations:
AND, XOR, NAND, XNOR, OR, Input A, NOR, One's complement of input A using appropriate SSI and MSI chips. The operation to be done is selected using a set of 3 switches.

Q 12. Design a counter that generates a binary code / grey code based on user input. Counter has to be designed using only flip-flops.

Q 13. Design a circuit that counts the number of people in a room. There are two counters (4-bit). One for entry and one for exit. The difference gives the number of people in the room. When a person crosses the door (entry or exit), a low pulse is generated.

Q 14. Design a circuit that adds two 4-bit BCD numbers and gives result in BCD. (The addition operation is done serially and adjustment of result is done parallelly.)

Q 15. Design a frequency comparator that generates outputs for $f_1>f_2$, $f_1<f_2$, $f_1=f_2$. The frequency f_1 and f_2 are between 1kHz and 15kHz.

Q 16. Design a J-K flip-flops using only NAND gates.

Q 17. Design a circuit that does excess-3 addition / subtraction using binary adders and other SSI chips. 9's complement arithmetic is used for subtraction process. (A switch decides addition or subtraction.)

Q 18. Design a sequential circuit that detects whether given input is a valid 2421 code.

Q 19. Design a sequential circuit that detects whether given input is a valid 7421 code.

Q 20. Design a sequential circuit that detects whether given input is a valid 5421 code.

Q 21. Design a stop watch for 5 minutes with accuracy of 0.5 seconds.

Q 22. Design a 4-bit saturating up / down counter. A saturating counter will be one that stops at max / min count even if clock pulses arrive.

Q 23. The decimal digits are to be represented by the 2421 self-complementing code. Develop an algorithm for adding together any two decimal digits using this code. With the aid of this algorithm, design a single stage 2421 adder / subtractor circuit. A 4-bit binary adder is to be used as the basic building block in conjunction with any other necessary logic gates and / or MSI chips.

Q 24. Design a binary multiplier that multiplies a 4-bit number, $B = B_3B_2B_1B_0$, by a 3-bit number $A = A_2A_1A_0$. The circuit is to be implemented using AND gates and 4-bit adders.

Q 25. Design an asynchronous lock operated by five input buttons labelled as A, B, C, D and R (The reset button). The unlocking operation can only take place if only one button is activated as a time in the order B, D, A, C.

Q 26. An arithmetic circuit has two selection signals, S0 and S1. The circuit is required to perform the operations listed below.

F = A + B	F = A + B + 1
F = A'	F = A' + 1
F = A + B'	F = A + B' + 1
F = B'	F = B' + 1

Using a 4-bit adder as the basic building block, design the circuit that will implement the above operations.