

Midterm 1 : Practice Midterm provided by Professor Meduri

Question 1.

P-type semiconductor has electrons (electrons/holes) as minority charge carriers. Holes are majority carriers!

N-type semiconductor has holes (electrons/holes) as minority charge carriers. Electrons are majority carriers!

Question 2.

When a voltage of 2V is applied between G and S of a NMOS, the transistor is: (assume $V_T = 1V$) ON.

An NMOS transistor, the transistor turns on and the 'switch' is closed when V_{GS} is greater than the threshold voltage.

In this case $V_{GS} = 2V$ and $V_T = 1V$, hence $V_{GS} > V_T$ so the transistor is on.

Question 3.

When a voltage of -2V is applied between G and S of a PMOS, the transistor is: (ASSUME $|V_{TPL}| = 1V$) ON.

An PMOS transistor, the transistor turns on and the 'switch' is closed when V_{GS} is less than the threshold voltage.

In this case $V_{GS} = -2V$ and $V_T = 1V$, hence $V_{GS} < V_T$ so the transistor is on.

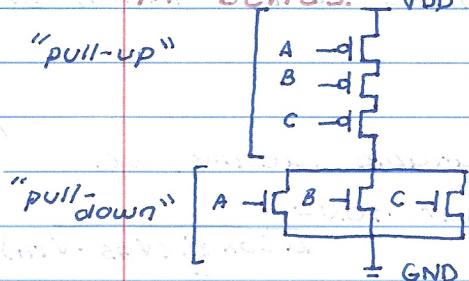
Question 4.

Pick the most appropriate statement from below. A 3-input NOR gate has:

a. 3 NMOS transistors in the pull down network &

c. 3 NMOS transistors in parallel and 3 PMOS transistors

in series.



$$A + B + C \quad \text{Remember:}$$

product =

nmos \rightarrow series

pmos \rightarrow parallel

addition/subtraction =

nmos \rightarrow parallel

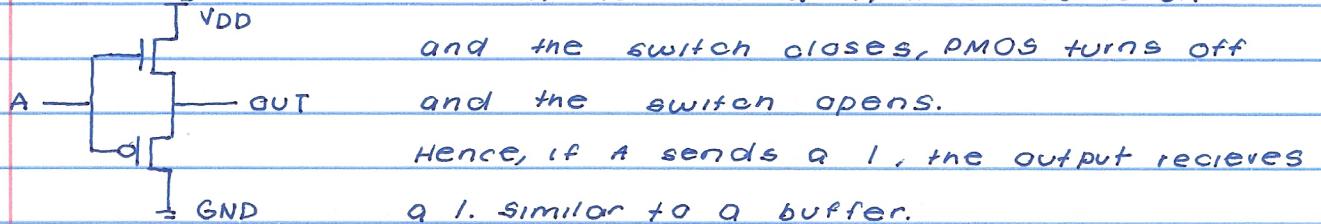
pmos \rightarrow series

Question 6.

If the NMOS and PMOS transistors switch places in an inverter, the resulting circuit is:

C. Weak Buffer

PROOF by example: If A is sent a 1, NMOS turns on



Why is it considered a 'weak' buffer?

The transistors are in the wrong place, doing the wrong job in their respective networks.

PMOS produces a 0 when it typically produces a good 1.

NMOS produces a 1 when it typically produces a good 0.

Question 6.

Which of the following is true about PMOS transistor?

a. It provides a good '1'

PMOS devices can't fully pull the output down to ground, they make bad '0'. NMOS devices can't fully pull the output to a high supply voltage, they make a bad '1'.

Question 7.

Input dependent phase shift is brought about by which of the following transistor non-ideality?

c. Non-zero ON-resistance

Phase of the switch is dependent on V_{in} levels, this is a non-linear correlation. Depending on the V_{in} level, the transistor turns on and off. The phase is a function of $R_{ON,OFF}$ and is not a constant; why?

$$R_{ON} = f(V_{in})$$

Because R_{ON} is non-zero and is variable. Ideally, we

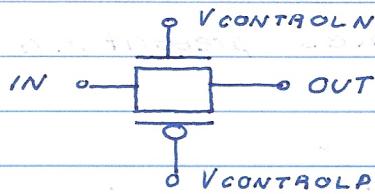
want $R_{ON} = 0$, but the reality is that $R_{ON} = 1$

$$\frac{\mu COX W}{L} (V_{GS} - V_{TH})$$

Question 8.

A 2:1 MUX implemented using transmission gates has uses how many PMOS transistors? 2

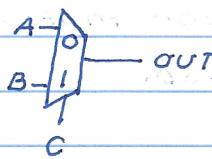
First, consider transmission gate characteristics.



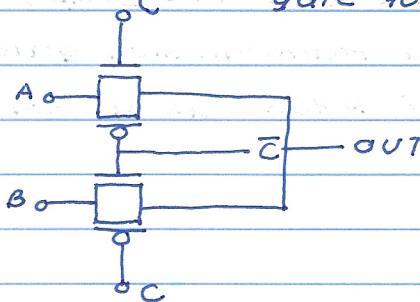
$$V_{\text{CONTROLN}} = V_{\text{CONTROLP}}$$

The control signal applied to the PMOS is the complement of the control signal applied to the NMOS. This solves the PMOS bad '0' and NMOS bad '1' issue.

Now, take a 2:1 MUX:



We need C when low, logic '0', the upper transmission gate turn off and not allow A to pass, at the same time, the lower transmission gate turn on and allow B to pass.



what about a 4:1?

a 4:1 MUX can be constructed out of two 2:1 MUX's.

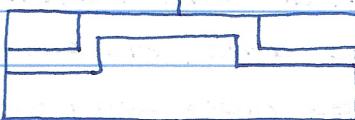
Question 9

which of the following capacitances is fundamental to the operation of a MOS transistor?

- D. Oxide capacitance between Gate and channel



The oxide capacitance between gate and channel.

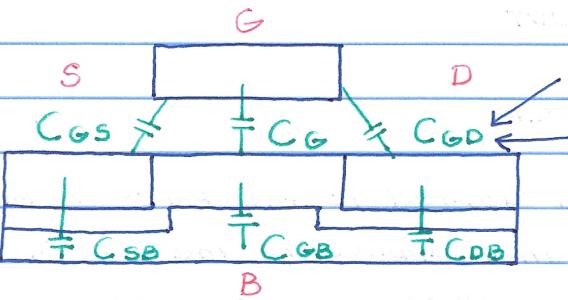


Question 10.

In the figure -1 shown below, which capacitance shorts the input to the output at high frequency?

C_{GD} .

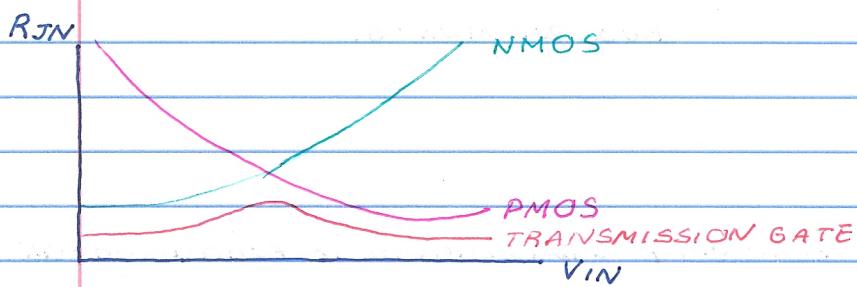
Let's observe the capacitances present in a MOSFET.



High frequency shorts capacitors! If the input is at the gate and we are looking for the capacitor that shorts the input to output that would be C_{GD} .

Question 11.

In the figure-2 shown below, plot the graph for the equivalent on-resistance of a transmission gate. The on-resistance of NMOS and PMOS as a function of V_{IN} .



Recall, in question 8's discussion of transmission's gate characteristics. As a mosfet's on-resistance is a function of the gate-to-source voltage, as one transistor becomes less conducting due to the gate drive, the other transistor takes over and becomes more conducting. Thus, the combined value of the two on-resistances stays more or less constant than would be case for a single switching transistor on its own.

Question 12.

shown below are transistor higher order effects. Identify a lateral field effect from below.

b. mobility degradation c. velocity saturation

E(lateral) : This field is due to the application of the drain voltage. As the magnitude of V_{DS} increases, the drain depletion region extends towards the source.

$\uparrow E_{\text{lateral}} = \frac{V_{DS}}{L} \uparrow$ carriers are attracted to the edge of the channel, moving downwards with the side surface that slows the carriers. Current saturation!

Question 13.

shown below are transistor higher order effects. Identify a vertical field effect from below.

b. mobility degradation

As the vertical electric field also increases on shrinking the channel lengths, it results in scattering of carriers near the surface. More surface collisions!

Question 14.

"pinch-off" occurs in which region of operation?

b. saturation

A new condition arises if we increase the drain voltage substantially. The drain voltage becomes large enough that the gate to substrate potential at the drain is smaller than threshold. Therefore, the channel thickness at this end goes to 0. Electrically, the effect of pinch off is that the channel no longer acts like a simple resistor. The current I_{DS} becomes fixed at the value just prior to pinch-off.

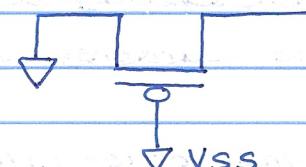
Question 15.

Because of short channel effect, the V_{TH} of a MOSFET increases (increases/decreases) with increasing values of L.

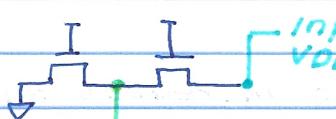
Refer to the Body Effect short channel effect, where V_{TH} increases as the channel length increases, more "real-estate" for carriers to go to surface, needing a higher threshold voltage to invert the channel.

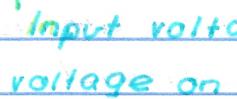
Question 16.

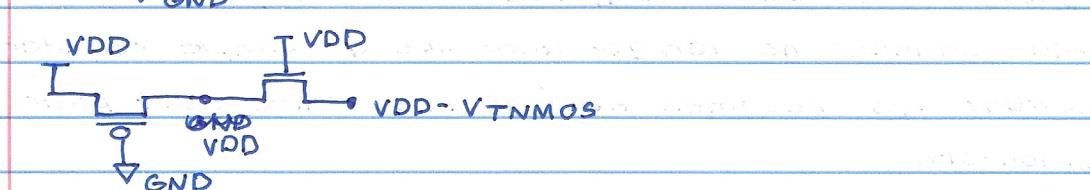
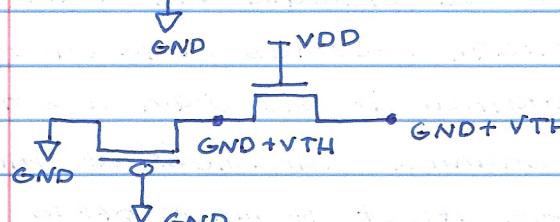
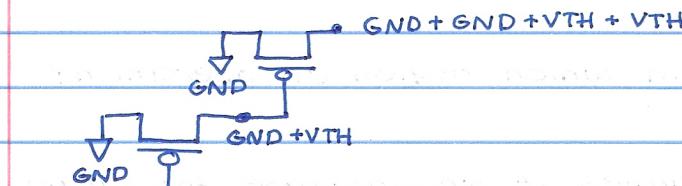
Recall, pmos transistors are not good at passing 0's so if both the gate and drain are tied to ground then the source voltage will be $GND + |V_{TH}|$



a couple more examples...

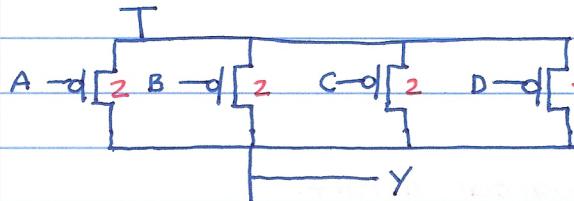
 Input voltage is 0 and the gate is tied to V_{DD} . The voltage on the node at the end will be zero.

 Input voltage is 0 and the gate is tied to V_{DD} . The voltage on the node in the middle will be zero.



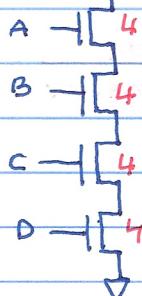
QUESTION 22/23/24

4-input NAND Gate $Y = \overline{ABCD}$



PULL-UP network is 4 PMOS in

parallel, so widths should be the same as unit inverter.



PULL-DOWN network is 4 NMOS transistors

in series. If we want fall resistance of gate to equal that of a unit inverter, the widths of the NMOS should be 4 times that of a unit inverter.

Calculate Logical Effort:

$g = \frac{C_{INAND}}{C_{ININVERTER}}$ (capacitance seen by one input)

$C_{ININVERTER}$ (capacitance seen by one input of inverter)

$C_{ININVERTER} = 1S + 2$ from the PMOS and 1 from NMOS. This forms the '3' base.

$$C_{INAND} = C_{INANDPMOS} + C_{INANDNMOS}$$

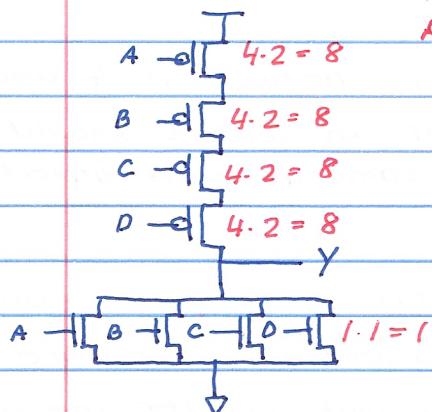
$$'2' \text{ (in the worst case rise time)} + '4' = 6$$

$$\text{Hence ... } \frac{6}{3}$$

Question 25

$$4\text{-input NOR } y = \overline{A+B+C+D}$$

~~pull up networks is 4 PMOS in series.~~



LOGICAL EFFORT:

$$g = \frac{C_{IN\text{NOR}}}{C_{IN\text{INVERTER}}} = \frac{8+1}{3} = \frac{9}{3}$$

