CpE 151 and EEE 234 CMOS and VLSI Design **Midterm Exam**

(For undergraduates: 2 lowest (wrong) questions will be dropped.)

Each question is 3 points, unless specified otherwise.

Name Sabina Mentukh Section: Practice CpE 151 EEE 234

1. P-type semiconductor has electrons (electrons holes) as minority charge carriers.

2. When a voltage of 2V is applied between the G and S of a NMOS, the transistor is: (assume V_t = 1 V)

   (a) ON (b) OFF (c) Not enough information

3. When a voltage of -2V is applied to between the G and S of a PMOS transistor, the transistor is (Assume $|V_{tp}|$ = 1V):

   (a) ON (b) OFF (c) Not enough information

4. Pick the most appropriate statement from below. A 3-input NOR gate has:
   (a) 3 NMOS transistors in the Pull Down Network
   (b) 3 PMOS transistors in the Pull Down Network
   (c) 3 NMOS transistors in parallel and 3 PMOS transistors in series
   (d) 3 NMOS transistors in series and 3 PMOS transistors in parallel
   (e) Both (a) and (c) are true
   (f) Both (b) and (d) are true

5. If the NMOS and PMOS transistors switch places in an inverter, the resulting circuit is:
   (a) Weak Inverter
   (b) Strong Inverter
   (c) Weak buffer
   (d) Strong buffer

6. Which of the following is true about PMOS transistor?
   (a) It provides a good '1'
   (b) It provides a good '0'
   (c) It uses p-well
   (d) It has positive threshold voltage Vtp

7. Input dependent phase shift is brought about by which of the following transistor non-ideality?
   a. Channel-charge injection
   b. Clock-feed through
   c. Non-zero ON-resistance
   d. Negative-bias Temperature Instability (NBTI)

8. A 2:1 MUX implemented using transmission gates has uses how many PMOS transistors?
   2

9. Which of the following Capacitances is fundamental to the operation of a MOS transistor?
   a. Depletion capacitance between Drain and Bulk
   b. Depletion capacitance between Source and Bulk
   c. Overlap Capacitance between Gate and Source Drain
   (d) Oxide Capacitance between Gate and Channel

10. In the Figure – 1 shown below, which capacitance shorts the input to the output at high frequencies?

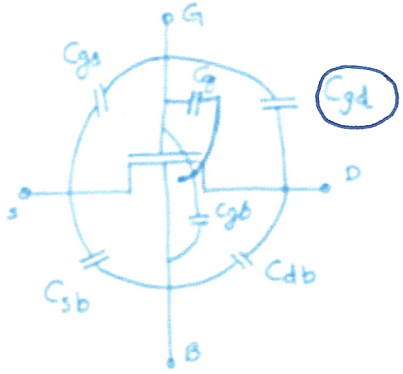


Figure – 1. MOSFET Capacitances

11. In the Figure – 2 shown below, plot the graph for the equivalent ON-resistance of a transmission gate. The On-resistance of NMOS and PMOS as a function of Vin.

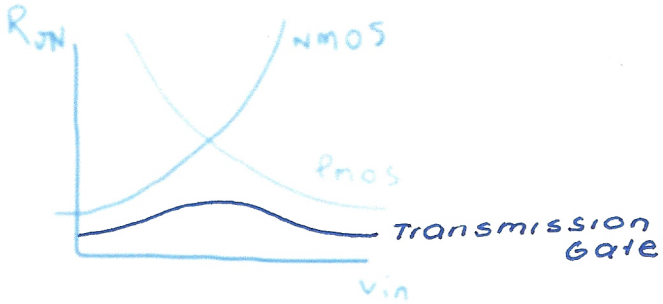


Figure – 2. On-resistance of NMOS, PMOS and transmission gate

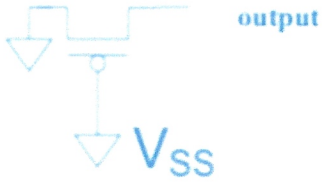
12. Shown below are transistor higher order effects. Identify a lateral field effect from below.
   a. Subthreshold conduction
   (b) Mobility degradation
   c. Body effect
   (d) Velocity saturation

13. Shown below are transistor higher order effects. Identify a vertical field effect from below.
    a. Subthreshold conduction
    b. Mobility degradation
    c. Body effect
    d. Velocity saturation

14. "Pinch-off" occurs in which region of operation?
    a. Subthreshold
    b. Saturation
    c. Linear
    d. Both (b) and (c)

15. Because of short channel effect, the V_{TH} of a MOSFET increases (increases/decreases) with increasing values of L.

16. For the pass transistor shown in figure - 3 below, what is the voltage at the output?



GND + |V_{TH}|

Figure – 3 PMOS Pass Transistor

17. By definition, the time from input to rising output crossing $V_{DD}/2$ is:
    a. Rise Time - (tr)
    b. Rising Propagation Delay (t_{pdr})
    c. Rising Contamination delay (t_{cdr})
    d. Setup – time

18. In RC Delay Model, which of the following substitutions is valid
    a. PMOS transistor with a width of k times the unit transistor has a resistance of R k
    b. NMOS transistor with a width of k times the unit transistor has a cap of 2kC on the gate
    c. PMOS transistor with a width of k times the unit transistor has a cap of kC on the gate
    d. NMOS transistor with a width of k times the unit transistor has a resistance of 2R k

19. While calculating the delay of a RC ladder using Elmore – Delay, which of the following is true?
    a. The Resistance closest to the load has the highest effect on the delay
    b. The Capacitance closest to the load has the highest effect on the delay
    c. The Resistance closest to the source has the highest effect on the delay
    d. The Capacitance closest to the source has the highest effect on the delay

20. For the figure – 4 shown below, what is the total delay in terms of T. T is defined as the delay of a parasitic–free fanout-of-1 inverter? Hint: T = 3RC

a. 2 T
b. 3 T
c. 4 T
(d.) 5 T

parasitic component = 1T

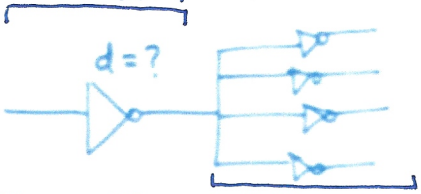


Figure – 4 Fanout-of-4 inverter

fanout component = 4T

21. When transistors switch, both nMOS and pMOS networks may be momentarily ON at the same time, leading to a blip of current called short-circuit current

22. Consider a 4 input NAND gate that is sized to provide the same current as a unit inverter. What is the value of k (width) for the PMOS?

Kp =

a. k = 1
(b.) k = 2
c. k = 4
d. k = 8

23. For the NAND gate in problem # 22, what is the value of k (width of the NMOS) for the NMOS?

Kn =

a. k = 1
b. k = 2
(c.) k = 4
d. k = 8

24. For the NAND gate in problem # 22, what is the value of g (logical effort)? Hint: g is defined as Cin(of the gate) Cin (of a unit inverter) **g = (Cin-gate/Cin-unit-inverter)**

(a.) g = 6 3
b. g = 7 3
c. g = 8 3
d. g = 9 3

25. Consider a 4 input NOR gate that is sized to provide the same current as a unit inverter. What is the value of g (logical effort)? 9/3