CPE 151 | Extra Questions That Could be Asked

The biggest saving in dynamic power consumption is brought about by reducing which of the following? Supply Voltage

Dynamic Power = ½ * Capactive Load * Voltage^2 * Frequency Switched

Which of these contributes significantly to the static power consumption of CMOS circuits? Pick the most significant one. Subthreshold- Leakage

The activity factor of memory components is relatively _low_ compared to that for logic components.

The activity factor of logic components is relatively _high_ compared to that for memory components.

The output of a dynamic logic circuit is valid only during which phase? Evaluate.

The charge leakage mechanism of capacitance imposes a _lower_ limit on the clock frequency of dynamic circuits.

In Dynamic Circuits, the output at a node can go higher than the supply voltage because of which effect? Clock Feed Through

In order to reduce the effect of charge sharing in Dynamic circuits, the critical nodes should be _pre-charged_.

CPE 151 | Long Answer Response

26. NOR is slower than NAND because NOR has PMOS in series which is slower.