Gigabit Ethernet over Unshielded Twisted Pair Cables

Kamran Azadet

DSP and VLSI Systems Research Department
Bell Laboratories, Lucent Technologies
Holmdel, NJ 07733, USA

Abstract

This paper presents 1000BASE-T, the physical layer of Gigabit Ethernet over copper. After an introduction to the overall Gigabit Ethernet standard, we describe unshielded twisted pair (UTP) channel impairments, modulation and coding of 1000BASE-T, the clocking scheme and start-up protocol. Finally, we summarize challenges in the monolithic VLSI implementation of a 1000BASE-T transceiver.

Introduction

Due to the rapid growth of applications requiring very high data transfer rates in local area networks (LAN), there is an on-going need to increase the bandwidth of these networks. Ethernet is the most widely used LAN standard, and has recently migrated to a data rate of 1Gb/s [1]. Fig. 1 shows the exponential growth in bit-rates of different Ethernet standard generations. In order to insure success in the market place, each new generation of Ethernet standard is backward compatible with previous generations. Backwards compatibility is also one of the motivations of the 1000BASE-T task force for selecting a baseband signaling scheme (1000BASE-T means 1000Mb/s, baseband signaling, Twisted pair cable). An example of Gigabit Ethernet network architecture is shown in Fig. 2.

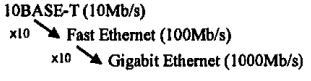

Figure 1: Migration to high-bandwidth Ethernet LAN

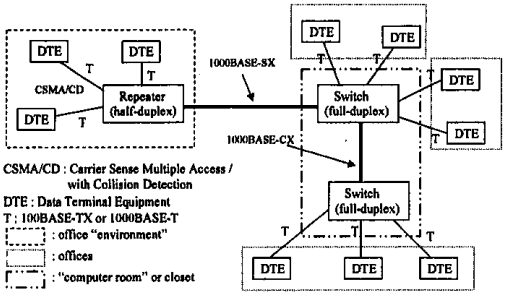

Figure 2: An example of Ethernet LAN

Due to long distance needs (often over 200m) for backbone links, the "vertical" connections use different types of fiber optics (802.3z standard). Short links (short haul copper), typically short connections inside a computer room or a network closet, use a specialized shielded copper cable called twinax. Finally, connections to desktop terminals or "horizontal" links use unshielded twisted pair cables mainly to allow the use of already existing UTP CAT-5 infrastructure. Typical distance targets for different media are shown in Table I. The structure of the overall Gigabit Ethernet standard is illustrated in Fig. 3.

Fiber PHY :				
SX :	850nm	multi-mode	62.5um	275m
			50um	500m
LX :	1300nm	multi-mode	62.5um	550m
			50um	550m
FX :	1300nm	single-mode	(9um)	5km
Short Haul :				
CX :	specialized STP (Twinax)			30m
Long Haul copper :				
T :	UTP CAT-5			100m

Table I: Operating distances over different media

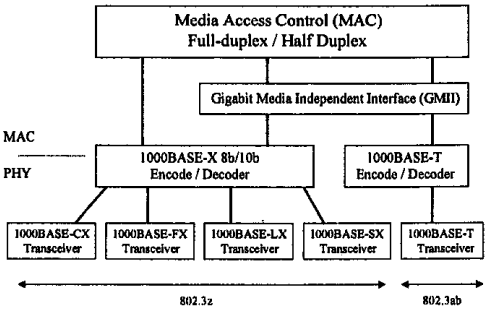

Figure 3: Structure of Gigabit Ethernet standard

The 1000BASE-T (802.3ab) task force is finalizing the standard for Gigabit Ethernet over copper (long haul copper). Its objectives have been to define a standard for full-duplex or half-duplex 1Gb/s effective bit-rate over a 100m category 5 (CAT-5) cable. The target bit error rate (BER) is $<10^{-10}$. The copper PHY (Physical layer) supports the Ethernet MAC layer (Media Access Control). It uses the Gigabit Media Independent Interface (GMII) to

transmit and receive bytes of data at a rate of 125MHz. Due to the high-bandwidth data transmission over an unshielded medium, gigabit transceivers have to comply with emission standards for office environments, such as FCC or CISPR (class A). Gigabit transceivers also have to tolerate noise due to cross-talk between different cables, RF interference, and other impairments inherent to the unshielded nature of the cabling structure. Noise susceptibility was one of the main motivations for the use of a forward error correction technique briefly described in this paper (see also [2]).

Channel Impairments

The transmission scheme used in fast Ethernet (100Mb/s) 100BASE-TX is shown in Fig. 4. One pair is used to transmit 125Mb/s in one direction, and a second pair for the other direction, allowing full-duplex transmission over CAT-5 cable (two other pairs are not used). In 100BASE-TX the main impairment is near-end cross-talk (NEXT).

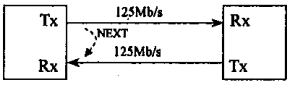

Figure 4: 100BASE-TX transmission scheme

The transmission scheme used in 1000BASE-T is shown in Fig. 5. It is based on full-duplex transmission over all four pairs of the CAT-5 (or better grade) cable. Full-duplex transmission on the same physical wire is made possible by the introduction of a device called a "hybrid". It can be implemented as a transformer or with active devices. In this scheme each receive signal is corrupted by 3 sources of NEXT, 3 sources of far-end cross-talk (FEXT), and echo from the transmit signal of the same pair. Echo is caused by a return signal generated at impedance discontinuities in hybrids, connectors (near and far end), and also inside the cable itself.

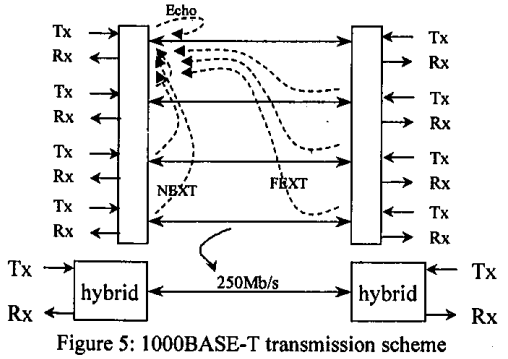

Figure 5: 1000BASE-T transmission scheme

Fig. 6 shows measured channel response of a "worst-case" CAT-5 cable. To meet the SNR requirements of a 1000BASE-T system, the NEXT signal has to be canceled at the receiver. Echo is far worse than NEXT. The echo signal can be up to 15dB larger than the signal itself (at 100MHz). Therefore echo has to be canceled. The maximum time span of the echo impulse response corresponds approximately to a round trip delay over 100m cable (close to 1100ns). For the 1000BASE-T baud-rate of 125MHz, the number of taps required to cancel near-end and far-end echo is 120 taps. This means that 480 taps of echo cancellation are required to implement all four receivers. This represents a considerable increase in complexity over 100BASE-TX where echo is not an issue.

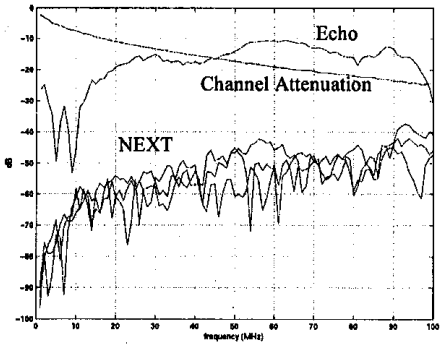

Figure 6: a measured CAT-5 channel response

Modulation and coding scheme

PAM-5 modulation (baseband signal) was chosen in order to achieve a bit-rate of 250Mb/s within the given 100MHz bandwidth CAT-5 cable. It carries over 2.25bit per symbol ($\log_2 5$=2.32bit) at a baud-rate of 125Mbaud, the same rate as the GMII interface (i.e., incoming and outgoing bytes). By grouping 4 PAM-5 symbols transmitted over the 4 pair, a 4-dimensional (4D) symbol is formed. Each 4D symbol belongs to a code space of 5x5x5x5 points = 625 points > 512 points (9bit). Since only 8bit need to be transmitted the extra bit can be used as a redundant parity bit for error correction. Note that despite the use of 1bit redundancy, there are still 625 − 512 = 113 points are left that are used to carry overhead information for the Ethernet protocol. The error correction scheme is based on a well-known Ungerboeck trellis code (TCM) [3]. This coding increases free euclidian distance of the code space by 6dB. The convolutional code specified in 1000BASE-T is shown in Fig. 7. In each byte two bits are used to generate a parity bit (9^{th} bit).

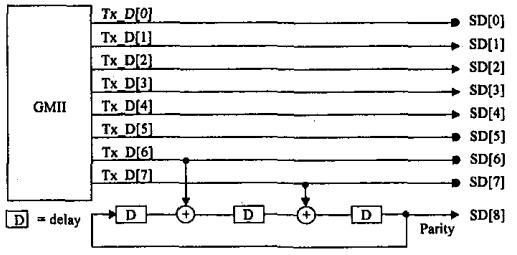

Figure 7: 1000BASE-T convolutional encoding

VLSI implementation

In order to compensate for the channel impairments described earlier, a 1000BASE-T receiver has to perform the following operations: channel equalization comprising Feed-Forward Equalizer (FFE), NEXT cancellation, Echo cancellation, and combined Decision-Feedback Equalization (DFE) / TCM decoding. Figure 10 shows the block diagram of a reference implementation of a 1000BASE-T transceiver (only one pair shown).

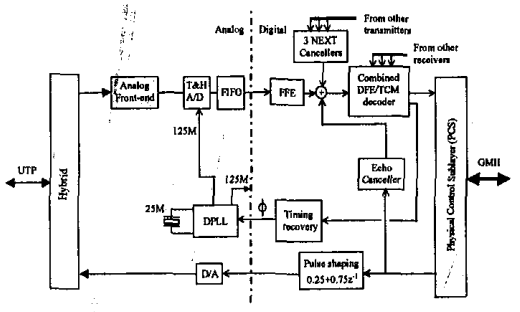

Figure 10: VLSI implementation of 1000BASE-T

On the transmit side:
A pulse-shaping filter is used in order to reduce high frequency energy of the signal for radiation purposes. Due to its simple coefficients its output is a 17 level signal. The D/A converter's input has therefore 17 levels (with at least 7bit linearity) and drives directly a 100ohm impedance. A possible implementation of the D/A is based on the current steering approach [4].

On the receive side:
The analog front-end, performs DC wander correction, automatic gain control, and continuous-time filtering. Some of these functions are similar to conventional designs used in 100BASE-TX systems [5]. The A/D converter is typically 7 or 8 bit (depending on the noise margin target), operating at 125MHz (for a baud-rate receiver) or 250MHz for a T/2 fractional spacing. Parallel A/D architectures are better candidates for this application than pipelined ADCs since they have lower latency. The total receiver latency has to meet a tight bit budget requirement to insure proper operation of the CSMA/CD protocol (CSMA/CD or Carrier Sense Multiple Access with Collision Detection is a protocol for media access in a "collision domain"). Another advantage of flash architectures is lower error rate. Folding and Interpolating ADCs are very suitable in that they achieve performance similar to full flash ADCs at a much lower power consumption [4]. Baud-rate clock recovery consists of a phase detector, a digital loop filter (proportional and integral) and a digital PLL (DPLL). Phase detectors are often based on a technique by Mueller and Muller [6]. One of the main requirements of the DPLL is to provide a low jitter clock. A phase interpolation technique is shown in Fig.11a. Note that in order to insure a small phase quantization error, the DPLL has to perform phase interpolation by a large factor. Fig.11b describes a modified version where phase interpolation is included inside the PLL loop in order to decrease clock jitter and increase phase resolution by using "time averaging" [7].

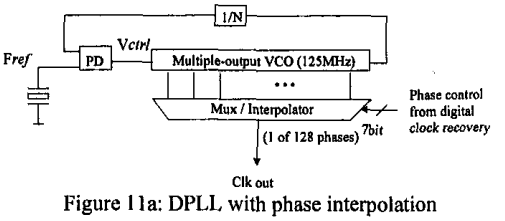

Figure 11a: DPLL with phase interpolation

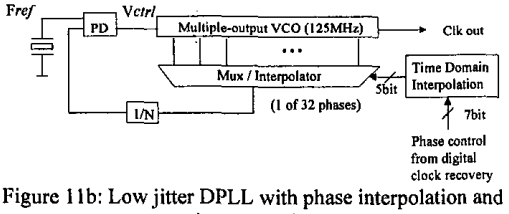

Figure 11b: Low jitter DPLL with phase interpolation and time averaging

The FFE is typically a 10-20 tap FIR filter with 10bit coefficients. The number of taps depends on the noise margin target. References [8] and [9] present low power techniques for reducing power consumption in adaptive FIR filters in high-speed transceivers. The NEXT/Echo cancellers are multiplier-less filters since their inputs are symbols with values 0, +/- 1, +/- 2. They represent a large portion of the DSP due to the large number of taps. There are a total of 12 NEXT cancellers with typically 20 taps each, giving a total of 240. Echo cancellation requires 480 taps. Another challenge in the implementation of 1000BASE-T receivers is

combining DFE and TCM decoding, as the DFE needs delay-free tentative decisions and Viterbi decoding has an inherent decoding latency. The combined TCM/DFE detector can be implemented using parallel DFEs [10] as shown in Fig.12.

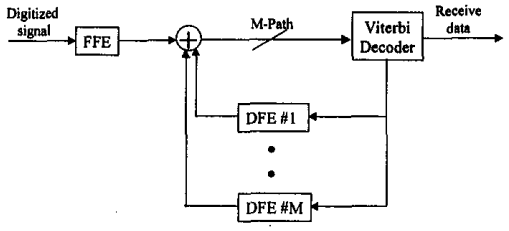

Figure 12: combined Viterbi/DFE using parallel DFEs

Clocking and start-up issues

In order to cancel echo and NEXT, the transmitter and receiver of the 1000BASE-T modem have to be synchronized. This is done using a master and slave configuration. The master is the origin of a reference clock, which is used in both its TX and RX paths. The Slave recovers the Master clock and uses it for its transmitter. Hence Master and Slave are both synchronized to the Master clock. The master-slave clocking scheme is shown in Fig.13.

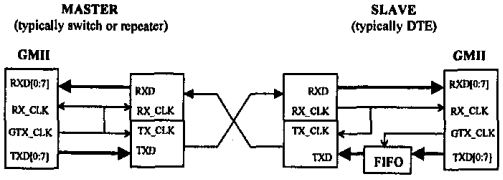

Figure 13: master-slave clock scheme

Note that the Slave has to recover both the frequency and phase during clock recovery, while the Master only has to recover phase. Another problem related to clock recovery occurs during start-up. Due to the existence of a large echo signal, clock recovery may synchronize to the echo signal instead of the remote transmitted signal. In order to facilitate clock recovery for the Slave, the start-up procedure of Fig.14 is defined.

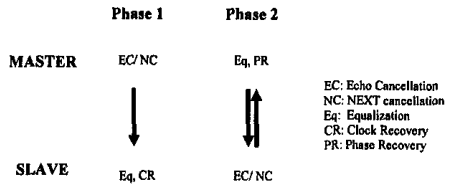

Figure 14: Start-up protocol

During the first phase only the master transmits. This allows the slave to recover the master clock (both frequency and phase) reliably without being disturbed by echo. It also computes its equalizer taps. Meanwhile the master's echo and NEXT cancellers converge. In a second step, the slave also starts transmitting. The master can start convergence of its equalizer and recover the phase information, while the slave performs convergence of its echo and NEXT cancellers.

Summary

1000BASE-T is a DSP-based transceiver for 1Gb/s full-duplex transmission over regular twisted pair cable (CAT-5 or better). It is a very complex system, requiring astonishing computational power to perform operations such as channel equalization, combined DFE/TCM decoding, Echo/NEXT cancellation, etc. Problems such as on chip noise coupling or power consumption make its monolithic implementation in CMOS technology extremely challenging.

References

[1] J. Kadambi, Ian Crayford, Mohan Kalkunte, *Gigabit Ethernet - Migrating to High Bandwidth LANs*, Prentice Hall, 1998

[2] M. Hatamian, O.E. Agazzi, et al. "Design Considerations for Gigabit Ethernet 1000BASE-T Twisted Pair Transceivers", *Proceedings of CICC*, 1998

[3] G. Ungerboeck "Trellis Code Modulation with Redundant Signal Sets, Part I: Introduction", *IEEE Communications Magazine* , February 1987

[4] Rudy Van de Plassche, *Integrated Analog-To-Digital And Digital-To-Analog Converters*, Kluwer Academic Publishers, 1994

[5] J. Everitt, J. Parker, P. Hurst, D. Nack, K. Konda, C. Raad "A 10/100Mb/s CMOS Ethernet Transceiver for 10BASE-T, 100BASE-TX, and 100BASE-FX", *ISSCC Digest of technical papers*, Feb 1998

[6] K. H. Mueller and M. Muller "Timing Recovery in Digital Synchronous Data Receivers", *IEEE Transactions on communications*, Vol. COM-24, No5, May 1976

[7] P. Larsson "A 2-1600MHz 1.2-2.5V CMOS Clock-Recovery PLL with Feedback Phase-Selection and Averaging Phase-Interpolation for Jitter Reduction", *ISSCC Digest of technical papers*, Feb 1999

[8] C. Nicol, P. Larsson, K. Azadet, and J. H. O'Neill "A Low-Power 128-Tap Digital Adaptive Equalizer for Broadband Modems", *IEEE Journal of Solid-State Circuits*, Vol. 32, No11, November 1997

[9] K. Azadet, C. Nicol "Low-Power Equalizer Architectures for High-Speed Modems", *IEEE Communications Magazine* , October 1998

[10] E. Haratsch "High-Speed VLSI Implementation of Reduced Complexity Sequence Estimation Algorithms with Application to Gigabit Ethernet 1000BASE-T", *proceedings of VLSI-TSA conference*, Taipei, June 1999