Chapter 15

ARM – Architecture, Programming and Development Tools

Lesson 1

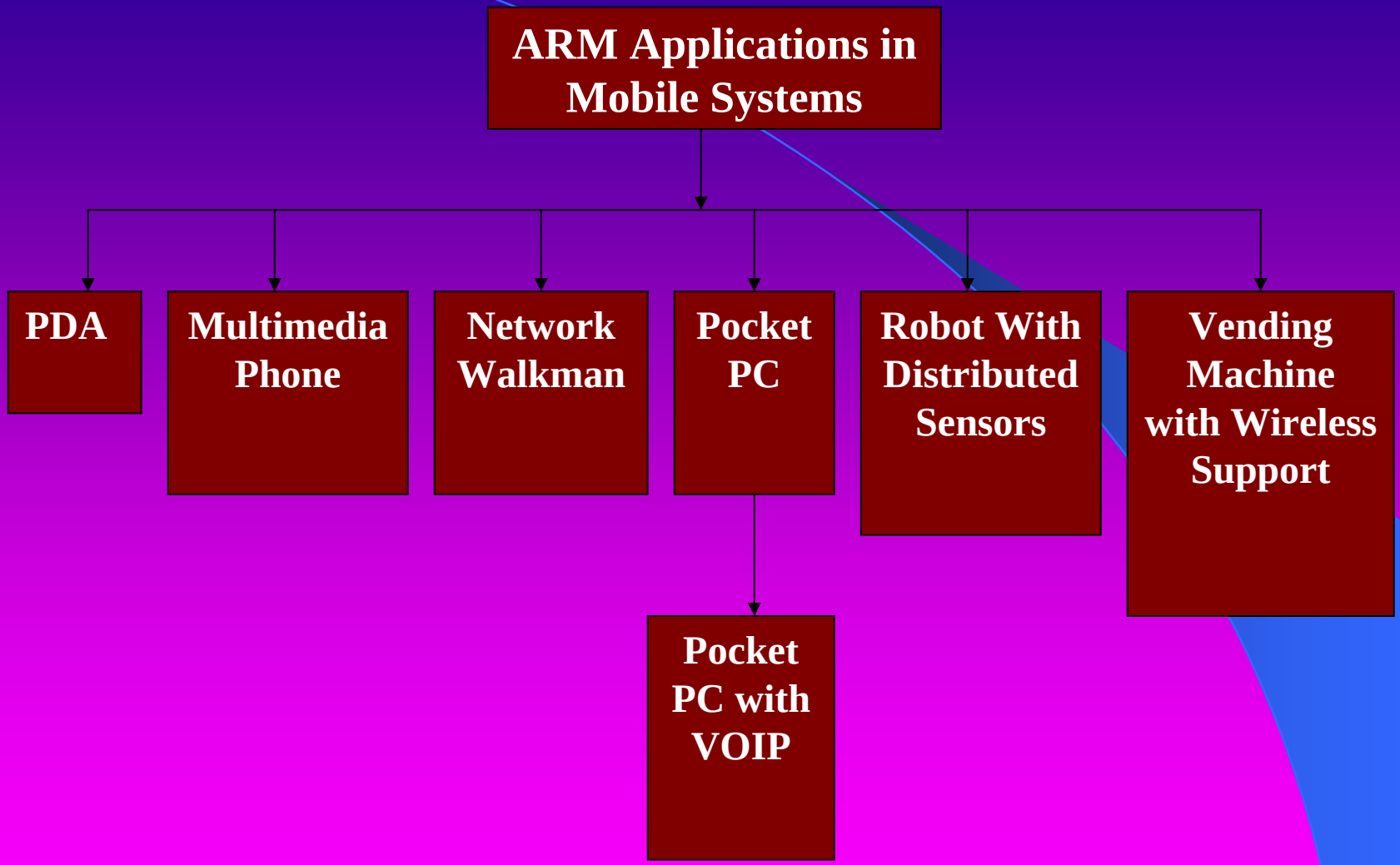
ARM CPUs

Outline

- ARM Processors
- Features of a RISC architecture
- ARM Family and ARM many variant architectures

Examples of Systems needing high-performance precise- computing

- Image processing,
- Video games,
- Robotics and
- Adaptive control
- Mobile Devices


ARM Applications in Mobile Systems
PDA
Multimedia Phone
Network Walkman
Pocket PC
Robot With Distributed Sensors
Vending Machine with Wireless Support
Pocket PC with VOIP

Mobile Device CPUs/MCUs -

- CPUs ARM-7 and ARM-9 (More than 50% devices)
- CPUs PowerPC 750,ColdFire, TigerSHARC
- MCUs ST72x, LPC21xx, …

Embedded RISC Core ARM7TDMI (http://www.arm.com/news/5135.html)

- ARM family of general-purpose 32-bit microprocessors offers *high performance* and *very low MIPS/watt power consumption*
- 32-bit RISC architecture

- **Design centers around and concentrate on simple instructions**
- **Smaller and simpler processor circuit, Simpler decoding sub-unit.**
- **Lower power– more space for other performing units**

Outline..

- ARM Processors
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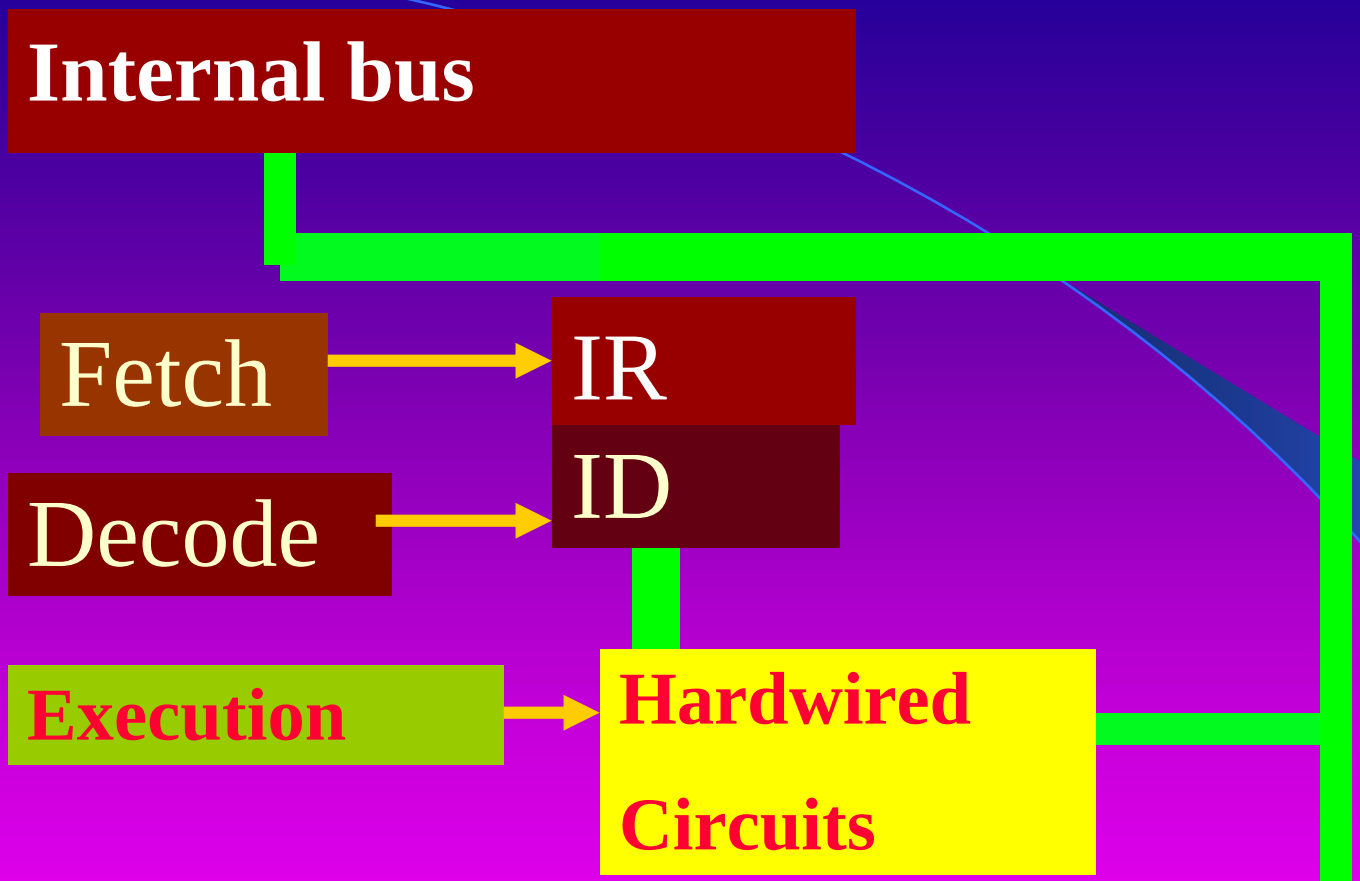
RISC Features

- Same Length instructions
- Single Cycle Execution
- Hardwired implementation of Instructions
- Large Register Set(s)
- Load and Store Architecture-



Hardwired Implementation

Outline…

- ARM Processors
- Features of a RISC architecture
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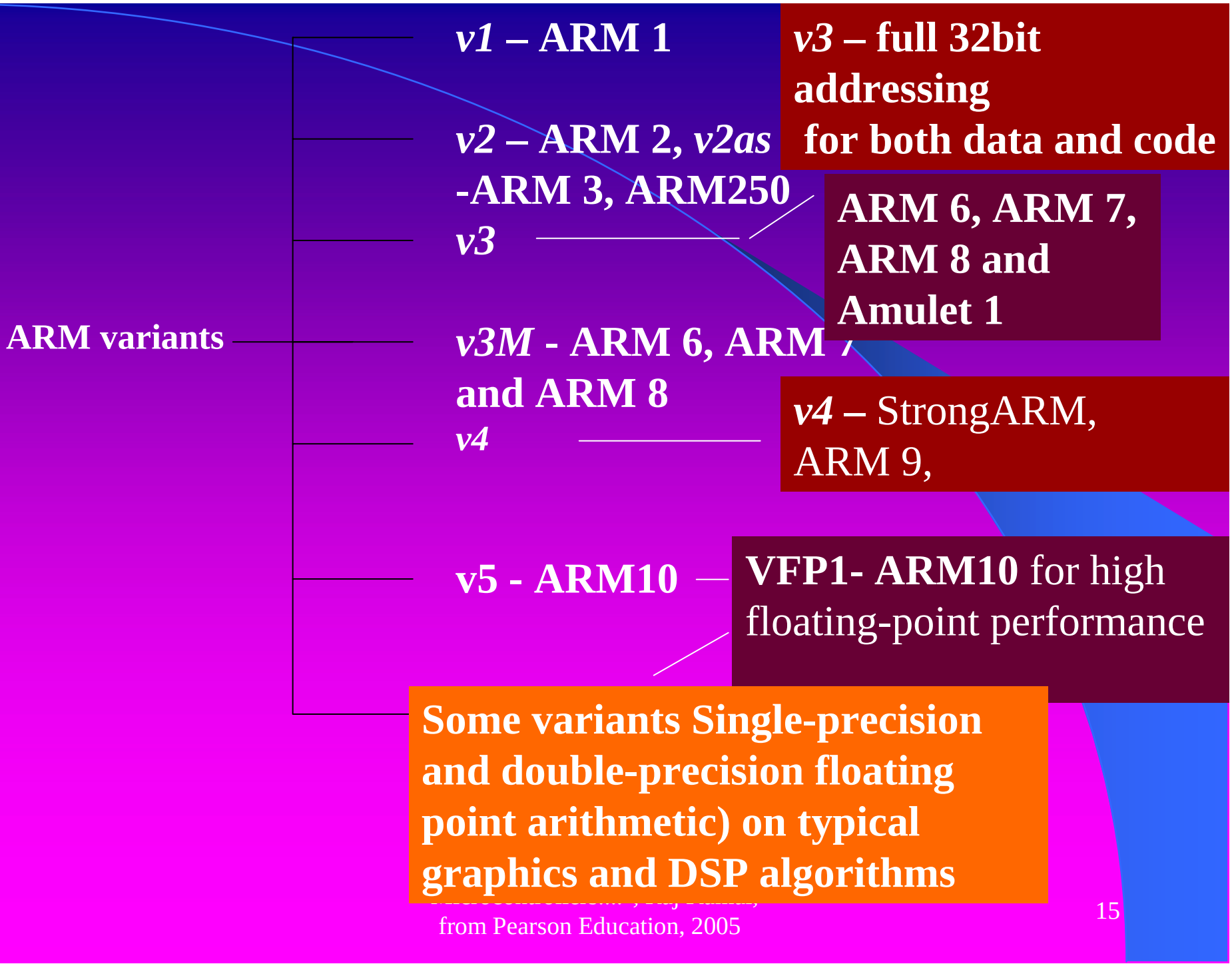
ARM® CPUs options-

- Extensive range of CPUs with third-party adaptation and application development tools

ARM Many Variant Architectures

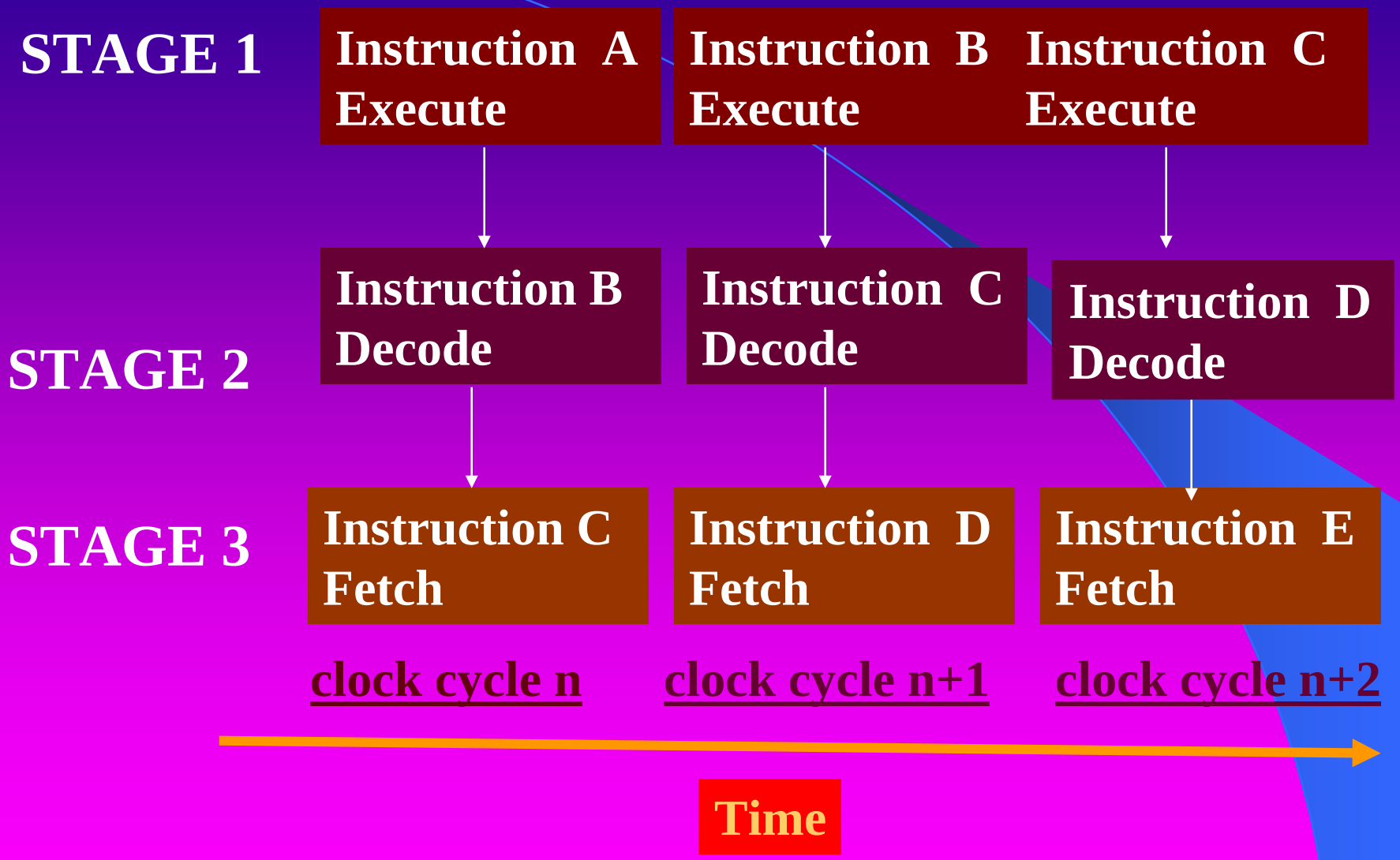
- ***ARM***
- Thumb (T) variants


ARM variants
v1 – ARM 1
v2 – ARM 2, v2as -ARM 3, ARM250
v3
v3M - ARM 6, ARM 7 and ARM 8
v4
v5 - ARM10
v3 – full 32bit addressing for both data and code
ARM 6, ARM 7, ARM 8 and Amulet 1
v4 – StrongARM, ARM 9,
VFP1- ARM10 for high floating-point performance
Some variants Single-precision and double-precision floating point arithmetic) on typical graphics and DSP algorithms

ARM® Special **Features**

- Speed-critical control signals pipelining –processing more than one instruction at the fetching, decoding and executing stages.

A three stage pipeline



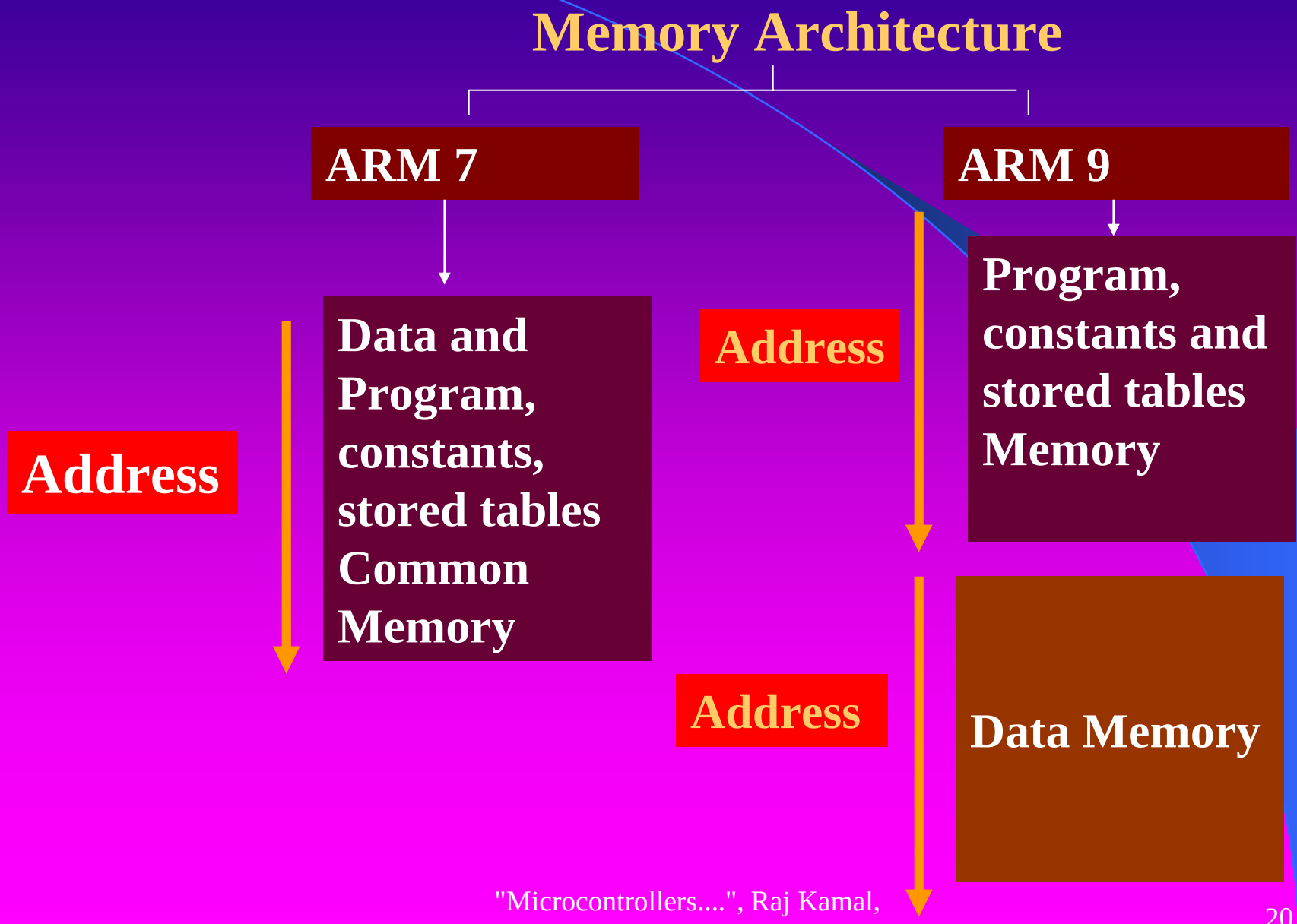
Contd…

- Three stage Pipelining in superscalar processor facilitating each instruction fetch is in single cycle, decoding in single cycle and execute in the single cycle: Three times execution speed boost up

Cond…

- ARM 7 common internal bus for the address and data of 32-bit in-32-bit Princeton architecture bus and bus interface for 32-bit data and instructions.
- ARM9 - Harvard Architecture.

Memory Architecture



Performance

- ARM 7 and ARM 9 support 300 MIPS (Million Instructions per Second) when die size is 0.13 μm.

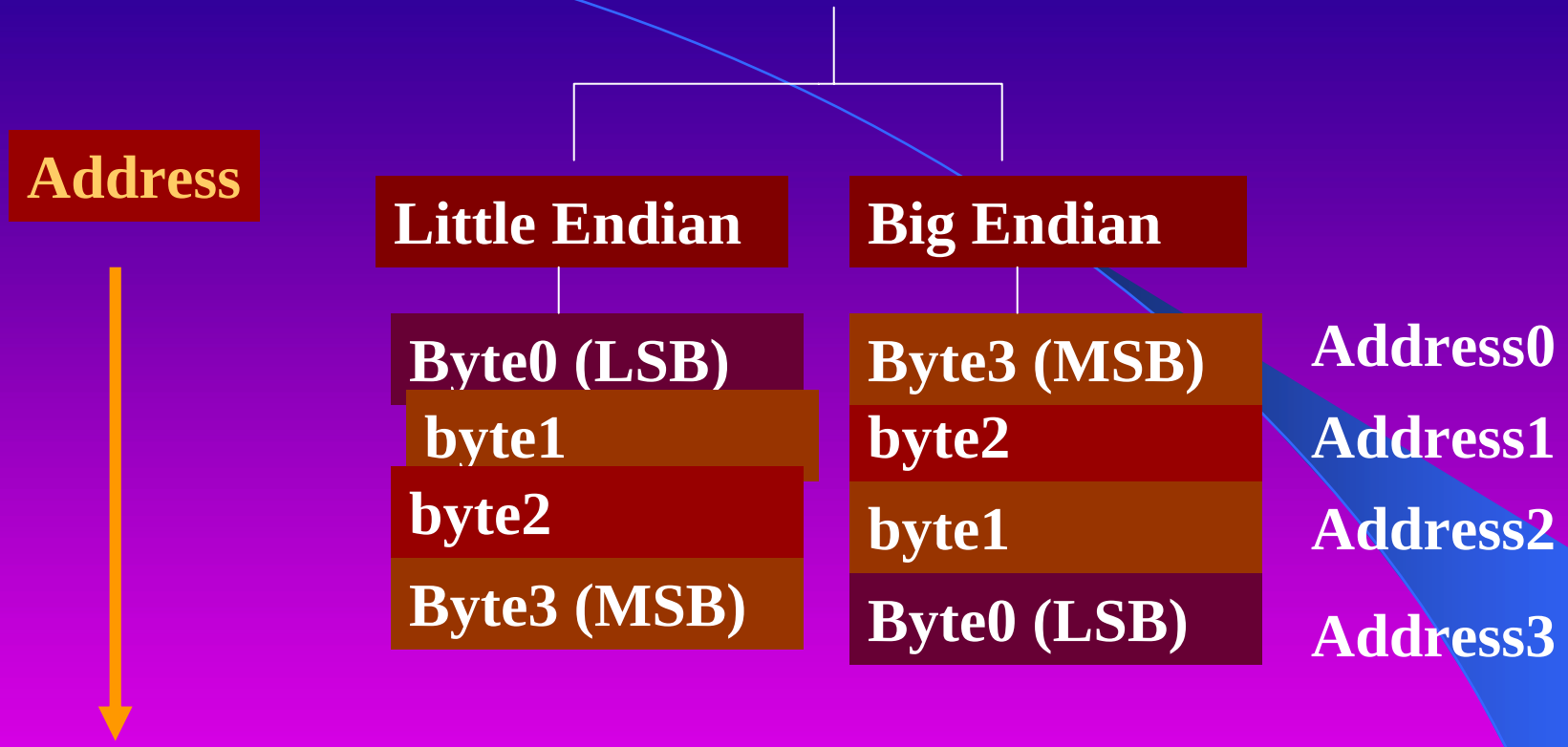
ARM 7 architecture

- Uses 0.25µm and less die size HCMOS technology, very small die size facilitating low voltage operations and low power consumption, (very small power consumption means very low MIPS/Watt)

Cond…

- Processor operation on the words *as per initialization*. A word alignment can then be in *big endian* [least significant byte stored as higher bits (address 3) of a word] or *little endian* [least significant byte stored as lower bits (address 0) of a word].

A 32bit word



Two Initialization options

Cond…

- Fully static operation- MCU clock can be reduced to 0 and since fully MOSFETs based

Cond…

- Optimized for fast interrupts and DSP algorithms
- There are two types of requests for interrupts- Fast interrupt request (FIQ) and interrupt request (IRQ). Fast means high priority.
- 4 gigabytes of linear address space

Cond…

- 32-bit large set of 16 general-purpose registers with program counter as one of the register (r15) plus CPSR and SPSR -are two other registers.

ARM Family Programming Model

- 16 general-purpose registers with program counter as one of the register (R15).

- Registers

R0 R1 R2 R3 R4 R5 R6 R7 Lo registers

R8 R9 R10 R11 R12 Hi registers

SP (R13) Stack Pointer

LR (R14) Link Register

PC (Rr15) Program Counter

CPSR SPSR

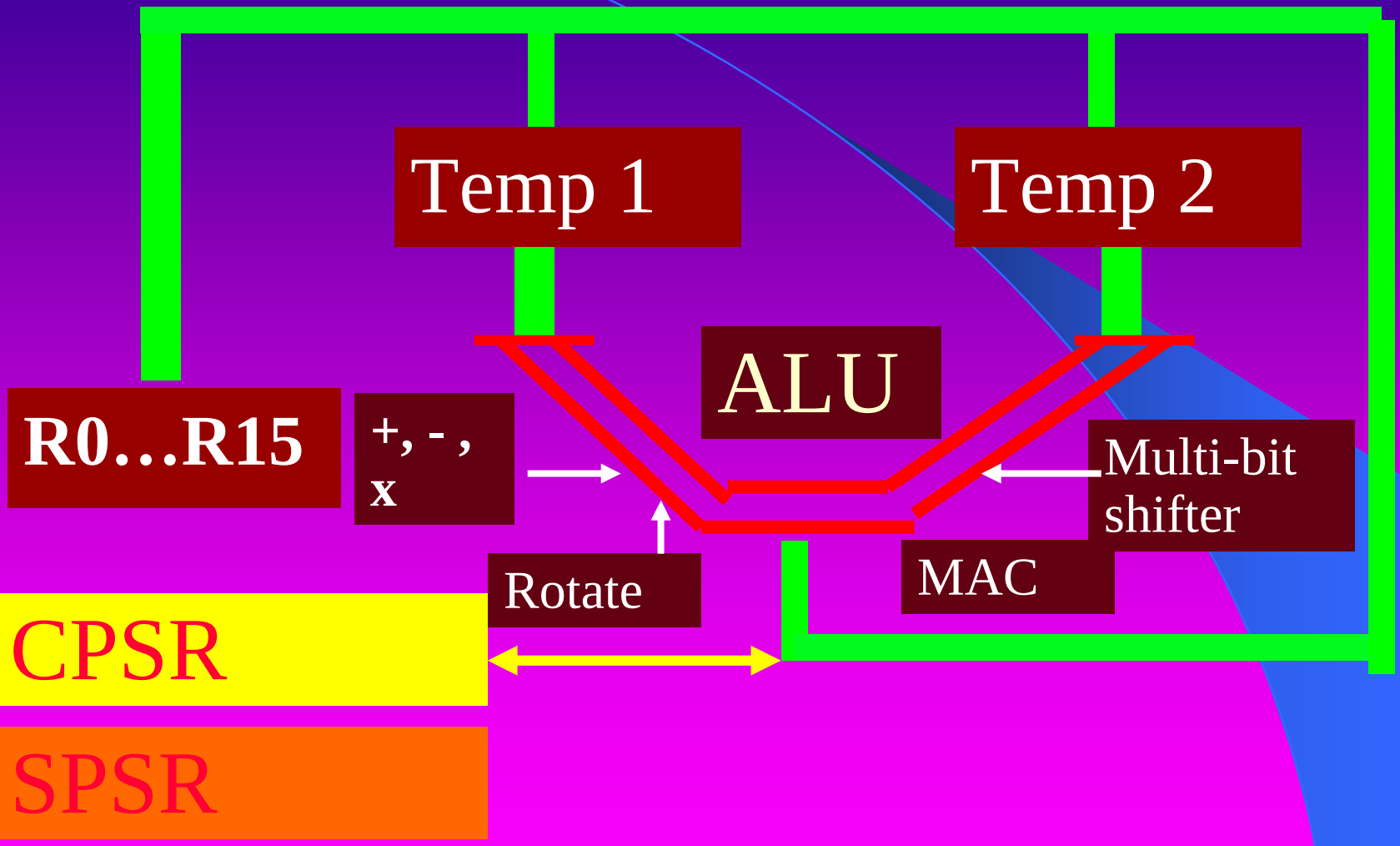
CPSR and SPSR

- CPSR (Conditions and Processor Status Register)
- SPSR (Saved Program Status Register) Saves Program Status Register from CPSR on branch and link (routine call) and SPSR can be stacked for each processor mode

Cond…

- 32-bit RALU and high-performance multiplier
- Instructions have 8-, 16-, and 32-bit data types

RALU


Temp 1
Temp 2
ALU
R0…R15
+, - , x
Multi-bit shifter
Rotate
MAC
CPSR
SPSR

Cond…

- Coprocessor interface to connect coprocessors, like DSP processors and Java Accelerators

Cond…

- System control functions implemented in standard low-power logic
- Cost-effective, compact chip

ARM 7 T Variants

ARM® TDMI ™ **instruction set** options-

1. High-performance 32-bit **instruction set-**
2. High-code-density **Thumb®**16-bit **instruction set** than 32-bit instruction architecture

Summary

- ARM family general-purpose 32-bit superscalar processors Three stage Pipeline
- High performance and very low MIPS/watt power consumption
- 32-bit RISC architecture

- 32 bit Sixteen Registers plus CPSR and SPSR
- ARM 9 and ARM7 Harvard and Princeton architectures
- Initialized options: little or big endian modes
- 32/16/8 bit data types
- Two interrupts - Fast interrupt request (FIQ) and interrupt request (IRQ)

- ARM has Many Variants
- T variants give alternate option of high code density with 16-bit instructions

- ARM 7 and ARM 9 popularly used

ARM applications

- Mobile Devices,
- PocketPC, PDA,
- Control Systems,
- DSP based applications
- Speech and Image processing
- Robotics

End of Lesson 1 on ARM CPUs

THANK YOU