DIGITAL MULTIPHASE

GEN 2 FIRMWARE 2.0.5.0 UPGRADE GUIDE

JUNE 202

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OVERVIEW

- This guide specifies the algorithm for patching firmware to version 2.0.5.0 on Renesas generation 2 digital multiphase products via PMBus communication.

- Unless noted otherwise, timing and voltage requirements are outlined in the PMBus specification version 1.3.

Note: This guide is valid only for devices using firmware version 2.0.0.4.

Prerequisites and Conventions

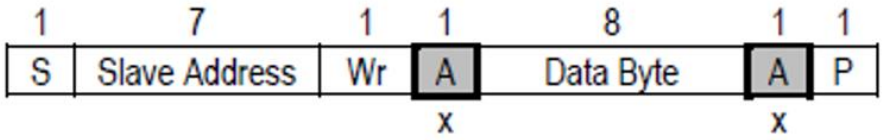
- Firmware patch files must be provided by Renesas.
- In this guide, address 0x60 (7-bit format) is used in all examples.
- Data on the bus may be reversed. Follow examples for correct byte order.

Minimum Pin and Component Requirements

The following pins must be connected when programming a device:

- PMSCL and PMSDA (I^2C clock and data pins). These are open drain and must be pulled to 3.3V via a resistor (1kΩ maximum).
- VCC, provided with an external 3.3V supply. A 1uF decoupling capacitor from this pin to ground is also needed.
- VCCS must be decoupled with 4.7µF or greater MLCC (X5R or better).
- Ground pin must be connected to ground.
- ADDRESS pin must have an address set resistor to ground. Connect directly to ground for address 0x60.
- Other pins may be floated.

PMBus Communication Key



S	Start Condition
Sr	Repeated Start Condition
Rd	Read (bit value of 1)
Wr	Write (bit value of 0)
x	Shown under a field indicates that that field is required to have the value of 'x'
A	Acknowledge (this bit position may be '0' for an ACK or '1' for a NACK)
P	Stop Condition
PEC	Packet Error Code
	Master-to-Slave
	Slave-to-Master
...	Continuation of protocol

Note: See PMBus/SMBus spec for additional details and timing requirements.

Direct Memory Access (DMA) Command Codes

Device programming is completed through 3 command codes:

- **DMA Address (Command Code 0xC7):** Used to set the register address to use with other DMA commands.
- **DMA Data (Command Code 0xC5):** Used to read from or write to the register selected by the DMA Address command.
- **DMA Sequential (Command Code 0xC6):** Used to read from or write to the register selected by the DMA Address command, then automatically increment the register address by 1.

Important Notes

- The command that commits the patch to the device is sent in step 4. Patch application can be aborted at any point before this, and no contents will be burned to OTP.

- This guide is only valid for upgrading firmware version 2.0.0.4 to version 2.0.5.0.

PATCH ALGORITHM

ALGORITHM OVERVIEW

1. **Read firmware version from device RAM. Verify the value is 0x02000004.**

2. **Halt device firmware.**
   - Patch process must wait at least 1ms after completing this step.

3. **Read and parse one line from firmware patch file. Write to device.**
   - This step must be repeated for all lines in the patch file.

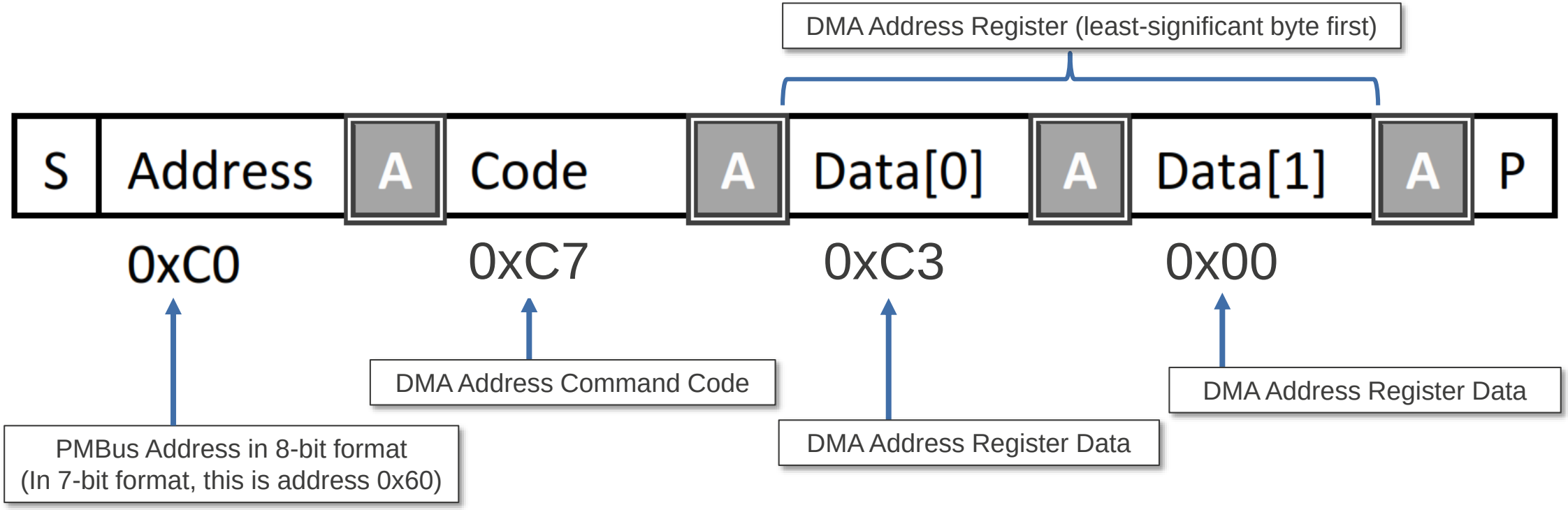
4. **Commit patch data to device.**

5. **Verify patch success.**
   a. Set DMA address register to address 0x00DA.
   b. Poll address 0x00DA until the complete bit is set.
   c. Read pass/fail bits from address 0x00DA to confirm a successful patch.

6. **Cycle VCC and verify new firmware version in device RAM.**

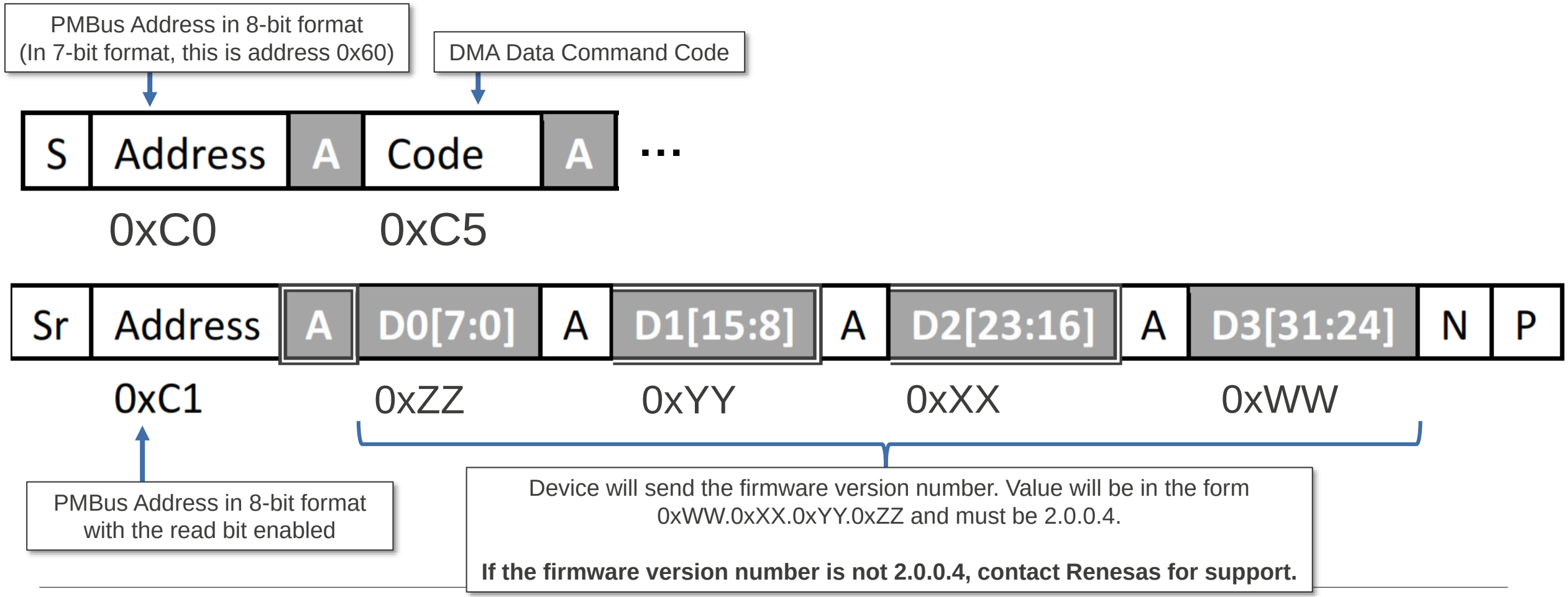
Step 1a – Write to DMA Address Register

To read the firmware version from device RAM, first set the DMA address as shown below.

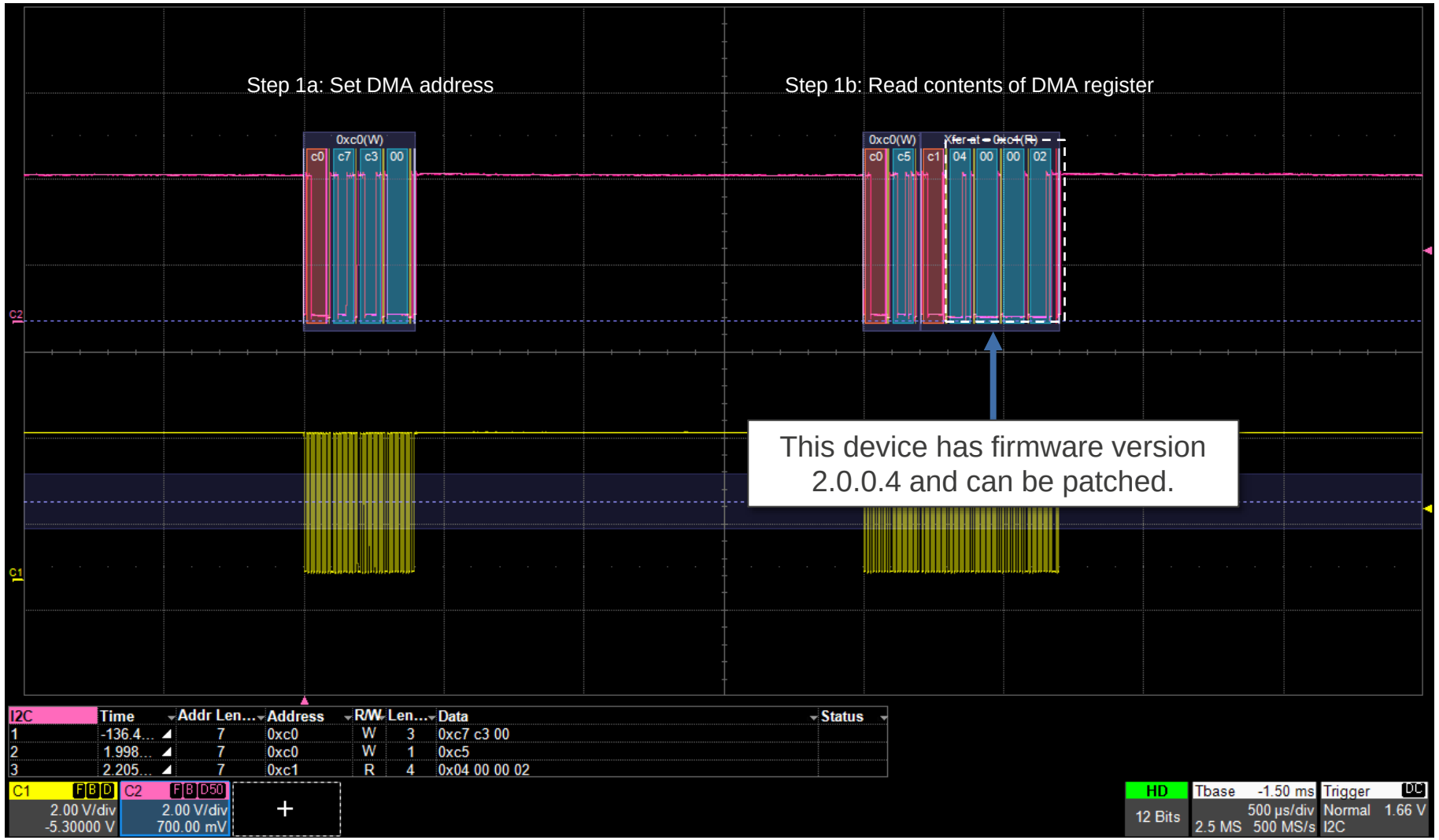


Step 1b – Read DMA Data Register

Next, Read the contents of the register pointed to in step 1a.

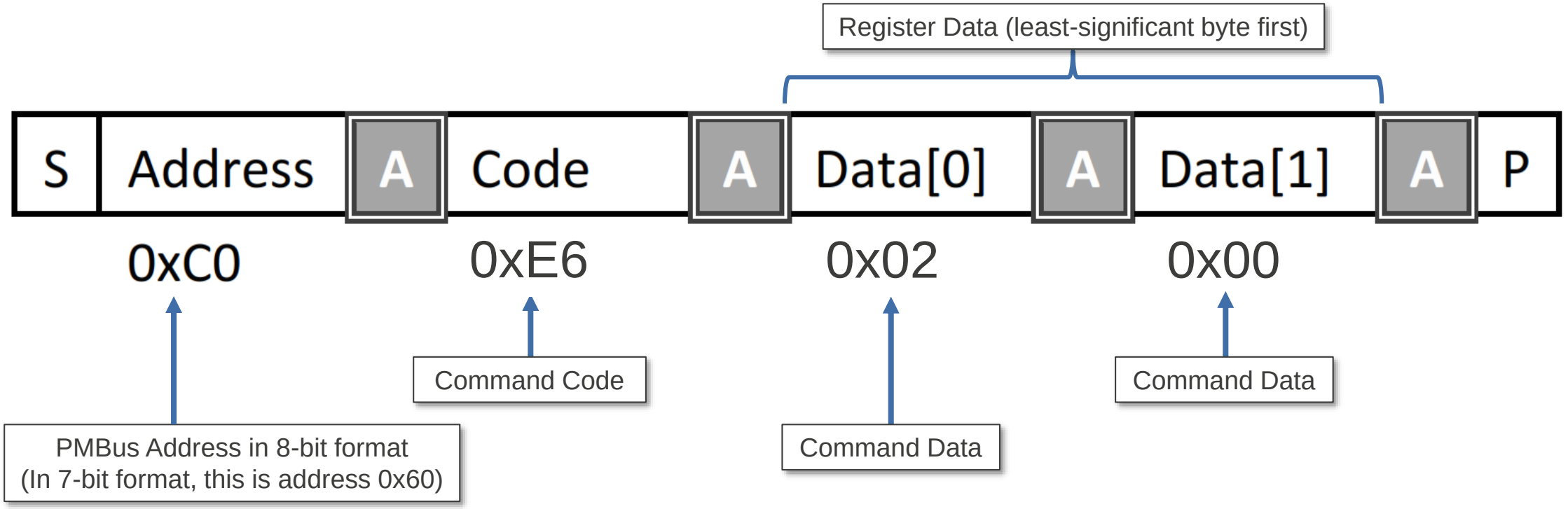


Step 1 – Example Waveforms

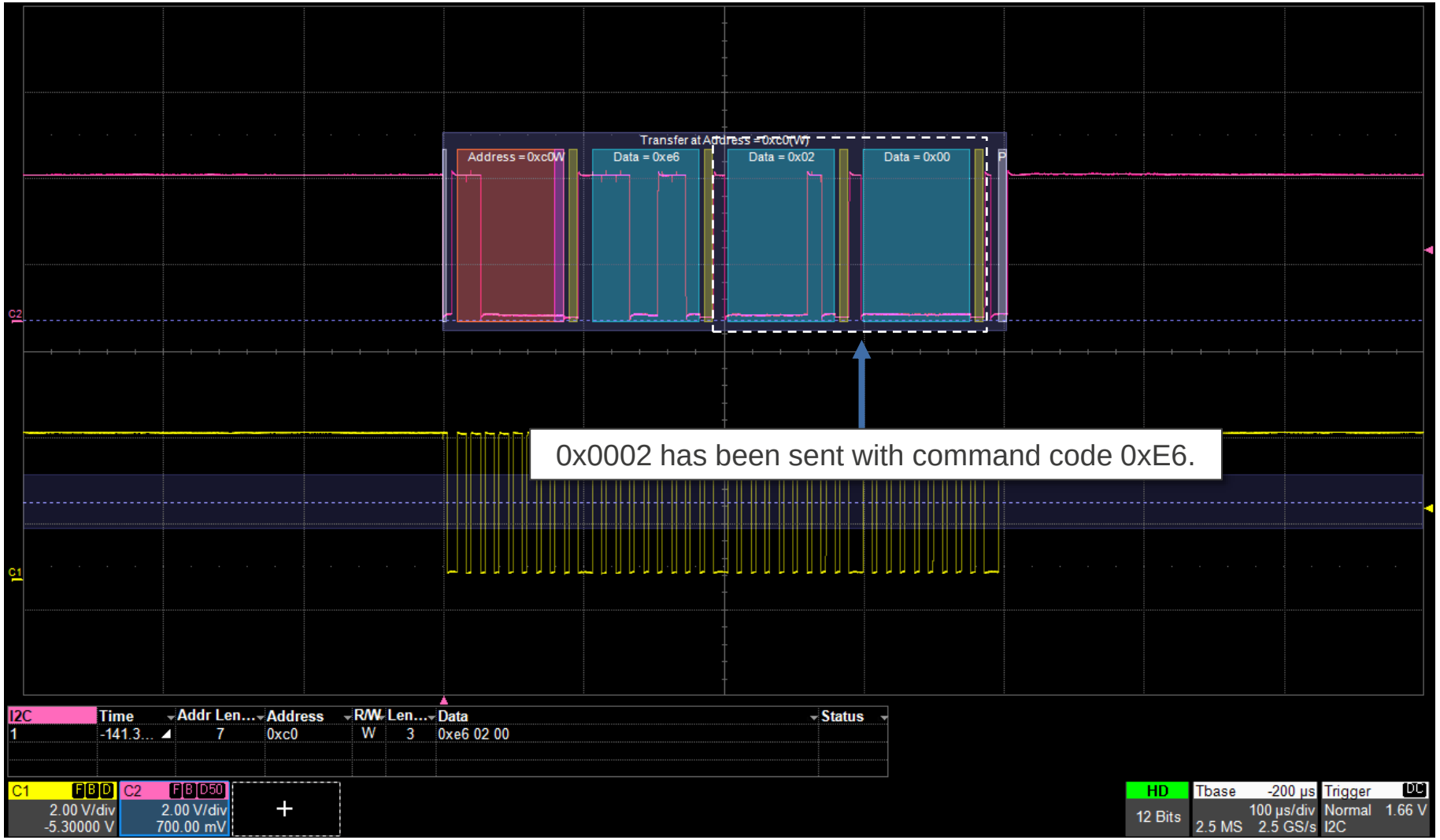


Step 2 – Halt Device Firmware

Next, send 0x02 using command code 0xE6. **Programmer must wait at least 1ms after completing this step.**



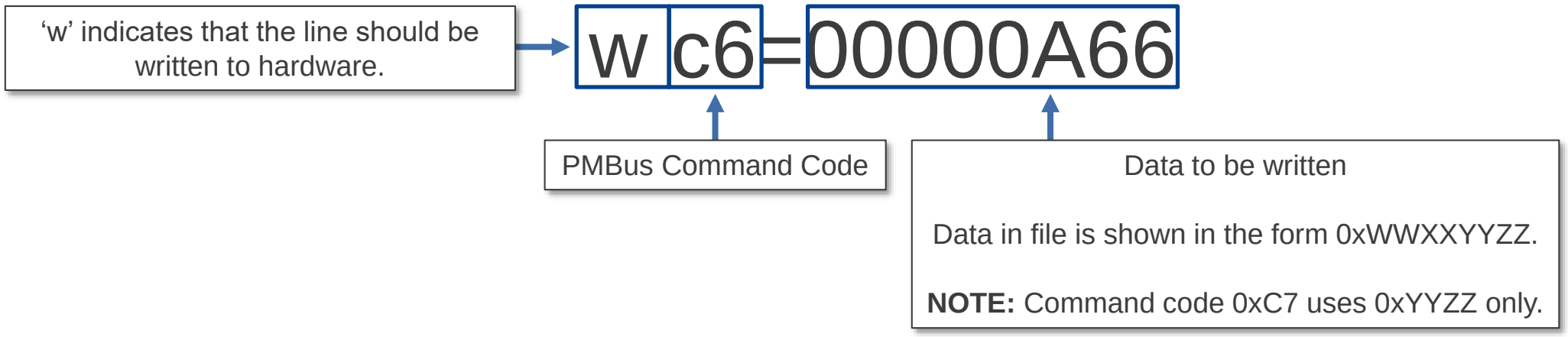
Step 2 – Example Waveform



Step 3 – Parse Patch File and Write to Hardware

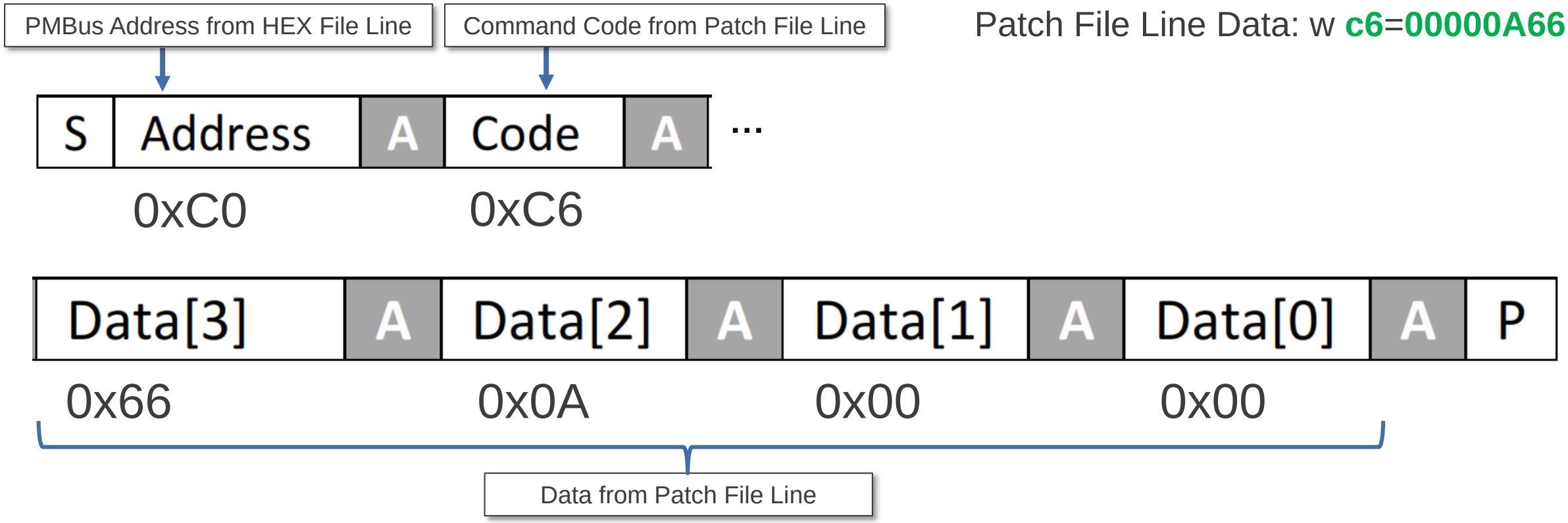
Parse lines from the firmware patch file and write to device.

Example Patch File Line:



Step 3 – Example Write of Patch File Data Line

Example PMBus Command:

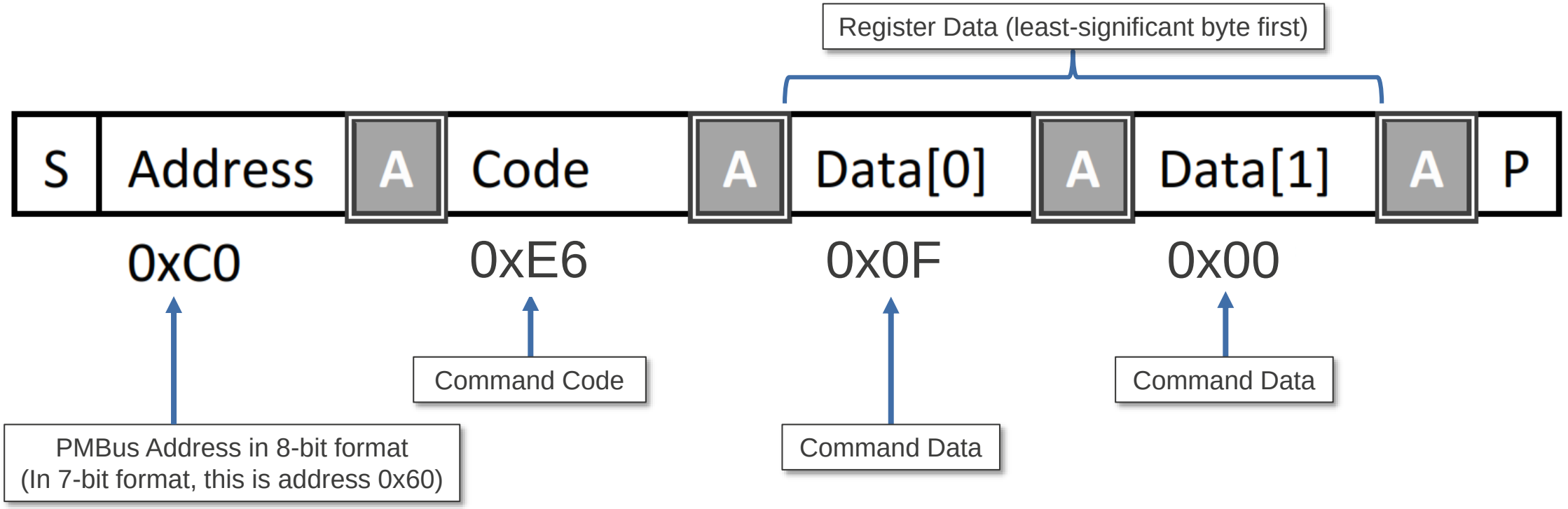


Patch File Line Data: w **c6**=**00000A66**

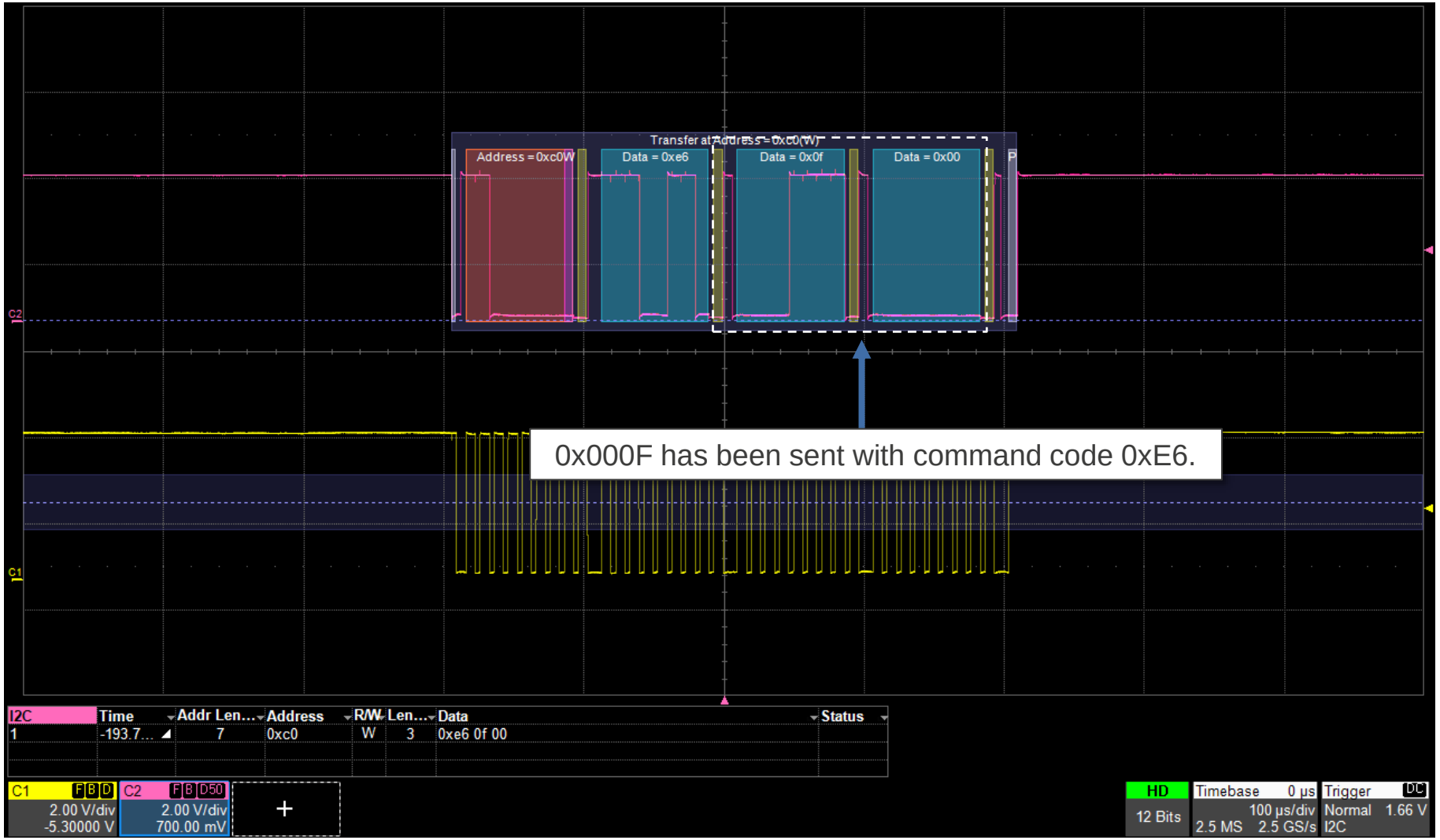
Step 3 – Example Write of Patch File Data Line

Step 4 – Commit Patch Data

Next, send 0x0F using command code 0xE6. **This command triggers the patch process and cannot be undone.**

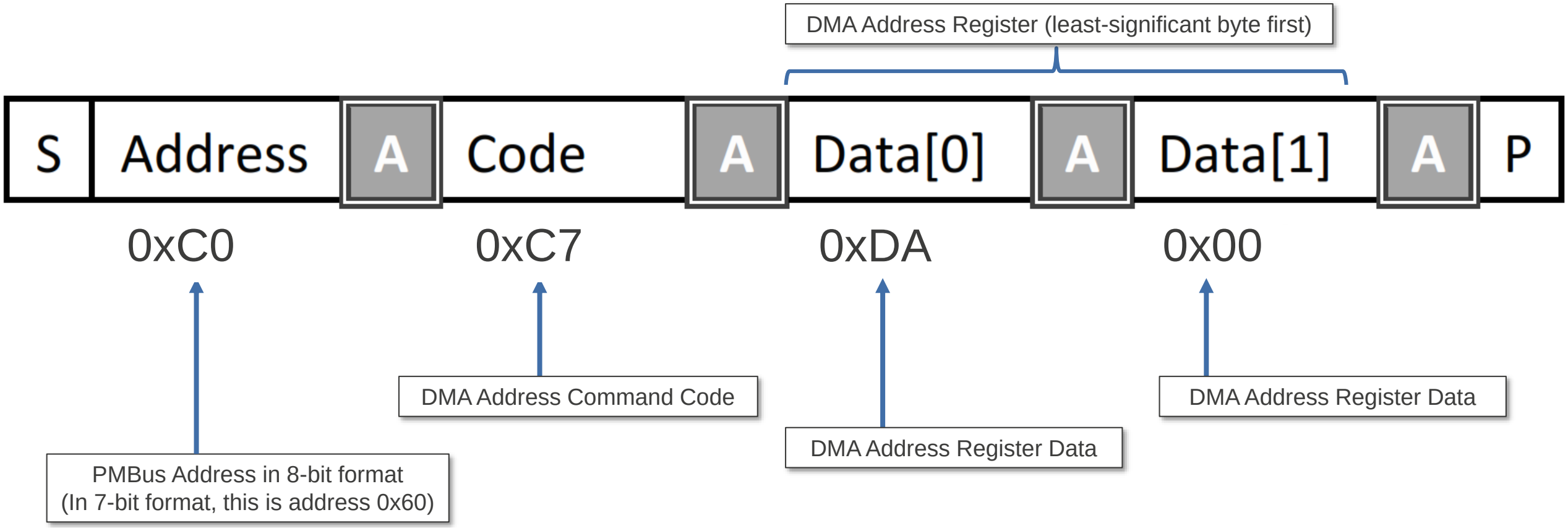


Step 4 – Example Waveform



Step 5a – Set DMA Address Register

To check for patch completion, first write to the DMA address register as shown below.

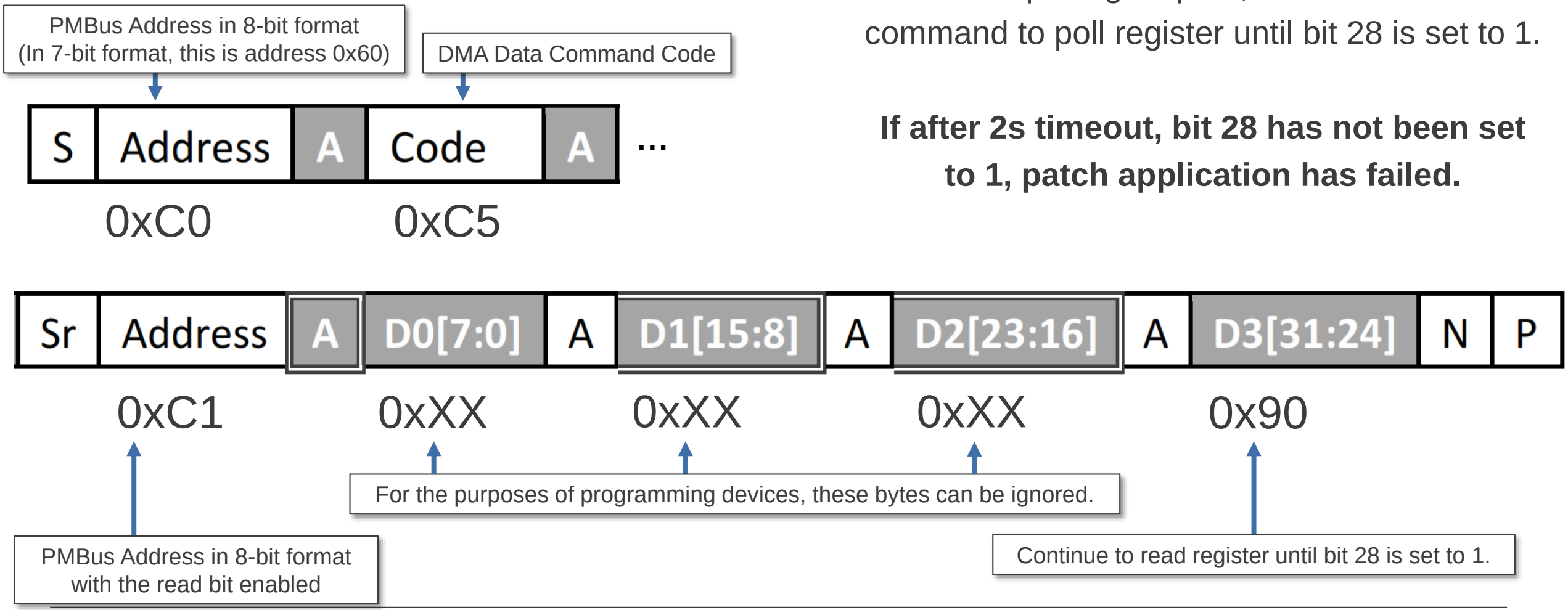


Step 5a – Example Waveform

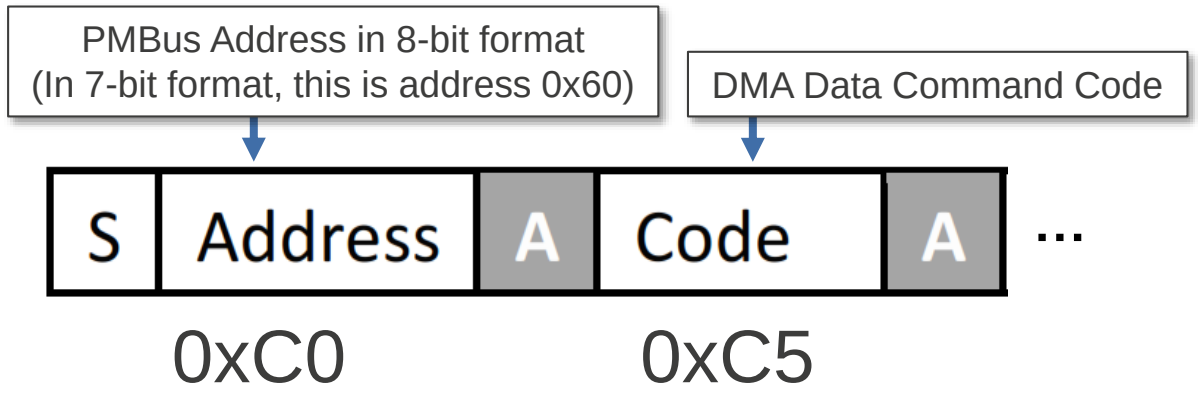
Step 5b – Poll Register for Complete Bit

After completing step 5a, use the DMA read command to poll register until bit 28 is set to 1.

If after 2s timeout, bit 28 has not been set to 1, patch application has failed.

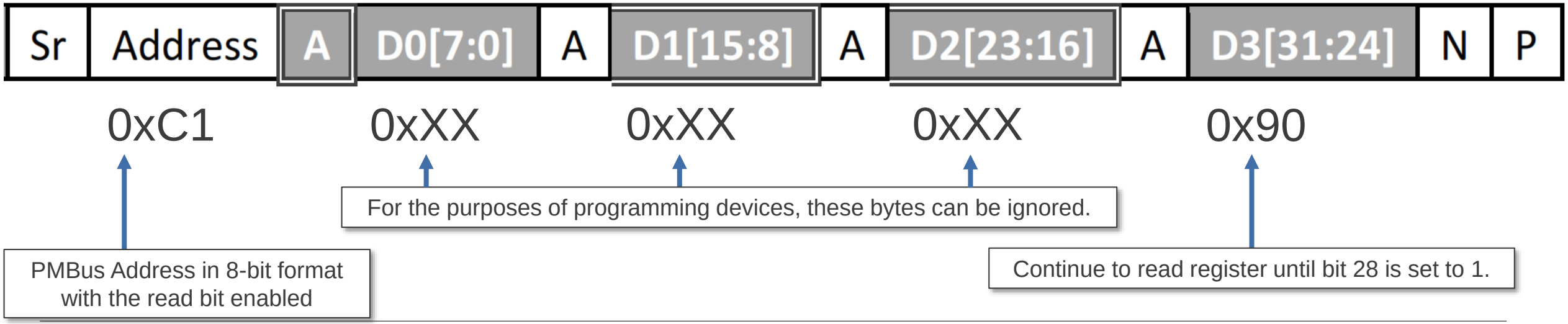


Step 5c – Read Pass/Fail Bits from Register

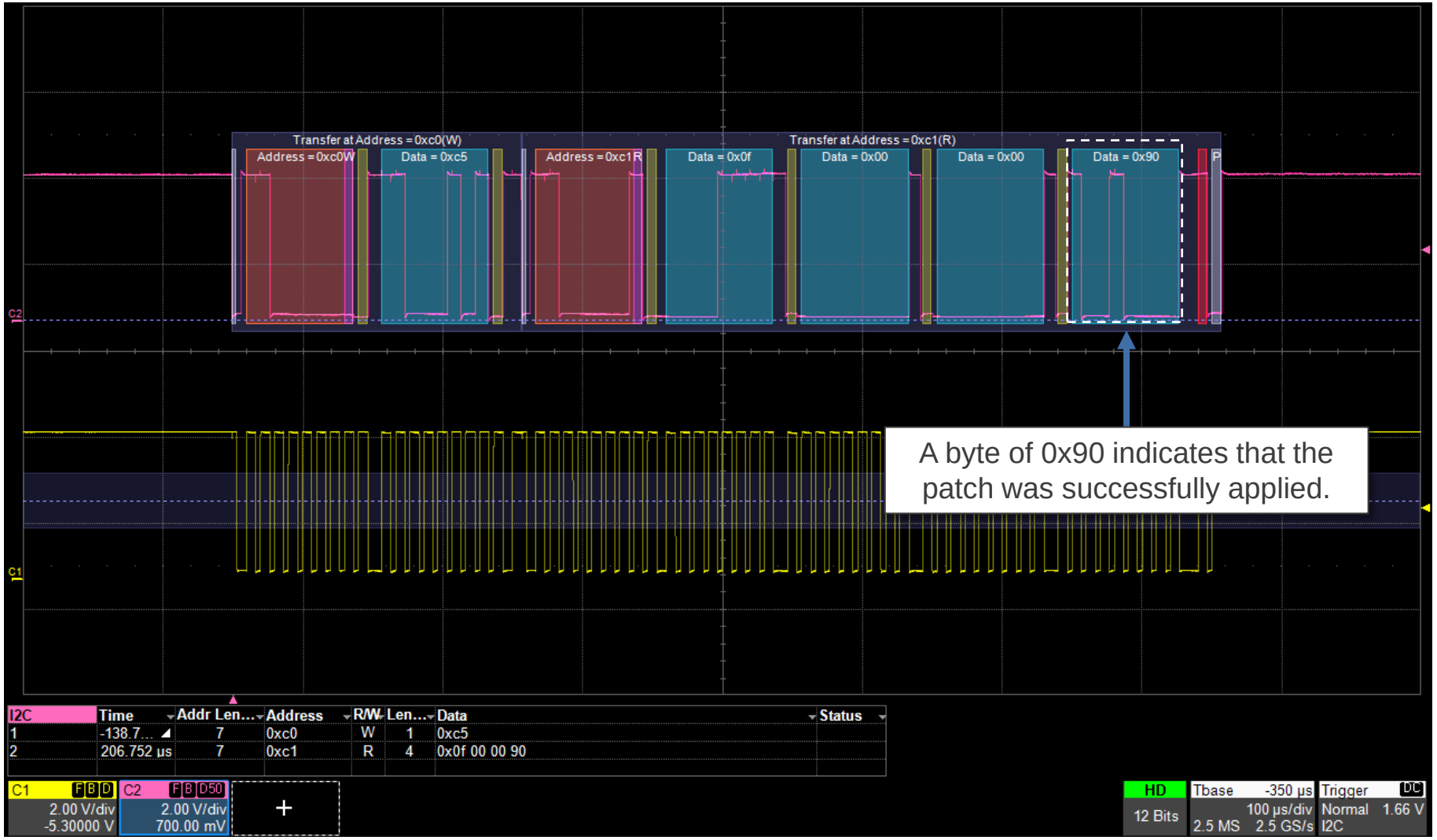


Once bit 28 is set, check bits [31:30] for the pass/fail status. Bits [31:30] must read b10.

If bits [31:30] are not b10, patch application has failed and the device is unusable.

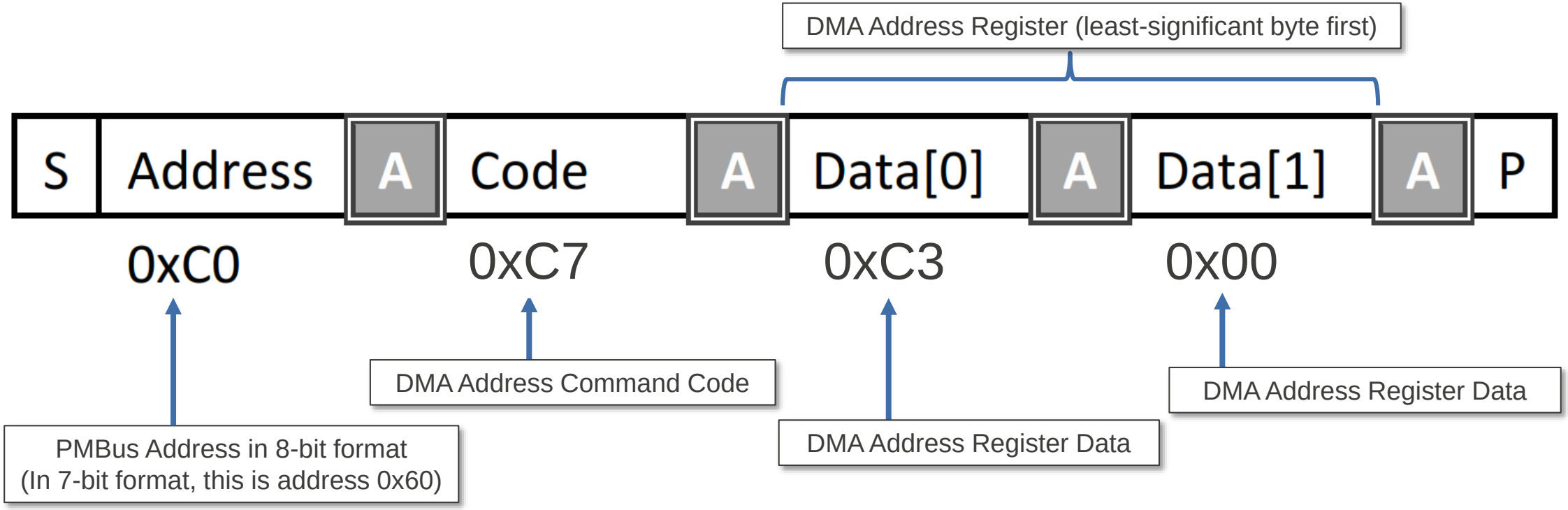


Step 5b, 5c – Example Waveform



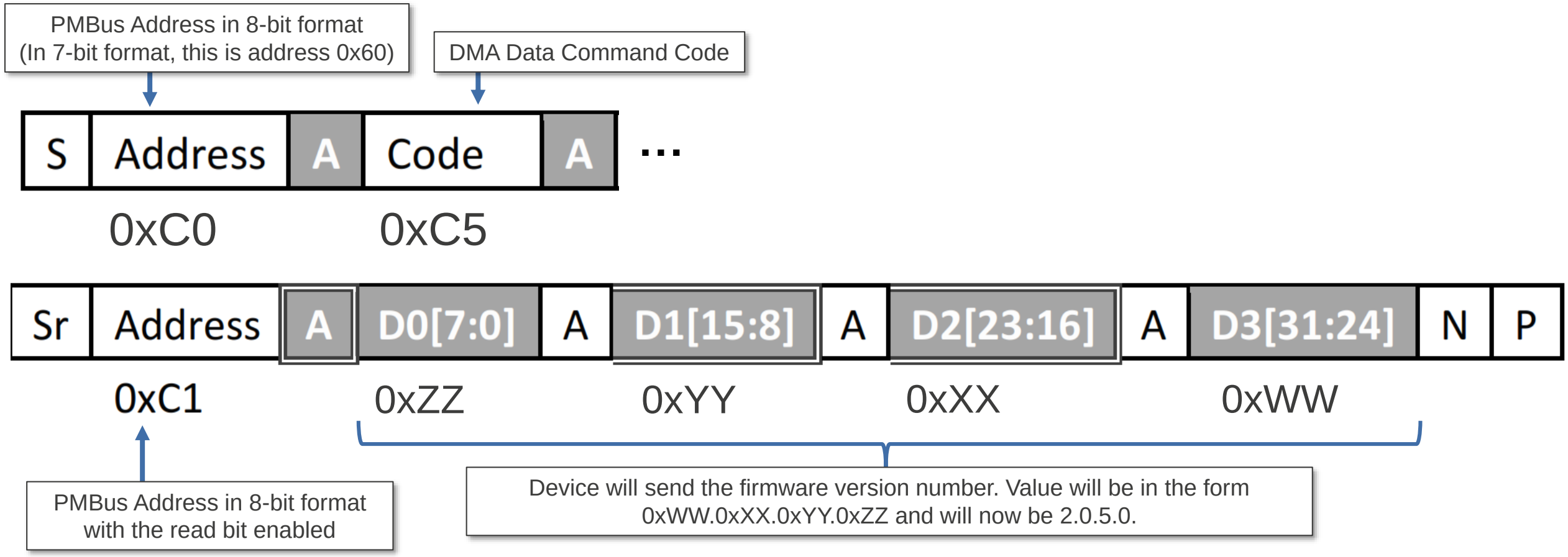
Step 6a – Write to DMA Address Register

After cycling device VCC, read the firmware version from device RAM.



Step 6b – Read DMA Data Register

Next, Read the contents of the register pointed to in step 6a.



Algorithm Completion

- After successfully applying the patch, 3.3V VCC must be powered down to apply changes if not cycled during Step 6.

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