TDA8920C

2 × 110 W class-D power amplifier

Rev. 01 — 29 September 2008 Preliminary data sheet

1. General description

The TDA8920C is a high-efficiency class-D audio power amplifier. The typical output power is 2 × 110 W with a speaker load impedance of 4 Ω.

The TDA8920C is available in both HSOP24 and DBS23P power packages. The amplifier operates over a wide supply voltage range from ±12.5 V to ±32.5 V and has a low quiescent current consumption.

2. Features

- Pin compatible with TDA8950/20B for both HSOP24 and DBS23P packages
- Symmetrical high operating supply voltage range from ±12.5 V to ±32.5 V
- Stereo full differential inputs, usable as stereo Single-Ended (SE) or mono Bridge-Tied Load (BTL) amplifier
- High output power at typical applications:
  - SE 2 × 110 W, R_L = 4 Ω (V_P = ±30 V)
  - SE 2 × 125 W, R_L = 4 Ω (V_P = ±32 V)
  - SE 2 × 120 W, R_L = 3 Ω (V_P = ±29 V)
  - BTL 1 × 210 W, R_L = 8 Ω (V_P = ±30 V)
- Low noise in BTL operation due to BD modulation
- Smooth pop noise-free start-up and switch off
- Zero dead time Pulse-Width Modulation (PWM) output switching
- Fixed frequency
- Internal or external clock switching frequency
- High efficiency
- Low quiescent current
- Advanced protection strategy: voltage protection and output current limiting
- Thermal foldback
- Fixed gain of 30 dB in SE and 36 dB in BTL
- Full short-circuit proof across load

3. Applications

- DVD
- Mini and micro receiver
- Home Theater In A Box (HTIAB) system
- High power speaker system

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4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
General, V_P = ±30 V							
V_P	supply voltage	Operating mode	[1]	±12.5	±30	±32.5	V
$V_{P(ovp)}$	overvoltage protection supply voltage	Non-Operating mode; $V_{DD} - V_{SS}$		65	-	70	V
$I_{q(tot)}$	total quiescent current	Operating mode; no load; no filter; no RC-snubber network connected		-	50	75	mA
Stereo single-ended configuration							
P_o	output power	L = 22 µH; C = 680 nF; T_j = 85 °C					
		THD = 10 %; R_L = 4 Ω; V_P = ±30 V	[2]	-	110	-	W
		THD = 10 %; R_L = 4 Ω; V_P = ±27 V		-	80	-	W
Mono bridge-tied load configuration							
P_o	output power	L = 22 µH; C = 680 nF; T_j = 85 °C; THD = 10 %; R_L = 8 Ω; V_P = ±30 V	[2]	-	210	-	W

[1] The circuit is DC adjusted at V_P = ±12.5 V to ±32.5 V.

[2] Output power is measured indirectly; based on R_{DSon} measurement; see Section 13.3.

5. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
TDA8920CJ	DBS23P	plastic DIL-bent-SIL power package; 23 leads (straight lead length 3.2 mm)	SOT411-1
TDA8920CTH	HSOP24	plastic, heatsink small outline package; 24 leads; low stand-off height	SOT566-3

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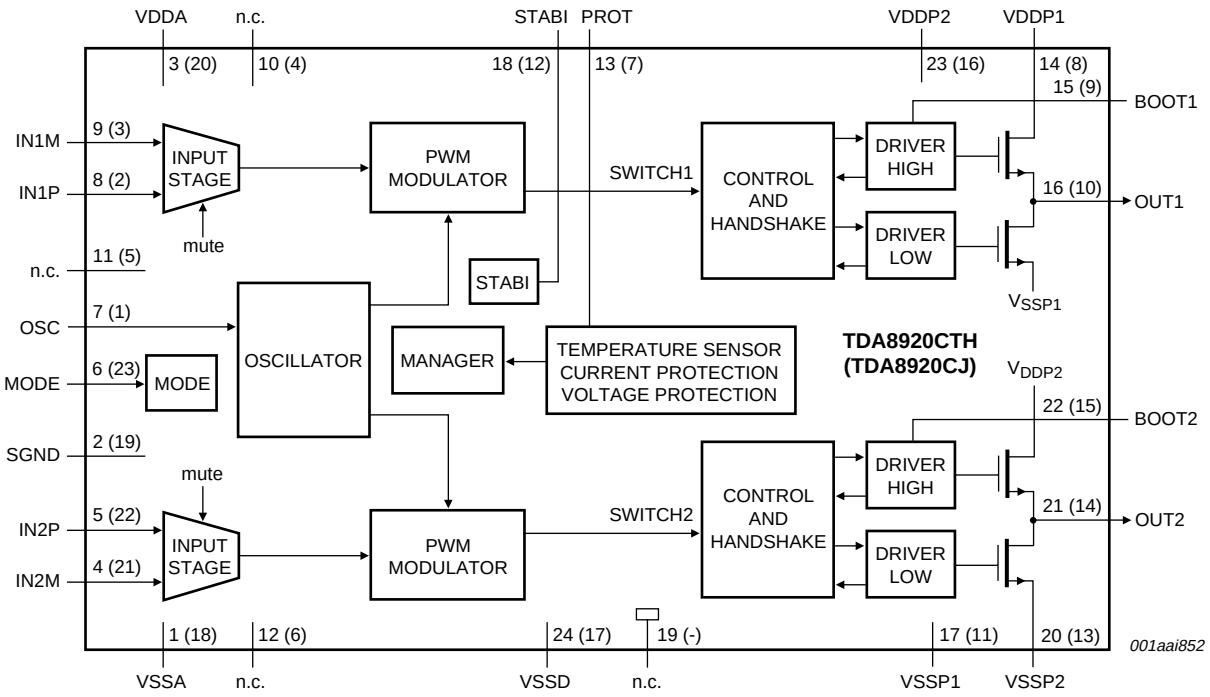
6. Block diagram



Pin numbers in brackets refer to type number TDA8920CJ.

Fig 1. Block diagram

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7. Pinning information

7.1 Pinning

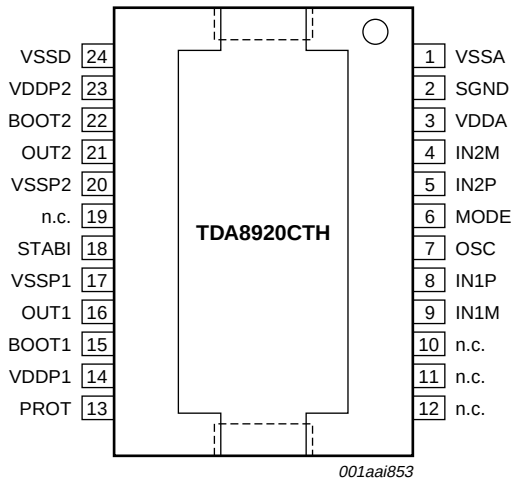

Fig 2. Pin configuration TDA8920CTH

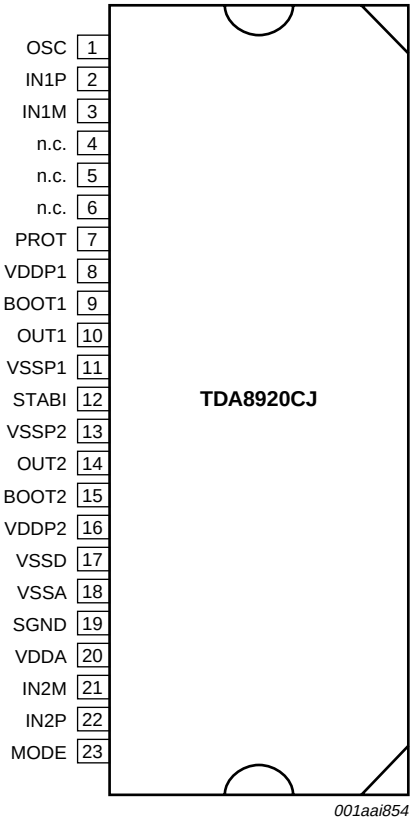

Fig 3. Pin configuration TDA8920CJ

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7.2 Pin description

Table 3. Pin description

Symbol	Pin		Description
	TDA8920CTH	TDA8920CJ	
VSSA	1	18	negative analog supply voltage
SGND	2	19	signal ground
VDDA	3	20	positive analog supply voltage
IN2M	4	21	channel 2 negative audio input
IN2P	5	22	channel 2 positive audio input
MODE	6	23	mode selection input: Standby, Mute or Operating mode
OSC	7	1	oscillator frequency adjustment or tracking input
IN1P	8	2	channel 1 positive audio input
IN1M	9	3	channel 1 negative audio input
n.c.	10	4	not connected
n.c.	11	5	not connected
n.c.	12	6	not connected
PROT	13	7	decoupling capacitor for protection (OCP)
VDDP1	14	8	channel 1 positive power supply voltage
BOOT1	15	9	channel 1 bootstrap capacitor
OUT1	16	10	channel 1 PWM output
VSSP1	17	11	channel 1 negative power supply voltage
STABI	18	12	decoupling of internal stabilizer for logic supply
n.c.	19	-	not connected
VSSP2	20	13	channel 2 negative power supply voltage
OUT2	21	14	channel 2 PWM output
BOOT2	22	15	channel 2 bootstrap capacitor
VDDP2	23	16	channel 2 positive power supply voltage
VSSD	24	17	negative digital supply voltage

8. Functional description

8.1 General

The TDA8920C is a two-channel audio power amplifier using class-D technology.

The audio input signal is converted into a digital pulse-width modulated signal using an analog input stage and PWM modulator; see Figure 1. To enable the output power transistors to be driven, the digital PWM signal is applied to a control and handshake block and driver circuits for both the high side and low side. This level-shifts the low-power digital PWM signal from a logic level to a high-power PWM signal switching between the main supply lines.

A 2nd-order low-pass filter converts the PWM signal to an analog audio signal across the loudspeakers.

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The TDA8920C single-chip class-D amplifier has built-in high-power switches, drivers, timing and handshaking between the power switches and some control logic. In addition, to secure maximum system robustness, an advanced protection strategy is implemented for voltage, temperature and maximum current.

Both of the TDA8920C audio channels contain a PWM modulator, an analog feedback loop and a differential input stage. The TDA8920C also contains circuits common to both channels such as the oscillator, all reference sources, the mode interface and a digital timing manager.

The two independent amplifier channels have high output power, high efficiency, low distortion and low quiescent current. The amplifier channels can be connected in the following configurations:

- Mono Bridge-Tied Load (BTL) amplifier
- Stereo Single-Ended (SE) amplifiers

The amplifier system can be switched to one of three operating modes using pin MODE:

- Standby mode: with a very low supply current
- Mute mode: the amplifiers are operational but the audio signal at the output is suppressed by disabling the voltage-to-current (VI) converter input stages
- Operating mode: the amplifiers are fully operational with the output signal

To ensure pop noise-free start-up, the DC output offset voltage is applied gradually to the output at a level between Mute mode and Operating mode levels. The bias-current setting of the VI-converters is related to the voltage on pin MODE. In Mute mode the bias-current setting of the VI-converters is zero (VI-converters are disabled). In Operating mode the bias current is at maximum. The time-constant required to apply the DC output offset voltage gradually between Mute and Operating mode levels can be generated using an RC network on pin MODE. An example of a switching circuit for driving pin MODE is illustrated in Figure 4. If the capacitor C is left out of the application the voltage on pin MODE is applied with a much smaller time-constant, which may result in audible pop noises during start-up (depending on the DC output offset voltage and loudspeaker used).

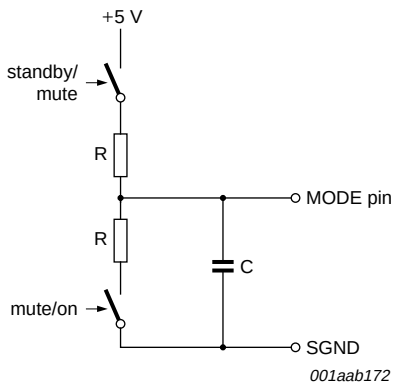

Fig 4. Example of mode selection circuit

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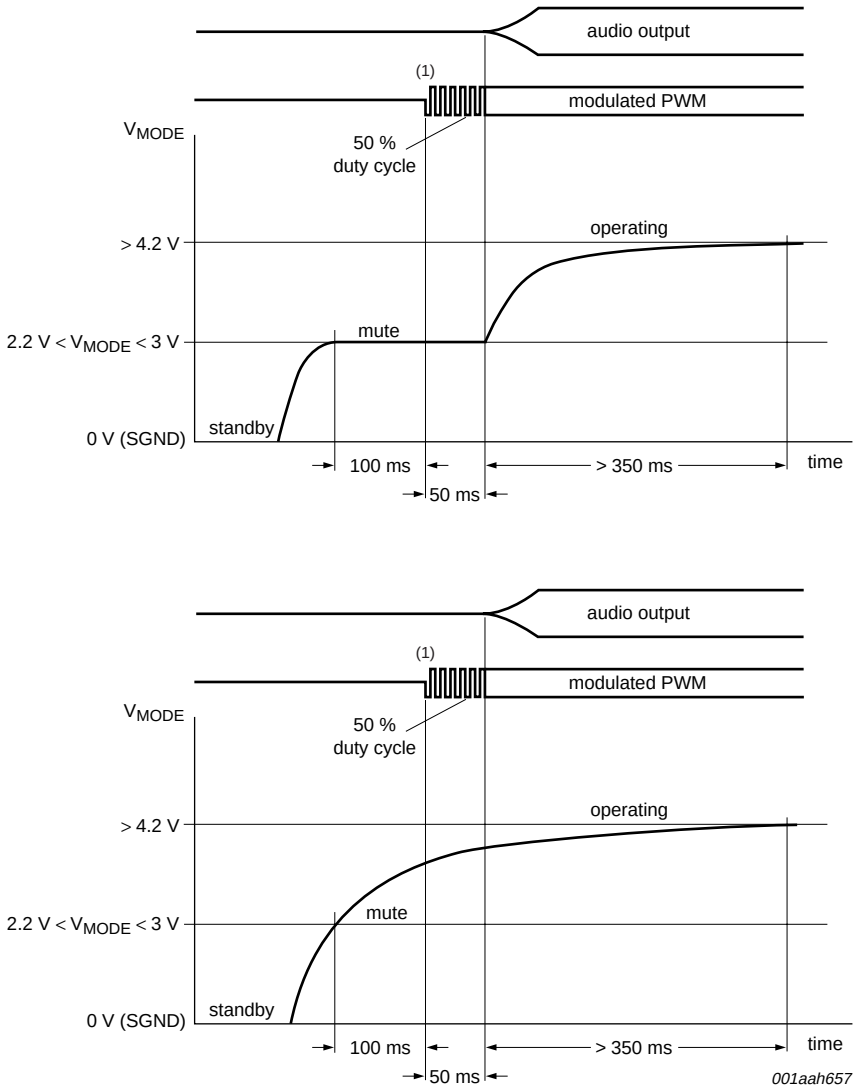
To fully charge the coupling capacitors at the inputs, the amplifier automatically remains in the Mute mode before switching to the Operating mode. A complete overview of the start-up timing is shown in Figure 5.



(1) First ¼ pulse down.

Upper diagram: When switching from standby to mute there is a delay of approximately 100 ms before the output starts switching. The audio signal is available after V_{MODE} is set to operating but not earlier than 150 ms after switching to mute. To start up pop noise-free, it is recommended that the time-constant applied to pin MODE is at least 350 ms for the transition between mute and operating.

Lower diagram: When switching directly from standby to operating there is a delay of 100 ms before the outputs start switching. The audio signal is available after a second delay of 50 ms. To start up pop noise-free, it is recommended that the time-constant applied to pin MODE is at least 500 ms for the transition between standby and operating.

Fig 5. Timing on mode selection input pin MODE

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8.2 Pulse-width modulation frequency

The output signal of the amplifier is a PWM signal with a carrier frequency typically between 300 kHz and 400 kHz. Using a 2nd-order LC demodulation filter in the application results in an analog audio signal across the loudspeaker. The carrier frequency is determined by an external resistor R_{OSC}, connected between pin OSC and pin VSSA. An optimal setting for the carrier frequency is between 300 kHz and 400 kHz.

The carrier frequency is set to 345 kHz by connecting a 30 kΩ external resistor between pin OSC and VSSA. See Table 8 for more details.

If two or more class-D amplifiers are used in the same audio application, it is recommended that all devices use an external clock circuit to ensure that they operate at the same switching frequency.

8.3 Protection

The following protection strategies are provided:

- Thermal protection:
  - Thermal FoldBack (TFB)
  - OverTemperature Protection (OTP)
- OverCurrent Protection (OCP, diagnostic output on pin PROT)
- Window Protection (WP)
- Supply voltage protection:
  - UnderVoltage Protection (UVP)
  - OverVoltage Protection (OVP)
  - UnBalance Protection (UBP)

The device reacts to fault conditions differently for each protection type.

8.3.1 Thermal protection

The TDA8920C has an advanced thermal protection strategy. It consists of a TFB function that gradually reduces the output power within a defined temperature range. If the temperature continues to rise, OTP is implemented, shutting down the device completely.

8.3.1.1 Thermal FoldBack (TFB)

If the junction temperature (T_j) exceeds the defined threshold value, the gain is gradually reduced. This reduces the output signal amplitude and the power dissipation, eventually stabilizing the temperature.

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TFB is specified at the thermal foldback activation temperature $T_{act(th_fold)}$ where the closed-loop voltage gain is reduced by 6 dB. The TFB range is:

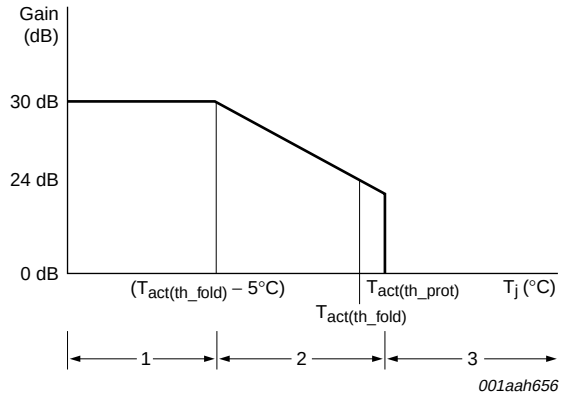
$T_{act(th_fold)} - 5\ °C < T_{act(th_fold)} < T_{act(th_prot)}$

The value of $T_{act(th_fold)}$ for the TDA8920C is approximately 153 °C; see Table 7 for more details.

8.3.1.2 OverTemperature Protection (OTP)

If despite the TFB function, the junction temperature (T_j) of the TDA8920C continues to rise exceeding the thermal protection activation temperature $T_{act(th_prot)}$, the amplifier shuts down immediately. The amplifier resumes switching approximately 100 ms after the temperature drops below $T_{act(th_prot)}$.

The thermal behavior is illustrated in Figure 6.



(1) Duty cycle of PWM output modulated according to the audio input signal.

(2) Duty cycle of PWM output reduced due to TFB.

(3) Amplifier is switched off due to OTP.

Fig 6. Behavior of TFB and OTP

8.3.2 OverCurrent Protection (OCP)

OverCurrent Protection (OCP) will detect a short-circuit applied to any of the demodulated outputs of the amplifier. If the output current exceeds the 9.2 A maximum, it is automatically limited to its maximum value by the OCP protection circuit, the amplifier is NOT shut down completely, and the amplifier outputs continue switching. If the active current limiting continues longer than time (τ), the TDA8920C shuts down. Activation of current limiting and the triggering of OCP are output at pin PROT.

OCP can distinguish between a loudspeaker impedance drop and a low-ohmic short-circuit across the load. In the TDA8920C, the impedance threshold (Z_{th}) depends on the supply voltage used.

If a short-circuit occurs across the load causing the impedance to drop below the threshold level (< Z_{th}), the amplifier switches off completely. After 100 ms, it tries to restart. If the short-circuit condition is still present, the cycle is repeated. The average power dissipation will be low because of the low duty cycle.

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If an impedance drop occurs (e.g. due to dynamic behavior of the loudspeaker) OCP is activated. The maximum output current stays limited to 9.2 A but the amplifier will not switch off completely, preventing audio holes from occurring. The result is a clipped output signal.

See Section 13.7 for more information on this maximum output current limiting feature.

8.3.3 Window Protection (WP)

Window Protection (WP) checks the conditions at the output terminals of the power stage and is activated:

- During the start-up sequence, when pin MODE is switched from standby to mute. In the event of a short-circuit at one of the output terminals to pin VDDPn or pin VSSPn, the start-up procedure is interrupted. The TDA8920C waits until the short-circuit to the supply lines is removed. No large currents will flow in the event of a short-circuit because the test is done before the power stages are enabled.
- When the amplifier shuts down completely due to OCP activation because of a short-circuit to one of the supply lines; WP is activated during a restart after 100 ms. The amplifier will not start up until the short-circuit to the supply lines is removed.

8.3.4 Supply voltage protection

If the supply voltage drops below the minimum supply voltage, the UnderVoltage Protection (UVP) circuit is activated and the system shuts down correctly. If the internal clock is used, the switch-off will be silent and without pop noise. When the supply voltage rises above the threshold level, the system restarts after 100 ms.

If the supply voltage exceeds the maximum supply voltage, the OVP circuit is activated and the power stages are shut down. When the supply voltage drops below the threshold level, the system restarts after 100 ms.

An additional UnBalance Protection (UBP) circuit compares the positive analog voltage (on pin VDDA) and the negative analog supply voltage (on pin VSSA) and is triggered if the voltage difference exceeds a factor of two.

When the supply voltage difference drops below the threshold level, the system restarts after 100 ms.

Example: With a symmetrical supply of ±30 V, the protection circuit is triggered if the unbalance exceeds approximately 15 V; see Section 13.7.

An overview is given of all protection strategies and their respective effects on the output signal in Table 4.

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Table 4. Overview of TDA8920C protection strategies

Protection name	Complete shutdown	Restart directly	Restart after 100 ms	Pin PROT detection
TFB[1]	N	N	N	N
OTP	Y	N	Y	N
OCP	Y[2]	N[2]	Y[2]	Y
WP	N[3]	Y	N	N
UVP	Y	N	Y	N
OVP	Y	N	Y	N
UBP	Y	N	Y	N

[1] Amplifier gain depends on the junction temperature and heatsink size.

[2] Only complete shutdown of the amplifier if short-circuit impedance is below the threshold of 1 Ω. In all other cases current limiting results in a clipped output signal.

[3] Fault condition detected during (every) transition between standby-to-mute and during a restart after activation of OCP (short-circuit to one of the supply lines).

8.4 Differential audio inputs

The audio inputs are fully differential ensuring a high common mode rejection ratio and maximum flexibility in the application.

- Stereo operation: it is advised to use the inputs in anti-phase and connect the speakers in anti-phase, to avoid acoustical phase differences. The construction advantages are:
  - minimized power supply peak current
  - minimized supply pumping effect, especially at low audio frequencies
- Mono BTL operation: it is required that the inputs are connected in anti-parallel. The output of one channel is inverted and the speaker load is connected between the two outputs of the TDA8920C. In principle, the output power to the speaker can be boosted to twice the output power of single-ended stereo.

  The input configuration for a mono BTL application is illustrated in Figure 7.

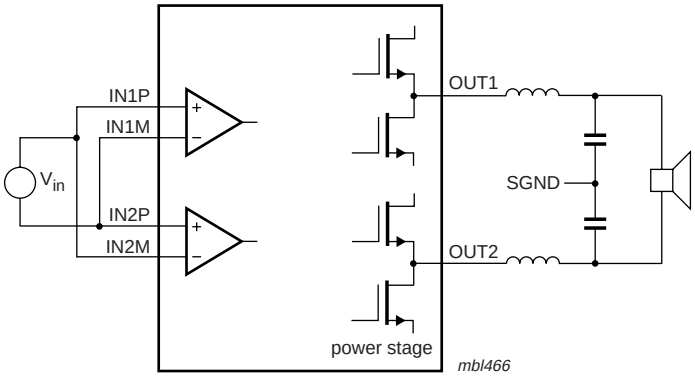

Fig 7. Input configuration for mono BTL application

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9. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_P	supply voltage	Non-Operating mode; $V_{DD} - V_{SS}$	-	65	V
I_{ORM}	repetitive peak output current	maximum output current limiting	9.2	-	A
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	ambient temperature		–40	+85	°C
T_j	junction temperature		-	150	°C
V_{MODE}	voltage on pin MODE	referenced to SGND	0	6	V
V_{OSC}	voltage on pin OSC		0	SGND + 6	V
V_I	input voltage	referenced to SGND; pin IN1P; IN1M; IN2P and IN2M	–5	+5	V
V_{PROT}	voltage on pin PROT	referenced to voltage on pin VSSD	0	12	V
V_{esd}	electrostatic discharge voltage	Human Body Model (HBM); pin VSSP1 with respect to other pins	–1800	+1800	V
		HBM; all other pins	–2000	+2000	V
		Machine Model (MM); all pins	–200	+200	V
		Charged Device Model (CDM)	–500	+500	V
$I_{q(tot)}$	total quiescent current	Operating mode; no load; no filter; no RC-snubber network connected	-	75	mA

10. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	40	K/W
$R_{th(j-c)}$	thermal resistance from junction to case		1.1	K/W

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11. Static characteristics

Table 7. Static characteristics

V_P = ±30 V; f_{osc} = 345 kHz; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supply							
V_P	supply voltage	Operating mode	[1]	±12.5	±30	±32.5	V
$V_{P(ovp)}$	overvoltage protection supply voltage	non-Operating mode; $V_{DD} - V_{SS}$		65	-	70	V
$V_{P(uvp)}$	undervoltage protection supply voltage	$V_{DD} - V_{SS}$		20	-	25	V
$I_{q(tot)}$	total quiescent current	Operating mode; no load; no filter; no RC-snubber network connected		-	50	75	mA
I_{stb}	standby current	measured at 30 V		-	480	600	µA
Mode select input; pin MODE							
V_{MODE}	voltage on pin MODE	referenced to SGND	[2]	0	-	6	V
		Standby mode	[2][3]	0	-	0.8	V
		Mute mode	[2][3]	2.2	-	3.0	V
		Operating mode	[2][3]	4.2	-	6	V
I_I	input current	V_I = 5.5 V		-	110	150	µA
Audio inputs; pins IN1M, IN1P, IN2P and IN2M							
V_I	input voltage	DC input	[2]	-	0	-	V
Amplifier outputs; pins OUT1 and OUT2							
$V_{O(offset)}$	output offset voltage	SE; Mute mode		-	-	±25	mV
		SE; Operating mode	[4]	-	-	±150	mV
		BTL; Mute mode		-	-	±30	mV
		BTL; Operating mode	[4]	-	-	±210	mV
Stabilizer output; pin STABI							
$V_{O(STABI)}$	output voltage on pin STABI	Mute and Operating modes; with respect to VSSP1		9.3	9.8	10.3	V
Temperature protection							
$T_{act(th_prot)}$	thermal protection activation temperature			-	154	-	°C
$T_{act(th_fold)}$	thermal foldback activation temperature	closed loop SE voltage gain reduced with 6 dB	[5]	-	153	-	°C

[1] The circuit is DC adjusted at V_P = ±12.5 V to ±32.5 V.

[2] With respect to SGND (0 V).

[3] The transition between Standby and Mute mode has hysteresis, while the slope of the transition between Mute and Operating mode is determined by the time-constant of the RC network on pin MODE; see Figure 8.

[4] DC output offset voltage is gradually applied to the output during the transition between the Mute and Operating modes. The slope caused by any DC output offset is determined by the time-constant of the RC network on pin MODE.

[5] At a junction temperature of approximately $T_{act(th_fold)}$ − 5 °C, gain reduction commences and at a junction temperature of approximately $T_{act(th_prot)}$, the amplifier switches off.

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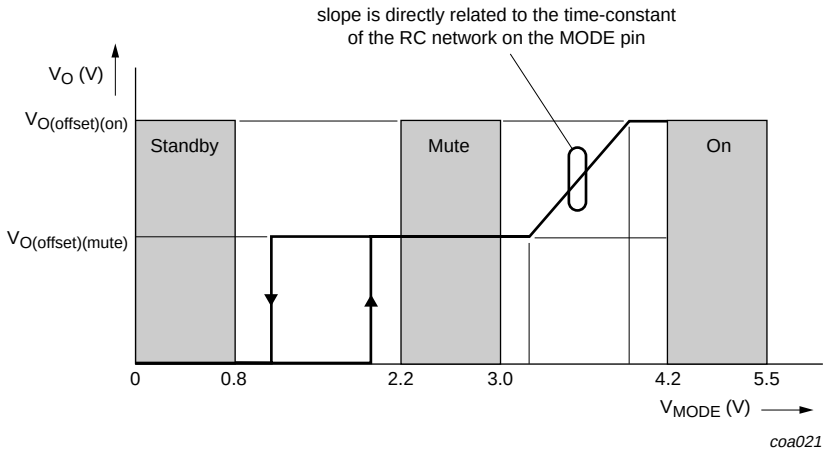

Fig 8. Behavior of mode selection pin MODE

12. Dynamic characteristics

12.1 Switching characteristics

Table 8. Dynamic characteristics

V_P = ±30 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Internal oscillator						
$f_{osc(typ)}$	typical oscillator frequency	R_{OSC} = 30.0 kΩ	325	345	365	kHz
f_{osc}	oscillator frequency		250	-	450	kHz
External oscillator or frequency tracking						
V_{OSC}	voltage on pin OSC		SGND + 4.5	SGND + 5	SGND + 6	V
$V_{trip(OSC)}$	trip voltage on pin OSC		-	SGND + 2.5	-	V
f_{track}	tracking frequency	[1]	250	-	450	kHz

[1] When using an external oscillator, the frequency $f_{osc(ext)}$ (500 kHz minimum, 900 kHz maximum) will result in a PWM frequency f_{track} (250 kHz minimum, 450 kHz maximum) due to the internal clock divider; see Section 8.2.

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12.2 Stereo and dual SE application characteristics

Table 9. Dynamic characteristics

V_P = ±30 V; R_L = 4 Ω; f_i = 1 kHz; f_{osc} = 345 kHz; R_{sL} < 0.1 Ω[1]; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
P_o	output power	L = 22 µH; C = 680 nF; T_j = 85 °C	[2]				
		THD = 0.5 %; R_L = 4 Ω		-	90	-	W
		THD = 10 %; R_L = 4 Ω		-	110	-	W
		THD = 10 %; V_P = ±27 V		-	80	-	W
THD	total harmonic distortion	P_o = 1 W; f_i = 1 kHz	[3]	-	0.05	-	%
		P_o = 1 W; f_i = 6 kHz	[3]	-	0.05	-	%
$G_{v(cl)}$	closed-loop voltage gain			29	30	31	dB
SVRR	supply voltage ripple rejection	between pin VDDPn and SGND					
		Operating mode; f_i = 100 Hz	[4]	-	90	-	dB
		Operating mode; f_i = 1 kHz	[4]	-	70	-	dB
		Mute mode; f_i = 100 Hz	[4]	-	75	-	dB
		Standby mode; f_i = 100 Hz	[4]	-	120	-	dB
		between pin VSSPn and SGND					
		Operating mode; f_i = 100 Hz	[4]	-	80	-	dB
		Operating mode; f_i = 1 kHz	[4]	-	60	-	dB
		Mute mode; f_i = 100 Hz	[4]	-	80	-	dB
		Standby mode; f_i = 100 Hz	[4]	-	115	-	dB
Z_i	input impedance	between the input pins and SGND		45	63	-	kΩ
$V_{n(o)}$	output noise voltage	Operating mode; R_s = 0 Ω	[5]	-	160	-	µV
		Mute mode	[6]	-	85	-	µV
α_{cs}	channel separation		[7]	-	70	-	dB
$\lvert\Delta G_v\rvert$	voltage gain difference			-	-	1	dB
α_{mute}	mute attenuation	f_i = 1 kHz; V_i = 2 V (RMS)	[8]	-	75	-	dB
CMRR	common mode rejection ratio	$V_{i(CM)}$ = 1 V (RMS)		-	75	-	dB
η_{po}	output power efficiency	SE, R_L = 4 Ω		-	88	-	%
		SE, R_L = 6 Ω		-	90	-	%
		BTL, R_L = 8 Ω		-	88	-	%
$R_{DSon(hs)}$	high-side drain-source on-state resistance		[9]	-	200	-	mΩ
$R_{DSon(ls)}$	low-side drain-source on-state resistance		[9]	-	190	-	mΩ

[1] R_{sL} is the series resistance of low-pass LC filter inductor in the application.

[2] Output power is measured indirectly; based on R_{DSon} measurement; see Section 13.3.

[3] THD is measured from 22 Hz to 20 kHz, using AES17 20 kHz brickwall filter. Maximum limit is guaranteed but may not be 100 % tested.

[4] V_{ripple} = $V_{ripple(max)}$ = 2 V (p-p); R_s = 0 Ω. Measured independently between VDDPn and SGND and between VSSPn and SGND.

[5] 22 Hz to 20 kHz, using AES17 20 kHz brickwall filter.

[6] 22 Hz to 22 kHz, using AES17 20 kHz brickwall filter; independent of R_s.

[7] P_o = 1 W; R_s = 0 Ω; f_i = 1 kHz.

[8] V_i = $V_{i(max)}$ = 1 V (RMS); f_i = 1 kHz.

[9] Leads and bond wires included.

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12.3 Mono BTL application characteristics

Table 10. Dynamic characteristics

V_P = ±30 V; R_L = 8 Ω; f_i = 1 kHz; f_{osc} = 345 kHz; R_{sL} < 0.1 Ω [1]; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
P_o	output power	L = 22 µH; C = 680 nF; T_j = 85 °C	[2]				
		THD = 0.5 %; R_L = 8 Ω		-	170	-	W
		THD = 10 %; R_L = 8 Ω		-	210	-	W
THD	total harmonic distortion	P_o = 1 W; f_i = 1 kHz	[3]	-	0.05	-	%
		P_o = 1 W; f_i = 6 kHz	[3]	-	0.05	-	%
$G_{v(cl)}$	closed-loop voltage gain			-	36	-	dB
SVRR	supply voltage ripple rejection	between pin VDDPn and SGND					
		Operating mode; f_i = 100 Hz	[4]	-	80	-	dB
		Operating mode; f_i = 1 kHz	[4]	-	80	-	dB
		Mute mode; f_i = 100 Hz	[4]	-	95	-	dB
		Standby mode; f_i = 100 Hz	[4]	-	120	-	dB
		between pin VSSPn and SGND					
		Operating mode; f_i = 100 Hz	[4]	-	75	-	dB
		Operating mode; f_i = 1 kHz	[4]	-	75	-	dB
		Mute mode; f_i = 100 Hz	[4]	-	90	-	dB
		Standby mode; f_i = 100 Hz	[4]	-	130	-	dB
Z_i	input impedance	measured between the input pins and SGND		45	63	-	kΩ
$V_{n(o)}$	output noise voltage	Operating mode; R_s = 0 Ω	[5]	-	190	-	µV
		Mute mode	[6]	-	45	-	µV
α_{mute}	mute attenuation	f_i = 1 kHz; V_i = 2 V (RMS)	[7]	-	75	-	dB
CMRR	common mode rejection ratio	$V_{i(CM)}$ = 1 V (RMS)		-	75	-	dB

[1] R_{sL} is the series resistance of low-pass LC filter inductor in the application.

[2] Output power is measured indirectly; based on R_{DSon} measurement; see Section 13.3.

[3] Total harmonic distortion is measured from 22 Hz to 20 kHz, using an AES17 20 kHz brickwall filter. Maximum limit is guaranteed but may not be 100 % tested.

[4] V_{ripple} = $V_{ripple(max)}$ = 2 V (p-p); R_s = 0 Ω.

[5] 22 Hz to 20 kHz, using an AES17 20 kHz brickwall filter; low noise due to BD modulation.

[6] 22 Hz to 20 kHz, using an AES17 20 kHz brickwall filter; independent of R_s.

[7] V_i = $V_{i(max)}$ = 1 V (RMS); f_i = 1 kHz.

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13. Application information

13.1 Mono BTL application

When using the power amplifier in a mono BTL application, the inputs of both channels must be connected in parallel and the phase of one of the inputs must be inverted; see Figure 7. In principle, the loudspeaker can be connected between the outputs of the two single-ended demodulation filters.

13.2 Pin MODE

To ensure a pop noise-free start-up, an RC time-constant must be applied to pin MODE. The bias-current setting of the VI-converter input is directly related to the voltage on pin MODE. In turn the bias-current setting of the VI-converters is directly related to the DC output offset voltage. A slow dV/dt on pin MODE results in a slow dV/dt for the DC output offset voltage, ensuring a pop noise-free start-up. A time-constant of 500 ms is sufficient to guarantee pop noise-free start-up; see Figure 4, Figure 5 and Figure 8 for more information.

13.3 Output power estimation

13.3.1 SE

Maximum output power:

$$P_{o(0.5\%)} = \frac{\left[\frac{R_L}{R_L + R_{DSon(hs)} + R_{sL}} \times V_P \times (1 - t_{min} \times 0.5 f_{osc})\right]^2}{2R_L} \quad (1)$$

Maximum output current internally limited to 9.2 A:

$$I_{o(peak)} = \frac{V_P \times (1 - t_{min} \times 0.5 f_{osc})}{R_L + R_{DSon(hs)} + R_{sL}} \quad (2)$$

Where:

- R_L: load impedance
- R_{sL}: series impedance of the filter coil
- $R_{DSon(hs)}$: high-side R_{DSon} of power stage output DMOS (temperature dependent)
- f_{osc}: oscillator frequency
- t_{min}: minimum pulse width (typical 150 ns, temperature dependent)
- V_P: single-sided supply voltage or $0.5 \times (V_{DD} + |V_{SS}|)$
- $P_{o(0.5\ \%)}$: output power at the onset of clipping

Remark: Note that $I_{o(peak)}$ should be below 9.2 A (Section 8.3.2). $I_{o(peak)}$ is the sum of the current through the load and the ripple current. The value of the ripple current is dependent on the coil inductance and voltage drop over the coil.

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13.3.2 Bridge-Tied Load (BTL)

Maximum output power:

$$P_{o(0.5\%)} = \frac{\left[\frac{R_L}{R_L + R_{DSon(hs)} + R_{DSon(ls)}} \times 2V_P \times (1 - t_{min} \times 0.5 f_{osc})\right]^2}{2R_L} \quad (3)$$

Maximum output current internally limited to 9.2 A:

$$I_{o(peak)} = \frac{2V_P \times (1 - t_{min} \times 0.5 f_{osc})}{R_L + (R_{DSon(hs)} + R_{DSon(ls)}) + 2R_{sL}} \quad (4)$$

Where:

- R_L: load impedance
- R_{sL}: series impedance of the filter coil
- $R_{DSon(hs)}$: high-side R_{DSon} of power stage output DMOS (temperature dependent)
- $R_{DSon(ls)}$: low-side R_{DSson} of power stage output DMOS (temperature dependent)
- f_{osc}: oscillator frequency
- t_{min}: minimum pulse width (typical 150 ns, temperature dependent)
- V_P: single-sided supply voltage or $0.5 \times (V_{DD} + |V_{SS}|)$
- $P_{o(0.5\ \%)}$: output power at the onset of clipping

Remark: Note that $I_{o(peak)}$ should be below 9.2 A; see Section 8.3.2. $I_{o(peak)}$ is the sum of the current through the load and the ripple current. The value of the ripple current is dependent on the coil inductance and voltage drop over the coil.

13.4 External clock

To ensure duty cycle independent operation of the device, the external clock input frequency is internally divided by two. This implies that the external clock frequency is twice the internal clock frequency (typically 2 × 345 kHz = 690 kHz).

If several class-D amplifiers are used together it is recommended that all devices run at the same switching frequency. This can be achieved by connecting all OSC pins together and feeding them from an external oscillator. When applying an external oscillator it is necessary to force pin OSC to a DC level above SGND. This disables the internal oscillator and causes the PWM to switch at half the external clock frequency.

The internal oscillator requires an external resistor R_{OSC} and capacitor C_{OSC} connected between pin OSC and pin VSSA.

The noise contribution of the internal oscillator is supply voltage dependent. An external low-noise oscillator is recommended for low-noise applications running at high supply voltages.

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13.5 Noise

Noise should be measured using a high-order low-pass filter with a cut-off frequency of 20 kHz. The standard audio band-pass filters used in audio analyzers, do not suppress the residue of the carrier frequency sufficiently to ensure a reliable measurement of the audible noise. Noise measurements should be carried out preferably using AES17 ('brickwall') filters or an audio precision AUX 0025 filter (designed specifically for measuring class-D switching amplifiers).

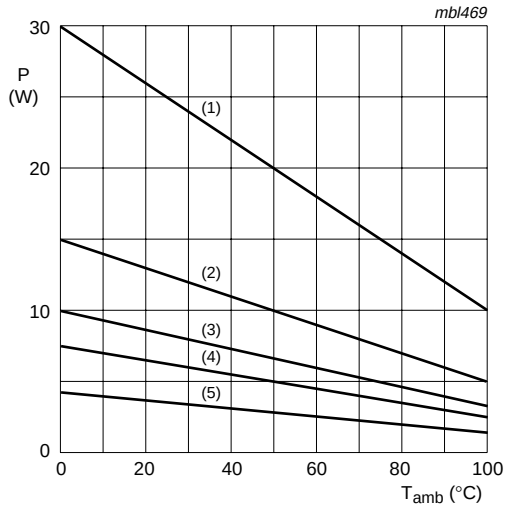
13.6 Heatsink requirements

In many applications it may be necessary to connect an external heatsink to the TDA8920C.

Equation 5 shows the relationship between the maximum power dissipation before activation of TFB and the total thermal resistance from junction to ambient.

$$R_{th(j-a)} = \frac{T_j - T_{amb}}{P} \quad (5)$$

Power dissipation (P) is determined by the efficiency of the TDA8920C. The efficiency measured as a function of output power is given in Figure 21. Power dissipation can be derived as a function of output power as shown in Figure 20.



(1) $R_{th(j-a)}$ = 5 K/W.
(2) $R_{th(j-a)}$ = 10 K/W.
(3) $R_{th(j-a)}$ = 15 K/W.
(4) $R_{th(j-a)}$ = 20 K/W.
(5) $R_{th(j-a)}$ = 35 K/W.

Fig 9. Derating curves for power dissipation as a function of maximum ambient temperature

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In the following example, a heatsink calculation is made for an 8 Ω BTL application with a ±30 V supply:

The audio signal has a crest factor of 10 (the ratio between peak power and average power (20 dB)), this means that the average output power is $\frac{1}{10}$ of the peak power.

Thus, the peak RMS output power level is the 0.5 % THD level, i.e. 170 W.

The average power is then $\frac{1}{10} \times 130$ W = 17 W.

The dissipated power at an output power of 17 W is approximately 5 W.

When the maximum expected ambient temperature is 85 °C, the total $R_{th(j-a)}$ becomes

$$\frac{(140-85)}{5} = 11 \text{ K/W}$$

$R_{th(j-a)} = R_{th(j-c)} + R_{th(c-h)} + R_{th(h-a)}$

$R_{th(j-c)}$ (thermal resistance from junction to case) = 1.1 K/W

$R_{th(c-h)}$ (thermal resistance from case to heatsink) = 0.5 K/W to 1 K/W (dependent on mounting)

Based on this the thermal resistance between heatsink and ambient temperature is:

$R_{th(h-a)}$ (thermal resistance from heatsink to ambient) = 11 – (1.1 + 1) = 8.9 K/W

The derating curves for power dissipation (for several $R_{th(j-a)}$ values) are illustrated in Figure 9. A maximum junction temperature T_j = 150 °C is taken into account. The maximum allowable power dissipation for a given heatsink size can be derived or the required heatsink size can be determined at a required power dissipation level; see Figure 9.

13.7 Output current limiting

To guarantee the robustness of the TDA8920C, the maximum output current that can be delivered by the output stage is limited to 9.2 A. OverCurrent Protection (OCP) is built in for each output power switch.

If the current flowing through any of the power switches exceeds the 9.2 A threshold current due to, for example, a short-circuit to a supply line or across the load, the maximum output current of the amplifier is regulated to 9.2 A.

The TDA8920C amplifier distinguishes between low-ohmic short-circuit conditions and other overcurrent conditions such as dynamic impedance drops of the loudspeakers used. The impedance threshold (Z_{th}) depends on the supply voltage used.

Depending on the impedance of the short-circuit, the amplifier reacts as follows:

- Short-circuit impedance (> Z_{th}): The maximum output current of the amplifier is regulated to 9.2 A but the amplifier will not shut down the PWM outputs. Effectively this results in a clipped output signal across the load (behavior very similar to voltage clipping).
- Short-circuit impedance (< Z_{th}): The amplifier limits the maximum output current to 9.2 A and at the same time discharges the capacitor on pin PROT. When the voltage across this capacitor drops below the threshold voltage, the amplifier shuts down completely and an internal timer is started.

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A typical value for the capacitor connected to pin PROT can be from 10 pF to 220 pF; see Figure 10. After a fixed time of 100 ms the amplifier switches on. If the requested output current is still too high, the amplifier switches off. Thus the amplifier tries to switch to the Operating mode every 100 ms. The average power dissipation will be low in this situation because of the low duty cycle.

If the overcurrent condition is removed, the amplifier stays in Operating mode after restarting. This fully protects the TDA8920C amplifier against short-circuit conditions while at the same time eliminating so-called audio holes resulting from loudspeaker impedance drops.

Table 11. Current limiting behavior during low output impedance conditions at different values of C_{PROT}

Type	V_P (V)	V_I (mV, p-p)	f (Hz)	C_{PROT} (pF)	PWM output stops		
					Short (0 Ω)	Short (0.5 Ω)	Short (1 Ω)
TDA8920CJ/N1	29.5	500	20	10	yes	yes	OVP[1]
			1000	10	yes	yes	no
			20	15	yes	yes	OVP[1]
			1000	15	yes	no	no
			1000	220	no	no	no

[1] Overvoltage protection activation caused by supply pumping due to the weak short-circuit; see Section 13.8.

13.8 Pumping effects

In a typical stereo half-bridge SE application the TDA8920C is supplied by a symmetrical voltage (e.g. V_{DD} = 30 V and V_{SS} = −30 V). When the amplifier is used in an SE configuration, a 'pumping effect' can occur. During one switching interval, energy is taken from one supply (e.g. V_{DD}), while a part of that energy is returned to the other supply line (e.g. V_{SS}) and vice versa. When the voltage supply source cannot sink energy, the voltage across the output capacitors of that voltage supply source increases and the supply voltage is pumped to higher levels. The voltage increase caused by the pumping effect depends on:

- Speaker impedance
- Supply voltage
- Audio signal frequency
- Value of supply line decoupling capacitors
- Source and sink currents of other channels

In applications using the TDA8920C ensure pumping effects are minimized and prevent malfunctions of either the audio amplifier and/or the voltage supply source. Amplifier malfunction due to the pumping effect can trigger UVP, OVP or UBP.

The most effective solution against pumping effects is to use the TDA8920C in a mono full-bridge application. In the case of stereo half-bridge applications, adapt the power supply, for example, by increasing the values of the supply decoupling capacitors.

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13.9 Application schematics

Notes for the application schematic:

- Connect a solid ground plane to V_{SS} around the switching amplifier to prevent emission
- Place 100 nF capacitors as close as possible to the TDA8920C power supply pins
- Internally connect the internal heat spreader of the TDA8920C to V_{SS}
- Connect the external heatsink to the ground plane
- Use a thermally conductive, electrically non-conductive, Sil-Pad between the backside of the TDA8920C and a small external heatsink
- Use differential inputs for the most effective system level audio performance with unbalanced signal sources. In case of hum due to floating inputs, connect the shielding or source ground to the amplifier ground. Jumpers J1 and J2 are open on set level and closed on the stand-alone demo board
- Minimum total required capacitance for each power supply line is 3300 μF

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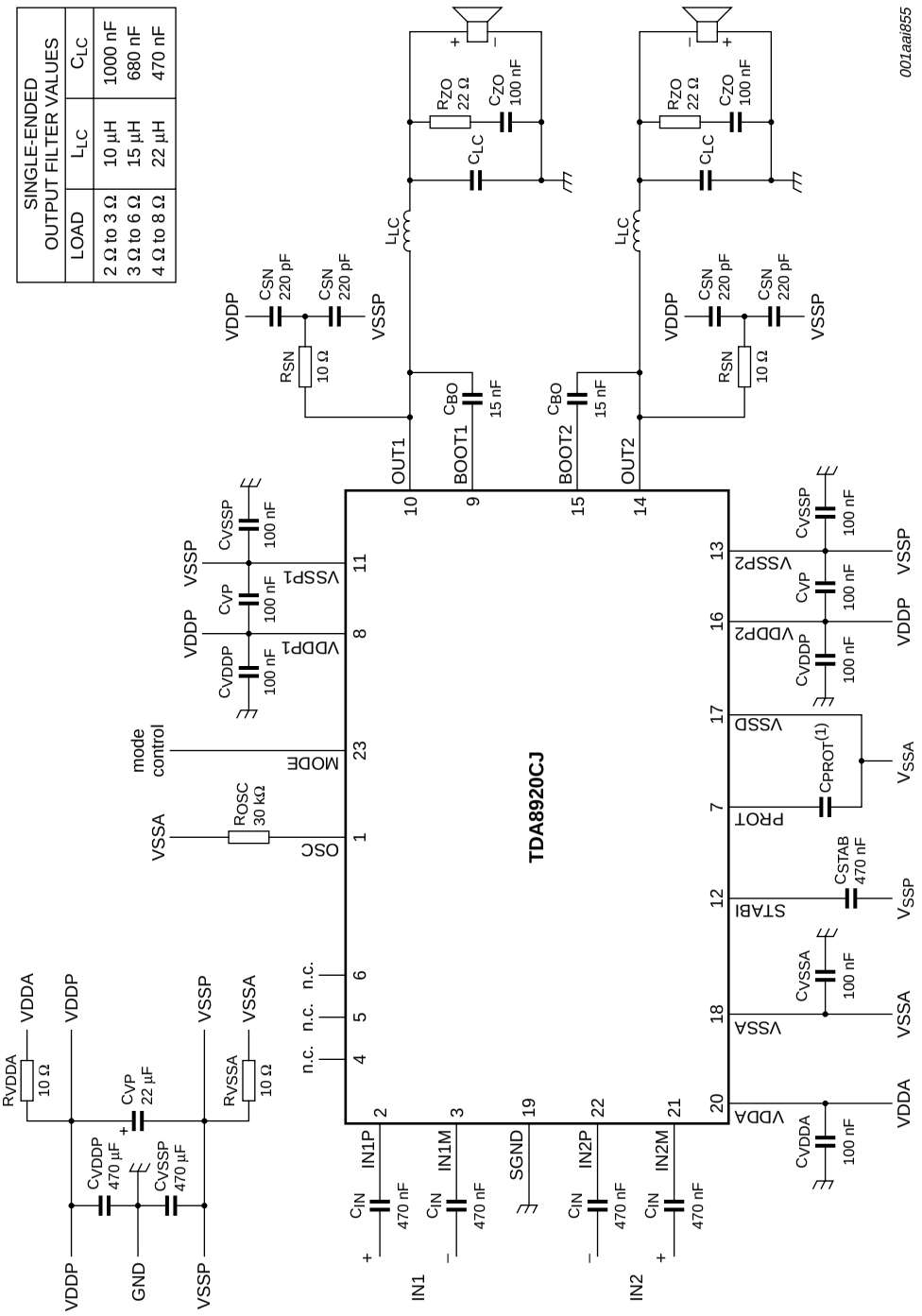

(1) Value of C_{PROT} can be in the range 10 pF to 220 pF.

Fig 10. Typical application diagram for pop noise-free start up and switch off

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13.10 Layout and grounding

To obtain a high-level system performance, certain grounding techniques are essential. The input reference grounds have to be tied to their respective source grounds and must have separate tracks from the power ground tracks. This prevents the large (output) signal currents from interfering with the small AC input signals. The small-signal ground tracks should be physically located as far as possible from the power ground tracks. Supply and output tracks should be as wide as possible to deliver maximum output power.

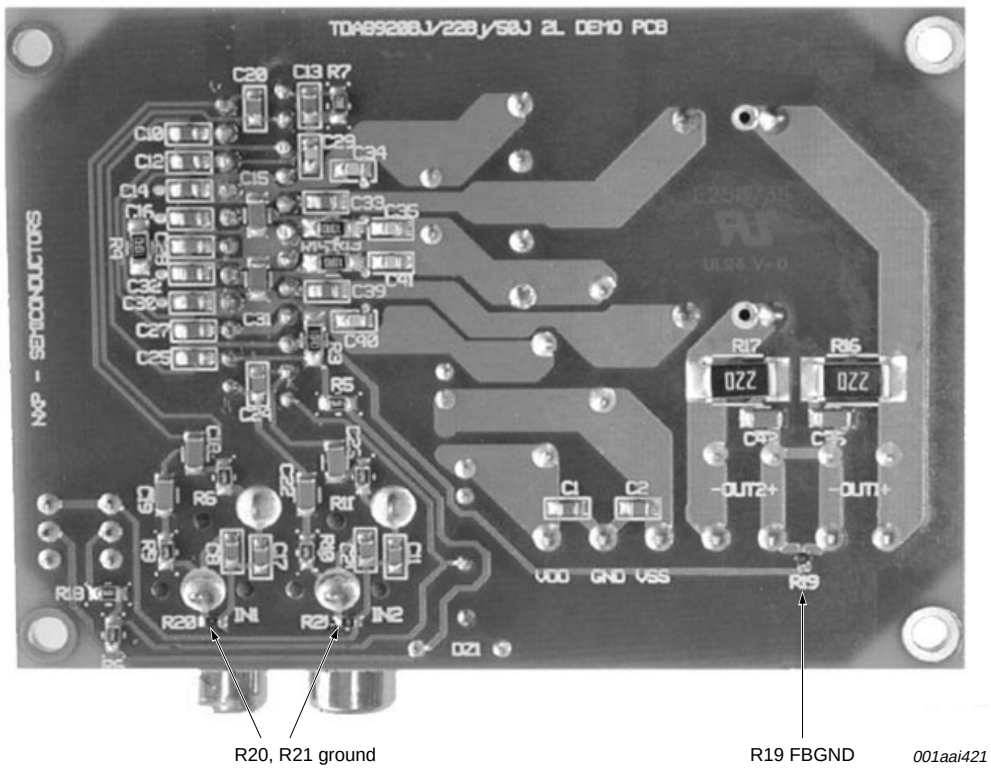

Fig 11. Printed-circuit board layout (quasi-single-sided); component view

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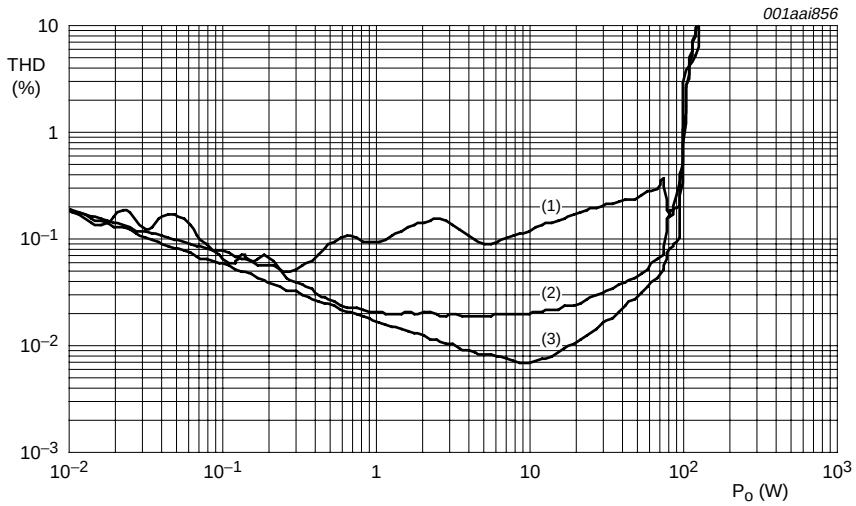
13.11 Curves measured in reference design



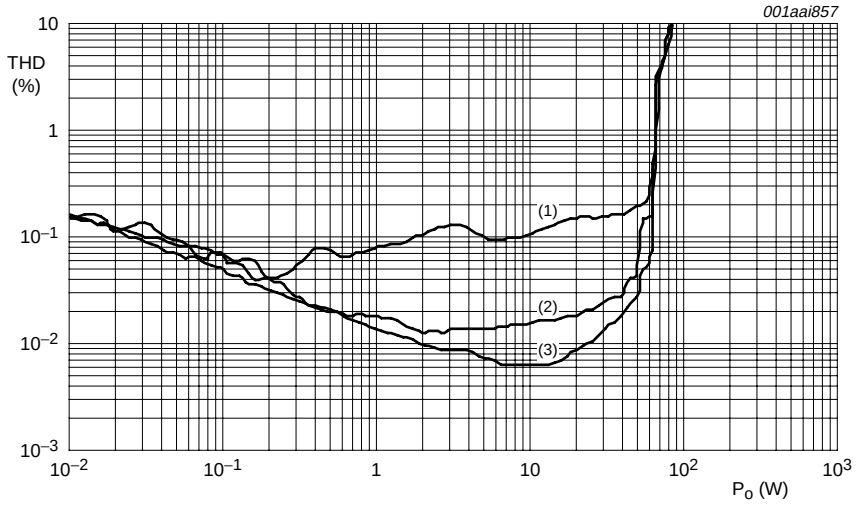
V_P = ±30 V, f_{osc} = 350 kHz, 2 × 4 Ω SE configuration.

(1) OUT2, f_i = 6 kHz.

(2) OUT2, f_i = 1 kHz.

(3) OUT2, f_i = 100 Hz.

Fig 12. THD as a function of output power, SE configuration with 2 × 4 Ω load



V_P = ±30 V, f_{osc} = 350 kHz, 2 × 6 Ω SE configuration.

(1) OUT2, f_i = 6 kHz.

(2) OUT2, f_i = 1 kHz.

(3) OUT2, f_i = 100 Hz.

Fig 13. THD as a function of output power, SE configuration with 2 × 6 Ω load

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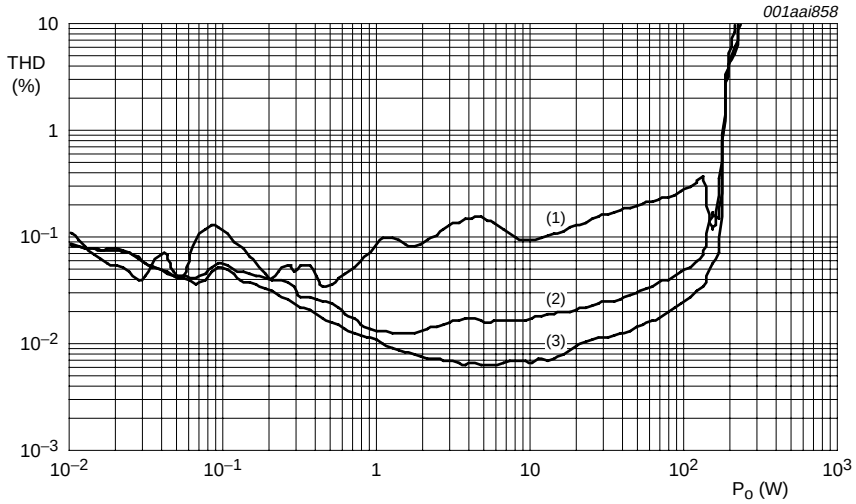


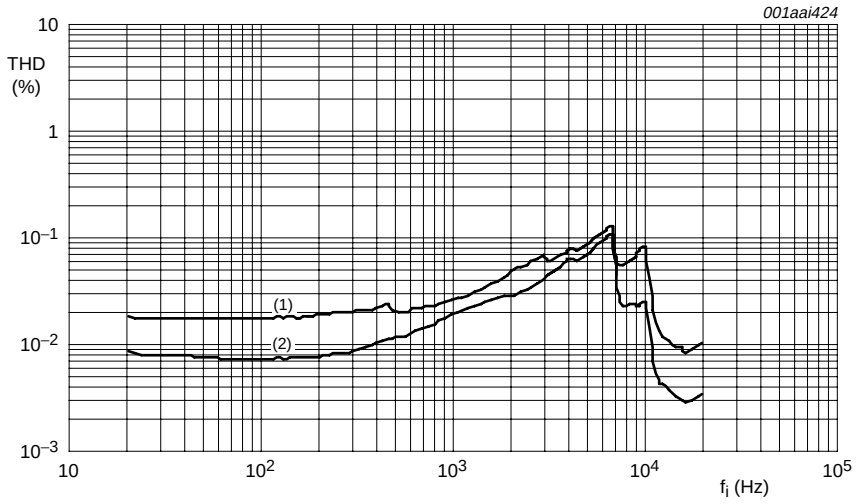
V_P = ±30 V, f_{osc} = 350 kHz, 1 × 8 Ω BTL configuration.

(1) f_i = 6 kHz.

(2) f_i = 1 kHz.

(3) f_i = 100 Hz.

Fig 14. THD as a function of output power, BTL configuration with 1 × 8 Ω load



V_P = ±30 V, f_{osc} = 350 kHz, 2 × 4 Ω SE configuration.

(1) OUT2, P_o = 1 W.

(2) OUT2, P_o = 10 W.

Fig 15. THD as a function of frequency, SE configuration with 2 × 4 Ω load

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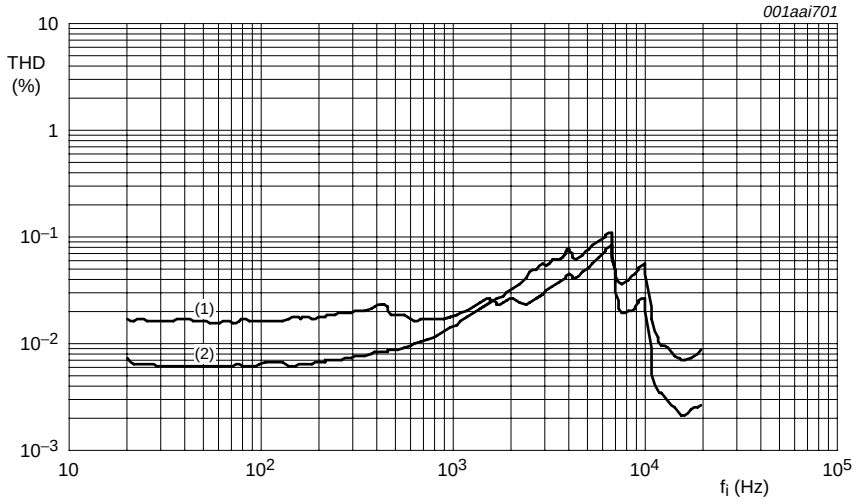
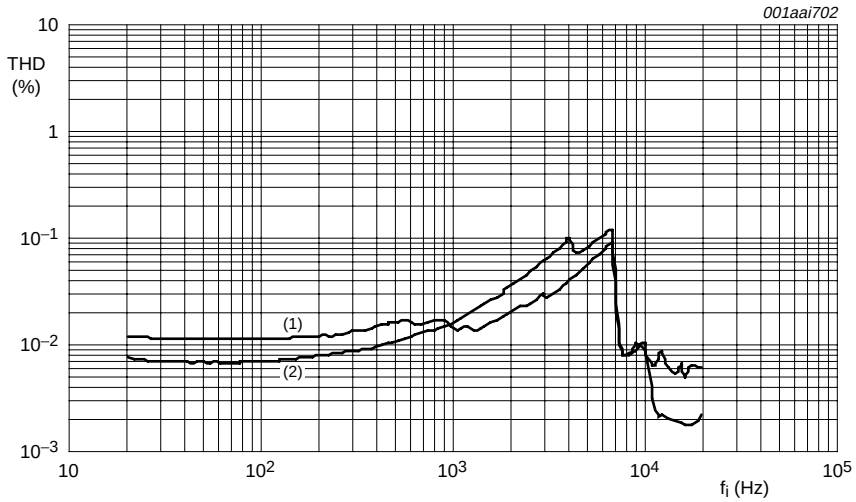


V_P = ±30 V, f_{osc} = 350 kHz, 2 × 6 Ω SE configuration.

(1) OUT2, P_o = 1 W.

(2) OUT2, P_o = 10 W.

Fig 16. THD as a function of frequency, SE configuration with 2 × 6 Ω load



V_P = ±30 V, f_{osc} = 350 kHz, 1 × 8 Ω BTL configuration.

(1) P_o = 1 W.

(2) P_o = 10 W.

Fig 17. THD as a function of frequency, BTL configuration with 1 × 8 Ω load

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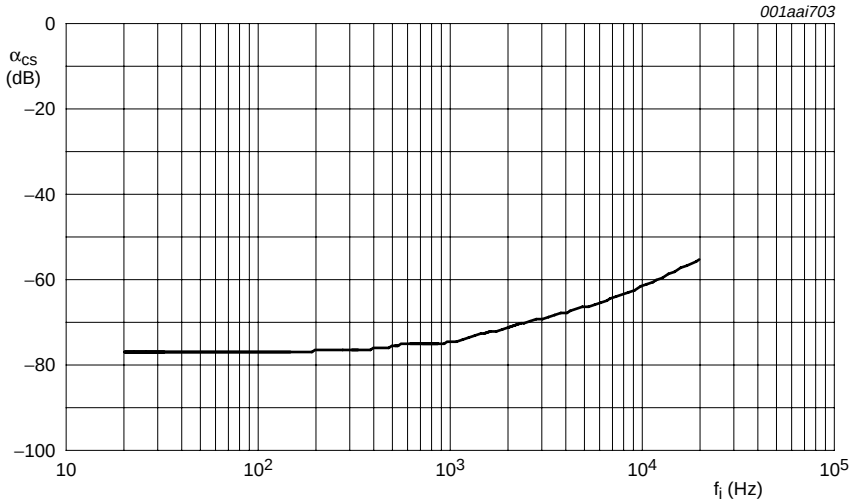
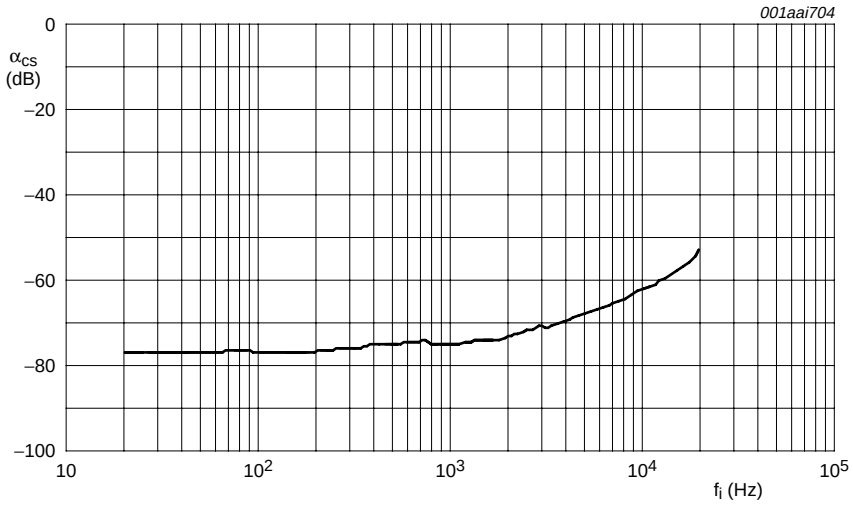


V_P = ±30 V, f_{osc} = 350 kHz, 2 × 4 Ω SE configuration.

OUT1 and OUT2 both 1 W and 10 W respectively.

Fig 18. Channel separation as a function of frequency, SE configuration with 2 × 4 Ω load



V_P = ±30 V, f_{osc} = 350 kHz, 2 × 6 Ω SE configuration.

OUT1 and OUT2 both 1 W and 10 W respectively.

Fig 19. Channel separation as a function of frequency, SE configuration with 2 × 6 Ω load

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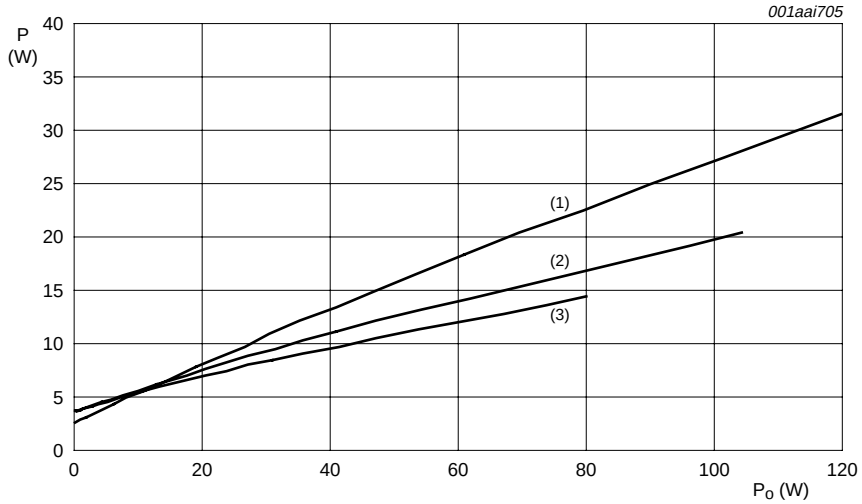


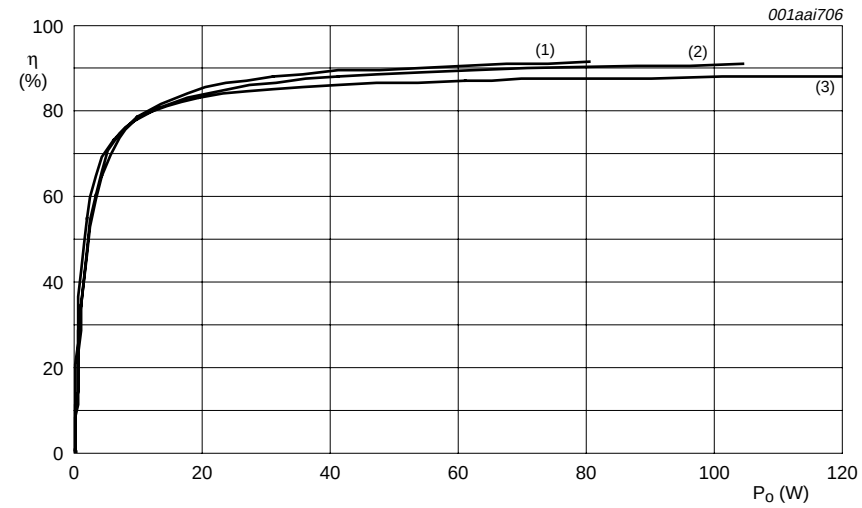
V_P = ±31.5 V, f_i = 1 kHz, f_{osc} = 325 kHz.

(1) 2 × 4 Ω SE configuration.

(2) 2 × 6 Ω SE configuration.

(3) 2 × 8 Ω SE configuration.

Fig 20. Power dissipation as a function of output power per channel, SE configuration



V_P = ±30 V, f_i = 1 kHz, f_{osc} = 325 kHz.

(1) 2 × 8 Ω SE configuration.

(2) 2 × 6 Ω SE configuration.

(3) 2 × 4 Ω SE configuration.

Fig 21. Efficiency as a function of output power per channel, SE configuration

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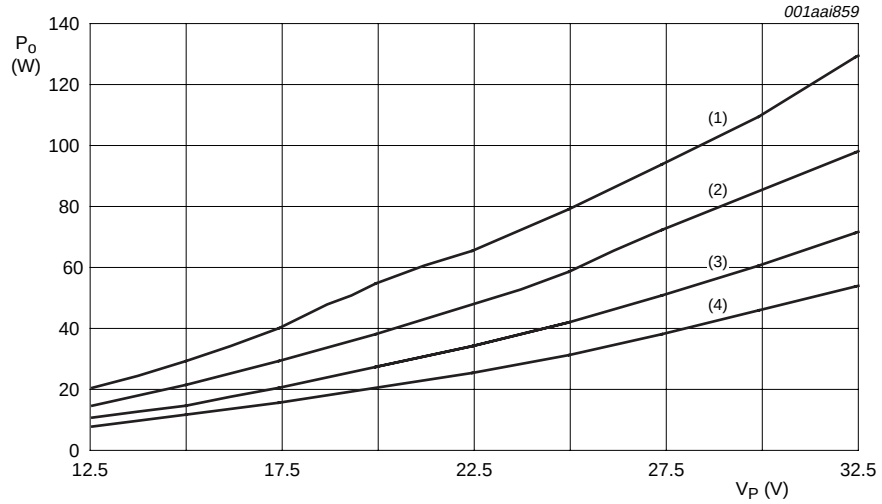


Infinite heat sink used.

f_i = 1 kHz, f_{osc} = 325 kHz.

(1) THD = 10 %, 4 Ω.

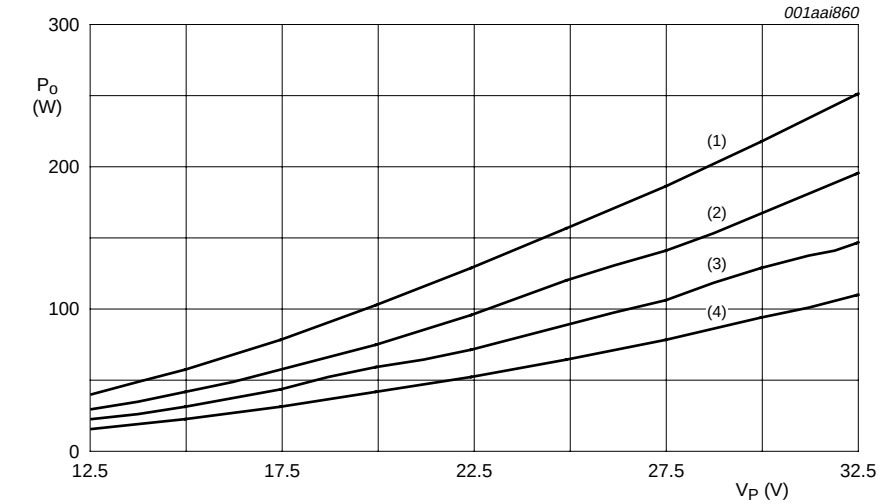
(2) THD = 0.5 %, 4 Ω; THD = 10 %, 6 Ω.

(3) THD = 10 %, 8 Ω.

(4) THD = 0.5 %, 6 Ω.

(5) THD = 0.5 %, 8 Ω.

Fig 22. Output power as a function of supply voltage, SE configuration



Infinite heat sink used.

f_i = 1 kHz, f_{osc} = 325 kHz.

(1) THD = 10 %, 8 Ω.

(2) THD = 0.5 %, 8 Ω.

(3) THD = 10 %, 16 Ω.

(4) THD = 0.5 %, 16 Ω.

Fig 23. Output power as a function of supply voltage, BTL configuration

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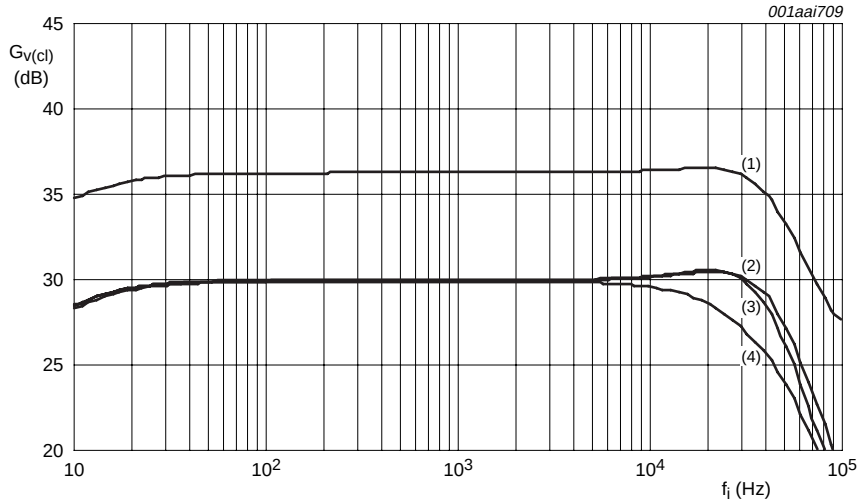


V_P = ±30 V, f_{osc} = 350 kHz, V_i = 100 mV, R_S = 0 Ω, C_i = 330 pF.

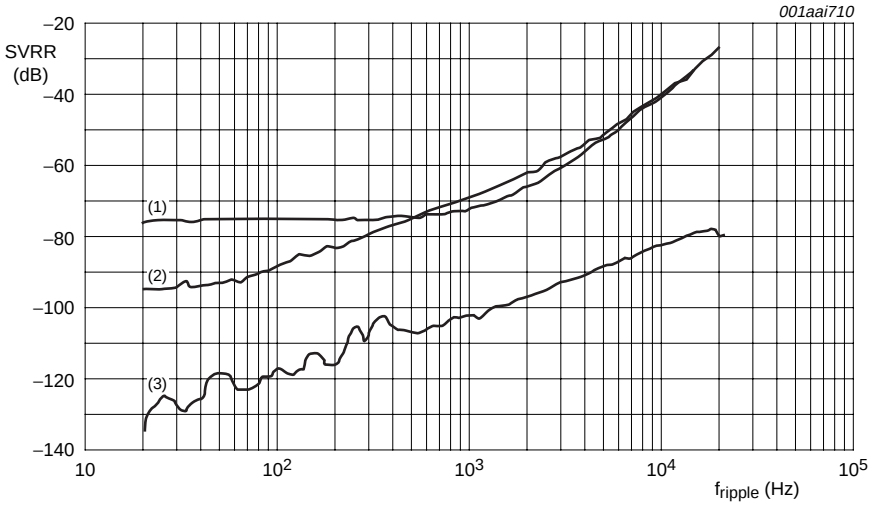
(1) 1 × 8 Ω BTL configuration.

(2) 2 × 4 Ω SE configuration.

(3) 2 × 6 Ω SE configuration.

(4) 2 × 8 Ω SE configuration.

Fig 24. Closed-loop voltage gain as a function of frequency, R_s = 0 Ω, C_i = 330 pF



Ripple on V_{DD}, short on input pins.

V_P = ±30 V, f_{osc} = 350 kHz, R_L = 4 Ω, V_{ripple} = 2 V (p-p).

(1) OUT2, Mute mode.

(2) OUT2, Operating mode.

(3) OUT2, Standby mode.

Fig 25. SVRR as a function of ripple frequency, ripple on V_{DD}

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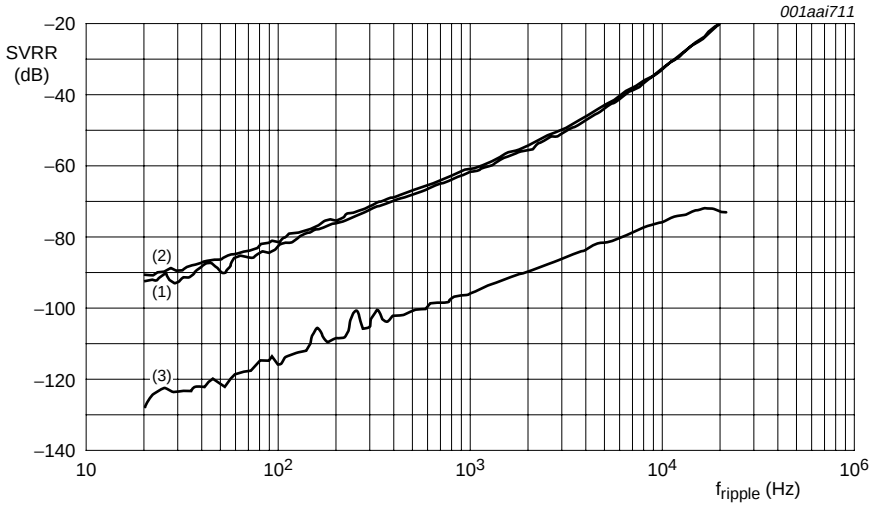


Ripple on V_{SS}, short on input pins.

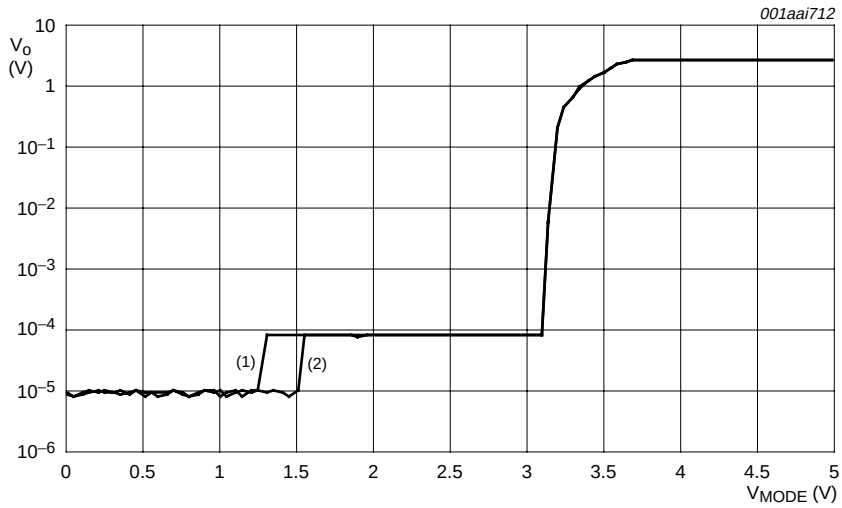
V_P = ±30 V, f_{osc} = 350 kHz, R_L = 4 Ω, V_{ripple} = 2 V (p-p).

(1) OUT2, Mute mode.

(2) OUT2, Operating mode.

(3) OUT2, Standby mode.

Fig 26. SVRR as a function of ripple frequency, ripple on V_{SS}



V_P = ±30 V, f_{osc} = 325 kHz.

(1) OUT1, down.

(2) OUT1, up.

Fig 27. Output voltage as a function of mode voltage

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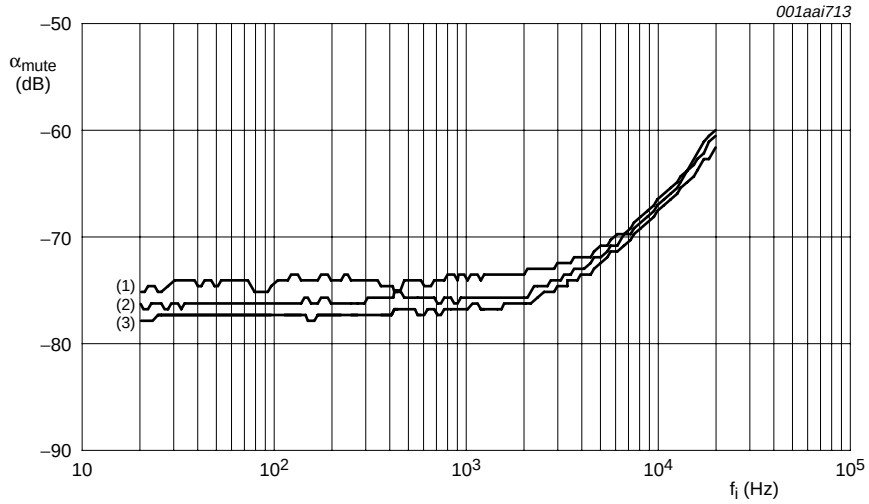

V_P = ±30 V, f_{osc} = 325 kHz, V_i = 2 V (RMS).

(1) OUT2, 8 Ω.

(2) OUT2, 6 Ω.

(3) OUT2, 0 Ω.

Fig 28. Mute attenuation as a function of frequency

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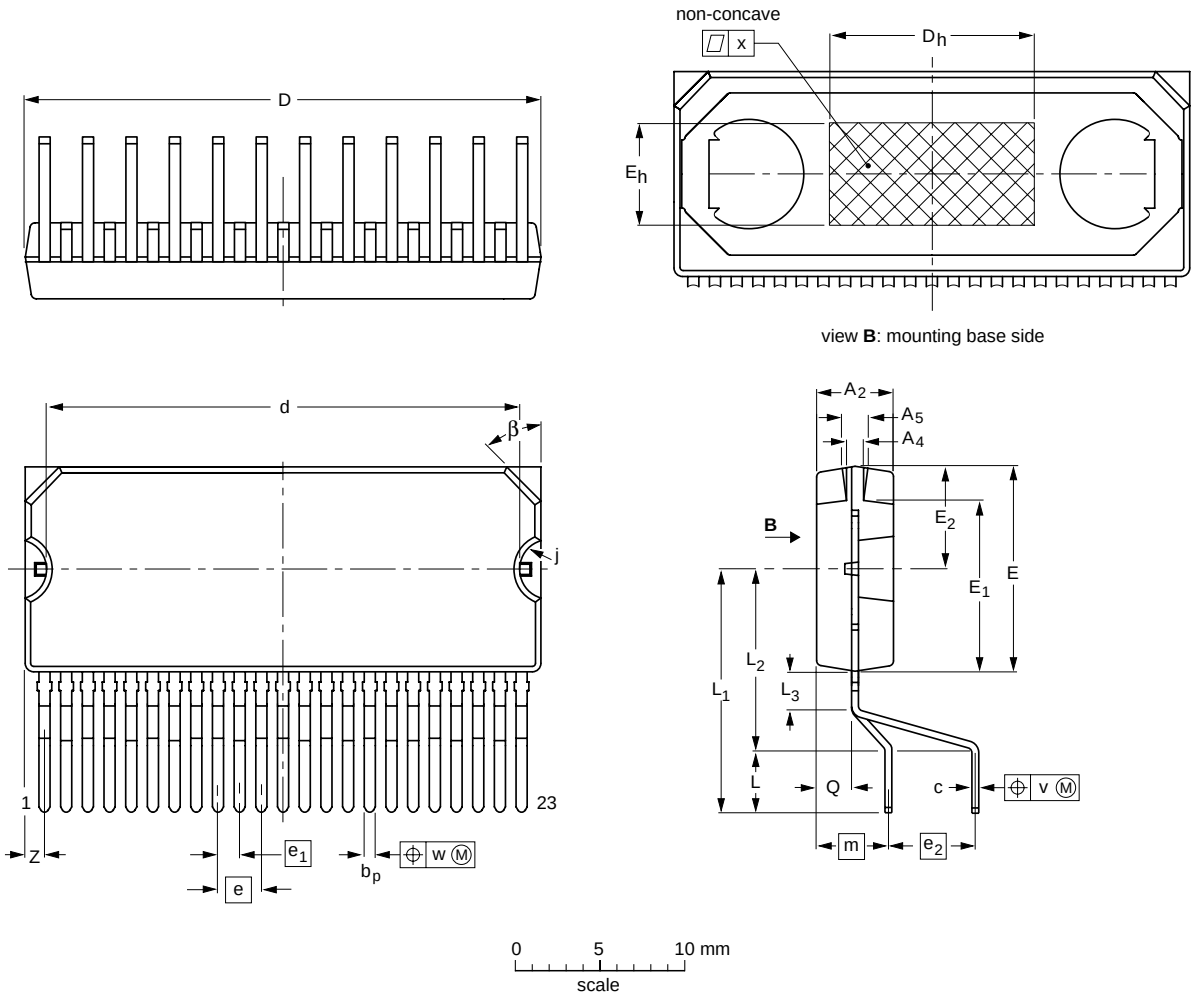
14. Package outline

DBS23P: plastic DIL-bent-SIL power package; 23 leads (straight lead length 3.2 mm) **SOT411-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A_2	A_4	A_5	b_p	c	$D^{(1)}$	d	D_h	$E^{(1)}$	e	e_1	e_2	E_h	E_1	E_2	j	L	L_1	L_2	L_3	m	Q	v	w	x	β	$Z^{(1)}$
mm	4.6 4.3	1.15 0.85	1.65 1.35	0.75 0.60	0.55 0.35	30.4 29.9	28.0 27.5	12	12.2 11.8	2.54	1.27	5.08	6	10.15 9.85	6.2 5.8	1.85 1.65	3.6 2.8	14 13	10.7 9.9	2.4 1.6	4.3	2.1 1.8	0.6	0.25	0.03	45°	1.43 0.78

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT411-1						~~98-02-20~~ 02-04-24

Fig 29. Package outline SOT411-1 (DBS23P)

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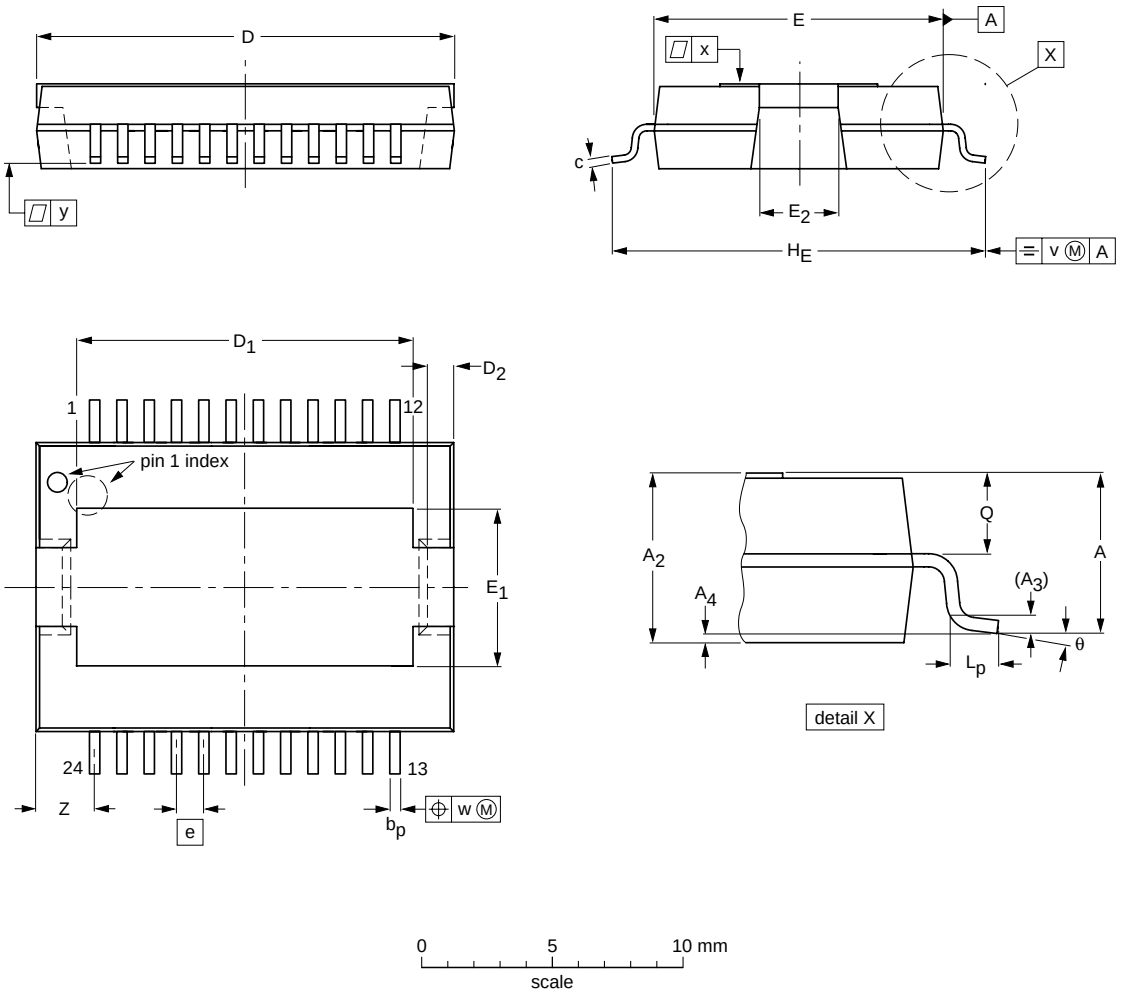
HSOP24: plastic, heatsink small outline package; 24 leads; low stand-off height **SOT566-3**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_2	A_3	A_4(1)	b_p	c	D(2)	D_1	D_2	E(2)	E_1	E_2	e	H_E	L_p	Q	v	w	x	y	Z	θ
mm	3.5	3.5 3.2	0.35	+0.08 –0.04	0.53 0.40	0.32 0.23	16.0 15.8	13.0 12.6	1.1 0.9	11.1 10.9	6.2 5.8	2.9 2.5	1	14.5 13.9	1.1 0.8	1.7 1.5	0.25	0.25	0.03	0.07	2.7 2.2	8° 0°

Notes

1. Limits per individual lead.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT566-3						~~03-02-18~~ 03-07-23

Fig 30. Package outline SOT566-3 (HSOP24)

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15. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

15.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

15.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

15.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

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15.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 31) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 12 and 13

Table 12. SnPb eutectic process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 13. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 31.

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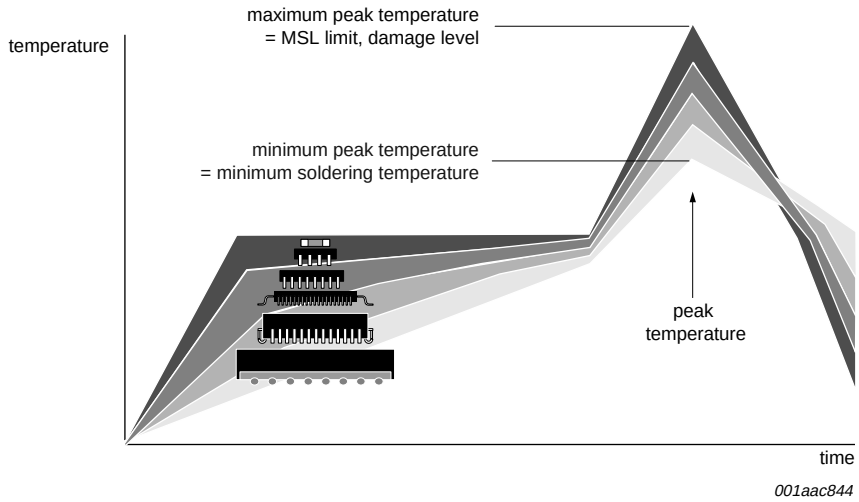

MSL: Moisture Sensitivity Level

Fig 31. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

16. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TDA8920C_1	20080929	Preliminary data sheet	-	-

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17.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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