I²C Buffer Chip



Features

- Dual, bi-directional buffer in 8-pin DIL/SO
- Bus speeds to 400 kHz
- I²C bus compatible
- Wide supply voltage range 2 15 V
- Can handle, or level shift, logic signals in the range 2 15 V
- Releases connected busses if supply fails
- Low power supply current, 1 mA
- Can split I²C into two unidirectional Tx and Rx data signals, or recombine these
- Simple interfacing to opto-couplers to provide safety isolation of the bus
- X10 bus impedance transformation option

Applications

- Building large or distributed I²C bus systems for automation/control
- Transmit I²C signals over twisted pair cabling
- Galvanic/safety (opto) isolation of sections of I²C bus
- · Interface between logic devices or busses on different voltages
- Hot-plugging bus interface protection
- Interfacing SMBus to I²C
- I²C signalling via differential bus hardware
- Prevent bus 'hang-up' by isolating devices or modules if supply fails
- Sending I²C signals over RF links

Ordering Information

Part number	12NC	Packing	Package	Pkg Drawing
P82B96PN	935262297112	Tube	DIP 8	SOT97-1
P82B96TD	935262295112	Tube	SO 8	SOT96-1
P82B96TD-T	935262295118	Reel	SO 8	SOT96-1



Description

The P82B96 is a bipolar IC designed to extend the application possibilities of I^2C and similar derivative bi-directional busses such as SMBus and DDB.

Providing true 'buffer' functionality to enable interconnection of several I²C or similar busses it effectively overcomes the I²C specification limitation of 400 pF max. bus capacitance.

Using analog techniques, 82B96 can also 'split' the special bi-directional bus signals into two conventional uni-directional data streams, allowing their transmission via any desired medium, or re-combine two such data streams to restore the original bi-directional I^2C signal.

Its wide guaranteed operating supply voltage range of $2\,V$ to $15\,V$, and its ability to process or level-shift logic signals anywhere within that range, can achieve big improvements in noise margin.

Ten times increase in sink capability of its buffered outputs (to 30 mA) allows decreased bus pull-ups for better impedance matching over long runs of low cost twisted-pair cabling.

Simple interfacing to low cost opto-couplers allows galvanic isolation of parts of an I^2C system to meet safety requirements for control equipment connected to the mains supply, telephone wiring, or for medical monitoring equipment.

Reliability in distributed bus systems having separate power supplies is enhanced by the 82B96 'bus release' feature that prevents system 'hang-ups' by releasing all connected busses if its supply voltage is removed. Bus disconnection, coupled with its low supply current (1 mA) and 15 V tolerant I/Os, will prove useful in resolving many of the problems inherent in "hot plugging" or "plug and play" bus applications.

The P82B96 is offered as a dual buffer in 8-pin DIL or SO packaging, complementing Philips Semiconductors' existing range of devices for $I^2C/SMBus$ system design.

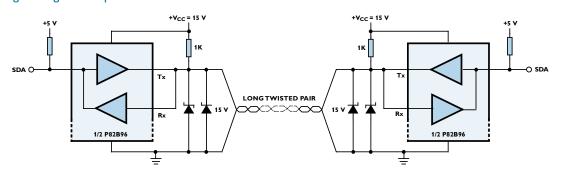


P82B96

I²C Buffer Chip

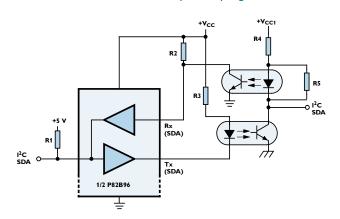


Driving a high voltage low impedance I²C bus



Note: Schottky diode and zener clamps applied to limits spurious signals

Galvanic isolation of I²C nodes via opto-coupling



This example shows the simplicity of a low speed application.

For example:	R1 = usual I ² C pull-up	$R2 = 10 \text{ K}\Omega$
	R3 = 680 Ω	$R4 = 2.2 K\Omega$
	$R5 = 2.2 \text{ K}\Omega$	$V_{CC} = 5 V$
	Vcci = EV	

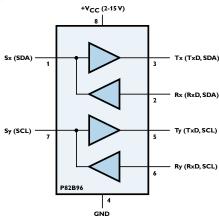


Purchase of Philips I²C components conveys a license under the Philips' patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips.

www.semiconductors.philips.com/logic/i2c



Block Diagram



Philips Semiconductors

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