

Low-Input-Voltage, Low-Power Boost Converter Design Issues

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Abstract—Issues associated with boost converter design and performance are investigated when a low input voltage is used. Low-input-voltage sources include single fuel cells, single solar cells, and thermoelectric devices. The primary context is interfacing single micro fuel cells to portable electronic loads, such as mobile phones. Efficiency and circuit startup are the two most difficult issues for a low-cost design. It is shown in theory and experiment that the boost converter has a voltage collapse point. A simple startup technique is proposed that is appropriate for some applications.

Index Terms—Boost, low voltage, micro fuel cell, power converter, startup circuit.

I. INTRODUCTION

The need for low-input-voltage, low-power boost converters is mainly driven by two issues. First, high demand for low-power, portable electronics will provide a large market for portable power. Second, the ongoing efforts in portable energy sources, especially micro fuel cells, necessitate power management circuitry to connect varying voltage to the fixed voltage load with high efficiency. Individual fuel cells naturally yield a low dc voltage, typically with peak less than 1 V, open circuit, and around 0.5 V under load.

Individual cells can, of course, be stacked to yield higher (and easier) voltage to work with. This is very sensible in bulk power or vehicular applications. For portable applications, packaging and capital cost are very important. Multicell packaging issues include the package of the fuel cells themselves, the added wiring involved with series cells, and routing fuel supply to multiple cells. In a mobile phone, for example, the fuel cell, fuel supply, and power management circuit must all fit in an area currently occupied by a single Li-ion battery while achieving several times the energy density. Therefore, a single-cell (low-voltage) solution is worth investigating.

Low-voltage converters have not been widely investigated to date, probably because low-voltage sources have only recently come of interest. In [1], a parallel solar array is considered in a relatively high power application. Several circuit topologies were discussed for that application and reasonable efficiency was demonstrated from a 0.5-V supply. For the low-power, portable systems considered here, the results in [1] are only

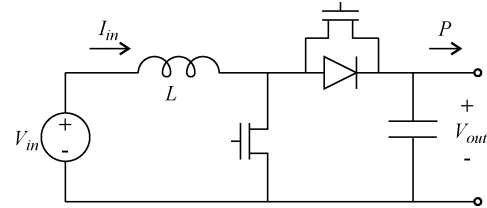


Fig. 1. Synchronous boost converter with signal definitions.

somewhat relevant. In [2], a thermoelectric (~ 0.3 -V input) application was considered. A synchronous boost converter with a startup circuit was shown; making it more in line with our application than [1]. The startup circuit is complicated and not applicable for portable use. Here, we propose a simple startup technique and investigate efficiency and design tradeoffs in more depth for low-power, portable systems than [2]. In [3], reference is made to a 0.4-V input solar power converter, but very little detail and confirmation is provided. The crux of [3] is actually in a novel inductor design. In a later journal publication, [4], the authors of [3] focus only on the inductor design with no discussion of the low-voltage power conversion problem. Commercially available integrated circuits available from many vendors are generally very useful for low-power design. However, they are built up on a market of batteries, which provide significantly higher voltage than the low-voltage sources considered here. Therefore, commercial circuits do not work significantly below 1-V input.

This letter extends our work to be presented in [5].

II. SYNCHRONOUS BOOST CONVERTER EFFICIENCY AND VOLTAGE COLLAPSE

Although efficiency analysis of boost converters has been carried out many times before, we will present it in context of low-input voltage and low power. This will yield simple but useful formulas for choosing MOSFETs and passive components as well as predict voltage collapse.

Consider the synchronous boost circuit of Fig. 1. In continuous mode, the input current I_{in} always flows through the inductor and one of the two MOSFETs and some length of printed circuit board traces. We designate this total series dc resistance as R , which yields a loss $I_{in}^2 R$. There is loss in the capacitor due to equivalent series resistance, r_C . The squared rms capacitor current is approximately

$$I_C^2 = I_{out}(I_{in} - I_{out}) \quad (1)$$

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where I_{out} is the dc output current and I_C is the rms capacitor current.

Switching loss can be approximated according to methods discussed in [6]. That is, the energy loss in one switching cycle for one switch is

$$W_{\text{switch}} = \frac{V_{\text{off}} I_{\text{on}} t_{\text{switch}}}{2} \quad (2)$$

where V_{off} is the off-state voltage, I_{on} is the on-state current, and t_{switch} is the switching time (the sum of the turn-on and turn-off times). Accounting for frequency, f , and both switches, the switching loss is approximately $K I_{\text{in}}$ where

$$K = f V_{\text{out}} t_{\text{switch}}. \quad (3)$$

The power balance equation for the circuit is

$$V_{\text{in}} I_{\text{in}} = P + K I_{\text{in}} + R I_{\text{in}}^2 + r_C I_C^2 + P_{\text{oh}} \quad (4)$$

where P_{oh} is the overhead power associated with running the control circuit and P is the output power. All variables in (4) are considered given except I_{in} , which can be easily solved for using the quadratic equation

$$0 = R I_{\text{in}}^2 + \left(K + r_C \frac{P}{V_{\text{out}}} - V_{\text{in}} \right) I_{\text{in}} + P_{\text{oh}} + P - r_C \left(\frac{P}{V_{\text{out}}} \right)^2. \quad (5)$$

Practical considerations dictate that the negative root must be used. When (5) has complex roots, there is no solution for I_{in} , indicating a voltage collapse. This occurs when the output power is too high. The input current becomes excessive, leading to high losses, which in turn reduces the efficiency further, requiring even more input current, and ultimately causes collapse.

III. EXAMPLE CIRCUIT

Considering the context of a cell phone powered by a single fuel cell, the maximum output power is 3 W (determined by our experimentation with commercially available mobile phones under low signal strength, analog mode). The output voltage must be at least 3.3 V, and the input voltage varies from 1.0 V down to 0.4 V.

Study of (5) revealed that any significant value for R resulted in voltage collapse. Therefore, use of the lowest resistance MOSFETs (4 m Ω) available was dictated. These MOSFETs have a very large gate area and thus have limited switching speed. We settled on a switching frequency of 200 kHz. Commercial ICs use 500 kHz to 1 MHz but have much smaller MOSFETs since they work only with higher input voltage. This lower switching frequency yields a larger inductance than one would like. To achieve low enough current ripple, a 10- μ H Coilcraft inductor was used. It had 10 m Ω of dc resistance. Even though this dc resistance was higher than what we would have preferred, the inductor is already physically large. In addition, a lower resistance inductor was not commercially available; therefore, a higher performance inductor would have to be designed specially for this application. Significant efforts were made to reduce trace and connection resistance, yet still about 4 m Ω of stray resistance resulted.

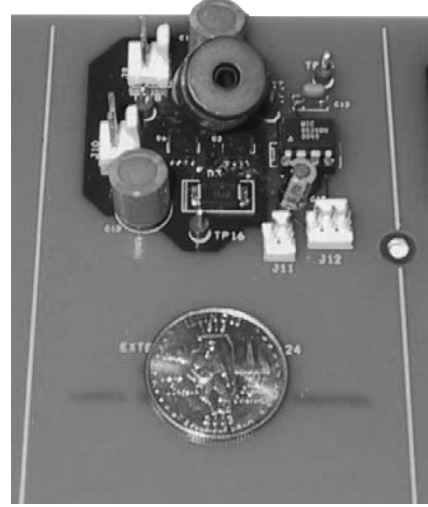


Fig. 2. Photograph of 3-W (nominal) low-input-voltage converter.

The capacitor has a high ESR (13 m Ω), but it is not nearly as critical as the MOSFET and inductor resistances. Indeed, only a few milliwatts are lost in the capacitor. Based on parts chosen, $K = 0.077$ V, which is small relative to the input voltage and has some, but not much, impact. The overhead power was also minimal (<5 mW). It is consumed by a synchronous boost control circuit.

Other factors in efficiency are not difficult to include in the model but were neglected here due to their small impact. For example, the ohmic loss in the inductor due to current ripple was negligible. In other systems, the reader may find it necessary to include it by approximating the rms current ripple and ac series resistance. The inductor used is not a closed core, which resulted in negligible core loss. Again, this design choice may not be the same as what others would use, but it can be easily accounted for in the model using manufacturer data sheets. Gating losses due to charge and discharge of the capacitor (approximately $f C_{gs} V_{gs}^2$) are also straightforward to include in overhead. Only a few milliwatts of loss are attributed here. The reasoning applies to the 1-W power range. At lower power, such as 100 mW and below, all of these effects would be very important.

The circuit as constructed is shown in Fig. 2. Several components would not be necessary in a packaged design (i.e., the plug connectors and test points). Also, a polished, manufacturable design would probably use surface-mount resistors and controller ICs. The purpose here was to demonstrate performance, not a finalized design.

The simulated performance, based on the model, is shown in Fig. 3. Therein, efficiency versus load for several different input voltages is shown. The drop in efficiency under heavy load and low input voltage is evident and probably unacceptable. Voltage collapse is also apparent. The measured efficiency versus load and input voltage is shown in Fig. 4. Slightly lower efficiency resulted than in the model, but the trends are definitely the same. By experimenting with the model, we found the efficiency is lower due to underestimation of switching losses, which was likely due to slight differences in switching times compared to the data sheet and the inexactness of (3) in modeling MOSFET switching energy. Fig. 5 shows the efficiency at 1 W. This is the

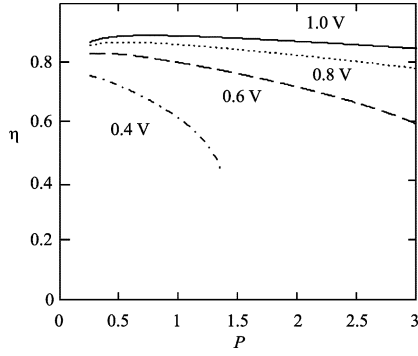


Fig. 3. Predicted efficiency versus power output for various input voltages.

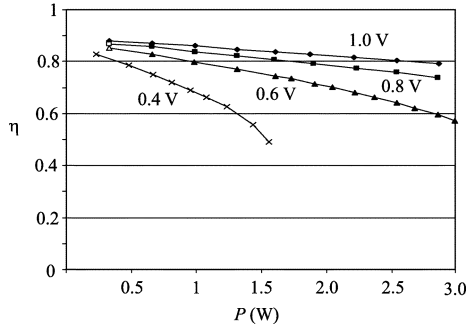


Fig. 4. Measured efficiency versus power output.

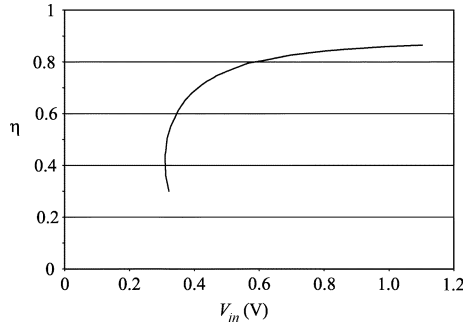


Fig. 5. Measured efficiency at 1 W versus input voltage.

typical talk-time power of a mobile phone as the input voltage is lowered. The voltage collapse at about 0.3 V is apparent.

The main factor in efficiency and voltage collapse is the dc resistance R . The other efficiency factors (core loss, overhead, etc.) can be managed, but the need for a low R is a fundamental issue with regard to available semiconductors, inductors, and standard circuit layout procedures. To quantify the voltage collapse, the designer must investigate (5) for complex roots for various conditions. For example, for a given P , there is a value of V_{in} that dictates complex solutions for I_{in} showing that R is too high. Therefore, a low enough R must be achieved to avoid complex solutions for the highest P and lowest V_{in} to avoid voltage collapse. To alleviate these problems, the source voltage should be as high as possible. For the single fuel cell, this means sizing it such that the current drawn is well below the short circuit current. In fact, the converter and fuel cell should be designed together such that maximum efficiency at based load for the whole system is achieved.

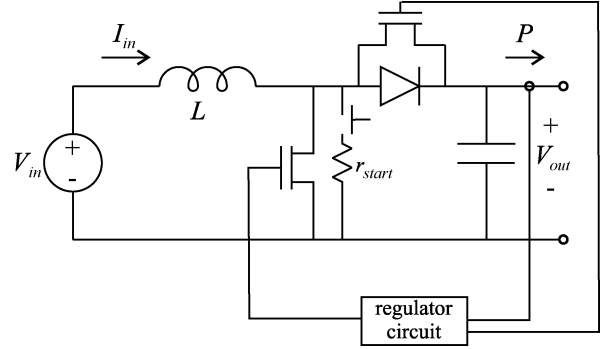


Fig. 6. Startup circuit technique.

IV. STARTUP CIRCUIT

Starting a low-voltage circuit is challenging, particularly when the input is less than about 0.8 V. Standard analog and digital circuits do not accept such a low voltage. Therefore, the control circuit cannot be powered from the source—it must be powered from the higher voltage output. Furthermore, the MOSFETs used will require at least 2 V to achieve low enough resistance for a successful start. In order to use a low-input-voltage source in a portable circuit, the startup issue must be addressed.

As stated, in [2] a startup technique was proposed. It consists of a unipolar junction transistor (UJT), a normally-on transistor, and a resonant tank circuit involving a transformer and capacitors. When the source is connected, it resonates such that the UJT is triggered on and off. The transformer turns ratio is scaled to provide just enough voltage to get the control circuit started. The circuit is difficult to design and more complicated than desired for portable power. The technique does work and was verified in experiment, though our own efforts with similar resonant transformer circuits were less successful. We also experimented with switching output capacitors arrays manually from parallel combinations to series. This worked but resulted in a complicated switching array with many capacitors. The result was an output capacitor with high inductance and series resistance.

As an alternative, we propose the technique illustrated in Fig. 6. Therein, a mechanical switch in series with a resistor is placed in parallel with the lower MOSFET. The mechanical switch is not intended to be an extra component. Instead, it is the switch that we would normally use to turn on the power supply, or at least an extra pole coming off the main switch. The technique works as follows: the user presses the switch and the inductor charges. The inductor current is limited by the resistor to a value chosen by the designer. The switch should be closed for at least four to five time constants of the inductor and start resistor. Normally, this requires only a few milliseconds at most. The current is ultimately limited to a consistent value by the start resistor. Given that the turn-on time is short, even a very briefest effort at switching on will generate consistent results. When the switch is released, the current diverts through the diode and onto the capacitor. By judiciously selecting the resistor, the capacitor can be made to charge to enough voltage to get the regulator circuit running.

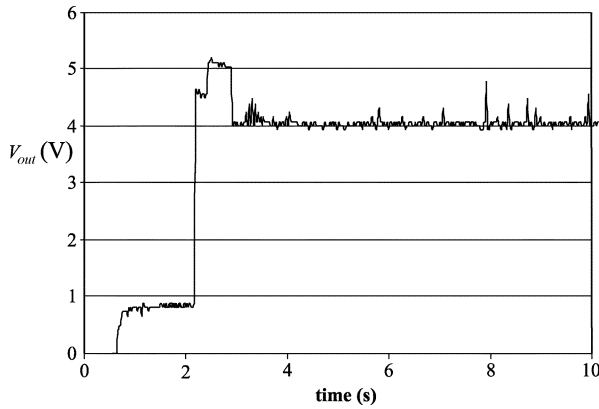


Fig. 7. Measured startup output voltage.

The resistor, r_{start} , is the only design parameter in the startup circuit. In practice, this is an equivalent resistance, composed of the intentional resistor and the stray resistances in the circuit. As a starting point for design, we assume that L and C are chosen to satisfy other converter criteria, such as current and voltage ripple. It can be shown that the ideal resistance to use is

$$r_{\text{start}} = \sqrt{\frac{L}{C}} \frac{V_{\text{in}}}{V_{\text{out}}}. \quad (6)$$

Since the components and layout are nonideal, it is likely the resistance will be chosen somewhat lower. If the converter is loaded at startup, the problem is more difficult. If possible, the load should be activated after startup (as is common in many situations), or a secondary diode and capacitor should be used off of the lower MOSFET drain.

Fig. 7 shows a start transient for a 0.7–4-V converter. The capacitor initially charges to about 0.7 V through the diode, a significant aid. The switch is depressed and released and it can

be observed that the voltage climbs up to over 4 V and then trickles down. Eventually, the regulator circuit is fully operable and the converter runs at the desired 4 V.

While this technique will not be appropriate for all situations, it does cover some. This technique is very simple and so far seems to be the most appropriate method for starting low-input-voltage converters—at least those with start voltages below about 0.8 V. Several minor modifications can be made to the method to accommodate other converters, circuit deactivation, load switches, auxiliary circuits, and so on.

V. CONCLUSIONS

Low-input-voltage, low-power boost converters were investigated with respect to startup and efficiency. It was shown that for powering a typical portable electronics device, low-input voltage can be very compromising in size and cost even though only a few watts are required. A condition for voltage collapse and a new startup technique were shown. Experimental data supported the work.

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