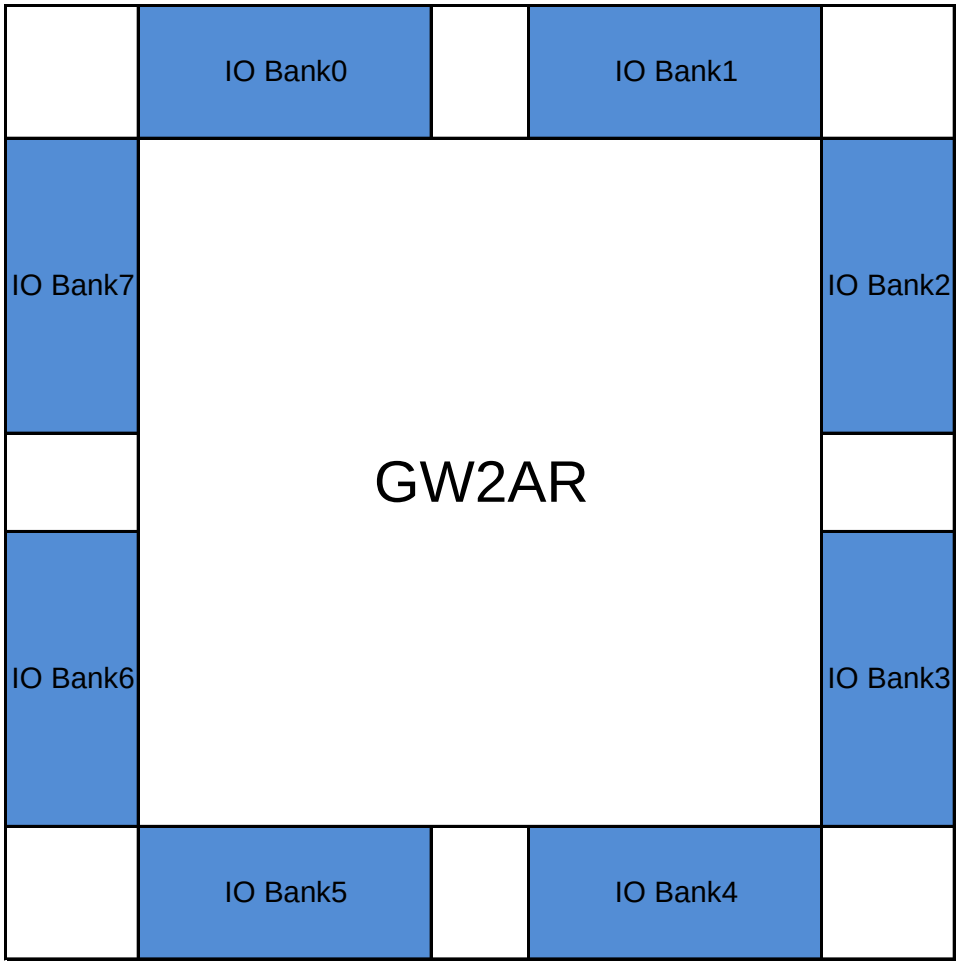
Version History

Date	Version	Description
05/11/2018	1.05E	Initial version published.
08/03/2018	1.06E	The signal "CLKHOLD_N" added in Pin List.
08/08/2018	1.07E	The cofiguration function of SSPI mode modified.
08/29/2018	1.08E	For the QN88 and LQ144 packages, VCCX connects with VCCO7.
11/14/2018	1.09E	The EQ144 package of devices embeded with SDRAM added; The QN88 and EQ144 package of devices embeded with PSRAM added; Power supply requirements added.
03/28/2019	1.1E	EQ176 package added.
03/10/2020	1.2E	Pin description of MODE0/MODE1/MODE2 updated.
06/30/2020	1.2.1E	The package name of QN88/EQ144 (PSRAM embedded) updated to QN88P/EQ144P.
08/07/2020	1.3E	QN88PF and EQ144PF packages added; The power supply pins of LQ176 package and EQ176 package updated.
04/22/2021	1.4E	PG256S package added.

Pins Name	Direction	Description
User I/O Pins		
IO [End][Row/Column Number][A/B]	I/O	[End] indicates the pin location, including L(left), R(right), B(bottom), and T(top)
		[Row/Column Number] indicates the pin Row/Column number. If [End] is T(top) or B(bottom), the pin indicates the column number of the corresponding CFU. If [End] is L(left) or R(right), the pin indicates the row number of the corresponding CFU.
		[A/B] indicaties differential signal pair information.
Multi-Function Pins		
IO [End][Row/Column Number][A/B]/MMM		/MMM represents one or more of the other functions in addition to being general purpose user I/O. When not used for the specical functions, these pins can be user I/O
D0	I/O	Data port D0 in CPU mode
D1	I/O	Data port D1 in CPU mode
D2	I/O	Data port D2 in CPU mode
D3	I/O	Data port D3 in CPU mode
D4	I/O	Data port D4 in CPU mode
D5	I/O	Data port D5 in CPU mode
D6	I/O	Data port D6 in CPU mode
D7	I/O	Data port D7 in CPU mode
WE_N	I	Select the I/O direction of D[7：0] in CPU mode
TMS	I, Internal Weak Pull Up	Serial mode input in JTAG mode
TCK	I	Serial clock input in JTAG mode; connecting 4.7K pull-down resistor on PCB is required
TDO	O	Serial data output in JTAG mode
TDI	I, Internal Weak Pull Up	Serial data input in JTAG mode
JTAGSEL_N	I, Internal Weak Pull Up	JTAG mode selection, active-low
RECONFIG_N	I, Internal Weak Pull Up	Start new GowinCONFIG mode when low pulse
FASTRD_N	I/O	In MSPI mode, FASTRD_N is used as Flash access speed port. Low indicates high-speed Flash access mode; high indicates regular Flash access mode
MI	I/O	MI in MSPI mode
MO	I/O	MO in MSPI mode
MCS_N	I/O	Enable signal MCS_N in MSPI mode, active-low
MCLK	I/O	Clock output MCLK in MSPI mode, the default frequency is 2.1Mhz and the accuracy is +/-5%
DOUT	O	Data output in SERIAL mode
DIN	I, Internal Weak Pull Up	Data input in SERIAL mode
SCLK	I	Clock input in SSPI, SERIAL, and CPU modes

Pins Name	Direction	Description
SO	I/O	SO in SSPI mode
SI	I/O	SI in SSPI mode
SSPI_CS_N	I/O	Enable signal SSPI_CS_N in SSPI mode,active-low, Internal Weak Pull Up
CLKHOLD_N	I, Internal Weak Pull Up	High, indicates that SSPI mode and CPU mode operation are enabled Low, indicates that SSPI mode and CPU mode operation are disabled
DONE	I/O	High indicates that successful completion of programming and configuration Low indicates that incomplete or failed programming and configuration
READY	I/O	High, indicates that device can be programmed and configured Low, indicates that device cannot be programmed and configured
GCLKC_[x]	I	Differential input pin of GCLKT_[x], C(Comp), [x]: global clock No.[1]
GCLKT_[x]	I	Pins for Global clock input, T(True), [x]:global clock number.
LPLL_C_fb/RPLL_C_fb	I	L/R PLL feedback input pins, C(Comp)
LPLL_T_fb/RPLL_T_fb	I	L/R PLL feedback input pins, T(True)
LPLL_C_in/RPLL_C_in	I	L/R PLL clock input pins, C(Comp)
LPLL_T_in/RPLL_T_in	I	L/R PLL clock input pins, T(True)
MODE2	I, Internal Weak Pull Up	GowinCONFIG modes selection pin; if this pin is not bonded, it's internal grounded.
MODE1	I, Internal Weak Pull Up	GowinCONFIG modes selection pin; if this pin is not bonded, it's internal grounded.
MODE0	I, Internal Weak Pull Up	GowinCONFIG modes selection pin; if this pin is not bonded, it's internal grounded.
EXTR	NA	External register of 10K 1% to ground
Other Pins		
NC	NA	Reserved.
VSS	NA	Ground.
VCC	NA	Power supply pins for core voltage.
VCCO#	NA	Power supply pins for I/O BANK#.
VCCX	NA	Power supply pins for auxiliary voltage.
VCCPLLL0/1	NA	Power supply pins for left PLL0/1, only available for LQFP.
VCCPLLR0/1	NA	Power supply pins for right PLL0/1, only available for LQFP.
VCCPLLL	NA	PBGA:Power supply pins for left PLL0/1.
VCCPLLR	NA	PBGA:Power supply pins for right PLL0/1.

Note!
[1]When the input is single-ended, the GCLKC_[x] pin is not a global clock pin.



Note!

1.Each Bank has independent reference volatge (VREF);

2.Users can select to use internal VREF of IOB (equals to 0.5*VCCO) or external VREF input (use any IO pins as external VREF input).

Note!
[1] Embeded with SDRAM.
[2] Embeded with PSRAM.
[3] Tie to VSS by 10K Resistor indicates that pull down to ground through 10K resistor.

Pin Name	Function	DQS	BANK	Configuration Function	Differential Pair	LVDS	QN88[1]	LQ144[1]	EQ144[1]	LQ176[1]	EQ176[1]	QN88P[2]	EQ144P[2]	EQ144PF[2]	QN88PF[2]	PG256S[1]
EXTR	Ground		N/A				47	75	75	91	91	47	75	75	47	(Tie to VSS by 10K Resisitor)
IOB12A	I/O	DQ5	5		True_of_IOB12B	TRUE		44	44	53	53		44	44		P4
IOB12B	I/O	DQ5	5		Comp_of_IOB12A	TRUE		45	45	54	54		45	45		T4
IOB13A	I/O	DQ5	5		True_of_IOB13B	NONE										
IOB13B	I/O	DQ5	5		Comp_of_IOB13A	NONE										
IOB14A	I/O	DQ5	5		True_of_IOB14B	TRUE	29	46	46	55	55	29	46	46	29	
IOB14B	I/O	DQ5	5		Comp_of_IOB14A	TRUE	30	47	47	56	56	30	47	47	30	
IOB15A	I/O	DQ5	5		True_of_IOB15B	NONE										
IOB15B	I/O	DQ5	5		Comp_of_IOB15A	NONE										
IOB16A	I/O	DQ5	5		True_of_IOB16B	TRUE										L8
IOB16B	I/O	DQ5	5		Comp_of_IOB16A	TRUE										L7
IOB17A	I/O	DQ5	5		True_of_IOB17B	NONE		48	48	57	57		48	48		
IOB17B	I/O	DQ5	5		Comp_of_IOB17A	NONE		49	49	58	58		49	49		
IOB18A	I/O	DQ5	5		True_of_IOB18B	TRUE	31			59	59	31			31	N5
IOB18B	I/O	DQ5	5		Comp_of_IOB18A	TRUE	32			60	60	32			32	P5
IOB19A	I/O	DQ5	5		True_of_IOB19B	NONE										
IOB19B	I/O	DQ5	5		Comp_of_IOB19A	NONE										
IOB20A	I/O	DQ5	5		True_of_IOB20B	TRUE		50	50				50	50		R5
IOB20B	I/O	DQ5	5		Comp_of_IOB20A	TRUE		51	51				51	51		T5
IOB21A	I/O	DQS5	5		True_of_IOB21B	NONE				61	61					
IOB21B	I/O	DQS5	5		Comp_of_IOB21A	NONE				62	62					
IOB22A	I/O	DQ5	5		True_of_IOB22B	TRUE		52	52				52	52		P6
IOB22B	I/O	DQ5	5		Comp_of_IOB22A	TRUE		54	54				54	54		T6
IOB23A	I/O	DQ5	5		True_of_IOB23B	NONE										
IOB23B	I/O	DQ5	5		Comp_of_IOB23A	NONE										
IOB24A	I/O	DQ5	5		True_of_IOB24B	TRUE	33					33			33	R7
IOB24B	I/O	DQ5	5		Comp_of_IOB24A	TRUE	34					34			34	T7
IOB25A	I/O	DQ5	5		True_of_IOB25B	NONE										
IOB25B	I/O	DQ5	5		Comp_of_IOB25A	NONE										
IOB26A	I/O	DQ5	5		True_of_IOB26B	TRUE										
IOB26B	I/O	DQ5	5		Comp_of_IOB26A	TRUE										
IOB27A/GCLKT_5	I/O	DQ5	5	GCLKT_5	True_of_IOB27B	NONE				63	63					P7
IOB27B/GCLKC_5	I/O	DQ5	5	GCLKC_5	Comp_of_IOB27A	NONE				64	64					M7
IOB2A	I/O	DQ4	5		True_of_IOB2B	TRUE										
IOB2B	I/O	DQ4	5		Comp_of_IOB2A	TRUE										
IOB30A/GCLKT_4	I/O	DQ6	4	GCLKT_4	True_of_IOB30B	TRUE	35	56	56	68	68	35	56	56	35	P8

Note!
[1] Embeded with SDRAM.
[2] Embeded with PSRAM.
[3] Tie to VSS by 10K Resistor indicates that pull down to ground through 10K resistor.

Pin Name	Function	DQS	BANK	Configuration Function	Differential Pair	LVDS	QN88[1]	LQ144[1]	EQ144[1]	LQ176[1]	EQ176[1]	QN88P[2]	EQ144P[2]	EQ144PF[2]	QN88PF[2]	PG256S[1]
IOB30B/GCLKC_4	I/O	DQ6	4	GCLKC_4	Comp_of_IOB30A	TRUE	36	57	57	69	69	36	57	57	36	T8
IOB31A	I/O	DQ6	4		True_of_IOB31B	NONE										
IOB31B	I/O	DQ6	4		Comp_of_IOB31A	NONE										
IOB32A	I/O	DQ6	4		True_of_IOB32B	TRUE										
IOB32B	I/O	DQ6	4		Comp_of_IOB32A	TRUE										
IOB33A	I/O	DQ6	4		True_of_IOB33B	NONE		58	58				58	58		
IOB33B	I/O	DQ6	4		Comp_of_IOB33A	NONE		59	59				59	59		
IOB34A	I/O	DQ6	4		True_of_IOB34B	TRUE	37	60	60	70	70	37	60	60	37	M9
IOB34B	I/O	DQ6	4		Comp_of_IOB34A	TRUE	38	61	61	71	71	38	61	61	38	N8
IOB35A	I/O	DQ6	4		True_of_IOB35B	NONE										
IOB35B	I/O	DQ6	4		Comp_of_IOB35A	NONE										
IOB36A	I/O	DQ6	4		True_of_IOB36B	TRUE										R9
IOB36B	I/O	DQ6	4		Comp_of_IOB36A	TRUE										T9
IOB37A	I/O	DQS6	4		True_of_IOB37B	NONE				72	72					
IOB37B	I/O	DQS6	4		Comp_of_IOB37A	NONE				73	73					
IOB38A	I/O	DQ6	4		True_of_IOB38B	TRUE		62	62	74	74		62	62		L10
IOB38B	I/O	DQ6	4		Comp_of_IOB38A	TRUE		63	63	75	75		63	63		M10
IOB39A	I/O	DQ6	4		True_of_IOB39B	NONE										
IOB39B	I/O	DQ6	4		Comp_of_IOB39A	NONE										
IOB3A	I/O	DQ4	5		True_of_IOB3B	NONE										
IOB3B	I/O	DQ4	5		Comp_of_IOB3A	NONE										
IOB40A	I/O	DQ6	4		True_of_IOB40B	TRUE	39	64	64	76	76	39	64	64	39	N9
IOB40B	I/O	DQ6	4		Comp_of_IOB40A	TRUE	40	65	65	77	77	40	65	65	40	P9
IOB41A	I/O	DQ6	4		True_of_IOB41B	NONE										
IOB41B	I/O	DQ6	4		Comp_of_IOB41A	NONE										
IOB42A	I/O	DQ6	4		True_of_IOB42B	TRUE		66	66	78	78		66	66		
IOB42B	I/O	DQ6	4		Comp_of_IOB42A	TRUE	42	67	67	79	79	42	67	67	42	
IOB43A	I/O	DQ6	4		True_of_IOB43B	NONE	41					41			41	
IOB43B	I/O	DQ6	4		Comp_of_IOB43A	NONE										
IOB44A	I/O	DQ6	4		True_of_IOB44B	TRUE				80	80					
IOB44B	I/O	DQ6	4		Comp_of_IOB44A	TRUE				81	81					
IOB45A	I/O	DQ6	4		True_of_IOB45B	NONE										
IOB45B	I/O	DQ6	4		Comp_of_IOB45A	NONE										
IOB48A	I/O	DQS7	4		True_of_IOB48B	TRUE		68	68	82	82		68	68		
IOB48B	I/O	DQS7	4		Comp_of_IOB48A	TRUE		69	69	83	83		69	69		
IOB49A	I/O	DQ7	4		True_of_IOB49B	NONE										
IOB49B	I/O	DQ7	4		Comp_of_IOB49A	NONE										
IOB4A	I/O	DQ4	5		True_of_IOB4B	TRUE										M4
IOB4B	I/O	DQ4	5		Comp_of_IOB4A	TRUE				47	47					M3

Note!
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[3] Tie to VSS by 10K Resistor indicates that pull down to ground through 10K resistor.

Pin Name	Function	DQS	BANK	Configuration Function	Differential Pair	LVDS	QN88[1]	LQ144[1]	EQ144[1]	LQ176[1]	EQ176[1]	QN88P[2]	EQ144P[2]	EQ144PF[2]	QN88PF[2]	PG256S[1]
IOB50A	I/O	DQ7	4		True_of_IOB50B	TRUE				84	84					
IOB50B	I/O	DQ7	4		Comp_of_IOB50A	TRUE				85	85					P11
IOB51A	I/O	DQ7	4		True_of_IOB51B	NONE										
IOB51B	I/O	DQ7	4		Comp_of_IOB51A	NONE										
IOB52A	I/O	DQ7	4		True_of_IOB52B	TRUE				86	86					N12
IOB52B	I/O	DQ7	4		Comp_of_IOB52A	TRUE										P12
IOB53A	I/O	DQ7	4		True_of_IOB53B	NONE		70	70				70	70		
IOB53B	I/O	DQ7	4		Comp_of_IOB53A	NONE		71	71				71	71		
IOB54A	I/O	DQ7	4		True_of_IOB54B	TRUE										M12
IOB54B	I/O	DQ7	4		Comp_of_IOB54A	TRUE										M11
IOB55A	I/O	DQ7	4		True_of_IOB55B	NONE										L11
IOB55B	I/O	DQ7	4		Comp_of_IOB55A	NONE		72	72				72	72		
IOB5A	I/O	DQ4	5		True_of_IOB5B	NONE		38	38	48	48		38	38		
IOB5B	I/O	DQ4	5		Comp_of_IOB5A	NONE		39	39				39	39		
IOB6A	I/O	DQ4	5		True_of_IOB6B	TRUE	25	40	40	49	49	25	40	40	25	
IOB6B	I/O	DQ4	5		Comp_of_IOB6A	TRUE	26	41	41	50	50	26	41	41	26	
IOB7A	I/O	DQ4	5		True_of_IOB7B	NONE		42	42				42	42		
IOB7B	I/O	DQ4	5		Comp_of_IOB7A	NONE		43	43				43	43		
IOB8A	I/O	DQ4	5		True_of_IOB8B	TRUE	27			51	51	27			27	M6
IOB8B	I/O	DQ4	5		Comp_of_IOB8A	TRUE	28			52	52	28			28	N6
IOB9A	I/O	DQS4	5		True_of_IOB9B	NONE										
IOB9B	I/O	DQS4	5		Comp_of_IOB9A	NONE										
IOL11A	I/O	DQ1	7		True_of_IOL11B	TRUE				6	6					B2
IOL11B	I/O	DQ1	7		Comp_of_IOL11A	TRUE										A2
IOL12A	I/O	DQ1	7		True_of_IOL12B	NONE										
IOL12B	I/O	DQ1	7		Comp_of_IOL12A	NONE										
IOL13A	I/O	DQ1	7		True_of_IOL13B	TRUE										G6
IOL13B	I/O	DQ1	7		Comp_of_IOL13A	TRUE										G5
IOL14A	I/O	DQ1	7		True_of_IOL14B	NONE										
IOL14B	I/O	DQ1	7		Comp_of_IOL14A	NONE				7	7					
IOL15A	I/O	DQ1	7		True_of_IOL15B	TRUE				8	8					C1
IOL15B	I/O	DQ1	7		Comp_of_IOL15A	TRUE				9	9					B1
IOL16A	I/O	DQ1	7		True_of_IOL16B	NONE										D1
IOL16B	I/O	DQ1	7		Comp_of_IOL16A	NONE										D3
IOL17A	I/O	DQ1	7		True_of_IOL17B	TRUE				10	10					
IOL17B	I/O	DQ1	7		Comp_of_IOL17A	TRUE				11	11					
IOL18A	I/O	DQ1	7		True_of_IOL18B	NONE				12	12					C3
IOL18B	I/O	DQ1	7		Comp_of_IOL18A	NONE										C2
IOL20A	I/O	DQ1	7		True_of_IOL20B	TRUE										K5

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Pin Name	Function	DQS	BANK	Configuration Function	Differential Pair	LVDS	QN88[1]	LQ144[1]	EQ144[1]	LQ176[1]	EQ176[1]	QN88P[2]	EQ144P[2]	EQ144PF[2]	QN88PF[2]	PG256S[1]
IOL20B	I/O	DQ1	7		Comp_of_IOL20A	TRUE										K6
IOL21A	I/O	DQ1	7		True_of_IOL21B	NONE										
IOL21B	I/O	DQ1	7		Comp_of_IOL21A	NONE										
IOL22A	I/O	DQS1	7		True_of_IOL22B	TRUE		9	9				9	9		E2
IOL22B	I/O	DQS1	7		Comp_of_IOL22A	TRUE		10	10				10	10		E1
IOL23A	I/O	DQ1	7		True_of_IOL23B	NONE				14	14					L4
IOL23B	I/O	DQ1	7		Comp_of_IOL23A	NONE										L5
IOL24A	I/O	DQ1	7		True_of_IOL24B	TRUE				15	15					
IOL24B	I/O	DQ1	7		Comp_of_IOL24A	TRUE				16	16					
IOL25A	I/O	DQ1	7		True_of_IOL25B	NONE										H4
IOL25B	I/O	DQ1	7		Comp_of_IOL25A	NONE				18	18					H3
IOL26A	I/O	DQ1	7		True_of_IOL26B	TRUE				17	17					
IOL26B	I/O	DQ1	7		Comp_of_IOL26A	TRUE				19	19					
IOL27A/GCLKT_7	I/O	DQ1	7	GCLKT_7	True_of_IOL27B	NONE		11	11	20	20		11	11		J6
IOL27B/GCLKC_7	I/O	DQ1	7	GCLKC_7	Comp_of_IOL27A	NONE		12	12	21	21		12	12		H5
IOL29A/GCLKT_6	I/O	DQ2	6	GCLKT_6	True_of_IOL29B	TRUE	10	25	25			10	25	25	10	K3
IOL29B/GCLKC_6	I/O	DQ2	6	GCLKC_6	Comp_of_IOL29A	TRUE	11	26	26			11	26	26	11	J4
IOL2A	I/O	DQ0	7		True_of_IOL2B	TRUE		3	3	3	3		3	3		B3
IOL2B	I/O	DQ0	7		Comp_of_IOL2A	TRUE		4	4	4	4		4	4		A3
IOL30A	I/O	DQ2	6		True_of_IOL30B	NONE										
IOL30B	I/O	DQ2	6		Comp_of_IOL30A	NONE										
IOL31A	I/O	DQ2	6		True_of_IOL31B	TRUE										F2
IOL31B	I/O	DQ2	6		Comp_of_IOL31A	TRUE										F1
IOL32A	I/O	DQ2	6		True_of_IOL32B	NONE		23	23				23	23		
IOL32B	I/O	DQ2	6		Comp_of_IOL32A	NONE		24	24				24	24		
IOL33A	I/O	DQ2	6		True_of_IOL33B	TRUE		27	27				27	27		
IOL33B	I/O	DQ2	6		Comp_of_IOL33A	TRUE		28	28				28	28		
IOL34A	I/O	DQ2	6		True_of_IOL34B	NONE										G3
IOL34B	I/O	DQ2	6		Comp_of_IOL34A	NONE										G1
IOL35A	I/O	DQ2	6		True_of_IOL35B	TRUE										
IOL35B	I/O	DQ2	6		Comp_of_IOL35A	TRUE										
IOL36A	I/O	DQS2	6		True_of_IOL36B	NONE		29	29				29	29		H2
IOL36B	I/O	DQS2	6		Comp_of_IOL36A	NONE		30	30				30	30		H1
IOL38A	I/O	DQ2	6		True_of_IOL38B	TRUE				24	24					
IOL38B	I/O	DQ2	6		Comp_of_IOL38A	TRUE				25	25					
IOL39A	I/O	DQ2	6		True_of_IOL39B	NONE										
IOL39B	I/O	DQ2	6		Comp_of_IOL39A	NONE										
IOL3A	I/O	DQ0	7		True_of_IOL3B	NONE										
IOL3B	I/O	DQ0	7		Comp_of_IOL3A	NONE										

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Pin Name	Function	DQS	BANK	Configuration Function	Differential Pair	LVDS	QN88[1]	LQ144[1]	EQ144[1]	LQ176[1]	EQ176[1]	QN88P[2]	EQ144P[2]	EQ144PF[2]	QN88PF[2]	PG256S[1]
IOL40A	I/O	DQ2	6		True_of_IOL40B	TRUE				26	26					
IOL40B	I/O	DQ2	6		Comp_of_IOL40A	TRUE				27	27					
IOL41A	I/O	DQ2	6		True_of_IOL41B	NONE										
IOL41B	I/O	DQ2	6		Comp_of_IOL41A	NONE										
IOL42A	I/O	DQ2	6		True_of_IOL42B	TRUE		32	32	28	28		32	32		J3
IOL42B	I/O	DQ2	6		Comp_of_IOL42A	TRUE		33	33	29	29		33	33		J1
IOL43A	I/O	DQ2	6		True_of_IOL43B	NONE										
IOL43B	I/O	DQ2	6		Comp_of_IOL43A	NONE										
IOL44A	I/O	DQ2	6		True_of_IOL44B	TRUE				30	30					
IOL44B	I/O	DQ2	6		Comp_of_IOL44A	TRUE				31	31					
IOL45A/LPLL2_T_in	I/O	DQ2	6	LPLL2_T_in	True_of_IOL45B	NONE	13	34	34	32	32	13	34	34	13	K2
IOL45B/LPLL2_C_in	I/O	DQ2	6	LPLL2_C_in	Comp_of_IOL45A	NONE		35	35	33	33		35	35		K1
IOL47A/LPLL2_T_fb	I/O	DQ3	6	LPLL2_T_fb	True_of_IOL47B	TRUE	15			35	35	15			15	R2
IOL47B/LPLL2_C_fb	I/O	DQ3	6	LPLL2_C_fb	Comp_of_IOL47A	TRUE	16			36	36	16			16	R1
IOL48A	I/O	DQ3	6		True_of_IOL48B	NONE										M2
IOL48B	I/O	DQ3	6		Comp_of_IOL48A	NONE										M1
IOL49A	I/O	DQ3	6		True_of_IOL49B	TRUE	17			37	37	17			17	L3
IOL49B	I/O	DQ3	6		Comp_of_IOL49A	TRUE	18					18			18	L1
IOL4A	I/O	DQ0	7		True_of_IOL4B	TRUE										F6
IOL4B	I/O	DQ0	7		Comp_of_IOL4A	TRUE										F5
IOL50A	I/O	DQS3	6		True_of_IOL50B	NONE				38	38					N3
IOL50B	I/O	DQS3	6		Comp_of_IOL50A	NONE				39	39					N1
IOL51A	I/O	DQ3	6		True_of_IOL51B	TRUE	19					19			19	P2
IOL51B	I/O	DQ3	6		Comp_of_IOL51A	TRUE	20					20			20	P1
IOL52A	I/O	DQ3	6		True_of_IOL52B	NONE										M5
IOL52B	I/O	DQ3	6		Comp_of_IOL52A	NONE										N4
IOL53A	I/O	DQ3	6		True_of_IOL53B	TRUE				41	41					
IOL53B	I/O	DQ3	6		Comp_of_IOL53A	TRUE				42	42					
IOL54A	I/O	DQ3	6		True_of_IOL54B	NONE										
IOL54B	I/O	DQ3	6		Comp_of_IOL54A	NONE										
IOL5A	I/O	DQ0	7		True_of_IOL5B	NONE										E4
IOL5B	I/O	DQ0	7		Comp_of_IOL5A	NONE										E3
IOL6A	I/O	DQS0	7		True_of_IOL6B	TRUE										
IOL6B	I/O	DQS0	7		Comp_of_IOL6A	TRUE										
IOL7A/LPLL1_T_in	I/O	DQ0	7	LPLL1_T_in	True_of_IOL7B	NONE	4	6	6			4	6	6	4	F4
IOL7B/LPLL1_C_in	I/O	DQ0	7	LPLL1_C_in	Comp_of_IOL7A	NONE		7	7				7	7		F3
IOL8A/LPLL1_T_fb	I/O	DQ0	7	LPLL1_T_fb	True_of_IOL8B	TRUE										
IOL8B/LPLL1_C_fb	I/O	DQ0	7	LPLL1_C_fb	Comp_of_IOL8A	TRUE										
IOL9A	I/O	DQ0	7		True_of_IOL9B	NONE										

Note!
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[3] Tie to VSS by 10K Resistor indicates that pull down to ground through 10K resistor.

Pin Name	Function	DQS	BANK	Configuration Function	Differential Pair	LVDS	QN88[1]	LQ144[1]	EQ144[1]	LQ176[1]	EQ176[1]	QN88P[2]	EQ144P[2]	EQ144PF[2]	QN88PF[2]	PG256S[1]
IOL9B	I/O	DQ0	7		Comp_of_IOL9A	NONE										
IOR11A	I/O	DQ10	2		True_of_IOR11B	TRUE										C15
IOR11B	I/O	DQ10	2		Comp_of_IOR11A	TRUE										C16
IOR12A	I/O	DQ10	2		True_of_IOR12B	NONE										
IOR12B	I/O	DQ10	2		Comp_of_IOR12A	NONE										
IOR13A	I/O	DQ10	2		True_of_IOR13B	TRUE										F15
IOR13B	I/O	DQ10	2		Comp_of_IOR13A	TRUE										F16
IOR14A	I/O	DQ10	2		True_of_IOR14B	NONE				126	126					E15
IOR14B	I/O	DQ10	2		Comp_of_IOR14A	NONE										E16
IOR15A	I/O	DQ10	2		True_of_IOR15B	TRUE										
IOR15B	I/O	DQ10	2		Comp_of_IOR15A	TRUE										
IOR16A	I/O	DQ10	2		True_of_IOR16B	NONE										G14
IOR16B	I/O	DQ10	2		Comp_of_IOR16A	NONE										G16
IOR17A	I/O	DQ10	2		True_of_IOR17B	TRUE										
IOR17B	I/O	DQ10	2		Comp_of_IOR17A	TRUE										
IOR18A	I/O	DQ10	2		True_of_IOR18B	NONE										H15
IOR18B	I/O	DQ10	2		Comp_of_IOR18A	NONE										H16
IOR20A	I/O	DQ10	2		True_of_IOR20B	TRUE		102	102	125	125		102	102		H13
IOR20B	I/O	DQ10	2		Comp_of_IOR20A	TRUE		101	101	124	124		101	101		H14
IOR21A	I/O	DQ10	2		True_of_IOR21B	NONE										
IOR21B	I/O	DQ10	2		Comp_of_IOR21A	NONE										
IOR22A	I/O	DQS10	2		True_of_IOR22B	TRUE		100	100	123	123		100	100		
IOR22B	I/O	DQS10	2		Comp_of_IOR22A	TRUE		99	99	122	122		99	99		
IOR23A	I/O	DQ10	2		True_of_IOR23B	NONE										G12
IOR23B	I/O	DQ10	2		Comp_of_IOR23A	NONE										H11
IOR24A	I/O	DQ10	2		True_of_IOR24B	TRUE										
IOR24B	I/O	DQ10	2		Comp_of_IOR24A	TRUE										
IOR25A/TDO	I/O	DQ10	2	TDO	True_of_IOR25B	NONE	8	18	18	121	121	8	18	18	8	E14
IOR25B/TMS	I/O	DQ10	2	TMS	Comp_of_IOR25A	NONE	5	13	13	119	119	5	13	13	5	A15
IOR26A/TCK	I/O	DQ10	2	TCK	True_of_IOR26B	TRUE	6	14	14	120	120	6	14	14	6	C14
IOR26B/TDI	I/O	DQ10	2	TDI	Comp_of_IOR26A	TRUE	7	16	16	117	117	7	16	16	7	C12
IOR27A/GCLKT_2	I/O	DQ10	2	GCLKT_2	True_of_IOR27B	NONE		98	98	116	116		98	98		J11
IOR27B/GCLKC_2	I/O	DQ10	2	GCLKC_2	Comp_of_IOR27A	NONE		97	97				97	97		J12
IOR29A/GCLKT_3	I/O	DQ9	3	GCLKT_3	True_of_IOR29B	TRUE	63			114	114	63			63	J13
IOR29B/GCLKC_3	I/O	DQ9	3	GCLKC_3	Comp_of_IOR29A	TRUE										K14
IOR2A	I/O	DQ11	2		True_of_IOR2B	TRUE										E13
IOR2B	I/O	DQ11	2		Comp_of_IOR2A	TRUE										E12
IOR30A/MODE0	I/O	DQ9	3	MODE0	True_of_IOR30B	NONE	88	144	144	113	113	88	144	144	88	T11
IOR30B/MODE1	I/O	DQ9	3	MODE1	Comp_of_IOR30A	NONE	87	142	142	111	111	87	142	142	87	N11

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Pin Name	Function	DQS	BANK	Configuration Function	Differential Pair	LVDS	QN88[1]	LQ144[1]	EQ144[1]	LQ176[1]	EQ176[1]	QN88P[2]	EQ144P[2]	EQ144PF[2]	QN88PF[2]	PG256S[1]
IOR31A/MODE2	I/O	DQ9	3	MODE2	True_of_IOR31B	TRUE		143	143	112	112		143	143		
IOR31B/RECONFIG_N	I/O	DQ9	3	RECONFIG_N	Comp_of_IOR31A	TRUE	9	20	20	108	108	9	20	20	9	T2
IOR32A/READY	I/O	DQ9	3	READY	True_of_IOR32B	NONE		22	22	109	109		22	22		R3
IOR32B/DONE	I/O	DQ9	3	DONE	Comp_of_IOR32A	NONE		21	21	107	107		21	21		P13
IOR33A/MI/D7	I/O	DQ9	3	MI/D7	True_of_IOR33B	TRUE	62	96	96	106	106	62	96	96	62	P10
IOR33B/MO/D6	I/O	DQ9	3	MO/D6	Comp_of_IOR33A	TRUE	61	95	95	105	105	61	95	95	61	T10
IOR34A/MCS_N/D5	I/O	DQ9	3	MCS_N/D5	True_of_IOR34B	NONE	60	94	94	104	104	60	94	94	60	T3
IOR34B/MCLK/D4	I/O	DQ9	3	MCLK/D4	Comp_of_IOR34A	NONE	59	93	93	103	103	59	93	93	59	R11
IOR35A/FASTRD_N/D3	I/O	DQ9	3	FASTRD_N/D3	True_of_IOR35B	TRUE	57	92	92	102	102	57	92	92	57	K12
IOR35B/SI/D2	I/O	DQ9	3	SI/D2	Comp_of_IOR35A	TRUE		90	90	101	101		90	90		K11
IOR36A/SO/D1	I/O	DQS9	3	SO/D1	True_of_IOR36B	NONE	56	88	88	100	100	56	88	88	56	N14
IOR36B/SSPI_CS_N/D0	I/O	DQS9	3	SSPI_CS_N/D0	Comp_of_IOR36A	NONE	55	87	87	99	99	55	87	87	55	N16
IOR38A/DIN/CLKHOLD_N	I/O	DQ9	3	DIN/CLKHOLD_N	True_of_IOR38B	TRUE	54	86	86	98	98	54	86	86	54	J14
IOR38B/DOUT/WE_N	I/O	DQ9	3	DOUT/WE_N	Comp_of_IOR38A	TRUE	53	85	85	97	97	53	85	85	53	J16
IOR39A/SCLK	I/O	DQ9	3	SCLK	True_of_IOR39B	NONE	52	15	15	96	96	52	15	15	52	
IOR39B	I/O	DQ9	3		Comp_of_IOR39A	NONE										
IOR3A	I/O	DQ11	2		True_of_IOR3B	NONE										
IOR3B	I/O	DQ11	2		Comp_of_IOR3A	NONE										
IOR40A	I/O	DQ9	3		True_of_IOR40B	TRUE										K15
IOR40B	I/O	DQ9	3		Comp_of_IOR40A	TRUE										K16
IOR41A	I/O	DQ9	3		True_of_IOR41B	NONE										
IOR41B	I/O	DQ9	3		Comp_of_IOR41A	NONE										
IOR42A	I/O	DQ9	3		True_of_IOR42B	TRUE		84	84				84	84		M15
IOR42B	I/O	DQ9	3		Comp_of_IOR42A	TRUE		83	83				83	83		M16
IOR43A	I/O	DQ9	3		True_of_IOR43B	NONE										L14
IOR43B	I/O	DQ9	3		Comp_of_IOR43A	NONE										L16
IOR44A	I/O	DQ9	3		True_of_IOR44B	TRUE										
IOR44B	I/O	DQ9	3		Comp_of_IOR44A	TRUE										
IOR45A/RPLL2_T_in	I/O	DQ9	3	RPLL2_T_in	True_of_IOR45B	NONE	51	82	82	93	93	51	82	82	51	M13
IOR45B/RPLL2_C_in	I/O	DQ9	3	RPLL2_C_in	Comp_of_IOR45A	NONE										M14
IOR47A/RPLL2_T_fb	I/O	DQ8	3	RPLL2_T_fb	True_of_IOR47B	TRUE				92	92					R15
IOR47B/RPLL2_C_fb	I/O	DQ8	3	RPLL2_C_fb	Comp_of_IOR47A	TRUE										R16

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Pin Name	Function	DQS	BANK	Configuration Function	Differential Pair	LVDS	QN88[1]	LQ144[1]	EQ144[1]	LQ176[1]	EQ176[1]	QN88P[2]	EQ144P[2]	EQ144PF[2]	QN88PF[2]	PG256S[1]
IOR48A	I/O	DQ8	3		True_of_IOR48B	NONE										
IOR48B	I/O	DQ8	3		Comp_of_IOR48A	NONE										
IOR49A	I/O	DQ8	3		True_of_IOR49B	TRUE	49	80	80			49	80	80	49	R14
IOR49B	I/O	DQ8	3		Comp_of_IOR49A	TRUE	48	79	79			48	79	79	48	T15
IOR4A	I/O	DQ11	2		True_of_IOR4B	TRUE										B15
IOR4B	I/O	DQ11	2		Comp_of_IOR4A	TRUE										B16
IOR50A	I/O	DQS8	3		True_of_IOR50B	NONE		78	78				78	78		T14
IOR50B	I/O	DQS8	3		Comp_of_IOR50A	NONE		76	76				76	76		T13
IOR51A	I/O	DQ8	3		True_of_IOR51B	TRUE										L12
IOR51B	I/O	DQ8	3		Comp_of_IOR51A	TRUE										L13
IOR52A	I/O	DQ8	3		True_of_IOR52B	NONE										
IOR52B	I/O	DQ8	3		Comp_of_IOR52A	NONE										
IOR53A	I/O	DQ8	3		True_of_IOR53B	TRUE										R12
IOR53B	I/O	DQ8	3		Comp_of_IOR53A	TRUE										T12
IOR54A	I/O	DQ8	3		True_of_IOR54B	NONE										P15
IOR54B	I/O	DQ8	3		Comp_of_IOR54A	NONE										P16
IOR5A	I/O	DQ11	2		True_of_IOR5B	NONE										F12
IOR5B	I/O	DQ11	2		Comp_of_IOR5A	NONE										G11
IOR6A	I/O	DQS11	2		True_of_IOR6B	TRUE										
IOR6B	I/O	DQS11	2		Comp_of_IOR6A	TRUE										
IOR7A/RPLL1_T_in	I/O	DQ11	2	RPLL1_T_in	True_of_IOR7B	NONE		106	106	129	129		106	106		D14
IOR7B/RPLL1_C_in	I/O	DQ11	2	RPLL1_C_in	Comp_of_IOR7A	NONE		105	105	128	128		105	105		D16
IOR8A/RPLL1_T_fb	I/O	DQ11	2	RPLL1_T_fb	True_of_IOR8B	TRUE										F13
IOR8B/RPLL1_C_fb	I/O	DQ11	2	RPLL1_C_fb	Comp_of_IOR8A	TRUE										F14
IOR9A	I/O	DQ11	2		True_of_IOR9B	NONE										
IOR9B	I/O	DQ11	2		Comp_of_IOR9A	NONE										
IOT12A	I/O	DQ14	0		True_of_IOT12B	TRUE		134	134	169	169		134	134		B6
IOT12B	I/O	DQ14	0		Comp_of_IOT12A	TRUE		133	133	168	168		133	133		A6
IOT13A	I/O	DQ14	0		True_of_IOT13B	NONE										
IOT13B	I/O	DQ14	0		Comp_of_IOT13A	NONE										
IOT14A	I/O	DQ14	0		True_of_IOT14B	TRUE		132	132	167	167		132	132		F7
IOT14B	I/O	DQ14	0		Comp_of_IOT14A	TRUE		131	131	166	166		131	131		E6
IOT15A	I/O	DQ14	0		True_of_IOT15B	NONE										
IOT15B	I/O	DQ14	0		Comp_of_IOT15A	NONE										
IOT16A	I/O	DQ14	0		True_of_IOT16B	TRUE				165	165					C7
IOT16B	I/O	DQ14	0		Comp_of_IOT16A	TRUE				164	164					A7
IOT17A	I/O	DQ14	0		True_of_IOT17B	NONE	82	130	130			82	130	130	82	
IOT17B	I/O	DQ14	0		Comp_of_IOT17A	NONE	81	129	129			81	129	129	81	
IOT18A	I/O	DQ14	0		True_of_IOT18B	TRUE				163	163					D6

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IOT18B	I/O	DQ14	0		Comp_of_IOT18A	TRUE				162	162					C6
IOT19A	I/O	DQ14	0		True_of_IOT19B	NONE		128	128				128	128		
IOT19B	I/O	DQ14	0		Comp_of_IOT19A	NONE										
IOT20A	I/O	DQ14	0		True_of_IOT20B	TRUE										
IOT20B	I/O	DQ14	0		Comp_of_IOT20A	TRUE										
IOT21A	I/O	DQS14	0		True_of_IOT21B	NONE				161	161					
IOT21B	I/O	DQS14	0		Comp_of_IOT21A	NONE				160	160					
IOT22A	I/O	DQ14	0		True_of_IOT22B	TRUE		125	125				125	125		B8
IOT22B	I/O	DQ14	0		Comp_of_IOT22A	TRUE										A8
IOT23A	I/O	DQ14	0		True_of_IOT23B	NONE		126	126				126	126		
IOT23B	I/O	DQ14	0		Comp_of_IOT23A	NONE		124	124				124	124		
IOT24A	I/O	DQ14	0		True_of_IOT24B	TRUE				159	159					C9
IOT24B	I/O	DQ14	0		Comp_of_IOT24A	TRUE				158	158					A9
IOT25A	I/O	DQ14	0		True_of_IOT25B	NONE										
IOT25B	I/O	DQ14	0		Comp_of_IOT25A	NONE										
IOT26A	I/O	DQ14	0		True_of_IOT26B	TRUE										
IOT26B	I/O	DQ14	0		Comp_of_IOT26A	TRUE										
IOT27A/GCLKT_0	I/O	DQ14	0	GCLKT_0	True_of_IOT27B	NONE	80	123	123	157	157	80	123	123	80	B10
IOT27B/GCLKC_0	I/O	DQ14	0	GCLKC_0	Comp_of_IOT27A	NONE	79	122	122	156	156	79	122	122	79	A10
IOT2A	I/O	DQ15	0		True_of_IOT2B	TRUE										C4
IOT2B	I/O	DQ15	0		Comp_of_IOT2A	TRUE		141	141				141	141		A4
IOT30A/GCLKT_1	I/O	DQ13	1	GCLKT_1	True_of_IOT30B	TRUE	77	121	121	152	152	77	121	121	77	E7
IOT30B/GCLKC_1	I/O	DQ13	1	GCLKC_1	Comp_of_IOT30A	TRUE	76	120	120	151	151	76	120	120	76	E8
IOT31A	I/O	DQ13	1		True_of_IOT31B	NONE										
IOT31B	I/O	DQ13	1		Comp_of_IOT31A	NONE										
IOT32A	I/O	DQ13	1		True_of_IOT32B	TRUE										E10
IOT32B	I/O	DQ13	1		Comp_of_IOT32A	TRUE										C10
IOT33A	I/O	DQ13	1		True_of_IOT33B	NONE										
IOT33B	I/O	DQ13	1		Comp_of_IOT33A	NONE										
IOT34A	I/O	DQ13	1		True_of_IOT34B	TRUE	75					75			75	
IOT34B	I/O	DQ13	1		Comp_of_IOT34A	TRUE	74					74			74	
IOT35A	I/O	DQ13	1		True_of_IOT35B	NONE										
IOT35B	I/O	DQ13	1		Comp_of_IOT35A	NONE										
IOT36A	I/O	DQ13	1		True_of_IOT36B	TRUE										
IOT36B	I/O	DQ13	1		Comp_of_IOT36A	TRUE										
IOT37A	I/O	DQS13	1		True_of_IOT37B	NONE				150	150					
IOT37B	I/O	DQS13	1		Comp_of_IOT37A	NONE				149	149					
IOT38A	I/O	DQ13	1		True_of_IOT38B	TRUE		119	119	148	148		119	119		
IOT38B	I/O	DQ13	1		Comp_of_IOT38A	TRUE		118	118	147	147		118	118		

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Pin Name	Function	DQS	BANK	Configuration Function	Differential Pair	LVDS	QN88[1]	LQ144[1]	EQ144[1]	LQ176[1]	EQ176[1]	QN88P[2]	EQ144P[2]	EQ144PF[2]	QN88PF[2]	PG256S[1]
IOT39A	I/O	DQ13	1		True_of_IOT39B	NONE										
IOT39B	I/O	DQ13	1		Comp_of_IOT39A	NONE										
IOT3A	I/O	DQ15	0		True_of_IOT3B	NONE										
IOT3B	I/O	DQ15	0		Comp_of_IOT3A	NONE										
IOT40A	I/O	DQ13	1		True_of_IOT40B	TRUE	73	117	117	146	146	73	117	117	73	D8
IOT40B	I/O	DQ13	1		Comp_of_IOT40A	TRUE	72	116	116	145	145	72	116	116	72	C8
IOT41A	I/O	DQ13	1		True_of_IOT41B	NONE										
IOT41B	I/O	DQ13	1		Comp_of_IOT41A	NONE										
IOT42A	I/O	DQ13	1		True_of_IOT42B	TRUE		115	115	144	144		115	115		C11
IOT42B	I/O	DQ13	1		Comp_of_IOT42A	TRUE		114	114	143	143		114	114		A11
IOT43A	I/O	DQ13	1		True_of_IOT43B	NONE										
IOT43B	I/O	DQ13	1		Comp_of_IOT43A	NONE										
IOT44A	I/O	DQ13	1		True_of_IOT44B	TRUE	71			142	142	71			71	F9
IOT44B	I/O	DQ13	1		Comp_of_IOT44A	TRUE	70			141	141	70			70	D9
IOT45A	I/O	DQ13	1		True_of_IOT45B	NONE										
IOT45B	I/O	DQ13	1		Comp_of_IOT45A	NONE										
IOT48A	I/O	DQS12	1		True_of_IOT48B	TRUE		113	113	140	140		113	113		B12
IOT48B	I/O	DQS12	1		Comp_of_IOT48A	TRUE		112	112	139	139		112	112		A12
IOT49A	I/O	DQ12	1		True_of_IOT49B	NONE										
IOT49B	I/O	DQ12	1		Comp_of_IOT49A	NONE										
IOT4A	I/O	DQ15	0		True_of_IOT4B	TRUE	86	140	140			86	140	140	86	B5
IOT4B	I/O	DQ15	0		Comp_of_IOT4A	TRUE	85	139	139	174	174	85	139	139	85	A5
IOT50A	I/O	DQ12	1		True_of_IOT50B	TRUE	69	111	111	138	138	69	111	111	69	C13
IOT50B	I/O	DQ12	1		Comp_of_IOT50A	TRUE		110	110	137	137		110	110		A13
IOT51A	I/O	DQ12	1		True_of_IOT51B	NONE										
IOT51B	I/O	DQ12	1		Comp_of_IOT51A	NONE										
IOT52A	I/O	DQ12	1		True_of_IOT52B	TRUE				136	136					F10
IOT52B	I/O	DQ12	1		Comp_of_IOT52A	TRUE				135	135					E11
IOT53A	I/O	DQ12	1		True_of_IOT53B	NONE										
IOT53B	I/O	DQ12	1		Comp_of_IOT53A	NONE										
IOT54A	I/O	DQ12	1		True_of_IOT54B	TRUE										B14
IOT54B	I/O	DQ12	1		Comp_of_IOT54A	TRUE										A14
IOT55A	I/O	DQ12	1		True_of_IOT55B	NONE										D11
IOT55B/JTAGSEL_N	I/O	DQ12	1	JTAGSEL_N	Comp_of_IOT55A	NONE										D12
IOT5A	I/O	DQ15	0		True_of_IOT5B	NONE										
IOT5B	I/O	DQ15	0		Comp_of_IOT5A	NONE										
IOT6A	I/O	DQ15	0		True_of_IOT6B	TRUE	84	138	138	173	173	84	138	138	84	
IOT6B	I/O	DQ15	0		Comp_of_IOT6A	TRUE	83	137	137	172	172	83	137	137	83	

Note!
[1] Embeded with SDRAM.
[2] Embeded with PSRAM.
[3] Tie to VSS by 10K Resistor indicates that pull down to ground through 10K resistor.

Pin Name	Function	DQS	BANK	Configuration Function	Differential Pair	LVDS	QN88[1]	LQ144[1]	EQ144[1]	LQ176[1]	EQ176[1]	QN88P[2]	EQ144P[2]	EQ144PF[2]	QN88PF[2]	PG256S[1]
IOT7A	I/O	DQ15	0		True_of_IOT7B	NONE		136	136				136	136		
IOT7B	I/O	DQ15	0		Comp_of_IOT7A	NONE		135	135				135	135		
IOT8A	I/O	DQ15	0		True_of_IOT8B	TRUE										
IOT8B	I/O	DQ15	0		Comp_of_IOT8A	TRUE										
IOT9A	I/O	DQS15	0		True_of_IOT9B	NONE				171	171					D5
IOT9B	I/O	DQS15	0		Comp_of_IOT9A	NONE				170	170					C5
VCC	Power		N/A				1					1			1	G7
VCC	Power		N/A				22			44	44	22			22	G9
VCC	Power		N/A				45			89	89	45			45	H8
VCC	Power		N/A				66			132	132	66			66	J9
VCC	Power		N/A							1	1					K10
VCC	Power		N/A													K8
VCC/VCCPLLL1	Power		N/A					1	1							
VCC/VCCPLLL1	Power		N/A					36	36							
VCC/VCCPLLL1	Power		N/A					73	73							
VCC/VCCPLLL1	Power		N/A					108	108							
VCC/VCCPLLL1	Power		N/A										1	1		
VCC/VCCPLLL1	Power		N/A										36	36		
VCC/VCCPLLL1	Power		N/A										73	73		
VCC/VCCPLLL1	Power		N/A										108	108		
VCCO0	Power		N/A				78			155	155	78			78	B4
VCCO0	Power		N/A					127	127				127	127		B9
VCCO0	Power		N/A							176	176					D7
VCCO1	Power		N/A				67	109	109	133	133		109	109		B13
VCCO1	Power		N/A							153	153					D10
VCCO2	Power		N/A											103	64	
VCCO2/VCCO3/ VCCO6/VCCO7	Power		N/A							5	5					
VCCO2/VCCO3/ VCCO6/VCCO7	Power		N/A							13	13					
VCCO2/VCCO3/ VCCO6/VCCO7	Power		N/A							22	22					
VCCO2/VCCO3/ VCCO6/VCCO7	Power		N/A							40	40					
VCCO2/VCCO3/ VCCO6/VCCO7	Power		N/A							95	95					
VCCO2/VCCO3/ VCCO6/VCCO7	Power		N/A							110	110					

Note!
[1] Embeded with SDRAM.
[2] Embeded with PSRAM.
[3] Tie to VSS by 10K Resistor indicates that pull down to ground through 10K resistor.

Pin Name	Function	DQS	BANK	Configuration Function	Differential Pair	LVDS	QN88[1]	LQ144[1]	EQ144[1]	LQ176[1]	EQ176[1]	QN88P[2]	EQ144P[2]	EQ144PF[2]	QN88PF[2]	PG256S[1]
VCCO2/VCCO3/ VCCO6/VCCO7	Power		N/A							118	118					
VCCO2/VCCO3/ VCCO6/VCCO7	Power		N/A							130	130					
VCCO2/VCCO7	Power		N/A										5			
VCCO2/VCCO7	Power		N/A										19			
VCCO2/VCCO7	Power		N/A										103			
VCCO2/VCCO7	Power		N/A									3				
VCCO2/VCCO7	Power		N/A									64				
VCCO3	Power		N/A				58	91	91			58	91	91	58	
VCCO3	Power		N/A					77	77				77	77		
VCCO4	Power		N/A				44			88	88	44			44	N10
VCCO4	Power		N/A					55	55	67	67					R8
VCCO5	Power		N/A				23	37	37	45	45	23	37	37	23	N7
VCCO5	Power		N/A							65	65					R4
VCCO7	Power		N/A											5	3	
VCCO7	Power		N/A											19		
VCCPLLL	Power		N/A													J7
VCCPLLL0	Power		N/A					8	8				8	8		
VCCPLLL1	Power		N/A				14			34	34	14			14	
VCCPLLR	Power		N/A													H10
VCCPLLR0	Power		N/A					104	104	127	127		104	104		
VCCPLLR1	Power		N/A				50	81	81	94	94	50	81	81	50	
VCCX	Power		N/A							23	23					
VCCX	Power		N/A							66	66					
VCCX	Power		N/A							115	115					
VCCX	Power		N/A							154	154					
VCCX/VCCO1/ VCCO6	Power		N/A									12			12	
VCCX/VCCO1/ VCCO6	Power		N/A									67			67	
VCCX/VCCO2/ VCCO6/VCCO7	Power		N/A				3									
VCCX/VCCO2/ VCCO6/VCCO7	Power		N/A				12									
VCCX/VCCO2/ VCCO6/VCCO7	Power		N/A				64									
VCCX/VCCO2/ VCCO6/VCCO7	Power		N/A					5	5							

Note!
[1] Embeded with SDRAM.
[2] Embeded with PSRAM.
[3] Tie to VSS by 10K Resistor indicates that pull down to ground through 10K resistor.

Pin Name	Function	DQS	BANK	Configuration Function	Differential Pair	LVDS	QN88[1]	LQ144[1]	EQ144[1]	LQ176[1]	EQ176[1]	QN88P[2]	EQ144P[2]	EQ144PF[2]	QN88PF[2]	PG256S[1]
VCCX/VCCO2/ VCCO6/VCCO7	Power		N/A					19	19							
VCCX/VCCO2/ VCCO6/VCCO7	Power		N/A					31	31							
VCCX/VCCO2/ VCCO6/VCCO7	Power		N/A					103	103							
VCCX/VCCO2/ VCCO3/VCCO6/ VCCO7	Power		N/A													D15
VCCX/VCCO2/ VCCO3/VCCO6/ VCCO7	Power		N/A													G13
VCCX/VCCO2/ VCCO3/VCCO6/ VCCO7	Power		N/A													J15
VCCX/VCCO2/ VCCO3/VCCO6/ VCCO7	Power		N/A													K13
VCCX/VCCO2/ VCCO3/VCCO6/ VCCO7	Power		N/A													N15
VCCX/VCCO2/ VCCO3/VCCO6/ VCCO7	Power		N/A													R13
VCCX/VCCO2/ VCCO3/VCCO6/ VCCO7	Power		N/A													K4
VCCX/VCCO2/ VCCO3/VCCO6/ VCCO7	Power		N/A													N2
VCCX/VCCO2/ VCCO3/VCCO6/ VCCO7	Power		N/A													J2
VCCX/VCCO2/ VCCO3/VCCO6/ VCCO7	Power		N/A													G4
VCCX/VCCO2/ VCCO3/VCCO6/ VCCO7	Power		N/A													D2

Note!
[1] Embeded with SDRAM.
[2] Embeded with PSRAM.
[3] Tie to VSS by 10K Resistor indicates that pull down to ground through 10K resistor.

Pin Name	Function	DQS	BANK	Configuration Function	Differential Pair	LVDS	QN88[1]	LQ144[1]	EQ144[1]	LQ176[1]	EQ176[1]	QN88P[2]	EQ144P[2]	EQ144PF[2]	QN88PF[2]	PG256S[1]
VCCX/VCCO2/ VCCO3/VCCO6/ VCCO7	Power		N/A													E5
VCCX/VCCO2/ VCCO3/VCCO6/ VCCO7	Power		N/A													F11
VCCX/VCCO2/ VCCO3/VCCO6/ VCCO7	Power		N/A													F8
VCCX/VCCO2/ VCCO3/VCCO6/ VCCO7	Power		N/A													G10
VCCX/VCCO2/ VCCO3/VCCO6/ VCCO7	Power		N/A													H6
VCCX/VCCO2/ VCCO3/VCCO6/ VCCO7	Power		N/A													J10
VCCX/VCCO2/ VCCO3/VCCO6/ VCCO7	Power		N/A													L6
VCCX/VCCO2/ VCCO3/VCCO6/ VCCO7	Power		N/A													L9
VCCX/VCCO4/ VCCO6	Power		N/A										31	31		
VCCX/VCCO4/ VCCO6	Power		N/A										55	55		
VSS	Ground		N/A				2	2	2	2	2	2	2	2	2	A1
VSS	Ground		N/A				21					21			21	A16
VSS	Ground		N/A				24					24			24	B11
VSS	Ground		N/A				43					43			43	B7
VSS	Ground		N/A				46	74	74	90	90	46	74	74	46	D13
VSS	Ground		N/A				65			131	131	65	107	107	65	D4
VSS	Ground		N/A				68					68			68	E9
VSS	Ground		N/A					17	17	134	134		17	17		G15
VSS	Ground		N/A					53	53	175	175		53	53		G2
VSS	Ground		N/A					89	89				89	89		G8
VSS	Ground		N/A					107	107							H12

Note!
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Pin Name	Function	DQS	BANK	Configuration Function	Differential Pair	LVDS	QN88[1]	LQ144[1]	EQ144[1]	LQ176[1]	EQ176[1]	QN88P[2]	EQ144P[2]	EQ144PF[2]	QN88PF[2]	PG256S[1]
VSS	Ground		N/A							43	43					H7
VSS	Ground		N/A							46	46					H9
VSS	Ground		N/A							87	87					J5
VSS	Ground		N/A													J8
VSS	Ground		N/A													K7
VSS	Ground		N/A													K9
VSS	Ground		N/A													L15
VSS	Ground		N/A													L2
VSS	Ground		N/A													M8
VSS	Ground		N/A													N13
VSS	Ground		N/A													P3
VSS	Ground		N/A													R10
VSS	Ground		N/A													R6
VSS	Ground		N/A													T1
VSS	Ground		N/A													T16
NC	N/A		N/A													P14

Note!
[1] Embeded with SDRAM.
[2] Embeded with PSRAM.

Pin Name	Function	DQS	BANK	Configuration Function	Differential Pair	LVDS	QN88[1]	LQ144[1]	EQ144[1]	LQ176[1]	EQ176[1]	QN88P[2]	EQ144P[2]	EQ144PF[2]	QN88PF[2]	PG256S[1]
BANK7 True LVDS Pair																
IOL11A	I/O	DQ1	7		True_of_IOL11B	TRUE										B2
IOL11B	I/O	DQ1	7		Comp_of_IOL11A	TRUE										A2
IOL13A	I/O	DQ1	7		True_of_IOL13B	TRUE										G6
IOL13B	I/O	DQ1	7		Comp_of_IOL13A	TRUE										G5
IOL15A	I/O	DQ1	7		True_of_IOL15B	TRUE				8	8					C1
IOL15B	I/O	DQ1	7		Comp_of_IOL15A	TRUE				9	9					B1
IOL17A	I/O	DQ1	7		True_of_IOL17B	TRUE				10	10					
IOL17B	I/O	DQ1	7		Comp_of_IOL17A	TRUE				11	11					
IOL20A	I/O	DQ1	7		True_of_IOL20B	TRUE										K5
IOL20B	I/O	DQ1	7		Comp_of_IOL20A	TRUE										K6
IOL22A	I/O	DQS1	7		True_of_IOL22B	TRUE		9	9				9	9		E2
IOL22B	I/O	DQS1	7		Comp_of_IOL22A	TRUE		10	10				10	10		E1
IOL24A	I/O	DQ1	7		True_of_IOL24B	TRUE				15	15					
IOL24B	I/O	DQ1	7		Comp_of_IOL24A	TRUE				16	16					
IOL26A	I/O	DQ1	7		True_of_IOL26B	TRUE				17	17					
IOL26B	I/O	DQ1	7		Comp_of_IOL26A	TRUE				19	19					
IOL2A	I/O	DQ0	7		True_of_IOL2B	TRUE		3	3	3	3		3	3		B3
IOL2B	I/O	DQ0	7		Comp_of_IOL2A	TRUE		4	4	4	4		4	4		A3
IOL4A	I/O	DQ0	7		True_of_IOL4B	TRUE										F6
IOL4B	I/O	DQ0	7		Comp_of_IOL4A	TRUE										F5
IOL6A	I/O	DQS0	7		True_of_IOL6B	TRUE										
IOL6B	I/O	DQS0	7		Comp_of_IOL6A	TRUE										
IOL8A/LPLL1_T_fb	I/O	DQ0	7	LPLL1_T_fb	True_of_IOL8B	TRUE										
IOL8B/LPLL1_C_fb	I/O	DQ0	7	LPLL1_C_fb	Comp_of_IOL8A	TRUE										

Note!
[1] Embeded with SDRAM.
[2] Embeded with PSRAM.

Pin Name	Function	DQS	BANK	Configuration Function	Differential Pair	LVDS	QN88[1]	LQ144[1]	EQ144[1]	LQ176[1]	EQ176[1]	QN88P[2]	EQ144P[2]	EQ144PF[2]	QN88PF[2]	PG256S[1]
BANK6 True LVDS Pair																
IOL29A/GCLKT_6	I/O	DQ2	6	GCLKT_6	True_of_IOL29B	TRUE	10	25	25			10	25	25	10	K3
IOL29B/GCLKC_6	I/O	DQ2	6	GCLKC_6	Comp_of_IOL29A	TRUE	11	26	26			11	26	26	11	J4
IOL31A	I/O	DQ2	6		True_of_IOL31B	TRUE										F2
IOL31B	I/O	DQ2	6		Comp_of_IOL31A	TRUE										F1
IOL33A	I/O	DQ2	6		True_of_IOL33B	TRUE		27	27				27	27		
IOL33B	I/O	DQ2	6		Comp_of_IOL33A	TRUE		28	28				28	28		
IOL35A	I/O	DQ2	6		True_of_IOL35B	TRUE										
IOL35B	I/O	DQ2	6		Comp_of_IOL35A	TRUE										
IOL38A	I/O	DQ2	6		True_of_IOL38B	TRUE				24	24					
IOL38B	I/O	DQ2	6		Comp_of_IOL38A	TRUE				25	25					
IOL40A	I/O	DQ2	6		True_of_IOL40B	TRUE				26	26					
IOL40B	I/O	DQ2	6		Comp_of_IOL40A	TRUE				27	27					
IOL42A	I/O	DQ2	6		True_of_IOL42B	TRUE		32	32	28	28		32	32		J3
IOL42B	I/O	DQ2	6		Comp_of_IOL42A	TRUE		33	33	29	29		33	33		J1
IOL44A	I/O	DQ2	6		True_of_IOL44B	TRUE				30	30					
IOL44B	I/O	DQ2	6		Comp_of_IOL44A	TRUE				31	31					
IOL47A/LPLL2_T_fb	I/O	DQ3	6	LPLL2_T_fb	True_of_IOL47B	TRUE	15			35	35	15			15	R2
IOL47B/LPLL2_C_fb	I/O	DQ3	6	LPLL2_C_fb	Comp_of_IOL47A	TRUE	16			36	36	16			16	R1
IOL49A	I/O	DQ3	6		True_of_IOL49B	TRUE	17					17			17	L3
IOL49B	I/O	DQ3	6		Comp_of_IOL49A	TRUE	18					18			18	L1
IOL51A	I/O	DQ3	6		True_of_IOL51B	TRUE	19					19			19	P2
IOL51B	I/O	DQ3	6		Comp_of_IOL51A	TRUE	20					20			20	P1
IOL53A	I/O	DQ3	6		True_of_IOL53B	TRUE				41	41					
IOL53B	I/O	DQ3	6		Comp_of_IOL53A	TRUE				42	42					

Note!
[1] Embeded with SDRAM.
[2] Embeded with PSRAM.

Pin Name	Function	DQS	BANK	Configuration Function	Differential Pair	LVDS	QN88[1]	LQ144[1]	EQ144[1]	LQ176[1]	EQ176[1]	QN88P[2]	EQ144P[2]	EQ144PF[2]	QN88PF[2]	PG256S[1]
BANK5 True LVDS Pair																
IOB12A	I/O	DQ5	5		True_of_IOB12B	TRUE		44	44	53	53		44	44		P4
IOB12B	I/O	DQ5	5		Comp_of_IOB12A	TRUE		45	45	54	54		45	45		T4
IOB14A	I/O	DQ5	5		True_of_IOB14B	TRUE	29	46	46	55	55	29	46	46	29	
IOB14B	I/O	DQ5	5		Comp_of_IOB14A	TRUE	30	47	47	56	56	30	47	47	30	
IOB16A	I/O	DQ5	5		True_of_IOB16B	TRUE										L8
IOB16B	I/O	DQ5	5		Comp_of_IOB16A	TRUE										L7
IOB18A	I/O	DQ5	5		True_of_IOB18B	TRUE	31			59	59	31			31	N5
IOB18B	I/O	DQ5	5		Comp_of_IOB18A	TRUE	32			60	60	32			32	P5
IOB20A	I/O	DQ5	5		True_of_IOB20B	TRUE		50	50				50	50		R5
IOB20B	I/O	DQ5	5		Comp_of_IOB20A	TRUE		51	51				51	51		T5
IOB22A	I/O	DQ5	5		True_of_IOB22B	TRUE		52	52				52	52		P6
IOB22B	I/O	DQ5	5		Comp_of_IOB22A	TRUE		54	54				54	54		T6
IOB24A	I/O	DQ5	5		True_of_IOB24B	TRUE	33					33			33	R7
IOB24B	I/O	DQ5	5		Comp_of_IOB24A	TRUE	34					34			34	T7
IOB26A	I/O	DQ5	5		True_of_IOB26B	TRUE										
IOB26B	I/O	DQ5	5		Comp_of_IOB26A	TRUE										
IOB2A	I/O	DQ4	5		True_of_IOB2B	TRUE										
IOB2B	I/O	DQ4	5		Comp_of_IOB2A	TRUE										
IOB4A	I/O	DQ4	5		True_of_IOB4B	TRUE										M4
IOB4B	I/O	DQ4	5		Comp_of_IOB4A	TRUE										M3
IOB6A	I/O	DQ4	5		True_of_IOB6B	TRUE	25	40	40	49	49	25	40	40	25	
IOB6B	I/O	DQ4	5		Comp_of_IOB6A	TRUE	26	41	41	50	50	26	41	41	26	
IOB8A	I/O	DQ4	5		True_of_IOB8B	TRUE	27			51	51	27			27	M6
IOB8B	I/O	DQ4	5		Comp_of_IOB8A	TRUE	28			52	52	28			28	N6

Note!
[1] Embeded with SDRAM.
[2] Embeded with PSRAM.

Pin Name	Function	DQS	BANK	Configuration Function	Differential Pair	LVDS	QN88[1]	LQ144[1]	EQ144[1]	LQ176[1]	EQ176[1]	QN88P[2]	EQ144P[2]	EQ144PF[2]	QN88PF[2]	PG256S[1]
BANK4 True LVDS Pair																
IOB30A/GCLKT_4	I/O	DQ6	4	GCLKT_4	True_of_IOB30B	TRUE	35	56	56	68	68	35	56	56	35	P8
IOB30B/GCLKC_4	I/O	DQ6	4	GCLKC_4	Comp_of_IOB30A	TRUE	36	57	57	69	69	36	57	57	36	T8
IOB32A	I/O	DQ6	4		True_of_IOB32B	TRUE										
IOB32B	I/O	DQ6	4		Comp_of_IOB32A	TRUE										
IOB34A	I/O	DQ6	4		True_of_IOB34B	TRUE	37	60	60	70	70	37	60	60	37	M9
IOB34B	I/O	DQ6	4		Comp_of_IOB34A	TRUE	38	61	61	71	71	38	61	61	38	N8
IOB36A	I/O	DQ6	4		True_of_IOB36B	TRUE										R9
IOB36B	I/O	DQ6	4		Comp_of_IOB36A	TRUE										T9
IOB38A	I/O	DQ6	4		True_of_IOB38B	TRUE		62	62	74	74		62	62		L10
IOB38B	I/O	DQ6	4		Comp_of_IOB38A	TRUE		63	63	75	75		63	63		M10
IOB40A	I/O	DQ6	4		True_of_IOB40B	TRUE	39	64	64	76	76	39	64	64	39	N9
IOB40B	I/O	DQ6	4		Comp_of_IOB40A	TRUE	40	65	65	77	77	40	65	65	40	P9
IOB42A	I/O	DQ6	4		True_of_IOB42B	TRUE		66	66	78	78		66	66		
IOB42B	I/O	DQ6	4		Comp_of_IOB42A	TRUE		67	67	79	79		67	67		
IOB44A	I/O	DQ6	4		True_of_IOB44B	TRUE				80	80					
IOB44B	I/O	DQ6	4		Comp_of_IOB44A	TRUE				81	81					
IOB48A	I/O	DQS7	4		True_of_IOB48B	TRUE		68	68	82	82		68	68		
IOB48B	I/O	DQS7	4		Comp_of_IOB48A	TRUE		69	69	83	83		69	69		
IOB50A	I/O	DQ7	4		True_of_IOB50B	TRUE				84	84					
IOB50B	I/O	DQ7	4		Comp_of_IOB50A	TRUE				85	85					
IOB52A	I/O	DQ7	4		True_of_IOB52B	TRUE										N12
IOB52B	I/O	DQ7	4		Comp_of_IOB52A	TRUE										P12
IOB54A	I/O	DQ7	4		True_of_IOB54B	TRUE										M12
IOB54B	I/O	DQ7	4		Comp_of_IOB54A	TRUE										M11

Note!
[1] Embeded with SDRAM.
[2] Embeded with PSRAM.

Pin Name	Function	DQS	BANK	Configuration Function	Differential Pair	LVDS	QN88[1]	LQ144[1]	EQ144[1]	LQ176[1]	EQ176[1]	QN88P[2]	EQ144P[2]	EQ144PF[2]	QN88PF[2]	PG256S[1]
BANK3 True LVDS Pair																
IOR29A/GCLKT_3	I/O	DQ9	3	GCLKT_3	True_of_IOR29B	TRUE										J13
IOR29B/GCLKC_3	I/O	DQ9	3	GCLKC_3	Comp_of_IOR29A	TRUE										K14
IOR31A/MODE2	I/O	DQ9	3	MODE2	True_of_IOR31B	TRUE		143	143	112	112		143	143		
IOR31B/RECONFIG_N	I/O	DQ9	3	RECONFIG_N	Comp_of_IOR31A	TRUE		20	20	108	108		20	20		
IOR33A/MI/D7	I/O	DQ9	3	MI/D7	True_of_IOR33B	TRUE	62	96	96	106	106	62	96	96	62	P10
IOR33B/MO/D6	I/O	DQ9	3	MO/D6	Comp_of_IOR33A	TRUE	61	95	95	105	105	61	95	95	61	T10
IOR35A/FASTRD_N/D3	I/O	DQ9	3	FASTRD_N/D3	True_of_IOR35B	TRUE		92	92	102	102		92	92		K12
IOR35B/SI/D2	I/O	DQ9	3	SI/D2	Comp_of_IOR35A	TRUE		90	90	101	101		90	90		K11
IOR38A/DIN/CLKHOLD_N	I/O	DQ9	3	DIN/CLKHOLD_N	True_of_IOR38B	TRUE	54	86	86	98	98	54	86	86	54	J14
IOR38B/DOUT/WE_N	I/O	DQ9	3	DOUT/WE_N	Comp_of_IOR38A	TRUE	53	85	85	97	97	53	85	85	53	J16
IOR40A	I/O	DQ9	3		True_of_IOR40B	TRUE										K15
IOR40B	I/O	DQ9	3		Comp_of_IOR40A	TRUE										K16
IOR42A	I/O	DQ9	3		True_of_IOR42B	TRUE		84	84				84	84		M15
IOR42B	I/O	DQ9	3		Comp_of_IOR42A	TRUE		83	83				83	83		M16
IOR44A	I/O	DQ9	3		True_of_IOR44B	TRUE										
IOR44B	I/O	DQ9	3		Comp_of_IOR44A	TRUE										
IOR47A/RPLL2_T_fb	I/O	DQ8	3	RPLL2_T_fb	True_of_IOR47B	TRUE										R15
IOR47B/RPLL2_C_fb	I/O	DQ8	3	RPLL2_C_fb	Comp_of_IOR47A	TRUE										R16
IOR49A	I/O	DQ8	3		True_of_IOR49B	TRUE	49	80	80			49	80	80	49	R14
IOR49B	I/O	DQ8	3		Comp_of_IOR49A	TRUE	48	79	79			48	79	79	48	T15
IOR51A	I/O	DQ8	3		True_of_IOR51B	TRUE										L12
IOR51B	I/O	DQ8	3		Comp_of_IOR51A	TRUE										L13
IOR53A	I/O	DQ8	3		True_of_IOR53B	TRUE										R12
IOR53B	I/O	DQ8	3		Comp_of_IOR53A	TRUE										T12

Note!
[1] Embeded with SDRAM.
[2] Embeded with PSRAM.

Pin Name	Function	DQS	BANK	Configuration Function	Differential Pair	LVDS	QN88[1]	LQ144[1]	EQ144[1]	LQ176[1]	EQ176[1]	QN88P[2]	EQ144P[2]	EQ144PF[2]	QN88PF[2]	PG256S[1]
BANK2 True LVDS Pair																
IOR11A	I/O	DQ10	2		True_of_IOR11B	TRUE										C15
IOR11B	I/O	DQ10	2		Comp_of_IOR11A	TRUE										C16
IOR13A	I/O	DQ10	2		True_of_IOR13B	TRUE										F15
IOR13B	I/O	DQ10	2		Comp_of_IOR13A	TRUE										F16
IOR15A	I/O	DQ10	2		True_of_IOR15B	TRUE										
IOR15B	I/O	DQ10	2		Comp_of_IOR15A	TRUE										
IOR17A	I/O	DQ10	2		True_of_IOR17B	TRUE										
IOR17B	I/O	DQ10	2		Comp_of_IOR17A	TRUE										
IOR20A	I/O	DQ10	2		True_of_IOR20B	TRUE		102	102	125	125		102	102		H13
IOR20B	I/O	DQ10	2		Comp_of_IOR20A	TRUE		101	101	124	124		101	101		H14
IOR22A	I/O	DQS10	2		True_of_IOR22B	TRUE		100	100	123	123		100	100		
IOR22B	I/O	DQS10	2		Comp_of_IOR22A	TRUE		99	99	122	122		99	99		
IOR24A	I/O	DQ10	2		True_of_IOR24B	TRUE										
IOR24B	I/O	DQ10	2		Comp_of_IOR24A	TRUE										
IOR26A/TCK	I/O	DQ10	2	TCK	True_of_IOR26B	TRUE	6	14	14	120	120	6	14	14	6	C14
IOR26B/TDI	I/O	DQ10	2	TDI	Comp_of_IOR26A	TRUE	7	16	16	117	117	7	16	16	7	C12
IOR2A	I/O	DQ11	2		True_of_IOR2B	TRUE										E13
IOR2B	I/O	DQ11	2		Comp_of_IOR2A	TRUE										E12
IOR4A	I/O	DQ11	2		True_of_IOR4B	TRUE										B15
IOR4B	I/O	DQ11	2		Comp_of_IOR4A	TRUE										B16
IOR6A	I/O	DQS11	2		True_of_IOR6B	TRUE										
IOR6B	I/O	DQS11	2		Comp_of_IOR6A	TRUE										
IOR8A/RPLL1_T_fb	I/O	DQ11	2	RPLL1_T_fb	True_of_IOR8B	TRUE										F13
IOR8B/RPLL1_C_fb	I/O	DQ11	2	RPLL1_C_fb	Comp_of_IOR8A	TRUE										F14

Note!
[1] Embeded with SDRAM.
[2] Embeded with PSRAM.

Pin Name	Function	DQS	BANK	Configuration Function	Differential Pair	LVDS	QN88[1]	LQ144[1]	EQ144[1]	LQ176[1]	EQ176[1]	QN88P[2]	EQ144P[2]	EQ144PF[2]	QN88PF[2]	PG256S[1]
BANK1 True LVDS Pair																
IOT30A/GCLKT_1	I/O	DQ13	1	GCLKT_1	True_of_IOT30B	TRUE	77	121	121	152	152	77	121	121	77	E7
IOT30B/GCLKC_1	I/O	DQ13	1	GCLKC_1	Comp_of_IOT30A	TRUE	76	120	120	151	151	76	120	120	76	E8
IOT32A	I/O	DQ13	1		True_of_IOT32B	TRUE										E10
IOT32B	I/O	DQ13	1		Comp_of_IOT32A	TRUE										C10
IOT34A	I/O	DQ13	1		True_of_IOT34B	TRUE	75					75			75	
IOT34B	I/O	DQ13	1		Comp_of_IOT34A	TRUE	74					74			74	
IOT36A	I/O	DQ13	1		True_of_IOT36B	TRUE										
IOT36B	I/O	DQ13	1		Comp_of_IOT36A	TRUE										
IOT38A	I/O	DQ13	1		True_of_IOT38B	TRUE		119	119	148	148		119	119		
IOT38B	I/O	DQ13	1		Comp_of_IOT38A	TRUE		118	118	147	147		118	118		
IOT40A	I/O	DQ13	1		True_of_IOT40B	TRUE	73	117	117	146	146	73	117	117	73	D8
IOT40B	I/O	DQ13	1		Comp_of_IOT40A	TRUE	72	116	116	145	145	72	116	116	72	C8
IOT42A	I/O	DQ13	1		True_of_IOT42B	TRUE		115	115	144	144		115	115		C11
IOT42B	I/O	DQ13	1		Comp_of_IOT42A	TRUE		114	114	143	143		114	114		A11
IOT44A	I/O	DQ13	1		True_of_IOT44B	TRUE	71			142	142	71			71	F9
IOT44B	I/O	DQ13	1		Comp_of_IOT44A	TRUE	70			141	141	70			70	D9
IOT48A	I/O	DQS12	1		True_of_IOT48B	TRUE		113	113	140	140		113	113		B12
IOT48B	I/O	DQS12	1		Comp_of_IOT48A	TRUE		112	112	139	139		112	112		A12
IOT50A	I/O	DQ12	1		True_of_IOT50B	TRUE		111	111	138	138		111	111		C13
IOT50B	I/O	DQ12	1		Comp_of_IOT50A	TRUE		110	110	137	137		110	110		A13
IOT52A	I/O	DQ12	1		True_of_IOT52B	TRUE				136	136					F10
IOT52B	I/O	DQ12	1		Comp_of_IOT52A	TRUE				135	135					E11
IOT54A	I/O	DQ12	1		True_of_IOT54B	TRUE										B14
IOT54B	I/O	DQ12	1		Comp_of_IOT54A	TRUE										A14

Note!
[1] Embeded with SDRAM.
[2] Embeded with PSRAM.

Pin Name	Function	DQS	BANK	Configuration Function	Differential Pair	LVDS	QN88[1]	LQ144[1]	EQ144[1]	LQ176[1]	EQ176[1]	QN88P[2]	EQ144P[2]	EQ144PF[2]	QN88PF[2]	PG256S[1]
BANK0 True LVDS Pair																
IOT12A	I/O	DQ14	0		True_of_IOT12B	TRUE		134	134	169	169		134	134		B6
IOT12B	I/O	DQ14	0		Comp_of_IOT12A	TRUE		133	133	168	168		133	133		A6
IOT14A	I/O	DQ14	0		True_of_IOT14B	TRUE		132	132	167	167		132	132		F7
IOT14B	I/O	DQ14	0		Comp_of_IOT14A	TRUE		131	131	166	166		131	131		E6
IOT16A	I/O	DQ14	0		True_of_IOT16B	TRUE				165	165					C7
IOT16B	I/O	DQ14	0		Comp_of_IOT16A	TRUE				164	164					A7
IOT18A	I/O	DQ14	0		True_of_IOT18B	TRUE				163	163					D6
IOT18B	I/O	DQ14	0		Comp_of_IOT18A	TRUE				162	162					C6
IOT20A	I/O	DQ14	0		True_of_IOT20B	TRUE										
IOT20B	I/O	DQ14	0		Comp_of_IOT20A	TRUE										
IOT22A	I/O	DQ14	0		True_of_IOT22B	TRUE										B8
IOT22B	I/O	DQ14	0		Comp_of_IOT22A	TRUE										A8
IOT24A	I/O	DQ14	0		True_of_IOT24B	TRUE				159	159					C9
IOT24B	I/O	DQ14	0		Comp_of_IOT24A	TRUE				158	158					A9
IOT26A	I/O	DQ14	0		True_of_IOT26B	TRUE										
IOT26B	I/O	DQ14	0		Comp_of_IOT26A	TRUE										
IOT2A	I/O	DQ15	0		True_of_IOT2B	TRUE										C4
IOT2B	I/O	DQ15	0		Comp_of_IOT2A	TRUE										A4
IOT4A	I/O	DQ15	0		True_of_IOT4B	TRUE	86	140	140			86	140	140	86	B5
IOT4B	I/O	DQ15	0		Comp_of_IOT4A	TRUE	85	139	139			85	139	139	85	A5
IOT6A	I/O	DQ15	0		True_of_IOT6B	TRUE	84	138	138	173	173	84	138	138	84	
IOT6B	I/O	DQ15	0		Comp_of_IOT6A	TRUE	83	137	137	172	172	83	137	137	83	
IOT8A	I/O	DQ15	0		True_of_IOT8B	TRUE										
IOT8B	I/O	DQ15	0		Comp_of_IOT8A	TRUE										

Note!
It is recommended to connect VCCX to the VCCO with the Max. voltage.

Recommended Operating Conditions for GW2AR-18 LQ144/EQ144/QN88 Packages embeded with SDR SDRAM			
Name	**Description**	**Min.**	**Max.**
VCC	Core voltage	0.95V	1.05V
VCCPLLL0/1	Left PLL 0/1 power supply; VCC/VCCPLLL1 of LQ144 package are internal short circuited	0.95V	1.05V
VCCPLLR0/1	Right PLL 0/1 power supply	0.95V	1.05V
VCCO0, VCCO1, VCCO4, VCCO5	I/O Bank Power	1.14V	3.465V
VCCO2, VCCO3, VCCO6, VCCO7	I/O Bank Power, connected to SDR SDRAM interface	3.135V	3.465V
VCCX/VCCO2/VCCO6/VCCO7	VCCX, VCCO2, VCCO7, providing voltage for SDR SDRAM, and VCCX/VCCO2/VCCO6/VCCO7 are internal short circuited	3.315V	3.465V

Recommended Operating Conditions for GW2AR-18 LQ176 Package embeded with DDR SDRAM			
Name	**Description**	**Min.**	**Max**
VCC	Core voltage	0.95V	1.05V
VCCPLLL0/1	Left PLL 0/1 power supply	0.95V	1.05V
VCCPLLR0/1	Right PLL 0/1 power supply	0.95V	1.05V
VCCO0, VCCO1, VCCO4, VCCO5	I/O Bank Power	1.14V	3.465V
VCCO2, VCCO3, VCCO6, VCCO7	I/O Bank Power, connected to DDR SDRAM interface, providing voltage for DDR SDRAM	2.3V	2.7V
VCCX	Auxiliary voltage	2.7V	3.465V

Recommended Operating Conditions for GW2AR-18 QN88P Package embeded with PSRAM			
Name	**Description**	**Min.**	**Max.**
VCC	Core voltage	0.95V	1.05V
VCCPLLL0/1	Left PLL 0/1 power supply	0.95V	1.05V
VCCPLLR0/1	Right PLL 0/1 power supply	0.95V	1.05V
VCCO0, VCCO3, VCCO4, VCCO5	I/O Bank Power	1.14V	3.465V
VCCO2/7	I/O Bank Power, connected to PSRAMinterface, VCCO2/VCCO7 provides working voltage for PSRAM	1.71V	1.89V
VCCX/VCCO1/VCCO6	VCCX/VCCO1/VCCO6 are internal short circuited	2.7V	3.465V

Note! It is recommended to connect VCCX to the VCCO with the Max. voltage.			
Recommended Operating Conditions for GW2AR-18 EQ144P Package embeded with PSRAM			
Name	**Description**	**Min.**	**Max.**
VCC	Core voltage	0.95V	1.05V
VCCPLLL0/1	Left PLL 0/1 power supply	0.95V	1.05V
VCCPLLR0/1	Right PLL 0/1 power supply	0.95V	1.05V
VCCO0, VCCO1, VCCO3, VCCO5	I/O Bank Power	1.14V	3.465V
VCCO2/7	I/O Bank Power, connected to PSRAM interface, VCCO2/VCCO7 provides PSRAM voltage	1.71V	1.89V
VCCX/VCCO4/VCCO6	VCCX/VCCO4/VCCO6 are internal short circuited.	2.7V	3.465V
Recommended Operating Conditions for GW2AR-18 EQ144PF Package embeded with PSRAM			
Name	**Description**	**Min.**	**Max.**
VCC	Core voltage	0.95V	1.05V
VCCPLLL0/1	Left PLL 0/1 power supply	0.95V	1.05V
VCCPLLR0/1	Right PLL 0/1 power supply	0.95V	1.05V
VCCO0, VCCO1, VCCO2, VCCO3, VCCO5	I/O Bank Power	1.14V	3.465V
VCCO7	I/O Bank power, connected to PSRAM interface, VCCO7 provides PSRAM voltage	1.71V	1.89V
VCCX/VCCO4/VCCO6	VCCX/VCCO4/VCCO6 are internal short circuited.	2.7V	3.465V
Recommended Operating Conditions for GW2AR-18 QN88PF Package embeded with PSRAM			
Name	**Description**	**Min.**	**Max.**
VCC	Core voltage	0.95V	1.05V
VCCPLLL0/1	Left PLL 0/1 power supply	0.95V	1.05V
VCCPLLR0/1	Right PLL 0/1 power supply	0.95V	1.05V
VCCO0, VCCO2, VCCO3, VCCO4, VCCO5	I/O Bank Power	1.14V	3.465V
VCCO7	I/O Bank Power, connected to PSRAM interface, VCCO7 provides PSRAM voltage	1.71V	1.89V
VCCX/VCCO1/VCCO6	VCCX/VCCO1/VCCO6 are internal short circuited	3.315V	3.465V

Note!
It is recommended to connect VCCX to the VCCO with the Max. voltage.

Recommended Operating Conditions for GW2AR-18 PG256S Package embeded with SDR PSRAM			
Name	**Description**	**Min.**	**Max.**
VCC	Core voltage	0.95V	1.05V
VCCPLLL	Left PLL power supply	0.95V	1.05V
VCCPLLR	Right PLL power supply	0.95V	1.05V
VCCO0, VCCO1, VCCO4, VCCO5	I/O Bank Power	1.14V	3.465V
VCCO2, VCCO3, VCCO6, VCCO7, VCCX	Auxiliary voltage and I/O Bank power supply voltage are short-circuited with DDR SDRAM interface to provide voltage for SDR SDRAM	3.135V	3.465V