GOWIN
PROGRAMMING FOR THE FUTURE

GW2AR series of FPGA Products

Package & Pinout User Guide

UG229-1.4E, 05/14/2021

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Revision History

Date	Version	Description
05/11/2018	1.06E	Initial version published.
09/10/2018	1.07E	For the QN88 and LQ144 packages, VCCX connects with VCCO7.
11/20/2018	1.08E	● LCDS pair added in Table 2-1; ● The EQ144 package added; ● Packages of devices embedded with PSRAM added.
01/10/2019	1.09E	Introduction to the I/O BANK updated.
03/27/2019	1.1E	The EQ176 package added.
03/10/2020	1.2E	A note for the Max. user I/O added.
06/30/2020	1.2.1E	The package name of QN88/EQ144 (PSRAM embedded) updated to QN88P/EQ144P.
08/07/2020	1.3E	QN88PF and EQ144PF added.
05/14/2021	1.4E	PG256S added.

Contents

List of Figures

List of Tables

1 About This Guide

1.1 Purpose

This manual contains an introduction to the GW2AR series of FPGA products together with a definition of the pins, list of pin numbers, distribution of pins, and package diagrams.

1.2 Related Documents

The latest user guides are available on GOWINSEMI Website. You can find the related documents at www.gowinsemi.com:

1. DS226, GW2AR series of FPGA Products Data Sheet
2. UG290, Gowin FPGA Products Programming and Configuration User Guide
3. UG115, GW2AR-18 Pinout

1.3 Abbreviations and Terminology

The abbreviations and terminologies used in this manual are delineated in Table 1-1 below.

Table 1-1 Abbreviations and Terminology

Abbreviations and Terminology	Name
FPGA	Field Programmable Gate Array
QN88	QFN88
LQ144	LQFP144
EQ144	eLQFP144
LQ176	LQFP176
EQ176	eLQFP176
EQ144P	eLQFP144P
QN88P	QFN88P
EQ144PF	eLQFP144PF
QN88PF	QFN88PF
PG256S	PBGA256S

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Overview

The GW2AR series of FPGA products are the first generation products of Arora family, and they are one kind of SIP chip. Compared with GW2A series, the difference is that GW2AR series of integrates abundant SDRAM. GW2AR series of products also provide the high-performance DSP resources, high-speed LVDS interface, and abundant BSRAM memory resources. These embedded resources with a streamlined FPGA architecture and 55nm process make GW2AR series of FPGA products suitable for high-speed and low-cost applications.

GOWINSEMI provides a new generation of FPGA hardware development environment through the market-oriented independent research and development. This supports GW2AR series of FPGA products and applies to FPGA synthesizing, layout, place and routing, data bitstream generation and download, etc.

2.1 PB-Free Package

The GW2AR series of FPGA Products are PB free in line with the EU RoHS environmental directives. The substances used in the GW2AR series of FPGA products are in full compliance with the IPC-1752 standards.

2.2 Max. I/O Information and LVDS Pair

Table 2-1 Max. I/O Information and LVDS Pair

Package	Pitch (mm)	Size (mm)	E-pad Size(mm)	GW2AR-18
LQ144	0.5	20 x 20	-	120(35)
EQ144	0.5	20 x 20	9.74 x 9.74	120(35)
EQ144P	0.5	20 x 20	9.74 x 9.74	120(35)
EQ144PF	0.5	20 x 20	9.74 x 9.74	120(35)
QN88	0.4	10 x 10	6.74 x 6.74	66(22)
QN88P	0.4	10 x 10	6.74 x 6.74	66(22)
QN88PF	0.4	10 x 10	6.74 x 6.74	66(22)
LQ176	0.4	20 x 20	-	140(45)
EQ176	0.4	20 x 20	6 x 6	140(45)
PG256S	1.0	17 x 17	-	192(62)

Note!

- The package types in this manual are written with abbreviations. See 1.3 Abbreviations and Terminology；
- The JTAGSEL_N and JTAG pins cannot be used as I/O simultaneously. The data in this table is when the loaded four JTAG pins (TCK, TDI, TDO, and TMS) are used as I/O.

2.3 Power Pin

Table 2-2 GW2AR Power Pin

VCC	VCCO0	VCCO1	VCCO2
VCCO3	VCCO4	VCCO5	VCCO6
VCCO7	VCCX	VSS	NC
VCCPLLL0	VCCPLLL1	VCCPLLR0	VCCPLLR1

2.4 Pin Quantity

Table 2-3 Quantity of GW2AR-18 Pins (Devices Embedded With SDRAM)

Pin Type		GW2AR-18					
		QN88	LQ144	EQ144	LQ176	EQ176	PG256S
I/O Single ended/Differential pair/LVDS[1]	BANK0	8/4/2	19/8/4	19/8/4	19/9/6	19/9/6	20/10/8
	BANK1	9/4/4	12/6/6	12/6/6	18/9/8	18/9/8	19/9/9
	BANK2	4/2/1	12/6/3	12/6/3	12/5/3	12/5/3	30/15/7
	BANK3	17/6/3	24/11/6	24/11/6	20/8/4	20/8/4	37/18/10
	BANK4	8/3/3	17/8/6	17/8/6	19/9/8	19/9/8	16/7/7
	BANK5	10/5/5	16/8/5	16/8/5	18/8/5	18/8/5	18/9/8
	BANK6	9/4/4	12/6/3	12/6/3	17/8/6	17/8/6	24/12/6
	BANK7	1/0/0	8/4/2	8/4/2	17/6/5	17/6/5	28/14/7
Max. User I/O[2]		66	120	120	140	140	192
Differential Pair		28	57	57	62	62	94
True LVDS Output		22	35	35	45	45	62
VCC		4	0	0	4	4	6
VCC/VCCPLLL1[3]		0	4	4	0	0	0
VCCX		0	0	0	4	4	0
VCCX/ VCCO2/ VCCO6/VCCO7[3]		3	4	4	0	0	0
VCCO2/VCCO3/VCCO6/VCCO7		0	0	0	8	8	0
VCCX/ VCCO2/VCCO3/VCCO6/VCCO7		0	0	0	0	0	19
VCCO0		1	1	1	2	2	3
VCCO1		1	1	1	2	2	2
VCCO2		0	0	0	0	0	0
VCCO3		1	2	2	0	0	0
VCCO4		1	1	1	2	2	2
VCCO5		1	1	1	2	2	2
VCCO6		0	0	0	0	0	0
VCCO7		0	0	0	0	0	0
VCCPLLL0		0	1	1	0	0	0
VCCPLLL1		1	0	0	1	1	0
VCCPLLR0		0	1	1	1	1	0
VCCPLLR1		1	1	1	1	1	0
VCCPLLL		0	0	0	0	0	1
VCCPLLR		0	0	0	0	0	1
VSS		7	6	6	8	8	26
MODE0		1	1	1	1	1	1
MODE1		1	1	1	1	1	1
MODE2		0	1	1	1	1	0

Pin Type	GW2AR-18					
	QN88	LQ144	EQ144	LQ176	EQ176	PG256S
EXTR	1	1	1	1	1	0
JTAGSEL_N	0	0	0	0	0	1
NC	0	0	0	0	0	1

Table 2-4 Quantity of GW2AR-18 Pins (Devices Embedded With PSRAM)

Pin Type		GW2AR-18			
		QN88P	EQ144P	QN88PF	EQ144PF
I/O Single end / Differential pair[1]	BANK0	8/4/2	19/8/4	8/4/2	19/8/4
	BANK1	9/4/4	12/6/6	9/4/4	12/6/6
	BANK2	4/2/1	12/6/3	4/2/1	12/6/3
	BANK3	17/6/3	24/11/6	17/6/3	24/11/6
	BANK4	8/3/3	17/8/6	8/3/3	17/8/6
	BANK5	10/5/5	16/8/5	10/5/5	16/8/5
	BANK6	9/4/4	12/6/3	9/4/4	12/6/3
	BANK7	1/0/0	8/4/2	1/0/0	8/4/2
Max. User I/O [2]		66	120	66	120
Differential Pair		28	57	28	57
True LVDS output		22	35	22	35
VCC		4	0	4	0
VCC/VCCPLLL1[3]		0	4	0	4
VCCX		0	0	0	0
VCCX/VCCO1/VCCO6[3]		2	0	2	0
VCCX/VCCO4/VCCO6[3]		0	2	0	2
VCCO2/VCCO7[3]		2	3	0	0
VCCO0		1	1	1	1
VCCO1		0	1	0	1
VCCO2		0	0	1	1
VCCO3		1	2	1	2
VCCO4		1	0	1	0
VCCO5		1	1	1	1
VCCO6		0	0	0	0
VCCO7		0	0	1	2
VCCPLLL0		0	1	0	1
VCCPLLL1		1	0	1	0
VCCPLLR0		0	1	0	1
VCCPLLR1		1	1	1	1
VSS		7	6	7	6
MODE0		1	1	1	1

Pin Type	GW2AR-18			
	QN88P	EQ144P	QN88PF	EQ144PF
MODE1	1	1	1	1
MODE2	0	1	0	1
EXTR	1	1	1	1
JTAGSEL_N	0	0	0	0

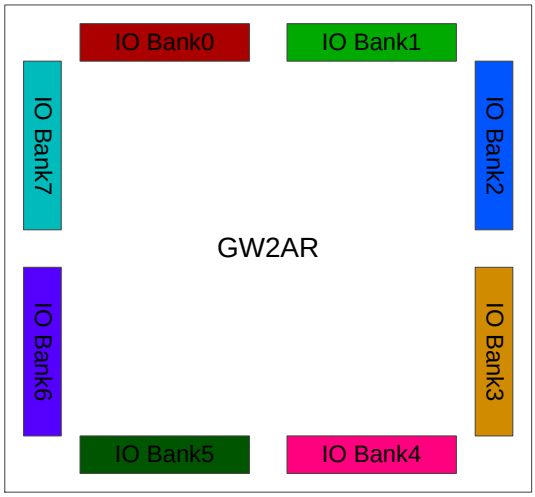
Note!

- [1] Single end/ Differential/LVDS I/O quantity include CLK pins, and download pins;
- [2] JTAGSEL_N and JTAG pins cannot be used as I/O simultaneously. The data in this table is when the loaded four JTAG pins (TCK, TDI, TDO, and TMS) are used as I/O;
- [3]Pin multiplexing;

2.5 Introduction to the I/O BANK

There are eight I/O Banks in the GW2AR series of FPGA products, as shown in Figure 2-1.

Figure 2-1 GW2AR I/O Bank Distribution



This manual provides an overview of the distribution view of the pins in the GW2AR series of FPGA products. Eight IO Banks in GW2AR series of FPGA products are marked with eight different colors.

User I/O, power, and ground are also marked with different symbols and colors. The different symbols and colors used for different pins are defined as follows:

- " " denotes I/Os in BANK0. The filling color changes with the BANK;
- " " denotes I/Os in BANK1. The filling color changes with the BANK;
- " " denotes I/Os in BANK2. The filling color changes with the BANK;
- " " denotes I/Os in BANK3. The filling color changes with the BANK;
- " " denotes I/Os in BANK4. The filling color changes with the BANK;
- " " denotes I/Os in BANK5. The filling color changes with the BANK;
- " " denotes I/Os in BANK6. The filling color changes with the BANK;
- " " denotes I/Os in BANK7. The filling color changes with the BANK;
- " " denotes VCC, VCCX, and VCCO. The filling color does not change;
- " " denotes VSS. The filling color does not change;
- " M " denotes MODE;
- " " denotes NC;
- " E " denotes dedicated pins EXTR.

3 View of Pin Distribution

3.1 GW2AR-18 Pins Distribution View

3.1.1 View of QN88 Pins Distribution (Embedded with SDRAM)

Figure 3-1 View of GW2AR-18 QN88 Pins Distribution (Embedded with SDRAM)

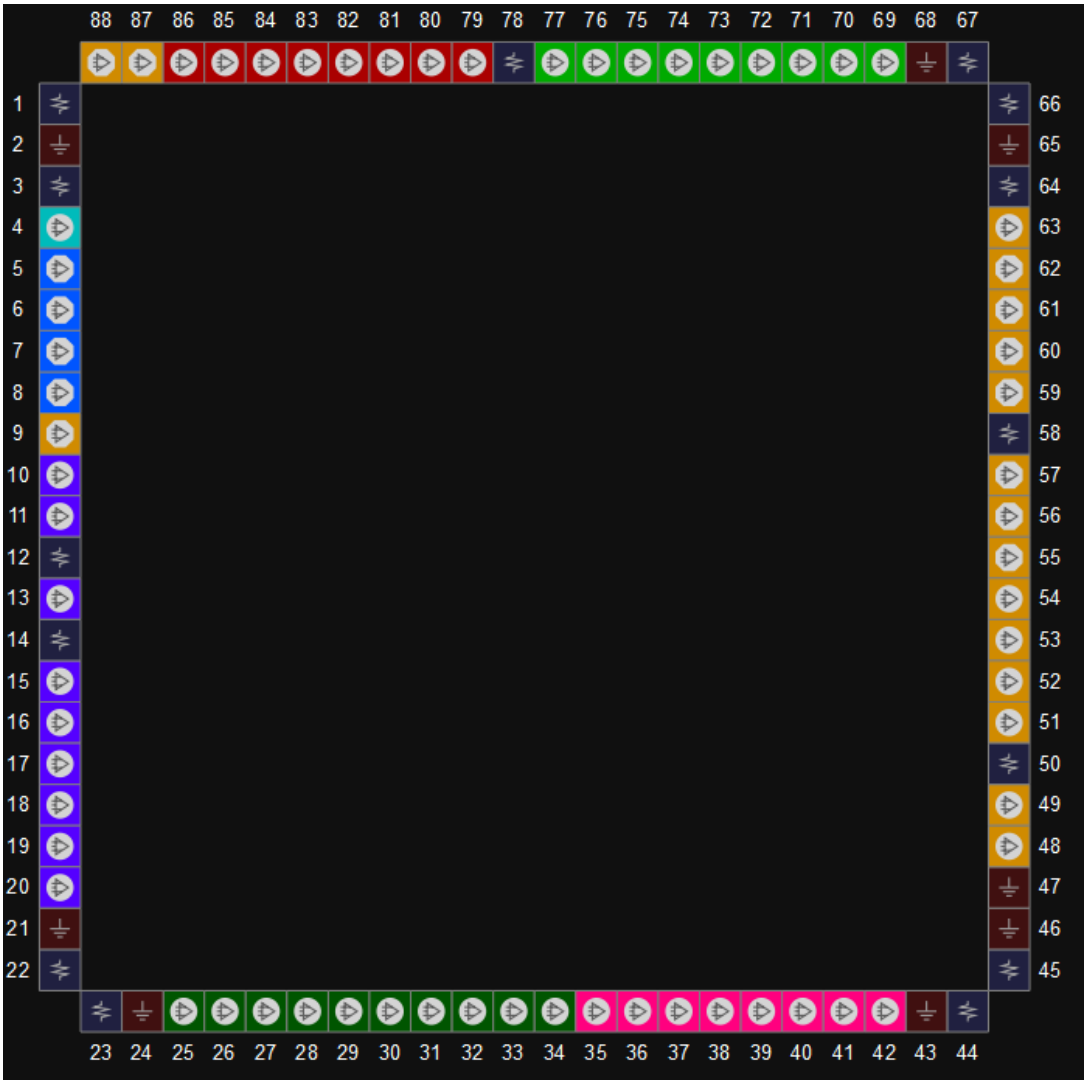


Table 3-1 Other pins in GW2AR-18 QN88 (Embedded with SDRAM)

VCC	1, 22, 45, 66
VCCO0	78
VCCO1	67
VCCO3	58
VCCO4	44
VCCO5	23
VCCX/ VCCO2/ VCCO6/ VCCO7	3,12, 64
VCCPLLL1	14
VCCPLLR1	50
VSS	2, 21, 24, 43, 46, 65, 68
EXTR	47
MODE	87, 88

3.1.2 View of QN88P Pins Distribution (Embedded with PSRAM)

Figure 3-2 View of GW2AR-18 QN88P Pins Distribution (Embedded with PSRAM)

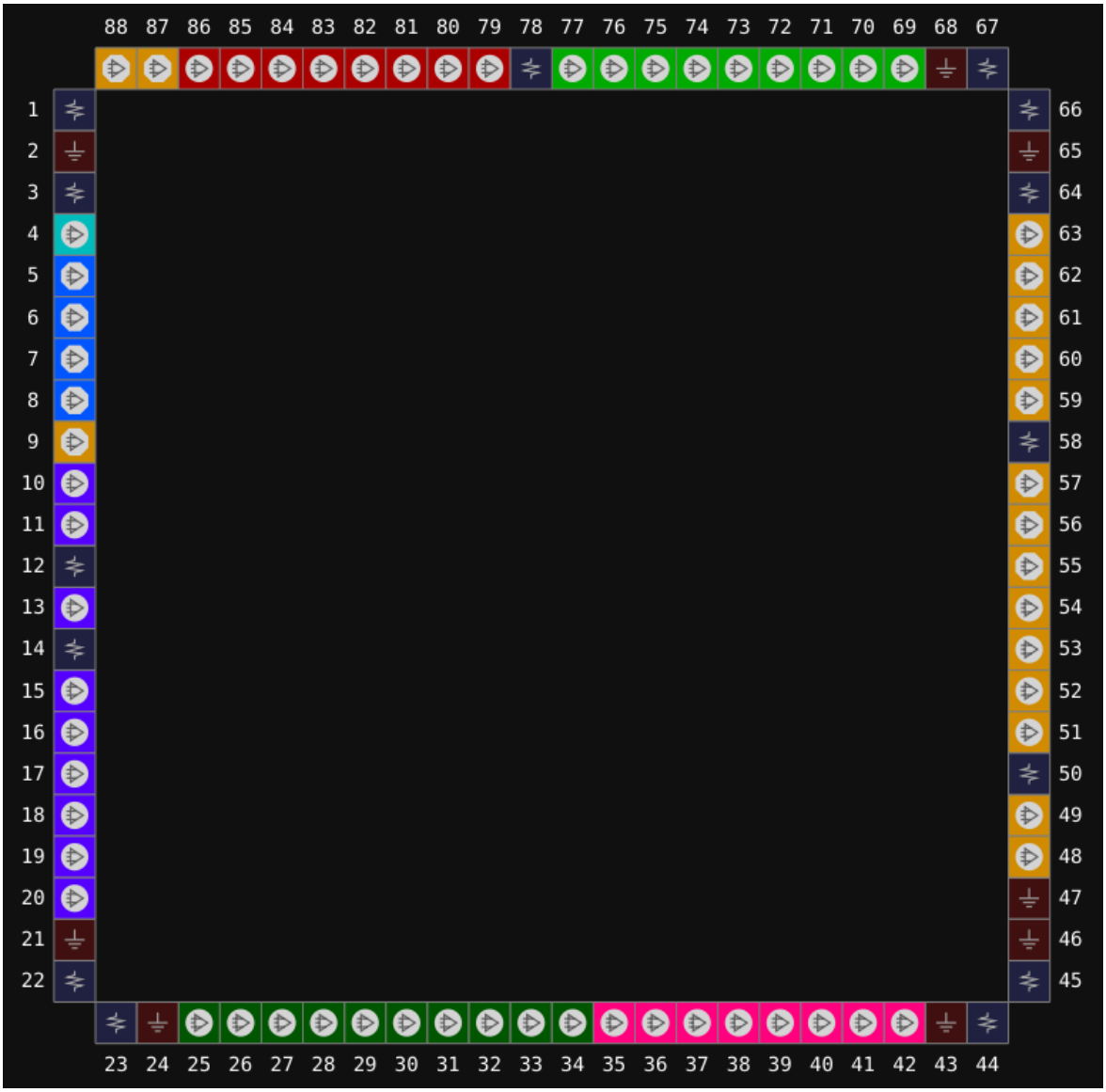


Table 3-2 Other pins in GW2AR-18 QN88P (Embedded with PSRAM)

VCC	1, 22, 45, 66
VCCO0	78
VCCO2/VCCO7	3，64
VCCO3	58
VCCO4	44
VCCO5	23
VCCX/VCCO1/VCCO6	12, 67
VCCPLLL1	14
VCCPLLR1	50
VSS	2, 21, 24, 43, 46, 65, 68
EXTR	47
MODE	87, 88

3.1.3 View of QN88PF Pins Distribution (Embedded with PSRAM)

Figure 3-3 View of GW2AR-18 QN88PF Pins Distribution (Embedded with PSRAM)

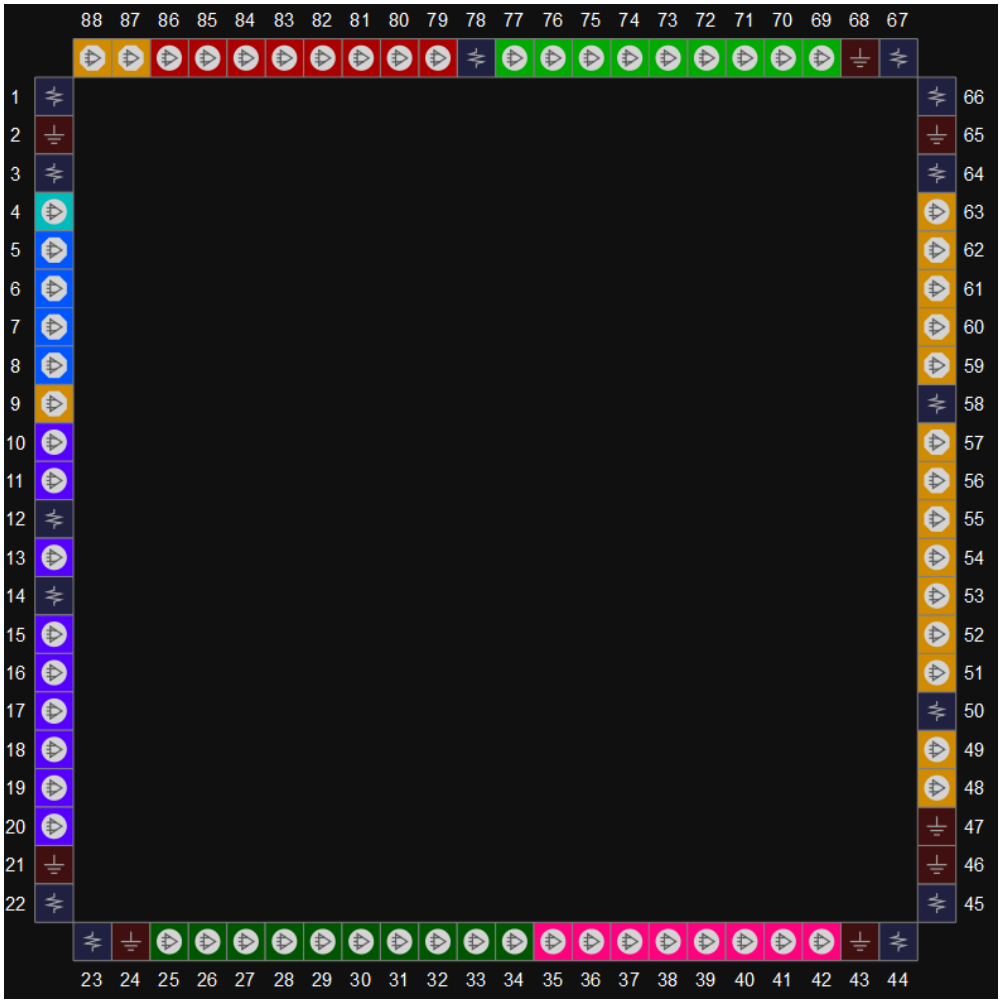


Table 3-3 Other pins in GW2AR-18 QN88PF (Embedded with PSRAM)

VCC	1, 22, 45, 66
VCCO0	78
VCCO2	64
VCCO3	58
VCCO4	44
VCCO5	23
VCCO7	3
VCCX/VCCO1/VCCO6	12, 67
VCCPLLL1	14
VCCPLLR1	50
VSS	2, 21, 24, 43, 46, 65, 68
EXTR	47
MODE	87, 88

3.1.4 View of LQ144/EQ144 Pins Distribution (Embedded with SDRAM)

Figure 3-4 GW2AR-18 LQ144/EQ144 Pins Distribution View (Embedded with SDRAM)

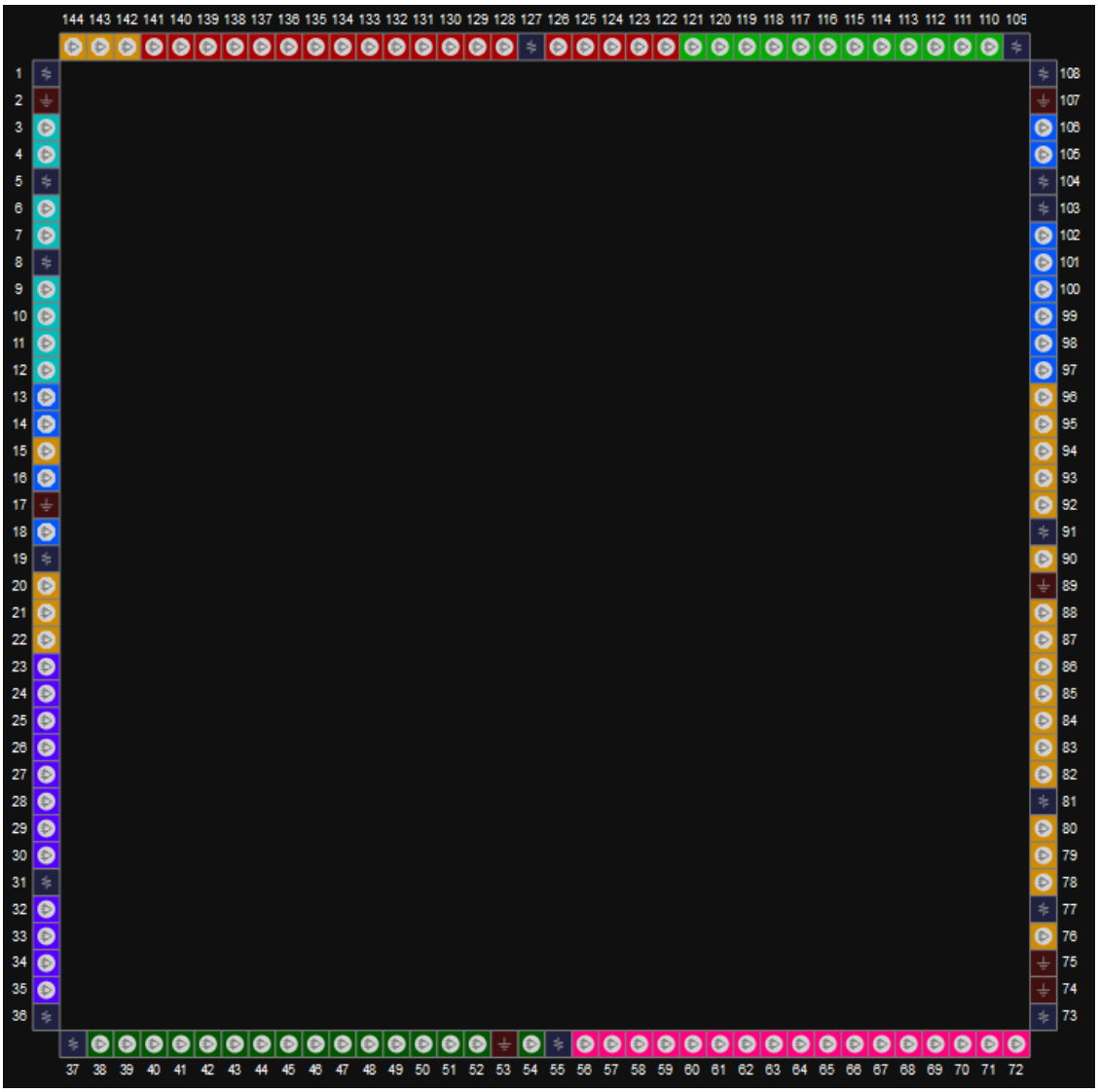


Table 3-4 Other pins in GW2AR-18 LQ144/EQ144 (Embedded with SDRAM)

VCC/VCCPLLL1	1, 36, 73, 108
VCCO0	127
VCCO1	109
VCCO3	77, 91
VCCO4	55
VCCO5	37
VCCX/ VCCO2/ VCCO6/ VCCO7	5,19,31,103
VCCPLLL0	8
VCCPLLR0	104
VCCPLLR1	81
VSS	2, 17, 53, 74, 89, 107
EXTR	75
MODE	142, 143, 144

3.1.5 View of EQ144P Pins Distribution (Embedded with PSRAM)

Figure 3-5 GW2AR-18 EQ144P Pins Distribution View (Embedded with PSRAM)

Table 3-5 Other pins in GW2AR-18 EQ144P (Embedded with PSRAM)

VCC/VCCPLLL1	1, 36, 73, 108
VCCO0	127
VCCO1	109
VCCO3	77, 91
VCCO5	37
VCCO2/VCCO7	5,19,103
VCCX/VCCO4/VCCO6	31,55
VCCPLLL0	8
VCCPLLR0	104
VCCPLLR1	81
VSS	2, 17, 53, 74, 89, 107
EXTR	75
MODE	142, 143, 144

3.1.6 View of EQ144PF Pins Distribution (Embedded with PSRAM)

Figure 3-6 GW2AR-18 EQ144PF Pins Distribution View (Embedded with PSRAM)

Table 3-6 Other pins in GW2AR-18 EQ144PF (Embedded with PSRAM)

VCC/VCCPLLL1	1, 36, 73, 108
VCCO0	127
VCCO1	109
VCCO2	103
VCCO3	77, 91
VCCO5	37
VCCO7	5,19
VCCX/VCCO4/VCCO6	31,55
VCCPLLL0	8
VCCPLLR0	104
VCCPLLR1	81
VSS	2, 17, 53, 74, 89, 107
EXTR	75
MODE	142, 143, 144

3.1.7 View of LQ176/EQ176 Pins Distribution (Embedded with SDRAM)

Figure 3-7 GW2AR-18 LQ176/EQ176 Pins Distribution View (Embedded with SDRAM)

Table 3-7 Other pins in GW2AR-18 LQ176/EQ176 (Embedded with SDRAM)

VCC	1, 44, 89, 132
VCCO0	155, 176
VCCO1	133, 153
VCCO4	67, 88
VCCO5	45, 65
VCCX	23, 66, 115, 154
VCCO2/VCCO3/VCCO6/VCCO7	5,13,22,40,95,110,130
VCCPLLL1	34
VCCPLLR0	127
VCCPLLR1	94

VSS	2, 43, 46, 87, 90, 131, 134, 175
EXTR	91
MODE	111, 112, 113

3.1.8 View of PG256S Pins Distribution (Embedded with SDRAM)

Figure 3-8 GW2AR-18 PG256S Pins Distribution View (Embedded with SDRAM)

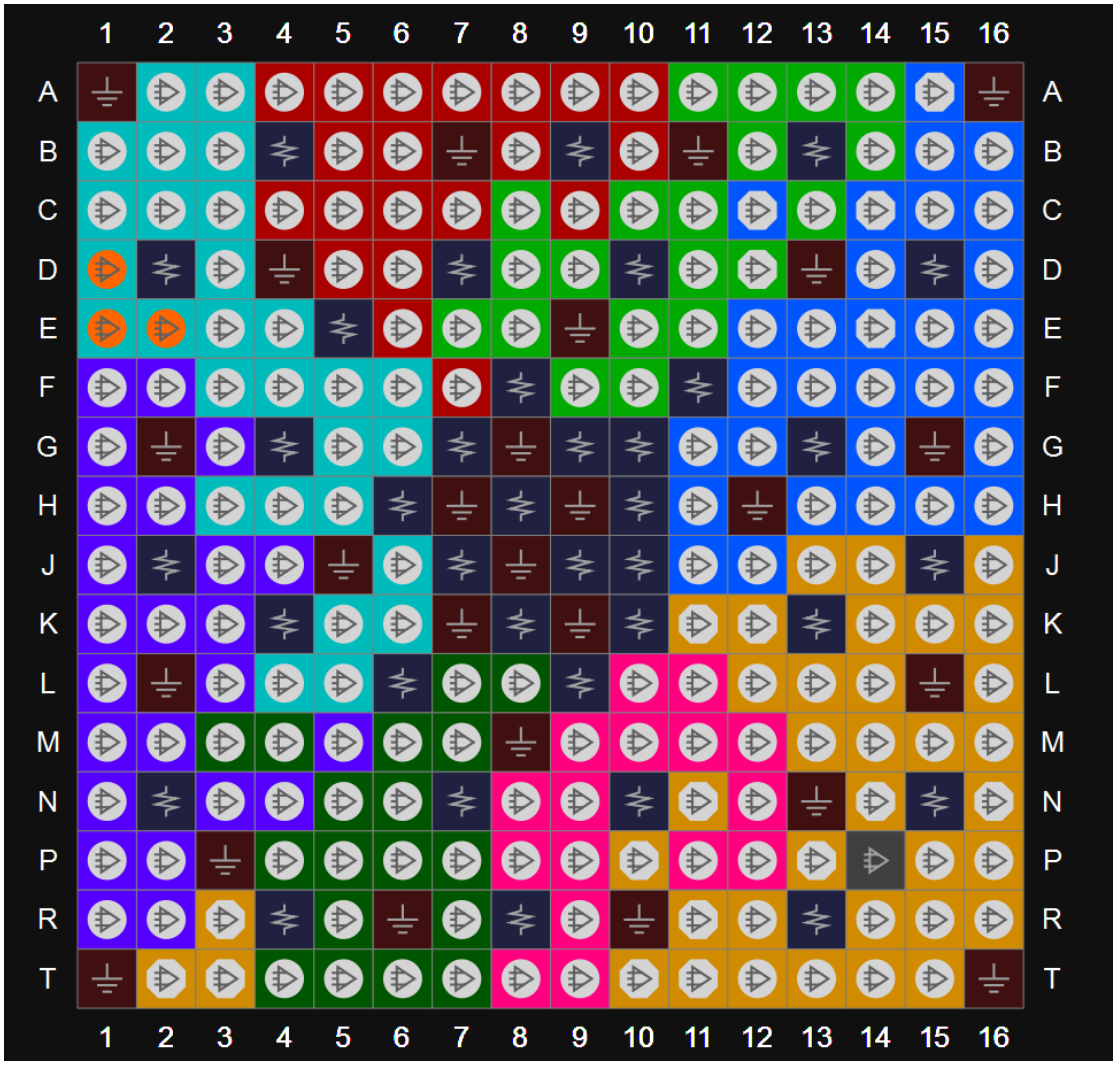


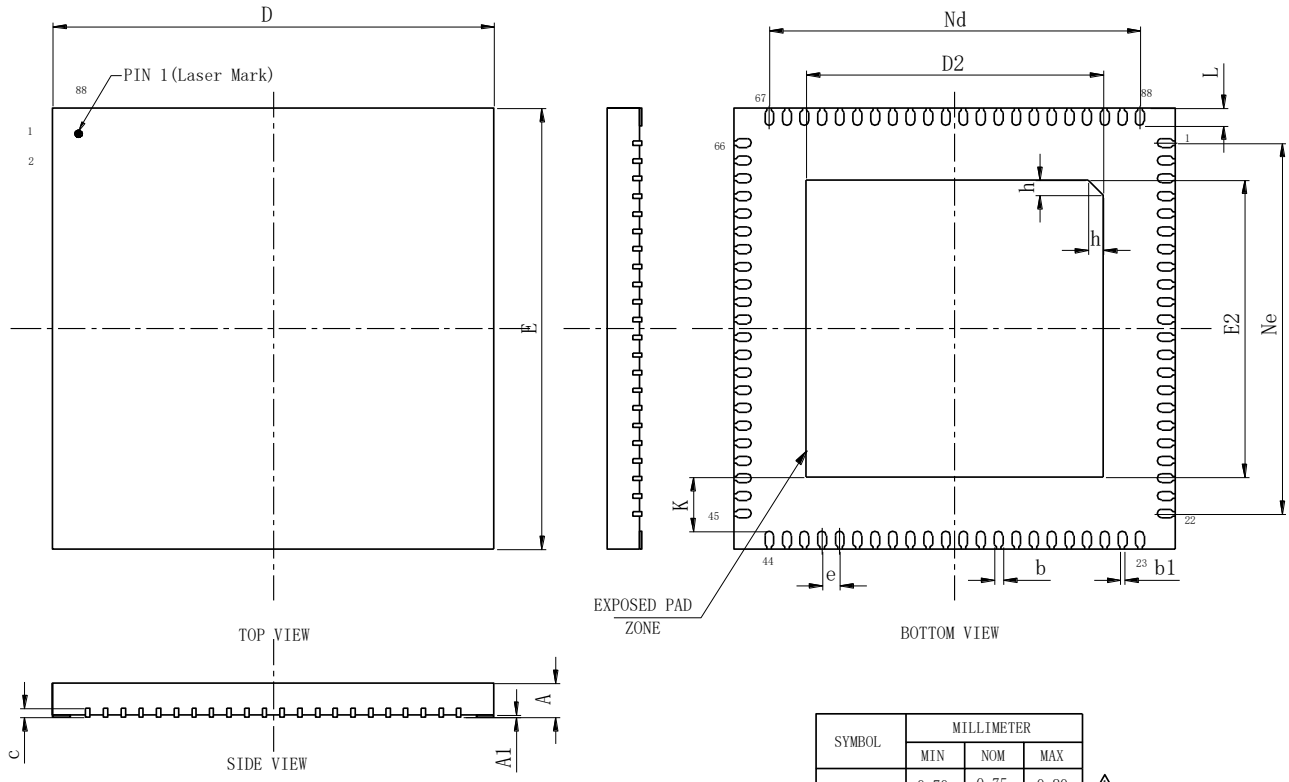
Table 3-8 Other pins in GW2AR-18 PG256S (Embedded with SDRAM)

VCC	G7,G9,H8,J9,K10,K8
VCCO0	B4,B9,D7
VCCO1	B13,D10
VCCO4	N10,R8
VCCO5	N7,R4
VCCX/VCCO2/VCCO3/VCCO6/ VCCO7	D15,D2,E5,F11,F8,G10,G13,G4,H6,J10,J15,J2, K13,K4,L6,L9,N15,N2,R13
VCCPLLL	J7
VCCPLLR	H10
VSS	A1 ,A16 ,B11 ,B7 ,D13 ,D4 ,E9 ,G15 ,G2 ,G8 ,H1 2 ,H7 ,H9 ,J5 ,J8 ,K7 ,K9 ,L15 ,L2 ,M8 ,N13 ,P3 , R10 ,R6 ,T1 ,T16
MODE	T11,N11

4 Package Diagrams

4.1 QN88/QN88P/QN88PF Package Outline (10mm x 10mm)

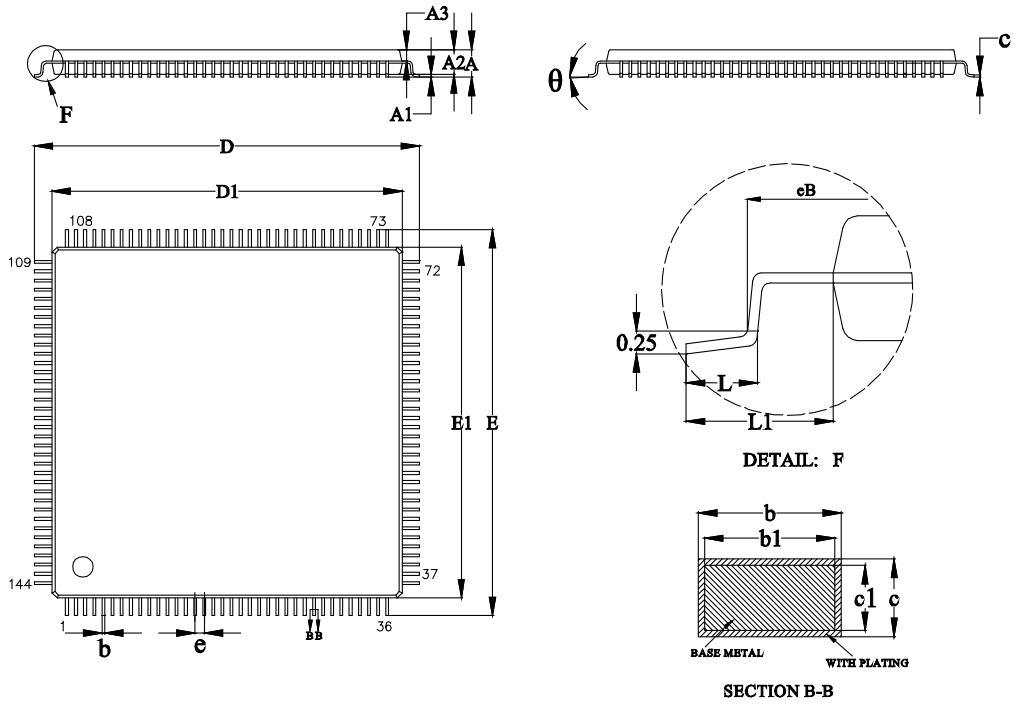
Figure 4-1 Package Outline QN88/QN88P



SYMBOL	MILLIMETER			
	MIN	NOM	MAX	
A	0.70	0.75	0.80	①
	0.80	0.85	0.90	
	0.85	0.90	0.95	②
A1	0	0.02	0.05	
b	0.15	0.20	0.25	
b1	0.10REF			③
c	0.18	0.20	0.25	
D	9.90	10.00	10.10	
D2	6.64	6.74	6.84	
e	0.40BSC			
Nd	8.40REF			
E	9.90	10.00	10.10	
E2	6.64	6.74	6.84	
Ne	8.40REF			
L	0.30	0.40	0.50	
K	0.20	-	-	
h	0.30	0.35	0.40	
L/F载体尺寸 (mil)	300x300			

4.2 LQ144 Package Outline (20mm x 20mm)

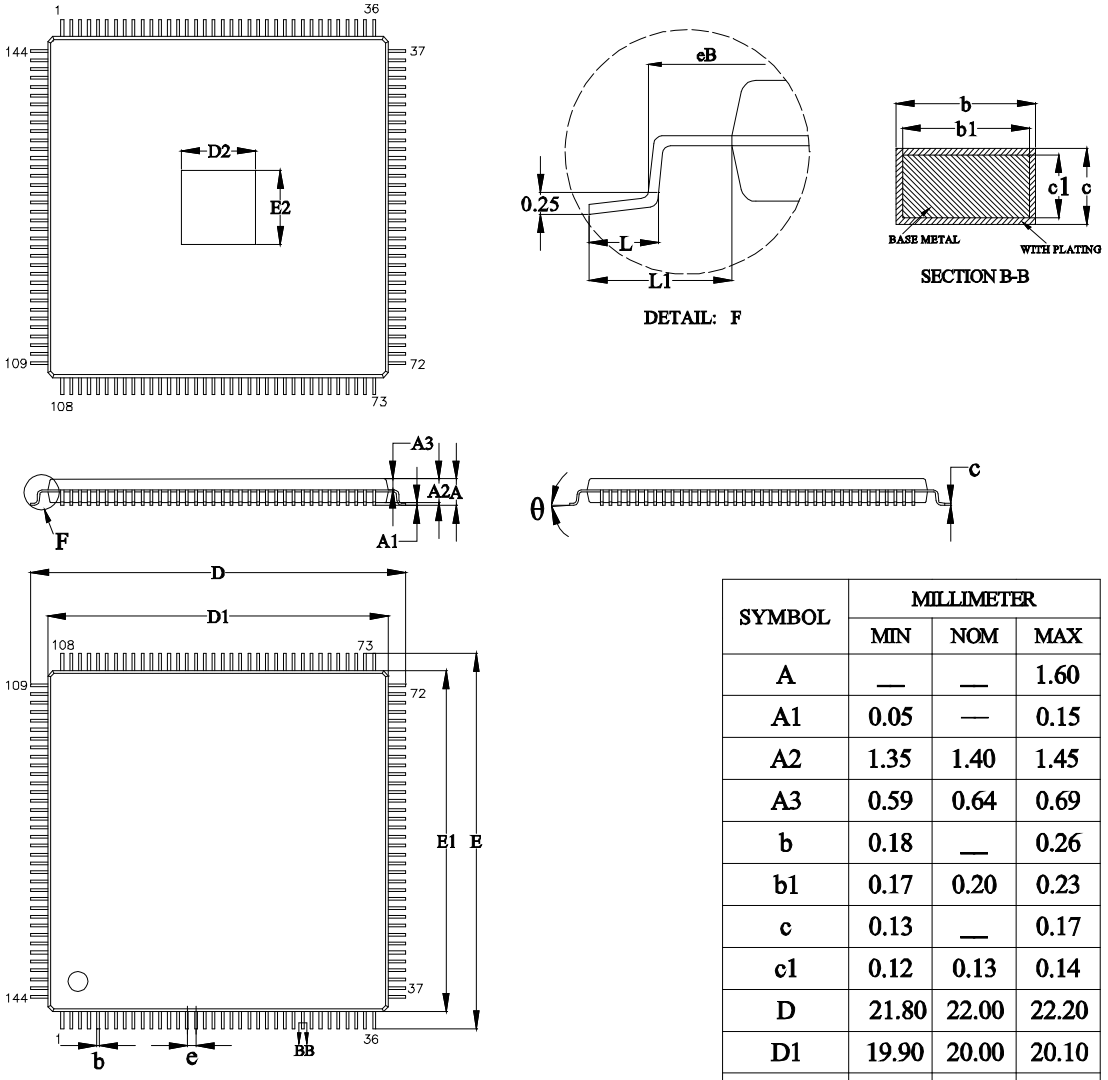
Figure 4-2 Package Outline LQ144



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	—	0.26
b1	0.17	0.20	0.23
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	21.80	22.00	22.20
D1	19.90	20.00	20.10
E	21.80	22.00	22.20
E1	19.90	20.00	20.10
e	0.50BSC		
L	0.45	—	0.75
L1	1.00REF		
θ	0	—	7°

4.3 EQ144/ EQ144P/EQ144PF Package Outline (20mm x 20mm)

Figure 4-3 Package Outline EQ144

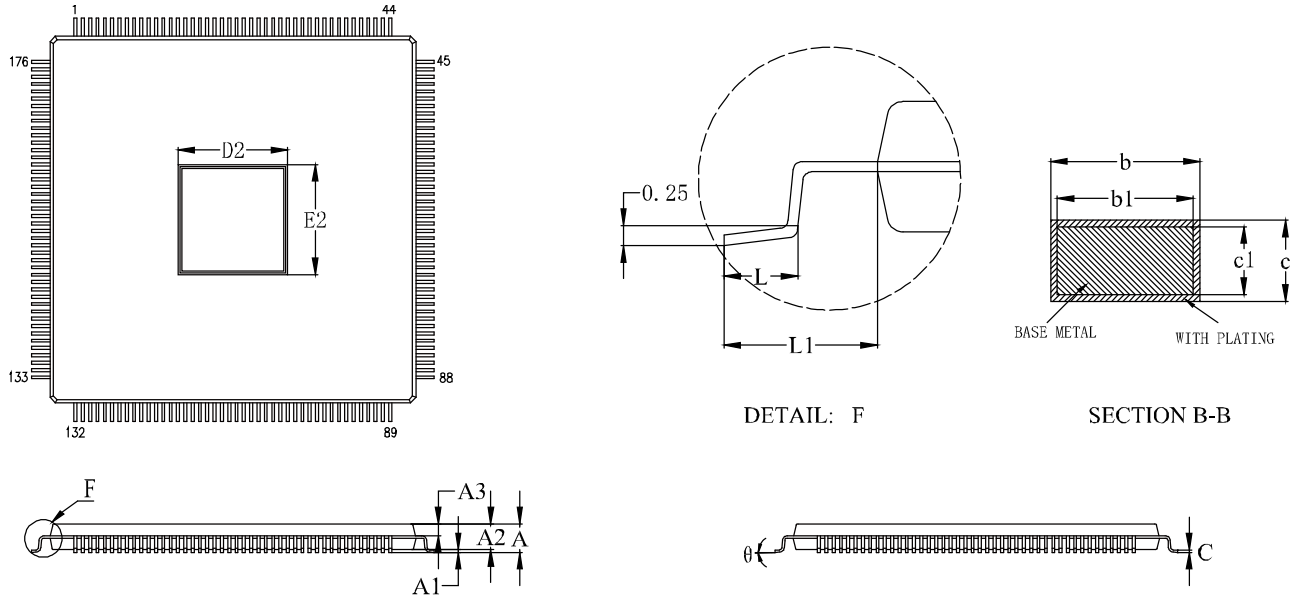


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	—	0.26
b1	0.17	0.20	0.23
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	21.80	22.00	22.20
D1	19.90	20.00	20.10
E	21.80	22.00	22.20
E1	19.90	20.00	20.10
e	0.50BSC		
eB	21.15		21.40
L	0.45	—	0.75
L1	1.00REF		
θ	0	—	7°

L/F Size (mil) \ Size (mm)	D2	E2
383*383	9.74REF	9.74REF

4.4 EQ176 Package Outline (20mm x 20mm)

Figure 4-4 Package Outline EQ176

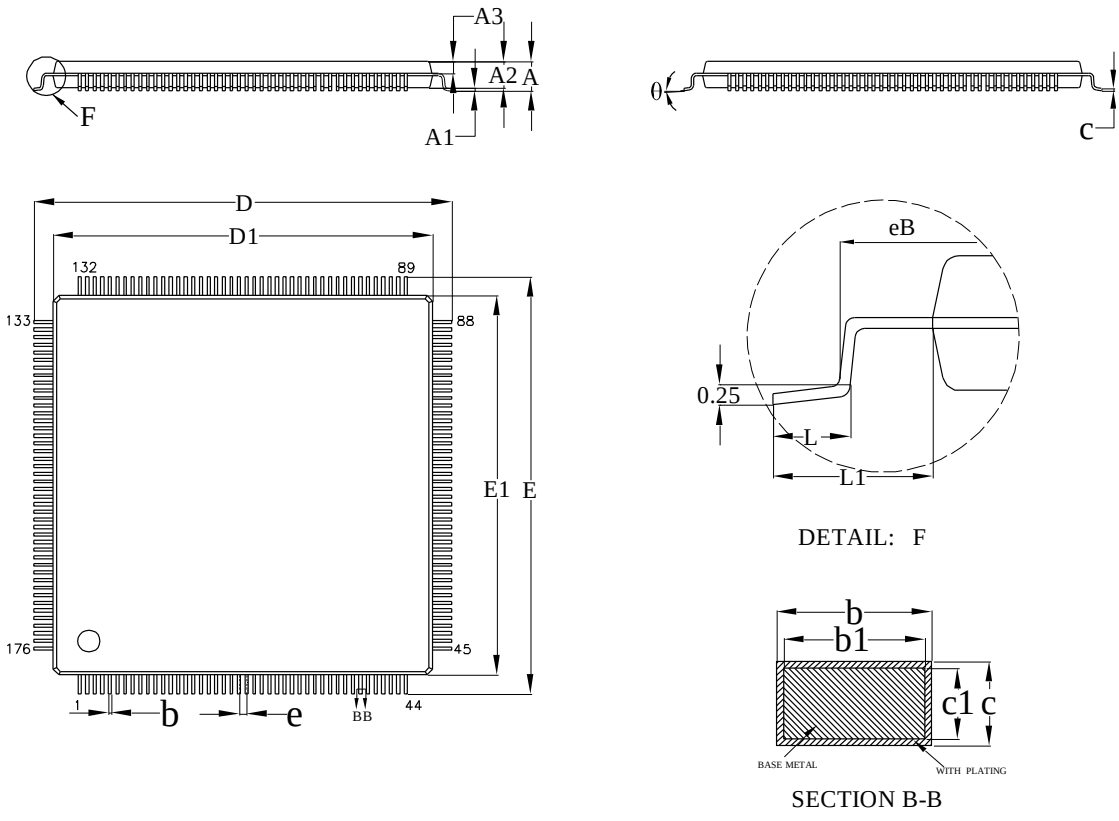


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	0.10	0.15
A2	1.30	1.40	1.50
A3	0.59	0.64	0.69
b	0.14	—	0.22
b1	0.13	0.16	0.19
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	21.80	22.00	22.20
D1	19.90	20.00	20.10
E	21.80	22.00	22.20
E1	19.90	20.00	20.10
e	0.40BSC		
L	0.45	0.60	0.75
L1	1.00REF		
θ	0	—	7°

	D2	E2
236*236	6.00REF	6.00REF

4.5 LQ176 Package Outline (20mm x 20mm)

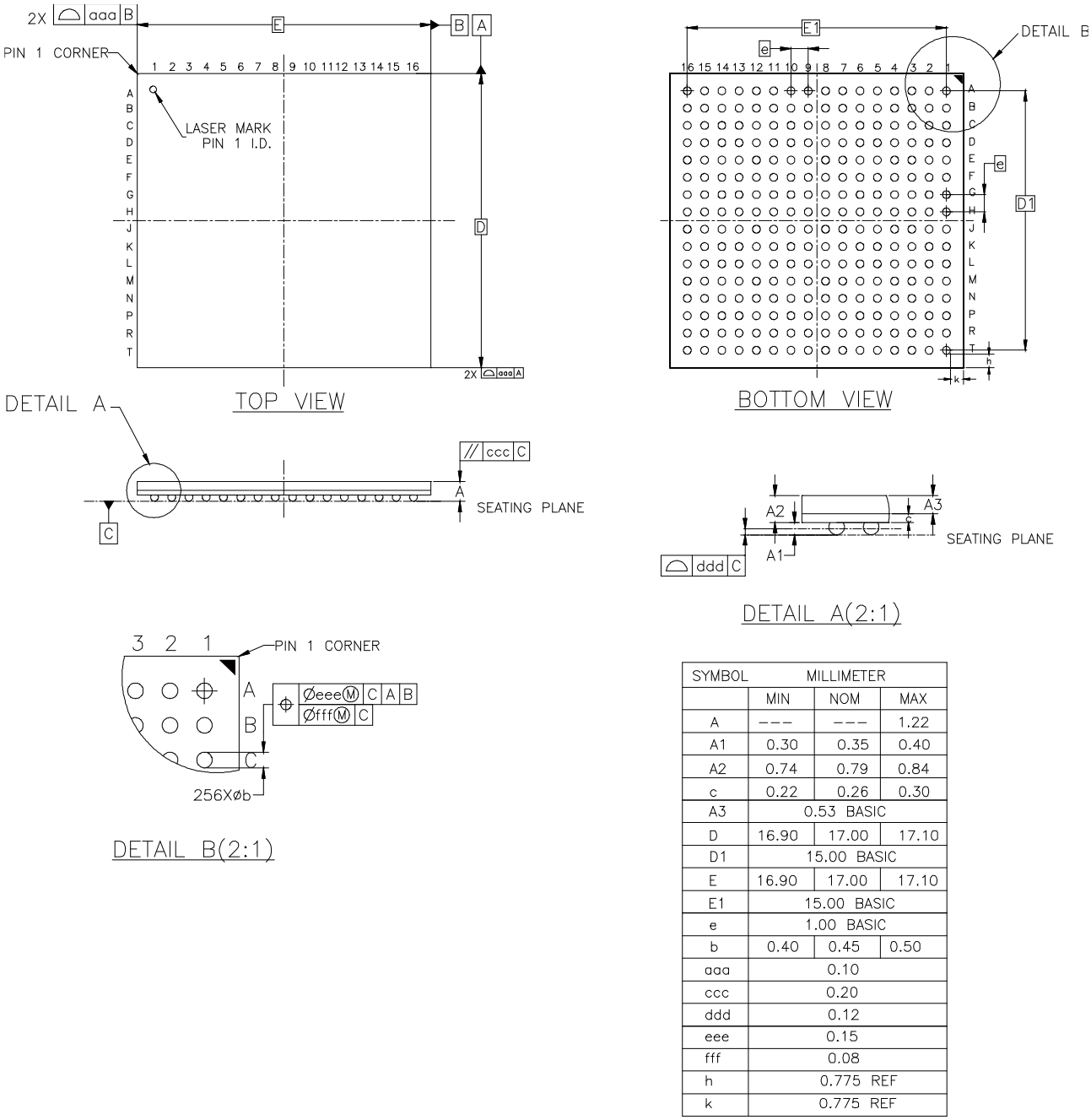
Figure 4-5 Package Outline LQ176



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	0.10	0.15
A2	1.30	1.40	1.50
A3	0.59	0.64	0.69
b	0.14	—	0.22
b1	0.13	0.16	0.19
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	21.80	22.00	22.20
D1	19.90	20.00	20.10
E	21.80	22.00	22.20
E1	19.90	20.00	20.10
e	0.40BSC		
eB	21.15	—	21.40
L	0.45	0.60	0.75
L1	1.00REF		
θ	0	—	7°

4.6 PG256S Package Outline (17mm x 17mm)

Figure 4-6 Package Outline PG256S



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	---	---	1.22
A1	0.30	0.35	0.40
A2	0.74	0.79	0.84
c	0.22	0.26	0.30
A3		0.53 BASIC	
D	16.90	17.00	17.10
D1		15.00 BASIC	
E	16.90	17.00	17.10
E1		15.00 BASIC	
e		1.00 BASIC	
b	0.40	0.45	0.50
aaa		0.10	
ccc		0.20	
ddd		0.12	
eee		0.15	
fff		0.08	
h		0.775 REF	
k		0.775 REF	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