GW2A/GW2AR Series of FPGA Products Schematic Manual

Introduction

You should follow a series of rules for circuit board design when using the GW2A/GW2AR series of FPGA products. This manual describes the characteristics and special features of GW2A/GW2AR series of FPGA products and provides a comprehensive checklist to guide design processes. The main contents of this guide are as follows.

- Power Supply
- JTAG Download
- MSPI Download
- Clock Pin
- Differential Pin
- READY, RECONFIG_N, DONE
- MODE
- JTAGSEL_N
- FASTRD_N
- EXTR
- Dual-purpose Pin
- FPGA External Crystal Oscillator Circuit Reference
- Bank Voltage
- Configuration Modes Supported by Each Device
- Pinout

Power Supply

Overview

Voltage types of the GW2A/GW2AR series of FPGA products include core voltage (V_{CC}), PLL voltage (V_{CCPLL}), auxiliary voltage (V_{CCX}) and Bank voltage (V_{CCO}).

V_{CCX} is an auxiliary power supply that is used to connect the internal part of the chip, with a 2.5V or 3.3V power supply. If no V_{CCX} exists, I/O, OSC, and BSRAM circuits will be impacted and the chip will not be functional.

Power Index

You should ensure GOWINSEMI products are always used within recommended operating conditions and range. Data beyond the working conditions and range are for reference only. GOWINSEMI® does not guarantee that all devices will operate as expected beyond the standard operating conditions and range.

Table 1 lists the recommended working range for each power voltage.

Table 1 Recommended Working Range

Name	Description	Min.	Max.
V_{CC}	Power voltage	0.95V	1.05V
V_{CCPLL}	PLL Power	0.95V	1.05V
V_{CCO}	I/O Bank Power	1.14V	3.6V
V_{CCX}	Auxiliary Power	2.375V	3.6V

Total Power

For specific density, packages, and resource utilization, GPA tools can be used to evaluate and analyze the power consumption.

Power-on Time

Reference range of power-on time: 0.2 ms ~ 2 ms.

Note!

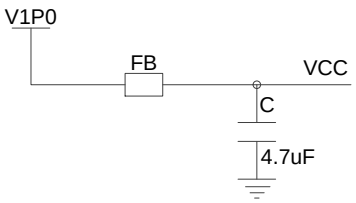
- If the power-on time is more than 2ms, you need to ensure that the power-on in sequence is V_{CC}, and then V_{CCX}/V_{CCO}.
- If the power-on time is less than 0.2ms, it is recommended to increase the capacitance to prolong the power-on time.

Power Filter

Each FPGA power input pin is connected to the ground with a 0.1uF ceramic capacitor.

The input end of the V_{CC} core voltage should primarily conduct the noise processing. Specific reference is as shown in Figure 1:

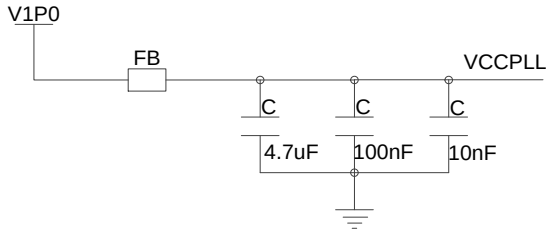
Figure 1 Noise Processing of the Input End of the V_{CC} Core Voltage



GW2A/GW2AR series of FPGA products isolate and filter the V_{CCPLL}.

Specific reference is as shown in Figure 2:

Figure 2 Isolate and Filter the V_{CCPLL}



FB is a magnetic bead, reference model mh2029-221Y, ceramic capacitance 4.7uF, 100nF and 10nF. It offers an accuracy of more than ±10%.

JTAG Download

Overview

JTAG download is used for downloading the bitstream data into the SRAM, on-chip flash or off-chip flash of the FPGA.

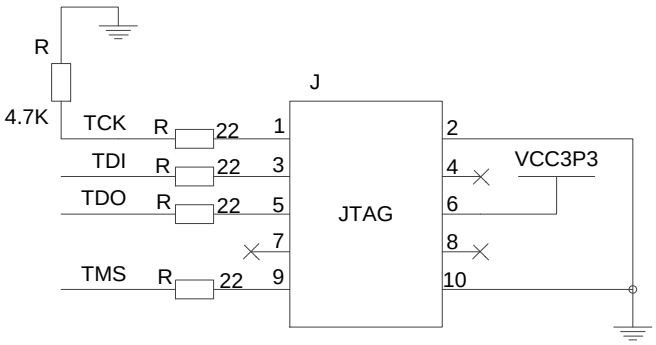
Signal Definition

Table 2 Signal Definition of JTAG Configuration Mode

Name	I/O	Description
TCK	I	Serial clock input in JTAG mode
TMS	I, internal weak pull-up	Serial mode input in JTAG mode
TDI	I, internal weak pull-up	Serial data input in JTAG mode
TDO	O	Serial data output in JTAG mode

JTAG Circuit Reference

Figure 3 JTAG Circuit Reference



Note!

- The resistance accuracy is not less than 5%.
- The power supply of the 6th pin in the JTAG socket can be adjusted to VCC1P2, VCC1P5, VCC1P8 and VCC2P5 as required.

MSPI Download

Overview

As a master device, the MSPI configuration mode reads the configuration data automatically from the off-chip flash and sends it to the FPGA SRAM.

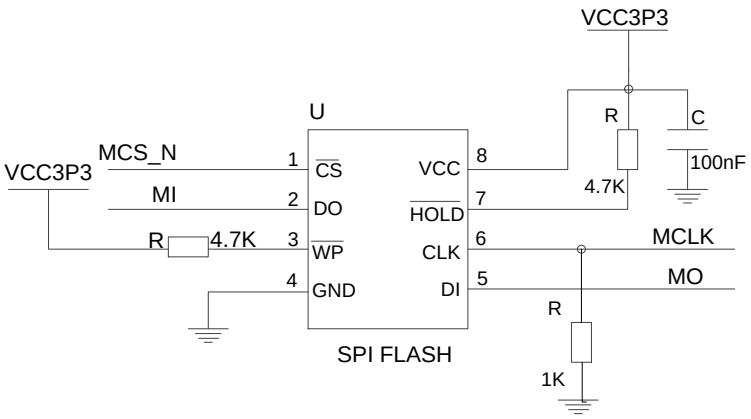
Signal Definition

Table 3 Signal Definition for MSPI Configuration Mode

Name	I/O	Description
MCLK	O	Clock output in MSPI mode
MCS_N	O	MCS_N in MSPI mode, low-active
MI	I	Data input in MSPI mode
MO	O	Data output in MSPI mode

MSPI Circuit Reference

Figure 4 MSPI Circuit Reference



Note!

- 1K pull-down resistance is required for MCLK signal.
- The resistance accuracy is not less than 5%.

Clock Pin

Overview

The clock pins include GCLK global clock pins and PLL clock pins.

- GCLK: The GCLK pins in the GW2A/GW2AR series of FPGA products distribute in four quadrants. Each quadrant provides eight GCLK networks. The optional clock resources of the GCLK can be pins or CRU. Selecting the clock from the dedicated I/Os can result in better timing.
- PLL: Frequency (multiply and division), phase, and duty cycle can be adjusted by configuring the parameters.

Signal Definition

Table 4 Signal Definition for Clock Pin

Name	I/O	Description
GCLKT_[x]	I/O	Pins in global clock input, T(True), [x]: global clock No.
GCLKC_[x]	I/O	Pins for Global clock input, C(Comp), [x]: global clock No.
LPLL_T_fb/RPLL_T_fb	I	L/R PLL feedback the input pin, T(True)
LPLL_C_fb/RPLL_C_fb	I	L/R PLL feedback the input pin, C(Comp)
LPLL_T_in/RPLL_T_in	I	L/R PLL clock input pin, T(True)
LPLL_C_in/RPLL_C_in	I	L/R PLL clock input pin, C(Comp)

Clock Input Selection

If the external clock inputs as a PLL clock, the user is advised to input from the PLL dedicated pin. And the PLL_T end is selected if the external clock inputs from the single-end.

GCLK is the global clock and is directly connected to all resources in the device. The GCLK_T end is advised if the GCLK inputs from the single-end.

Differential Pin

Overview

Differential transmission is a form of signal transmission technology that operates according to differences between the signal line and the ground line. The differential transmit signals on these two lines, the amplitude of the two signals are equal and have the same phase but demonstrate opposite polarity.

LVDS

LVDS is a low-voltage differential signal that offers low power, low bit error rate, low crosstalk, and low radiation. It facilitates the transmission of data using a low-voltage swing high-speed differential. Different packages employ different signals. Please refer to the True LVDS section of the Package Pinout Manual for further details.

Note!

- All BANKs in the GW2A/GW2AR series of FPGA products support True LVDS output.
- Differential input requires an external100 ohm termination resistor.
- If the BANK is used as the differential input, 100-ohm termination resistor is needed.
- The differential line impedance of PCB is controlled at about 100 ohms.

READY, RECONFIG_N, DONE

Overview

RECONFIG_N is a reset function within the FPGA programming configuration. FPGA can't configure if RECONFIG_N is low.

As a configuration pin, a low level signal with pulse width no less than 25ns is required to start GowinCONFIG to reload bitstream data according to the MODE setting value. You can control the pin via the write logic and trigger the device to reconfigure.

READY, the FPGA can configure only when the READY signal is high. The device should be restored by using the power on or triggering RECONFIG_N when the READY signal is low.

As an output configuration pin, FPGA can be indicated for the current configuration state. If the device meets the configuration condition, READY signal is high. If the device fails to configure, the READY signal changes to low. As an input configuration pin, you can reduce the READY signal via its own logic or manually operate outside the device to delay configuration.

DONE, the DONE signal indicates that the FPGA is configured successfully. The signal is high after successful configuration.

As an output configuration pin, FPGA can be indicated whether the current configuration is successful. If configured successfully, DONE is high, and the device enters into a working state. If the device failed to configure, the DONE signal remains low. For the input type, the user can reduce the READY signal via its own internal logic or manually operate outside the device to delay progression to user mode.

When the RECONFIG_N or READY signals is low. The DONE signal is low. DONE has no influence when SRAM is configuried through the JTAG circuit.

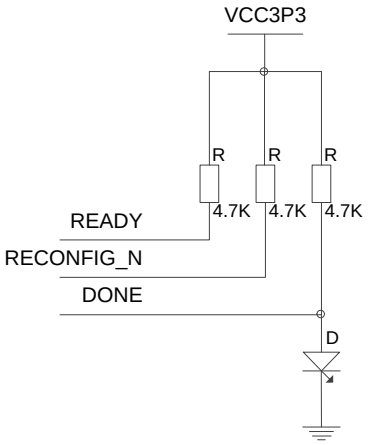
Signal Definition

Table 5 Signal Definition

Name	I/O	Description
RECONFIG_N	I, internal weak pull-up	Low-level pulse: Start new GowinCONFIG configuration
READY	I/O	High-level pulse: The device can currently be programmed and configured;
		Low-level pulse: The device cannot be programmed and configured,
DONE	I/O	High-level pulse: The device has been successfully programmed and configured;
		Low-level pulse: The configuration is incomplete or has failed.

Reference Circuit

Figure 5 Reference Circuit



Note!

- The upper pull power supply is the bank voltage value of the corresponding pin;
- The resistance accuracy is not less than ± 5%.

MODE

Overview

MODE spans the MODE0, MODE1, MODE2, and GowinCONFIG configuration MODE modes. When the FPGA powers on or a low pulse triggers the RECONFIG_N mode, the device enters the corresponding GowinCONFIG state according to the MODE value. As the number of pins for each package is different, some MODE pins are not all bonded, and the unbonded MODE pins are grounded inside. Please refer to the corresponding PINOUT manual for further details.

Signal Definition

Table 6 Signal Definition

Name	I/O	Description
MODE2	I, internal weak pull-up	GowinCONFIG modes selection pin.
MODE1	I, internal weak pull-up	GowinCONFIG modes selection pin.
MODE0	I, internal weak pull-up	GowinCONFIG modes selection pin.

Mode Selection

Table 7 Mode Selection

Configuration Modes		MODE[2:0][1]	Description
JTAG		XXX[2]	External Host configures Arora Family of FPGA products via JTAG interface.
GowinCONFIG	MSPI[3]	000	As Master, FPGA reads data from external Flash (or other devices) via the SPI interface.
	SSPI[3]	001	External Host configures Arora Family of FPGA products via SPI interface.
	SERIAL[4]	101	External Host configures Arora Family of FPGA products via DIN interface.
	CPU[4]	111	External Host configures Arora Family of FPGA products via DBUS interface.

Note!

[1] The unbound mode pins are grounded by default.
[2] The JTAG configuration mode is independent of MODE value.
[3] The SPI interfaces of the SSPI and MSPI modes are independent of each other.
[4] The CPU configuration mode and SERIAL configuration mode share SCLK, WE_N and CLKHOLD_N. The data bus pins for the CPU configuration mode share pins with MSPI and SSPI configuration modes.

JTAGSEL_N

Overview

Select the signal in JTAG mode. If the JTAG pin is set as GPIO in Gowin software, the JTAG pin is changed to GPIO pin after being powered on and successfully configured. The JTAG pin can be recovered by reducing the JTAGSEL_N. The JTAG configuration functions are always available if no JTAG pin multiplexing is set.

Signal Definition

Table 8 Signal Definition

Pin Name	I/O	Description
JTAGSEL_N	I, internal weak pull-up	Restore JTAG pin from GPIO to configuration pin. Low level is valid

Note!

As GPIO, the JTAGSEL_N pin and the four pins (TCK, TMS, TDI, and TDO) configured with JTAG are mutual exclusive.

- If JTAGSEL_N is set to GPIO, the JTAG pin can only be used as a configuration pin.
- If JTAG is set to GPIO, the JTAGSEL_N pin can only be used as a configuration pin.

FASTRD_N

Overview

In MSPI configuration mode, signals are selected via reading the SPI flash speed rate. FASTRD_N is normal read mode if high level; FASTRD_N is high speed read mode if low level. Each manufacturer's flash high speed read instruction is different. Please refer to the corresponding flash data manual.

Signal Definition

Table 9 Signal Definition

Pin Name	I/O	Description
FASTRD_N	I	As a configuration pin: Input, internal weak pull up, sample MSPI configuration value at READY signal rising edge; As a GPIO: Input or putput.

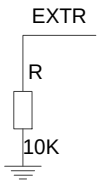
Note!

- High-level: Normal Flash access mode, the clock frequency should be less than 30MHz;
- Low-level: High-speed Flash access mode, the clock frequency is greater than 30MHz and less than 80MHz.

EXTR

EXTR is a dedicated pin that needs to be connected to the ground with 10K resistance. The resistor precision is 1%.Specific reference is as shown below.

Figure 6 EXTR Pin Configuration



Dual-purpose Pin

Overview

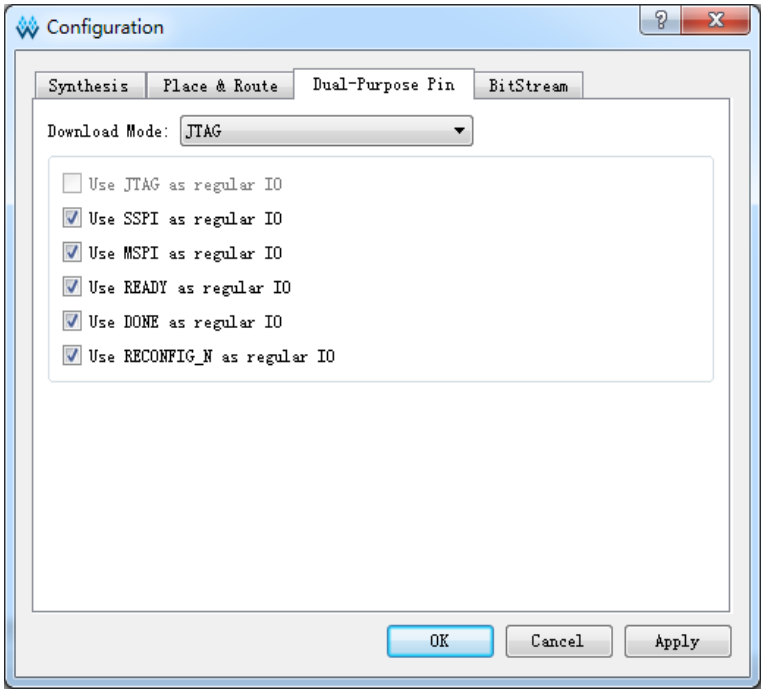
Configure pin multiplexing refers to configuring during power-on, which is used as a normal I/O after downloading the bitstream file.Configure pin multiplex via the Gowin software:

a). Open the corresponding project in Gowin software.

b). Select “Project > Configuration > Dual Purpose Pin” from the menu options, as shown in Figure 7.

c). Check the corresponding option to set the pin multiplex.

Figure 7 Dual-purpose Pin



Dual-purpose Pin

- SSPI: As a GPIO, SSPI can be used as input or output type;
- MSPI: As a GPIO, MSPI can be used as input or output type;
- RECONFIG_N GPIO can only be used as an output type. For smooth configuration, set the initial value of RECONFIG_N as high when multiplexing it.
- READY: As a GPIO, READY can be used as an input or output. As an input GPIO for READY, the initial value of READY should be 1 before configuring. Otherwise, the FPGA will fail to configure;
- DONE: As a GPIO, DONE can be used as an input or output type. If DONE is used as an input GPIO, the initial value of DONE should be 1 before configuring. Otherwise, the FPGA will fail to enter the user mode after configuring;
- JTAG: As a GPIO, JTAG can be used as an input or output type;
- JTAGSEL_N: As a GPIO, JTAGSEL_N can be used as an input or output type.
- DONE: As a GPIO, JTAG can be used as an input or output type. In order to smoothly configure, the user multiplexes the MODE pin, the correct configuration mode value is needed to provided during configuration (power-on or low-level pulse triggers RECONFIG_N). Less than three pins can be multiplexed in the MODE. Unbonded products are grounded internally. Please refer to PINOUT manual of the corresponding device for details. For the MODE value

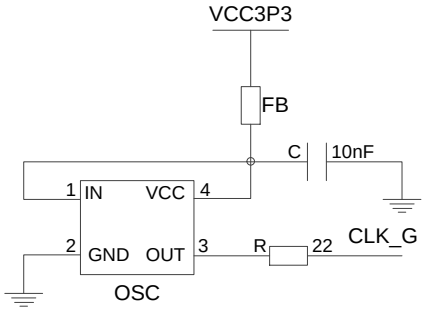
corresponding to different configuration modes, please refer to *UG290, Gowin FPGA Products Programming and Configuration Guide*.

Note!

If the Number of I/O ports are sufficient, use non-multiplexed pins first.

FPGA External Crystal Oscillator Circuit Reference

Figure 8 FPGA External Crystal Oscillator Circuit



FB is a magnetic bead, with MH2029-221Y reference model, more than ±5% resistance accuracy, and more than ±10% capacitance accuracy.

Bank Voltage

For the detailed Bank voltage requirements, please refer to the following manuals.

- UG115, GW2AR-18 Pinout
- UG110, GW2A-18 Pinout
- UG113, GW2A-55 Pinout

Configuration Modes Supported by Each Device

GW2A-18

Table 10 GW2A-18 Configuration Modes

Configuration Mode	JTAG	SSPI	MSPI	SERIAL	CPU
QN88	Yes	No	Yes	No	No
LQ144	Yes	Yes	Yes	Yes	Yes
EQ144	Yes	Yes	Yes	Yes	Yes
MG196	Yes	No	Yes	No	No
PG256	Yes	Yes	Yes	Yes	Yes
PG256S	Yes	No	Yes	No	No
PG256C	Yes	No	Yes	No	No
PG256E	Yes	No	Yes	No	No
PG256SF	Yes	No	No	Yes	No
PG256CF	Yes	Yes	No	Yes	No
PG484	Yes	Yes	Yes	Yes	Yes
UG324	Yes	No	Yes	No	Yes
UG484	Yes	Yes	Yes	Yes	Yes

GW2A-55

Table 11 GW2A-55 Configuration Modes

Configuration Mode	JTAG	SSPI	MSPI	SERIAL	CPU
UG324	Yes	No	Yes	No	Yes
UG324D	Yes	No	Yes	No	Yes
UG324F	Yes	Yes	Yes	Yes	No
UG676	Yes	Yes	Yes	Yes	Yes
PG484	Yes	Yes	Yes	Yes	Yes
PG1156	Yes	Yes	Yes	Yes	Yes

GW2AR-18

Table 12 GW2AR-18 Configuration Modes

Configuration Mode	JTAG	SSPI	MSPI	SERIAL	CPU
QN88	Yes	No	Yes	No	No
QN88P	Yes	No	Yes	No	No
QN88PF	Yes	No	Yes	No	No
LQ144	Yes	Yes	Yes	Yes	Yes
EQ144	Yes	Yes	Yes	Yes	Yes
EQ144P	Yes	Yes	Yes	Yes	Yes
EQ144PF	Yes	Yes	Yes	Yes	Yes
LQ176	Yes	Yes	Yes	Yes	Yes
EQ176	Yes	Yes	Yes	Yes	Yes
PG256S	Yes	No	Yes	No	No

Pinout

Before designing circuits, you should take the overall FPGA pinout needs into consideration and make informed decisions related to the application of the device architecture features, including I/O LOGIC, global clock resources, PLL resources, etc.

All banks of the GW2A/GW2AR bank support true LVDS output, please refer to GW2A/GW2AR series of FPGA Product Pinout to ensure that the corresponding pins support true LVDS output.

To support SSTL, HSTL, etc., each bank also provides one independent voltage source (V_{REF}) as the reference voltage. Users can choose V_{REF} from the internal reference voltage of the bank (0.5 x VCCO) or external reference voltage V_{REF} using any I/O from the bank.

For DDR pinout, please see *TN662, Based on Gowin FPGA DDR2 & DDR3 Hardware Design Reference Manual*.

Note!

The device I/Os (except TCK) are all internal weak pull-up. After configuration, I/O status is determined by user programs and constraints.

Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website:www.gowinsemi.com

E-mail: support@gowinsemi.com

Revision History

Date	Version	Description
2018/01/02	1.0E	Initial version published.
06/29/2018	1.2E	Revise the schematic diagram style uniformly.
04/03/2019	1.3E	The description of FASTRD_N updated.
04/12/2019	1.4E	The description added: The device I/Os (except TCK) are all internal weak pull-up.
05/10/2019	1.5E	Pull-down resistance for MCLK signal added.
06/04/2019	1.6E	Bank Voltage description updated.
10/28/2019	1.7E	The link of DDR pins distribution document added.
12/06/2021	1.8E	● The value described in Table 1 Recommended Working Range fixed. ● The configuration modes supported by each device updated.
02/21/2022	1.8.1E	The configuration modes supported by each device updated.
03/04/2022	1.8.2E	The configuration modes supported by GW2A-18 and GW2A-55 series of devices updated.

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