Intel Xeon Phi Coprocessor Architecture And Tools

Author : Rezaur Rahman / **Category :**Computers / **Total Pages** : 232 pages

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Summary : Free intel xeon phi coprocessor architecture and tools pdf download - intel xeon phi coprocessor architecture and tools the guide for application developers provides developers a comprehensive introduction and in-depth look at the intel xeon phi coprocessor architecture and the corresponding parallel data structure tools and algorithms used in the various technical computing applications for which it is suitable it also examines the source code-level optimizations that can be performed to exploit the powerful features of the processor xeon phi is at the heart of world s fastest commercial supercomputer which thanks to the massively parallel computing capabilities of intel xeon phi processors coupled with xeon phi coprocessors attained 33 86 teraflops of benchmark performance in 2013 extracting such stellar performance in real-world applications requires a sophisticated understanding of the complex interaction among hardware components xeon phi cores and the applications running on them in this book rezaur rahman an intel leader in the development of the xeon phi coprocessor and the optimization of its applications presents and details all the features of xeon phi core design that are relevant to the practice of application developers such as its vector units hardware multithreading cache hierarchy and host-to-coprocessor communication channels building on this foundation he shows developers how to solve real-world technical computing problems by selecting deploying and optimizing the available algorithms and data structure alternatives matching xeon phi s hardware characteristics from rahman s practical descriptions and extensive code examples the reader will gain a working knowledge of the xeon phi vector instruction set and the xeon phi microarchitecture whereby cores execute 512-bit instruction streams in parallel what you ll learn how to calculate theoretical gigaflops and bandwidth numbers on the hardware and measure them through code segment how to estimate latencies in fetching data from different cache hierarchies including memory subsystems how to measure pcie bus bandwidth between the host and coprocessor how to exploit power management and reliability features built into the hardware how to select and manipulate the best tools to tune particular xeon phi applications algorithms and data structures for optimizing xeon phi performance case studies of real-world xeon phi

technical computing applications in molecular dynamics and financial simulations who this book is for this book is for developers wishing to design and develop technical computing applications to achieve the highest performance available in the intel xeon phi coprocessor hardware it provides a solid base on the coprocessor architecture as well as algorithm and data structure case studies for xeon phi coprocessor the book may also be of interest to students and practitioners in computer engineering as a case study for massively parallel core microarchitecture of modern day processors table of contents 1 introduction to xeon phi architecture 2 programming xeon phi 3 xeon phi vector architecture and instruction set 4 xeon phi core microarchitecture 5 xeon phi cache and memory subsystem 6 xeon phi pcie bus data transfer and power management 7 xeon phi system software 8 xeon phi application development tools 9 xeon phi application design and implementation considerations 10 application performance tuning on xeon phi 11 algorithms and data structures for xeon phi 12 xeon phi application development on windows os 13 opencl on intel 14 shared memory programming on intel xeon phi

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