Compendium of Single-Event Latchup and Total Ionizing Dose Test Results of Commercial Analog to Digital Converters

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***Abstract*—This paper reports single-event latchup and total dose results for a variety of analog to digital converters targeted for possible use in NASA spacecraft's. The compendium covers devices tested over the last 15 years.**

I. Introduction

The analog-to-digital, A/D converter (ADC) is one of the critical components sought by engineers designing electronic hardware for flight projects. The performance requirements for an A/D cover a wide spectrum: the three main features being the bit resolution, power and speed. In addition, each project has their radiation and reliability requirements that the selected ADC is expected to meet or exceed.

Because of the number of flight worthy suppliers is dwindling, there has been increased interest in the possible infusion of unhardened commercial-off-the-shelf (COTS) ADCs into NASA Space projects. The COTS ADCs offer cutting-edge technology in terms of speed, and have superior electrical performance compared to hardened devices. However, unhardened COTS ADCs are susceptible to upset and degradation from radiation; more information is needed on how they respond to radiation before they can be used in space. In order to evaluate these devices for space radiation environments, one must measure the single-event effect (SEE) cross section and total ionizing dose (TID) response. In SEE measurements, the ADC is basically monitored for hard errors, such as single event latchup (SEL). In TID measurements degradation in voltage reference, integral nonlinearity (INL), differential nonlinearity (DNL), gain and offsets errors are main critical parameters for considerations.

This compendium represents SEL and TID sensitivity of the available COTS ADCs, to SEL and TID.

II. Data Organization

This compendium is intended to serve as a reference list for available COTS ADCs as far as radiation is concern. ADCs are grouped by bit resolution, from 8-bit converters to 24-bit parts. SEL sensitivity as well as their TID respond is shown in the Table I. The data tables contain abbreviated information mainly due to spatial constraints. It is highly recommended that the reader review the referenced article. For some of the parts no SEL or TID data are presented because of lack of radiation data. We encourage readers to provide us any missing data for the parts which we did not provide SEL or TID data.

Some of the SEL data and SEL susceptibility referred to in this compendium are obtained during measurements with low range ions irradiation. In general, SEL involves deeper regions in the CMOS device (greater than 50 μm) and long range ions required to perform SEL measurements. The proper ion range for SEL measurements is about 70 μm [1]. These results should be considered with caution.

Also, most of the data presented in this compendium are results of room temperature measurements. It is known that the SEL has a temperature dependency. The SEL threshold LET decreases while cross section increases with temperature [2]. Some parts might show no susceptibility to SEL at room temperature, but at elevated temperature show sensitivity to SEL.

III. SEL Test Results

1. AD670

The Analog Devices AD670 is a complete 8-bit signal conditioning ADC. AD670 is built on a bipolar process and it is immune to SEL. In general devices which are fabricated with bipolar process are SEL immune.

2. *AD7821*

The 8-bit ADC AD7821 from Analog Devices was tested for SEL at the Cyclotron Institute at Texas A&M University facility (TAMU). The lot date code was 0034. SEL measurements were performed only at room temperature. No SEL events were observed up to the maximum tested LET of 80 MeV•cm^2/mg and a fluence of 6x10^6 ions/cm^2 [3].

3. ADC1175

The 8-bit ADC ADC1175 from Texas Instruments (TI) was tested for SEL at TAMU. The lot date code was 1317. The measurements were performed only at room temperature. The TI ADC1175 evaluation board was used for the SEE testing. This board operates the AD1175 from a single +5V supply at a 20 MHz clock. The device was not sensitive to SEL up to an LET of ~23 MeV•cm^2/mg. The SEL cross section is about 4.6x10^{-6} cm^2/device at an LET of 118 MeV•cm^2/mg [3].

4. SPT7725

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The Fairchild SPT7725 is a monolithic 8-bit, 300 MSPS flash ADC. SPT7725 is built on a bipolar process and it is immune to SEL.

5. HI1276

The Intersil HI1276 is ultra-high speed 8-bit, flash ADC capable of digitizing analog signals at a maximum rate of 500 MSPS. HI1276 is built on a bipolar process and it is immune to SEL.

6. HS-9008RH

The Intersil HS-9008RH is a 8-Bit relatively low power, very fast conversion speed flash ADC. Per the manufacturer the HS-9008RH is immune to SEL.

7. AD571

The Analog Devices AD571 is a 10-bit successive ADC. The device was monitored for SEL while exposing it to a number of heavy-ion beams at the Brookhaven National Laboratory (BNL). SEL measurements were performed only at room temperature. Supply current was monitored for an increase or decrease. No SELs were observed for the AD571 ADC up to LET of 60 MeV•cm^2/mg [4].

8. AD9200

The Analog Devices AD9200 is a monolithic, single supply, 10-bit, 20 MSPS ADC. This part showed susceptibility to latchup during SEL measurements with Californium source.

9. AD574

The Analog Devices AD574 is a complete 12-bit successive approximation ADC. AD574 is built on a bipolar/I^2 process and it is immune to SEL.

10. AD9042

The Analog Devices AD9042 is a high speed, high performance, low power, monolithic 12-bit ADC. The AD9042 is built on a high speed complementary bipolar process (XFCB) and it is immune to SEL. In general devices which are fabricated with XFCB process are SEL immune.

11. AD1672

The Analog Devices AD1672 is monolithic single supply 12-bit, 3 MSPS ADC. This device was tested for SEL at TAMU by Jet Propulsion Laboratory (JPL) [5]. The lot date codes were 9803, 0310, and 0302. Fluences over 1x10^{7}cm^{-2} were irradiated onto the device. The AD1672 did not experience SEL up at any LET up to 80 MeV-cm^2/mg.

12. LTC1409

The Linear technology LTC1409 is a 12-bit 800ksps Sampling ADC with Shutdown. This device was tested for SEL at TAMU by the JPL group. No SELs were observed up to LET 80 MeV-cm^2/mg [5].

13. AD1674

The Analog Devices AD1674 is a complete, multipurpose, 12-bit ADC. This devise was tested for SEL at BNL. The lot date code was 9848. SEL measurements were performed only at room temperature. No SELs were observed for LET of 37 MeV•cm^2/mg to a fluence of 1x10^7 ions/cm^2 [6].

14. AD6640

The Analog Devices AD6640 12-bit ADC was tested for SEL at BNL. The AD6640 is a 65 MHz, ADC fabricated in Analog Devices XFCB dielectrically isolated bipolar process. The lot date code was 9951. No evidence of SEL was observed up to a fluence of 2x10^6 ions/cm^2 for LET of 37 MeV•cm^2/mg [6]. This part is fabricated with XFCB process and is immune to SEL.

15. AD7854

The Analog Devices AD7854 is a CMOS single-channel, 200 kbps 12-bit ADC. It was tested for SEL only at room temperature and found to be susceptible to SEL with a threshold LET between 8 and 11 MeV•cm^2/mg and with a limiting cross section between 1x10^{-4} and 1x10^{-3} cm^2. The device under test (DUT) lot date code was 9930. The device was susceptible for both 3.6 and 5 volt supply voltages [6].

16. AD7858

The Analog Devices AD7858 is a CMOS 8 channel, 200 kbps 12-bit ADC. It was tested for SEL at only room temperature and found to be susceptible with a threshold LET between 11 and 22 MeV•cm^2/mg and a limiting cross section between 1x10^{-4} and 1x10^{-3} cm^2 [6]. The lot date code was 0026. The device was susceptible for both 3.6 and 5 volt supply voltages.

17. AD7888

The Analog Devices AD7888 is a CMOS 8 channel, 125 kbps 12-bit ADC. It was tested for SEL only and found to be susceptible with a threshold LET between 16 and 22 and a limiting cross section between 1x10^{-5} and 1x10^{-4} cm^2 [6]. The lot date codes were 0002 and 0016.The device was susceptible for both 3.6 and 5 volt supply voltages.

18. AD7472

The Analog Devices AD7472 is a 12-bit high speed, low power; successive-approximation ADC manufactured on 0.6 um CMOS process. This device was tested for SEL at BNL at room temperature. Devices were tested in a 5V configuration and at only room temperature. The lot date code was 9919. The LET$_{th}$ is less the 12 MeV-cm^2/mg and the saturated cross section is about 1.2x10^{-4} cm^2 [7].

19. AD7476

The Analog Devices AD7476 is a 12-bit high speed successive-approximation ADC manufactured on 0.6 um CMOS process. This device was tested for SEL at BNL. DUTs were tested in a 5V configuration and at room

temperature. The lot date code was 9944. SEL events were detected on the supply, input voltage, and chip select lines at an LET of 59.8 MeV-cm2/mg. The latchup was destructive [7].

20. AD9223

The 12-bit ADC AD9223 from Analog Devices was tested SEL at TAMU. The measurements were performed only at room temperature. The lot date code was 0015. The device exhibited SEL sensitivity at an LET of 20 MeV•cm^2/mg. The SEL cross section at the maximum tested LET of 40 MeV•cm^2/mg was about 1x10^{-4} cm^2/device [8].

21. LTC1272

The 12-bit ADC LTC1272 from Linear Technology was tested for SEL at TAMU. The lot date code was 0018. SEL measurements were performed only at room temperature. This device was very sensitive to SEL; the SEL LET$_{th}$ was less than 5.6 MeV•cm^2/mg and the cross section at the maximum tested LET of 20 MeV•cm^2/mg was 1x10^{-4} cm^2/device [8].

22. *AD1671*

The AD1671 is a 12-bit 1.25MSPS ADC manufactured by Analog Devices and constructed with a bipolar/CMOS process. This part was tested for SEL by the Goddard at BNL [9]. The measurements were performed only at room temperature. No SEL events were observed up to 90 MeV-cm^2/mg.

23. LTC1407

The Linear Technology LTC1407A-1 is 14-bit, 3Msps ADC with two 1.5Msps simultaneously sampled differential inputs realized in CMOS technology. The LTC1407A-1 was tested for SEL at Université Catholique de Louvain la Neuve (UCL) using the two available cocktails: "High LET" and "High penetration". All the measurements were performed only at room temperature. The LTC1407 was sensitive to latchup [10]. Testing was performed to determine the latchup threshold LET. For all runs, the devices were exposed to the ion beam until one hundred latchup occurred or up to a fluence of 1x10^7 ions/cm^2. At LET of 55.9MeV-cm^2/mg and a range of 43μm the three parts showed latchup with a cross section of 1x10^{-5} cm^2. At LET= 32.4MeV-.cm^2/mg and range = 92μm, no latchup occurred. Ref. [10] concludes that the SEL LET$_{th}$ is between 32.4 and 55.9 MeV-cm^2/mg for this part.

24. LTC2297

The Linear Technology LTC2297 is 14-bit 40Msps, low power dual 3V ADC designed for digitizing high frequency, wide dynamic range signals. Three samples were irradiated using both UCL "High LET" and "High penetration" cocktails. The lot date code was 0452. The SEL measurements were performed only at room temperature. The results were quite homogeneous between the three parts. The threshold LET was between 10 and 20.6MeV-cm^2/mg, and the saturation cross section was 4x10^{-4} cm^2 [10].

25. AD9240

The Analog Devices AD9240 is a 14-bit CMOS ADC. It was tested for SEL by Applied Physics Laboratory (APL). The measurements were performed only at room temperature. The lot date code was 0021. The AD9240 showed sensitivity to SEL. The LET$_{th}$ was less the 19 MeV-cm^2/mg and the saturated cross section is about 2x10^{-4} cm^2 [7].

AD9240 also was tested for SEL by the JPL group at BNL and TAMU [11]. The threshold LET in these measurements was about 15 MeV-cm^2/mg and saturated cross section was about 2x10^{-4} cm^2.

26. AD9244

The Analog Devices AD9244 is a monolithic, single 5 V supply, 14-bit, 40 MSPS/65 MSPS ADC. This device was tested for SEL at TAMU by the JPL group [5]. The threshold LET$_{th}$ was less than 16.2 MeV-cm^2/mg at room temperature.

27. LTC1417

The Linear Technology LTC1417 is a low power, 14-bit, 400-ksps sampling ADC. Lot date code 0240 was tested for SEL at TAMU by the JPL group [5]. No latchup events were observed at room temperature up to a LET of 80 MeV-cm^2/mg. One latchup was observed at an LET of 67 MeV-cm^2/mg and device temperature of 82°C. The LET threshold is therefore estimated to be approximately 67 MeV-cm^2/mg at a device temperature of 82°C. Large numbers of latchups occurred at LET of 90 MeV-cm^2/ mg and device temperature of 82°C. Latchup events were destructive.

28. *LTC1419*

The Linear Technology LTC1419 is a 800ksps, 14-bit sampling ADC that draws only 150mW from ±5V supplies.

The SEL measurements were performed at the TAMU facility by the JPL group [12]. The lot date codes were 0612. The LTC1419 was tested at room temperature and elevated temperatures of 50 and at 85°C. The sample size was 3. No latchup was observed at room and application temperature of 50°C. At evaluated temperature of 85°C latchups were observed at LET of 68.3 MeV-cm^2/mg but no latchup was observed at LET of 64.0 MeV-cm^2/mg. The latchup threshold at the elevated temperature of 85°C is therefore between an LET of 64.0 MeV-cm^2/mg and an LET of 68.3.0 MeV-cm^2/mg. In Fig. 1, we show the result of the SEL measurements at 85°C.

The JPL group latchup measurements indicate that LTC1419 is not highly sensitive to latchup. The cross section is relatively small, and rises to about 3x10^{-6} at high LETs. The LTC1419 was tested for destructive latchup by turning off latchup protection. When the device went into a latchup state, the supply current increased to ~1.2A. The lack of an

output signal from the device indicated that the device was not functioning in this high current state. To determine if this condition was recoverable, the beam was turned off and the device was power cycled. The device did not recover, after power cycling, indicating that device had destructively failed.

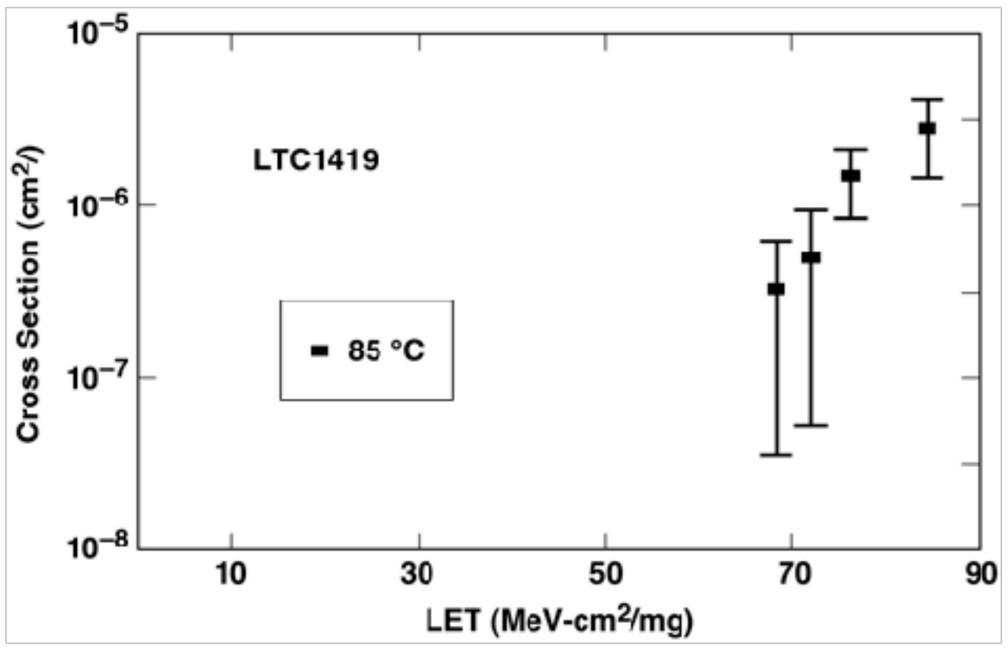

Fig.1.SEL measurements for LTC1419 at 85°C. Measurements were performed at the TAMU by the JPL group.

29. ADC14155

The Texas Instruments ADC14155 is a high-performance CMOS ADC capable of converting analog input signals into 14-bit digital words at rates up to 155 Mega Samples Per Second (MSPS). The Space Level version of the ADC14155 is immune to SEL with LET's up to 121.89 MeV/mg/cm^2 at room and elevated Temperatures [13].

30. AD9259

The Analog Devices AD9259 is a quad, 14-bit, 50Msps ADC with an on-chip sample-and-hold circuit realized in 0.18µm CMOS technology. Two parts were tested for SEL at UCL using the "High LET" cocktail. The lot date code was 0621. The devices was biased and clocked at 10Mhz while I_{dd} and functionality were monitored. The measurements were performed at only room temperature. The results showed that the AD9259 was not sensitive to SEL [10].

31. *LTC1604*

The Linear Technology LTC1604 is a 333ksps, 16-bit ADC that draws 220mW from ±5V supplies.

The SEL measurements were performed at the TAMU by the JPL group [14]. The lot date code was 0123. The LTC1604 was tested at room temperature and at 85ºC. SELs were observed at a LET of 70.0 MeV-cm^2/mg but no latchups were observed at a LET of 55.0 MeV-cm^2/mg. The latchup LET threshold is between 55 and 70 MeV-cm^2/mg. In Fig. 2, the result of room temperature measurements with that of the heated measurements are compared. As one might expect, the latchup cross section is higher for the heated device.

TAMU SEL measurements indicate that LTC1604 is not highly sensitive to latchup. The cross section is relatively small, and rises to about 10^{-6} at high LETs. The LTC1604 was tested for destructive latchup by turning off latchup protection. When the device went into a latchup state, the supply current increased to 600mA. The lack of an output signal from the device indicated that the device was not functioning in this high current state. To determine if this condition was recoverable, the beam was turned off and the device was power cycled. The device did not recover, after power cycling, indicating that device had been destructively failed.

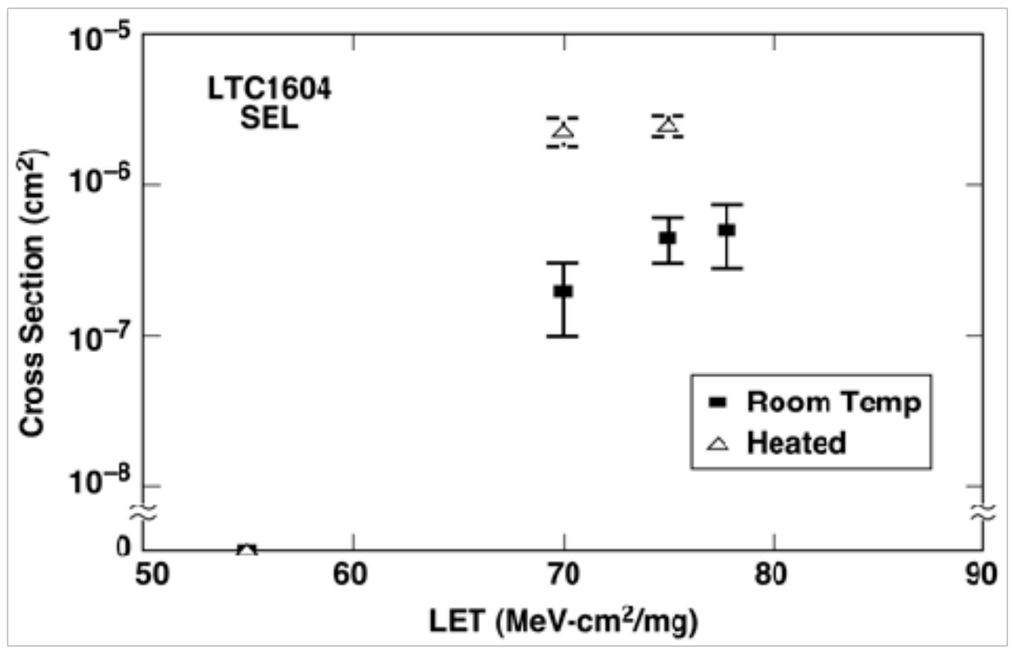

Fig. 2. Comparison of data obtained at room temperature with the heated measurement for LTC1604. Measurements were performed at the TAMU by the JPL group.

32. LTC1609

The Linear Technology LTC1609 is a 200ksps, serial 16-bit ADC that draws 65mW from ±5V supplies.

The LTC1609 serial ADC was tested for SEL at TAMU and BNL by the JPL group [14]. At both facilities devices were tested at room temperature and at an elevated temperature of 85ºC.

In Fig. 3, we compare room temperature measurements and heated measurement taken at both facilities. The square symbols represent the room temperature measurements taken at the BNL and the TAMU facilities. The triangle symbols represent the heated measurements taken at the BNL and the TAMU facilities. Although, the TAMU facility ions have longer range, there is very little difference between the two sets of data. At room temperature, the latchup LET threshold is between 8.0 and 11.7 MeV-cm^2/mg. For the heated device, the latchup LET threshold is between 5.3 and 8.0 MeV-cm^2/mg. This data indicates that LTC1609 is sensitive to latchup, and has an LET threshold of about 10 MeV-cm^2/mg. The cross section is relatively small, at low LETs, and gradually increases to about $5x10^{-4}$ at high LET (saturation cross section). As one might expect, the latchup cross section is higher for the heated measurements. There was a factor of 1.5 - 2 increase in latchup cross section for the heated device which is much less than the increase between heated and room temperature for LTC1609.

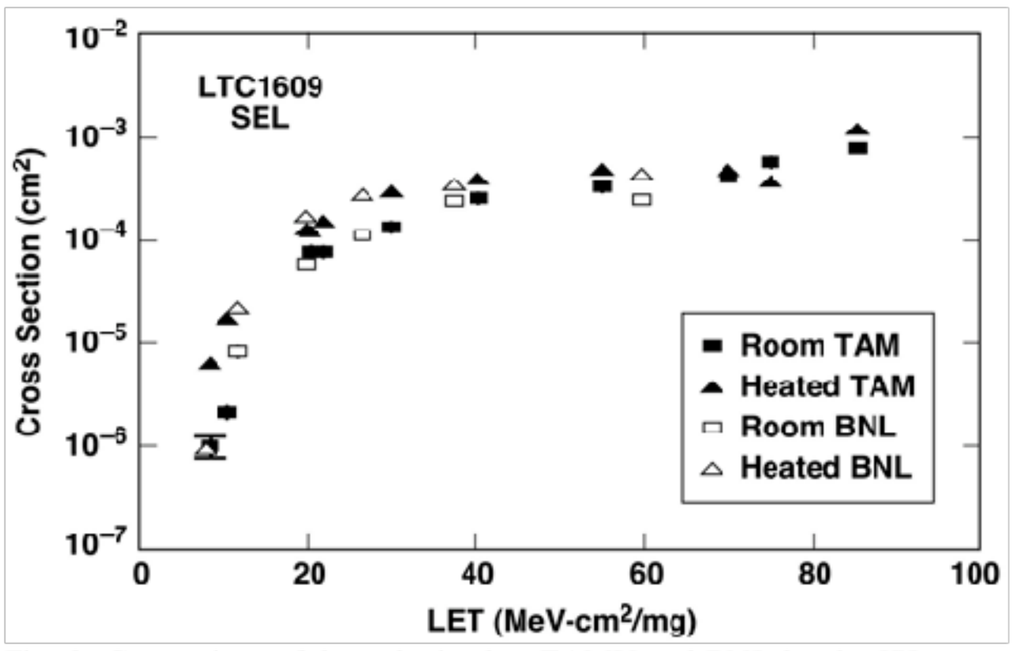

Fig. 3. Comparison of data obtained at TAMU and BNL by the JPL group for both room temperature and heated measurement for LTC1609.

LTC1609 was tested for destructive latchup. During the irradiation, with latchup current protection turned off, the supply current increased to 1.2A and the lack output signal from the device indicated that the device was not functioning. To determine if this condition was recoverable, the beam was turned off and the device was power cycled. The device did not recover and therefore had been destructively damaged.

33. LTC1608

The Linear Technology LTC1608 is a 500ksps, 16-bit sampling ADC. LTC1608 was tested at BNL for SEL at only room temperature by the Goddard. The lot date code was 0224. No SEL event was observed up to an LET of 82 MeV•cm2/mg up to a fluence of $1x10^7$ ions/cm^2 [3]. The DUTs lot date code was 0120.

Also, this part was tested for SEL at IPN tandem van de Graaf (France) [10]. The measurements were performed only at room temperature. No SEL were observed at LET of 60.4 MeV-cm^2/mg up to a fluence of $1x10^7$ions/cm^2.

34. LTC1864

The Linear Technology LTC1864 is a 250ksps, 16-bit ADC. This device was tested for SEL by the JPL group at TAMU [14]. SELs were observed at a LET of 8.5 MeV-cm^2/mg with the device at room temperature. The SEL saturated cross section was $5x10^{-5}$ cm^2. The SEL events were destructive.

35. ADS7809

The ADS7809 is a 16-bit sampling ADC from Texas Instruments using state-of-the-art CMOS structures. This part was tested at TAMU for SEL by the JPL group [5]. The measurements were performed at room temperature. The SEL LET_{th} is between 19-22 MeV-cm^2/mg.

36. AD977

The Analog Devices AD977 is a 200 ksps, high speed, low power 16-bit ADC that operates from 5V supply.

The SEL measurements were performed at the TAMU by the JPL group [15]. No latchups were observed for either at an elevated temperature of 85ºC or room temperature.

37. AD7664

The Analog Devices 16-bit AD7664 ADC was tested for SEL at BNL. The lot date code was 864065-2. The ADCs were tested under the bias conditions of + 5 V. SEL measurements were performed only at room temperature. Testing was performed to determine the latchup threshold LET. Both devices tested showed the same threshold characteristics with an LET threshold of 8-10 MeV•cm2/mg. For all test conditions, the devices were exposed to the ion beam until latchup occurred. At this point the fluence was recorded. Typically, 2 to 3 fluence readings were taken for each test condition to allow for some statistics in calculating a cross section. The reasonable estimate of the saturation cross section is $\sigma_{sat} \cong 2$ to 3 x 10^{-4} cm^2 [3].

38. MAX195

The MAXIM MAX195 is a 16-bit successive-approximation ADC that combines high speed, high accuracy, low power consumption, and a 10µA shutdown mode. This part was tested for SEL at BNL. The measurements were performed only at room temperature. The SEL LET_{th} is above 50 MeV-cm^2/mg [16].

39. ADS5483

ADS5483 is a 16-bit ADC from Texas Instruments. It is built with TI complementary bipolar process BiCom3x. The Goddard group has used the TI evaluation board, ADS548xEVM to test this part for SEL. The ADS5483 devices were tested at the TAMU using 15 MeV/amu at only room temperature. All tests were run with 10^3 <flux rate < 10^4 ions/cm^2/Sec. Effective LETs ranged from 2.5 MeV•cm^2/mg to 83.4 MeV•cm^2/mg by varying the ion and by varying the angle of incidence. No SEL events were observed up to LET >75 MeV-cm^2/mg [17].

40. LTC1605

The Linear Technology 16-bit ADC LTC1605 was tested for SEL using 15 MeV/amu ion Beams at TAMU. The lot date code was 9914. The measurements were performed at only room temperature. This part showed a very high SEL sensitivity. Latchup was not destructive [3].

41. AD976

The Analog Devices AD976 is a high speed, low power 16-bit ADC that operates from a single 5 V supply. This part was tested for SEL at IPN heavy ion facility, Orsay, France. The measurements were performed at room temperature. AD976 showed no SEL sensitivity in these measurements [16].

42. CS5016

The Cirrus Logic CS5016 is a 16-bit monolithic ADC with conversion 16.25 s. it is built on a CMOS process. CS5016 ADC was tested for SEL at UCL, Belgium. The

measurements were performed only at room temperature. CS5016 ADC showed sensitivity to SEL. The SEL LETth is around 8 MeV-cm^2/mg and the saturated cross section is about 8x10^{-3} cm^2 [16].

43. AD7621

The Linear Technology AD7621 is a 16-bit, 3Msps, charge redistribution Successive Approximation Register, fully differential ADC that operates from a single 2.5 V power supply. It is realized in 0.25µm CMOS technology. The DUTs lot date code was 0501. The AD7621AST was tested for SEL at UCL using the two available cocktails: "High LET" and "High penetration". No SEL events were observed for normal incidence Xe (LET of 55.9MeV-cm²/mg and range of 43µm) and Kr (LET of 32.4 MeV-cm²/mg and range of 92µm) up to a fluence of 1x10^7 ions/cm^2[10].

44. *AD7714*

The Analog Devices AD7714 is a 24-bit 3 V/5 V, 500 µA signal conditioning ADC.

The SEL measurements were performed at TAMU by the JPL group [15]. The lot date code was 0539. At room temperature, the latchup threshold is below LET of 27 MeV-cm^2/mg. At 85°C, the latchup threshold is below LET of 19 MeV-cm^2/mg.

In Fig. 4, we compare the result of room temperature measurements with that of the heated measurements. There was a factor of 1.5 -2.0 increase in the latchup cross section for the heated device.

The AD7714 was tested for destructive latchup by turning off latchup protection. When the device went into a latchup state, the supply current increased to 1.2A. The lack of an output signal from the device indicated that the device was not functioning in this high current state. To determine if this condition was recoverable, the beam was turned off and the device was power cycled. The device did not recover, after power cycling, indicating that device had destructively failed.

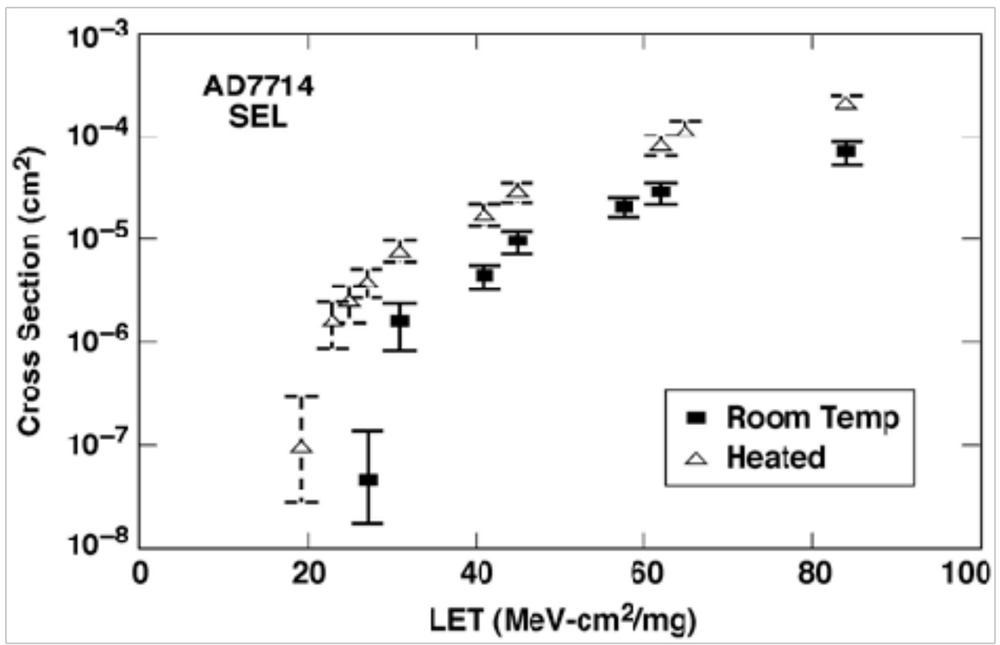

Fig. 4. Comparison of data obtained at room temperature with the heated measurement for AD7714. Measurements were performed by the JPL group at TAMU.

45. AD7760

The Analog Devices AD7760 is a high performance, 24-bit Σ-Δ ADC.

The AD7760 was tested for SEL at TAMU by the JPL group [18]. The beam flux ranged from10^4 to 10^5 ions/(cm^{2}sec). Beam fluence of 10^7 ions/cm^2 was used to determine the each cross-section point. Tests were done in the air with normal incident beam. The lot date code was 0935.

An evaluation board, EVAL-AD7760, the companion Blackfin ADSP-BF537, and evaluation software, all available for Analog Devices were used for the test. The three components provided a means of monitoring device functionality while the device was tested for SEL.

The AD7760 was tested at room temperature, and at an elevated temperature of 85°C. The sample size was 2. Latchup events were observed at both cases. The latchup events were observed at LET as low as 8.3 MeV-cm^2/mg. The latchup threshold therefore is below LET of 8.3 MeV-cm^2/mg. In Fig. 5, we compare the result of the room temperature and elevated temperature measurements. This data indicates AD7760 is highly sensitive to latchup, and has an LET threshold below LET of 8.3 MeV- cm^2/mg. Furthermore, the cross section is relatively large, and gradually rising to about 5x10^{-4} at high LET's (saturation cross section).

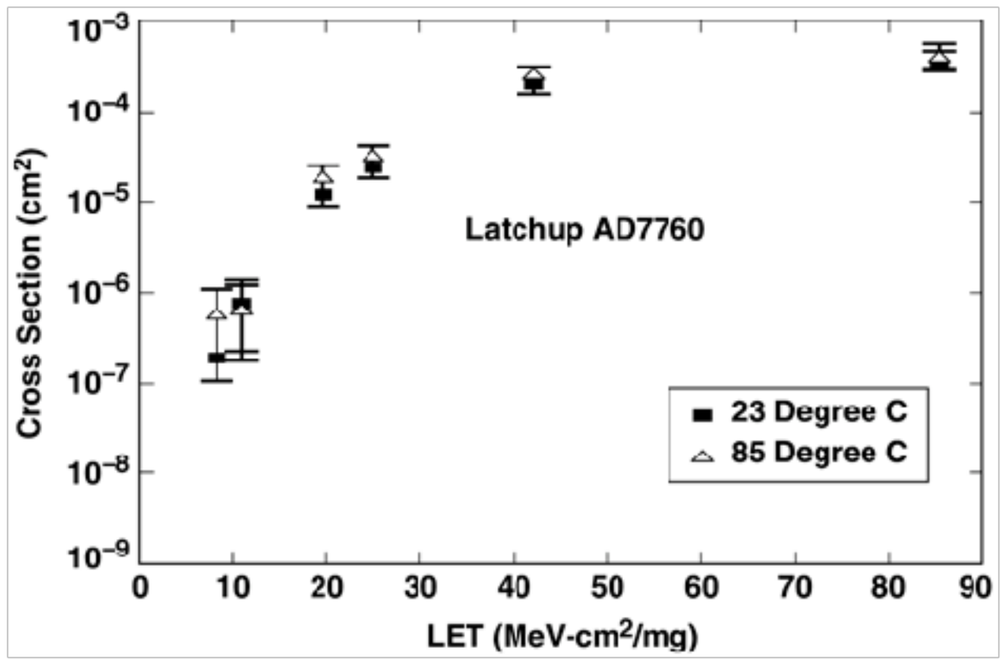

Fig. 5. SEL Measurements for AD7760 obtained at room and elevated temperature of 85 degree C. Measurements were performed at the TAMU by the JPL group.

IV. TID Test Results

1. AD670

The Analog Devices AD670, lot date code 0626, was tested for high and low dose TID by the JPL group [19]. The high dose rate was 25 rad/s and low dose rate was 0.01 rad/s at a dose rate of 50 rad/s. Parametric degradation was measured up to 40 krad(Si) at low dose rate (LDR) and 100 krad(Si) at high dose rate (HDR) for both biased and unbiased irradiation. For LDR DUTs exceeded manufacturer's specification limit for Input Bias Current starting at 6 krad(Si), with functional failure occurring between 8 and 10 krad(Si). The unbiased condition showed more parametric degradation than the biased condition typical of enhanced low dose radiation sensitivity (ELDRS) effect. DUTs continued to exceed manufacturer's specification limits and by 40 krad(Si) all samples were functionally failing with devices unable to

convert. In HDR measurements DUTs were irradiated under biased and unbiased conditions up to 100 krad(Si). DUTs exceeded manufacturer's specification limits above 10 krad(Si) and became nonfunctional between 10 and 20 krad(Si).

The Goddard group also tested AD670 lot date code 044A for TID with dose rate of 0.02 rad/s [20]. In their measurements one part failed functionally between 5 and 10 krad(Si). Two parts failed functionally between 10 and 15 krad(Si) and one part failed functionally between 15 krad(Si) and 20 krad(Si). The functional failure manifested itself as a complete failure to convert so that the digital output did not change with changes in input voltage.

2. AD7821

The Analog Devices AD7821, lot date code 9727, was tested for TID by the Goddard group [22]. The dose rate was 0.04 rad/s. During the radiation testing, eight parts were irradiated under bias and two parts were used as control samples. The total dose radiation levels were 2.5. 5.0, 10.0, 20.0, 30.0, and 50.0 krad(Si) . All parts passed all tests up to 30kRads. After the 50 krad(Si) irradiation, four parts had one Missing Code in all four Modes. One part marginally exceeded the specification limit for INL. After annealing the parts at 25°C for 168 hours, the parts showed significant recovery in Missing Codes and INL. No significant change was noted in any other parameter.

The Goddard group repeated the TID measurements on lot date code 0449B. In these new measurements, conversion errors began after 10 krad(Si); slight drop (~ 2% per 5k dose) in supply current [23].

3. ADC1175

The Texas Instruments ADC1175 was tested for TID by the Goddard group [24]. The dose rate varied from 0.04 to 0.25 rad/s. During the radiation testing, eight parts were irradiated under bias and two parts were used as control samples. The bias condition corresponds to the conversion of a 0/5V 4 MHz sinus signal with a clock frequency of 20 MHz.. The total dose radiation levels were 2.5. 4.5, 10.0, 16.0, 27.0, and 48.0 krad(Si). The Integral Non Linearity is significantly degraded on one part after 10 krad. Four parts have a power supply bias current out of specification limits after 19 krad(Si). All parts are functional up to the maximum test dose level of 48 krad(Si).

4. SPT7725

The Fairchild SPT7725 was tested for HDR TID. SPT7725 didn't show any degradation up to 100 krad. No low dose data is available for this part.

5. HI1276

No TID data is available.

6. HS-9008RH

The Intersil HS-9008RH is a radhard ADC. Per manufacturer there are no degradations up to 100 krad(Si).

7. AD571

The Analog Devices AD571, lot date code 9746, was tested for TID by the Goddard group. The dose rate was 033 rad/s. During the radiation testing, eight parts were irradiated under bias and two parts were used as control samples. The total dose radiation levels were 20, 40, 60, 80, 100, 150 and 200 krads. All parts passed all tests through 200 krad(Si) with no significant degradation in any parameter. No change was noted after any annealing step at 25°C for 24 hours [25].

8. AD9200

The Analog Devices AD9200 was tested for TID at Air Force Research Laboratory (ARFL) [26]. Two parameters, supply current (I_s) and differential non-linearity (DNL) were most sensitive parameters. Device failure was based on evaluation against these two parameters. No degradations were observed in Is and DNL up to 80 krad(Si).

9. AD574

The Analog Devices AD574, lot date code 0247A was tested for high and low dose TID by the JPL group. The high dose rate was 25 rad/s and low dose rate was 0.01 rad/s. Parametric degradation was measured up t 50 krad (Si) at low dose rate and 100 krad(Si) at high dose rate for both biased and unbiased irradiations. At high dose rate the devices tested began to exceed pre-radiation limits above 5 krad(Si) starting with 12-bit differential non-linearity, then integral non-linearity error and bipolar zero error above 20 and 50 krad(Si) respectively. All devices tested at high dose rate remained functional to 100 Krad(Si), the highest level tested. At low dose rate the devices tested passed all post-radiation specification limits up to 40 Krad. Functional failure occurred at 40 krad(Si) for the unbiased case [19].

10. AD9042

The Analog Devices AD9042 was tested for TID. The total dose tests were performed on six parts up to 1600 krad(Si). During irradiation there was virtually no change in supply current or DNL [26].

11. AD1672

No TID data is available.

12. LTC1409

The Linear Technology LTC1409, lot date code 9702 was tested for high dose TID by the JPL group [19]. The dose rate was 25 rad/s. The total dose radiation levels were 5, 10, 15, 20, 30, 50, and 100 krad(Si). The device performed within the manufacturer's specification to about 20 -30 Krad(Si), where a minor increase in IEE supply current for sleep shutdown mode begins to occur at this level. Other parameters were not significantly affected until after 100 Krad(Si). At dose levels 100 Krad(Si) and higher,

parameters such as voltage reference, bipolar offset and bipolar gain error begins to fall slightly out of specification.

13. AD1674

No TID data is available.

14. AD6640

NAVSEA Crane Division performed total dose testing on a total of five Analog Devices AD6640; three parts were statically biased, two dynamically biased. Results of the total dose testing indicate that AD6640 experienced no functional or parametric failures up to 30 krad(Si).Two devices were tested to 100 krad(Si) and no functional or parametric failures were observed [27].

15. AD7854

No TID data is available.

16. AD7858

No TID data is available.

17. AD7888

No TID data is available.

18. AD7472

The Analog Devices AD7472, lot date code 9919 was tested for TID by Applied Physics Laboratory (APL) up to 20 krad(Si). AD7472 showed parametric and functional hardness up to 10 krad(Si). Functional failure between 10 and 20 krad(Si) [7].

19. AD7476

No TID data is available.

20. AD9223

The Analog Devices AD9223 was tested for by European Space Agency (ESA). The lot date codes were 9702 and 9644. Dose rates in the range of 0.07 to 0.27 rad/s were used. TID measurements were performed in biased and unbiased conditions. The AD9223 was found to show large changes in supply current and DNL for biased devices above 10 krad(Si), but these changes annealed out. Other parameters showed little change up to 66 krad(Si) [28].

21. LTC1272

The ADC LTC1272 from Linear Technology was tested to total dose up to a dose of 30 krad(Si) at a dose rate of 0.83 rad/s. Tests have been performed at NAVSEA/CRANE laboratories [29]. Two parts were statically biased, six dynamically biased. Results of the total dose testing indicate that both devices biased statically and one device biased dynamically had missing codes at 7.5 krad(Si). Both devices biased statically showed degradation in effective number of bits at 7.5 krad(Si). Three devices biased dynamically showed degradation in effective number of bits at 7.5 krad(Si). Both devices biased statically had (maximum) differential non-linearity greater than +1.0 (specification limit) at 7.5 krad(Si). Five devices biased dynamically had (maximum) differential non-linearity greater than 1.0 at 7.5 krad(Si). Parametric shifts were observed at 5 krad(Si). All eight devices were still functional, though at a significantly degraded performance level, at 30 krad(Si). After a 168-hour biased room temperature anneal, all eight devices showed a significant improvement in performance, but did not improve to pre-rad levels.

22. AD1671

The Analog Devices AD1671, lot date code 0512was tested for TID with dose rate of 0.02 rad/s by the Goddard group [30]. No parametric degradation to 5 krads(Si). After 10 krads(Si) INL exceeded specification limits.

23. LTC1407

No TID data is available.

24. LTC2297

No TID data is available.

25. AD9240

No TID data is available.

26. AD9244

No TID data is available.

27. LTC1417

The Linear Technology LTC1417, lot date code 0240 was tested for high dose TID by the JPL group [31]. The dose rate was 25 rad/s. The total dose radiation levels were 2, 5, 7, 10, 15, 20, 25, 30, and 50 krad(Si). The device fails catastrophically at radiation levels above 30 krad(Si), and is not recommended for radiation levels above 20 krad(Si) because of the catastrophic failure mode. The results do not necessarily apply to other date codes, and lot-sample testing is recommended for devices from other date codes, or devices that are only guaranteed over the more restricted temperature range of 0 to 70 ºC because of the possibility that selection of devices that meet tighter performance requirements will skew the population towards higher radiation tolerance.

28. LTC1419

The Linear Technology LTC1419, lot date code 9926CD was tested for TID by the JPL group at a dose rate of 50 rad/s [19]. The device performed within the manufacturer's specification to about 20 Krad(Si), with a minor increase in IEE supply current at this level. Other parameters were not significantly affected up to 20 Krad(Si). Severe degradation occurred at the next test level, 30 Krad(Si), with significant increases in INL and DNL, 25 and 50 LSB respectively. Similarly, supply current increased beyond specification at this level. Due to the occurrence of functional failures at 30

Krad(Si) and the limited number of devices tested, this lot is recommended for applications below 15 Krad(Si).

29. ADC14155

The Texas Instruments ADC14155 was tested for TID by the manufacturer. The DUTs were irradiated at 3, 10, 30, 50 and 100 krad(Si). During irradiation the supply voltages were set to 2.0 and 3.9V and input clock was set to 125 MHz. The DUTs passed to 100 krad(Si) [32].

30. AD9259

No TID data is available.

31. LTC1604

The Linear Technology LTC1604, lot date code 0123 was tested for TID by the JPL group at a dose rate of 100 rad/s [19]. Functional failure in most cases was observed by 100 krad(Si). This was preceded by increasing amounts of degradation at levels less than 100 krad(Si). Most parameters exhibited significant levels of degradation at these earlier levels of dose. Functional failure was observed by 300 krad(Si) for all units. In biased units, degradation was particularly severe for both positive and negative supply currents (I_{dd} and I_{ss} respectively). These currents are related to the sleep and nap modes of operation of the device. Any departure from specification in these parameters would impact the expected power savings to be realized by use of this device in either the nap or sleep mode. Significant levels of degradation were also observed for bipolar gain error in biased units, and +/- INL and +/- DNL for all samples. These are fundamentally critical parameters of operation of any analog to digital converter. Large degradation of these parameters severely compromises the converter.

32. LTC1609

No TID data is available.

33. *LTC1608*

The Linear Technology LTC1608, lot date code 0224 was tested for TID up to 75 krad(Si) with dose rate of 0.07 rad/s. Four parts were statically biased and two parts were unbiased during irradiation. There was no significant drift up to 75krads (Si) but after 168h/100°C annealing step, biased parts were no more functional. Because of the unexpected functional failure a second test was performed at a lower final dose (40krads (Si)) and at a lower dose rate (0.03 rad/s). This test showed that all the parameters were in the specification during irradiation and after annealing [10].

LTC1608 was also tested up to 100 krad(Si) at HDR under biased and unbiased conditions by the JPL group [19]. The lot date code was 0422. The biased devices exceeded manufacturer's specification limits for levels above 10 krad(Si) and exhibited the largest amount of degradation as compared to those unbiased. The unbiased devices exceeded manufacturer's specification limits for levels above 30 krad(Si). Devices did not exhibit any functional failures or anomalies up to 30 krad(Si).

34. LTC1864

No TID data is available.

35. ADS7809

No TID data is available.

36. AD977

The AD977 from Analog Devices, lot date codes 0951 and 1020, was tested by the JPL group at low dose rate, 0.01 rad/s to 15 krad(Si). Performance of irradiation at this low dose rate was done to improve the overall performance through annealing. All devices remained within the manufacturer's specification to the highest level tested, 15 krad(Si) [33].

37. AD7664

The AD7664 16-bit ADC from Analog Devices was tested with protons at IUCF by the Goddard group. While performing other tests, the devices were left in the beam until TID failure. The devices failed at a TID of 21.7 ± 1.1 krads(Si) [24].

38. MAX195

The MAX195 from Maxim was tested for TID at a dose rate of 0.055 rad/s. The total dose radiation levels were 5, 10, 15, 20, 25, 30, and 35 krad(Si). No major parametric or functional drift was observed. The only parameter to be slightly out of specification at 35 krad is BP/UP [16].

39. ADS5483

No TID data is available.

40. LTC1605

No TID data is available.

41. AD976

The AD976 were tested for TID at a dose rate of 0.023 rad/s up to 74 krad(Si). No major parametric or functional drift was observed up to 30 krad(Si) in the 16-bit mode. In 11-bit mode, the part was functional up to 70 krad(Si)[16].

Lot date code 9723 of this part also was tested by the Goddard group [22]. HDR measurements were performed with dose rate of 0.033 rad/s. In their measurements degradation in INL and DNL were observed at TID levels below 5 Krad(Si). They noted that this part might exhibit low dose-rate susceptibility.

42. CS5016

No TID data is available.

43. AD7621

No TID data is available.

44. AD7714

The Analog Devices AD7714, lot date code 0539, was

tested for TID by the JPL group at a dose rate of 50 rad/s [19]. The failure level for all devices biased during radiation was between 10-15 krad(Si). There was no change in device parameters at irradiation levels up to 7.5 krad(Si). Small changes in parameters were seen at 10 krad(Si) but had no impact on the functionality of the devices. The failure was due to damage to the command register that prevented initializing the correct mode. The part-to-part and lot-to-lot variation is very small, and therefore, the data presented here can be applied to other lots without modification unless the die mask is changed or foundry parameters are changed.

45. AD7760

The Analog devices AD7760, lot date code 0935 was tested for TID at dose rate of 9 rad/s up to 60 krad(Si) by the JPL group [33]. The total dose radiation levels were 10, 20, 30, 40, 45, and 60 krad(Si). The TID measurements were performed using an evaluation board from Analog devices (EVAL-AD7760EDZ). Measurements were performed on 3 biased and 3 unbiased parts. No degradation were observed up to 30 krad(Si). Devices were functional up to 60 krad(Si) with some small amount of degradation in Power Down function.

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TABLE 1

Part	Manuf.	Description	Process	SEL	SEL Reference	TID	TID Reference
AD670	Analog Devices	8-bit ADC	Bipolar	SEL immune		Parametric failure at 6 krad(Si) and functionally failure between 8 and 10 krad(Si)	A.J. Kenna, et al., NSREC Data Workshop, 2009
AD7821	Analog Devices	8-bit ADC	LC^2MOS	SEL LET_{th} > 75 MeV-cm^2/mg	M. V. O'Bryan, et al., NSREC Data Workshop, 2003	In LDC 9727 measurments no degradation up to 30 krad(Si) In LDC 0449B measurements converstion errors after 10 krad(Si)	M. V. O'Bryan, et al., NSREC Data Workshop, 2000, D. J. Cochran, et al., NSREC Data Workshop, 2008
ADC1175	Texas Instruments	8-bit ADC	CMOS	SEL LET_{th} ~ 23 MeV-cm^2/mg	M. V. O'Bryan, et al., NSREC Data Workshop, 2002	Parameteric failure after 19 krad(Si). Functional to more than 48 krad(Si)	D. J. Cochran, et al., NSREC Data Workshop, 2003
SPT7725	Fairchild	8-bit ADC	Bipolar	SEL immune		No degradation error up to 100 krad(Si) in HDR. No LDR data avialable	
HI1276	Intersil	8-bit ADC	Bipolar	SEL immune			
HS-9008RH	Intersil	8-bit ADC	CMOS	SEL LET_{th} > 75 MeV-cm^2/mg @25°	Per manufacturer	Radhard 100 krad(Si)	
AD571	Analog Devices	10-bit ADC	CMOS	SEL LET_{th} > 60 MeV-cm^2/mg @25° C	M. V. O'Bryan, et al., NSREC Data Workshop, 2000	No functional failure up to 200 krad(Si)	http://radhome.gsfc.nasa.gov/radhome/papers/tid/PPM-98-024.pdf
AD9200	Analog Devices	10-bit ADC	CMOS	Susceptibile to SEL at low LETs		No degradations were observed in Is and DNL up to 80 krad(Si)	J. D. Black, et al., NSREC Data Workshop, 1998
AD574	Analog Devices	12-bit ADC	Bipolar/I^2L process	SEL immune		HDR exceed spec above 10 krad(Si). No functional failures at HDR up to 100 krad(Si). Functional failure at 50 krad(Si) at LDR	A.J. Kenna, et al. NSREC Data Workshop, 2009
AD9042	Analog Devices	12-bit ADC	XFCB	SEL immune		> 1600 krad(Si)	J. D. Black, et al., NSREC Data Workshop, 1998
AD1672	Analog Devices	12-bit ADC	BiCMOS	SEL LET_{th} > 75 MeV-cm^2/mg @25°	G. R. Allen, et al., NSREC Data Workshop, 2008		
LTC1409	Linear Technology	12-bit ADC	CMOS	SEL LET_{th} > 75 MeV-cm^2/mg @25° C	G. R. Allen, et al., NSREC Data Workshop, 2008	No signeficant deviation from manufacturer's specification up to 100 krad(Si)	A.J. Kenna, et al., NSREC Data Workshop, 2009
AD1674	Analog Devices	12-bit ADC	BICMOS II	SEL LET_{th} >37 MeV-cm^2/mg	M. V. O'Bryan, et al., NSREC Data Workshop, 2001		
AD6640	Analog Devices	12-bit ADC	XFCB	SEL immune	M. V. O'Bryan, et al., NSREC Data Workshop, 2001	> 100 krad(Si)	http://radhome.gsfc.nasa.gov/radhome/papers/N103001_AD6640.pdf
AD7854	Analog Devices	12-bit ADC	CMOS	MeV-cm^2/mg 6.7<SEL LET_{th}<11.4 MeV-cm^2/mg	M. V. O'Bryan, et al., NSREC Data Workshop, 2001		
AD7858	Analog Devices	12-bit ADC	CMOS	MeV-cm^2/mg 11.4<SEL LET_{th}<22.8 MeV- cm^2/mg	M. V. O'Bryan, et al., NSREC Data Workshop, 2001		

Part	Manuf.	Description	Process	SEL	SEL Reference	TID	TID Reference
AD7888	Analog Devices	12-bit ADC	CMOS	MeV-cm^2/mg 16.7<SEL LET$_{th}$<22.8 MeV-cm^2/mg	M. V. O'Bryan et al., NSREC Data Workshop, 2001		
AD7472	Analog Devices	12-bit ADC	CMOS	SEL LET$_{th}$ ~ 12 MeV-cm^2/mg	K. Warren, et al., NSREC Data Workshop, 2001	Functional failure between 10 to 20 krad(Si)	K. Warren, et al., NSREC Data Workshop, 2001
AD7476	Analog Devices	12-bit ADC	CMOS	SEL LET$_{th}$ < 60 MeV-cm^2/mg	K. Warren et al., NSREC Data Workshop, 2001		
AD9223	Analog Devices	12-bit ADC	CMOS	MeV-cm^2/mg 11.4<SEL LET$_{th}$ <20.0 MeV-cm^2/mg	M. V. O'Bryan, et al. NSREC Data Workshop, 2002	Large changes in Is and DNL above 10 krad(Si) for bias condition. Other parameters show little change up to 66 krad(Si)	G. R. Hopkinson, et al., NSREC Data Workshop, 2000
LTC1272	Analog Devices	12-bit ADC	BICMOS	SEL LET$_{th}$ < 5.6 MeV-cm^2/mg	M. V. O'Bryan, et al., NSREC Data Workshop, 2002	Parametric shifts were observed at 5 krad(Si)	http://radhome.gsfc.nasa.gov/radhome/papers/N121901_LTC1272.pdf
AD1671	Analog Devices	12-bit ADC	ABCMOS	SEL LETth > 75 MeV-cm2/mg @25° C	http://nepp.nasa.gov/docuploads/8742E655-056B-4568-9F06CCA49C54B502/nsrec94a.pdf	No parametric degradation to 5 krad. After 10 krad INL exceeds specification limit	D. J. Cochran et al., NSREC Data Workshop, 2006
LTC1407	Linear Technology	12 14-bit ADC	CMOS	MeV-cm^2/mg 32.4<SEL LET$_{th}$ <55.9 MeV-cm^2/mg, σ is 1x10^{-5} cm^2	F. Malou, et al., RADECS Data Workshop, 2007		
LTC2297	Linear Technology	14-bit ADC	CMOS	MeV-cm^2/mg 10.0<SEL LET$_{th}$ <20.6 MeV-cm^2/mg, σ is 4x10^{-4} cm^2	F. Malou, et al., RADECS Data Workshop, 2007		
AD9240	Analog Devices	14 bit ADC	CMOS	LET th < 19 MeV-cm2/mg @ 25° C, σ is 2x10-4 cm2	K. Warren, et al. NSREC Data Workshop, 2001, T. F. Miyahira, et al., TNS Vol. 48, no. 6, pp. 1833-1840 Dec. 2001		
AD9244	Analog Devices	14-bit ADC	CMOS	SEL LET$_{th}$ <12.9 MeV-cm^2/mg @25° C	G. R. Allen, et al., NSREC Data Workshop, 2008		
AD9240	Analog Devices	14-bit ADC	CMOS	SEL LET$_{th}$ <16.2 MeV-cm^2/mg @25° C	G. R. Allen, et al., NSREC Data Workshop, 2008	> 41 krad	
LTC1417	Linear Technology	14-bit ADC	CMOS	SEL LET$_{th}$> 75 MeV-cm^2/mg @82° C	G. R. Allen, et al., NSREC Data Workshop, 2008	Catastrophic failure at 30 krad. Not recommended above 20 krad.	R. M. Rivas, et al., NSREC Data Workshop, 2004

Part	Manuf.	Description	Process	SEL	SEL Reference	TID	TID Reference
LTC1419	Linear Technology	14-bit ADC	CMOS	MeV-cm^2/mg 64 <SEL LET$_{th}$ < 68.3 MeV-cm^2/mg @> 60° C Destructive latchup	T. F. Miyahira, F. Irom, NSREC Data Workshop, 2008	Performed within the manufacturer's specification to about 20 krad(Si), with minor increase in supply current. Recommended for use below 15 krad()Si)	A.J. Kenna, et al., NSREC Data Workshop, 2009
ADC14155	Texas Instruments	14-bit ADC	CMOS	SEL LET$_{th}$ > 75 MeV-cm^2/mg	Texas Instruments SEL test report	Good to 100 krad(Si)	http://www.ti.com/lit/an/snaa151/snaa151.pdf
AD9259	Analog Devices	14-bit ADC	CMOS	SEL LET$_{th}$ > 32.4 MeV-cm^2/mg	F. Malou, et al., RADECS Data Workshop, 2007		
LTC1604	Linear Technology	16-bit ADC	CMOS	MeV-cm^2/mg 63 < LET$_{th}$ <65 MeV-cm^2/mg @25° C MeV-cm^2/mg 55 < LET$_{th}$ <58 MeV-cm^2/mg @ 85° C Destructive latchup	F. Irom, T. F. Miyahira, NSREC Data Workshop, 2005	All device parameters remained within the manufacturer's pre-radiation specification for test levels up to 100 krad with the exception of bipolar gain error	A.J. Kenna, et al. NSREC Data Workshop, 2009
LTC1609	Linear Technology	16-bit ADC	CMOS	MeV-cm^2/mg 8.0<LET$_{th}$<11.7 MeV-cm^2/mg @25° C MeV-cm^2/mg 5.3<LET$_{th}$<8.0 MeV-cm^2/mg @85° C Destructive latchup	F. Irom, T. F. Miyahira, NSREC Data Workshop, 2005		
LTC1608	Linear Technology	16-bit ADC	CMOS	LET$_{th}$ >60 MeV-cm^2/mg	F. Malou, et al., RADECS Data Workshop, 2007, M. V. O'Bryan et al., NSREC Data Workshop 2003	No degradation up to 40 krad(Si)	F. Malou, et al., RADECS Data Workshop, 2007
LTC1864	Linear Technology	16-bit ADC	CMOS	LET$_{th}$ < 8.5 MeV-cm^2/mg @25° C Destructive latchup	F. Irom, T. F. Miyahira, NSREC Data Workshop, 2005		
ADS7809	Burr Brown	16-bit ADC	CMOS	MeV-cm^2/mg 19 <LET$_{th}$< 22 MeV-cm^2/mg @25° C	G. R. Allen, et al., NSREC Data Workshop, 2008		
AD977	Analog Devices	16-bit ADC	BiCMOS	LET$_{th}$ > 75 MeV-cm^2/mg @85° C	F. Irom, T. F. Miyahira, NSREC Data Workshop, 2006	In LDR measurments all the parameters remained within the manufacturer's specification to the highest level tested, 15 krad(Si)	J. N. Bowles-Martinez, et al., NSREC Data Workshop, 2011
AD7664	Analog Devices	16-bit ADC	CMOS	LETth ~ 8 - 10 MeV-cm^2/mg @ 25° C , σ_{sat} ~ 3x10^{-4} cm^2	M. V. O'Bryan, et al., NSREC Data Workshop, 2003	During proton irradation, failed at a TID of 21.7 ± 1.1 krads(Si)	D. J. Cochran et al., NSREC Data Workshop, 2003
MAX195	MXM	16-bit ADC	CMOS	LET$_{th}$ >50 MeV-cm^2/mg	E. Vergnault, et al., NSREC Data Workshop, 2000	No degradation or faultier up to 35 krad(Si)	E. Vergnault, et al., NSREC Data Workshop, 2000

Part	Manuf.	Description	Process	SEL	SEL Reference	TID	TID Reference
LTC1605	Linear Technology	16-bit ADC	CMOS	Destructive SEL at very low LETs	M. V. O'Bryan, et al. NSREC Data Workshop, 2003		
AD976	Aanlog Devices	16-bit ADC	BiCMOS	No latchup	E. Vergnault, et al., NSREC Data Workshop, 2000	No degradation or faultier up to 30 krad(Si)	E. Vergnault, et al., NSREC Data Workshop, 2000
CS5016	Cirrus Logic	16-bit ADC	CMOS	LET_{th} ~ 8 MeV-cm^2/mg @ 25° C, σ is 8x10^{-3} cm^2	E. Vergnault et al., NSREC Data Workshop, 2000		
AD7621	Aanlog Devices	16-bit ADC	CMOS	LET_{th} > 32 MeV-cm^2/mg @ 25° C	F. Malou, et al. RADECS Data Workshop, 2007		
AD7714	Analog Devices	24-bit ADC	BiCMOS	LET_{th} < 27 MeV-cm^2/mg @ 25° C LET_{th} < 19 MeV-cm^2/mg @85° C Destructive latchup	F. Irom, T. F. Miyahira, NSREC Data Workshop, 2006	Parametric failure at 7.5 krad. Functional failure between 10-15 krad.	A.J. Kenna, et al., NSREC Data Workshop, 2009
AD7760	Analog Devices	24-bit ADC	BiCMOS	LET_{th} < 8.3 MeV-cm^2/mg @ 25° C	S. S. McClure, et al., NSREC Data Workshop, 2010	No Degradation up to 30 krad. Functional up to 60 krad and and beyond with failures only in Power Down function.	J.N. Bowles-Martinez, et al., NSREC Data Workshop, 2011