ES3D8: FUNDAMENTALS OF MODERN VLSI DESIGN

Assignment Deadline: 24 April 2023 (week 30)

ASSIGNMENT	TITLE	SUBMISSION	WEIGHTING
ES3D8	WRITTEN REPORT BASED ON CADENCE IC DESIGN	12 noon 24 April 2023	60% (9 credits)

By successfully completing this assignment, students will demonstrate understanding of the role of Electronic Design Automation (EDA), and gain skills in the use of EDA Software for Integrated Circuit Design. The students will also be able to appreciate the properties of CMOS technology and its effect on logic implementation, optimisation and system design. They will also examine how IC technology affects logic implementation and optimisation of simple CMOS integrated circuits.

Learning Outcomes:

- Demonstrate basic knowledge on how different circuit families can be used in IC design for trade-offs in speed, power, complexity and robustness.
- Acquire skills in the use of Electronic Design Automation (EDA) Software for IC design such as Cadence.
- Use CMOS technology, design and analysis techniques for implementation of digital IC systems.

DESIGN OF A CMOS 4-BIT MAGNITUDE COMPARATOR USING CADENCE

The assignment is related to the design of a 4-bit Magnitude Comparator. You will submit a **written report (2,500 words/12 pages)** describing the design approach including simulation results, power and delay measurements and reflecting on how the design could be optimised further in terms of size, speed and power.

In addition, you will submit a zipped folder with all the design files: the schematic designs of a 4-bit Magnitude Comparator together with the simulation result files; the layout files and post layout verification and simulation result files.

In order to complete the design of a 4-bit Magnitude Comparator, you will be using the latest version of Cadence EDA software for your designs. The software is available within the School of Engineering and can also be accessed remotely through the Engineering VDI desktop system or via VPN access (instructions for both are available on ES3D8 Moodle pages).

DESIGN BRIEF

Your task is to design a 4-bit magnitude comparator. A Magnitude Comparator determines the larger of two binary numbers. Comparators are used in central processing units (CPUs) and microcontroller units (MCUs). They are used in control applications when physical variables, such as temperature, position, etc., are represented by binary numbers and compared with a reference value. They are found in biometric applications and password verification. The recommended textbook CMOS VLSI Design A Circuits And Systems Perspective (the online edition is accessible from ES3D8 Moodle pages) contains a section on comparators within Chapter 11, section 11.4.

1. You need to design your own 4-bit magnitude comparator based on your own research. Even a simple google search will give you several options that you can choose from.

2. You are required to optimise the design in terms of the number of transistors, efficient use of area, speed (propagation delay) and power consumption.

3. Submit via Tabula a **written report (2,500 words/12 pages)** in pdf format, describing the design approach including simulation results, power and delay measurements as well as the values for area efficiency, transistor count, speed, and power.

4. In addition to the written report, zip and submit all relevant design and simulation result files. The detailed instruction regarding submission of Cadence design files will be given on Moodle pages so please do follow them carefully.

5. **Important!** Tabula will allow you to submit both pdf and zipped design folder but they **must be submitted at the same time.**

SUMMARY OF ASSESSMENT CRITERIA:

Description	***% Mark***
Design and functionality of basic cells	30
Use of hierarchical design including use of structured/standard layout style	10
Design and functionality of complete (top-cell) magnitude comparator including correct post-layout simulation	20
Efficient use of area	20
Number of transistors used	10
Power consumption and propagation delay measurement results	10

N.B. submission after the deadline will attract the usual late penalties.

Professor M Cole, *February 2023*