WARWICK
SCHOOL OF ENGINEERING

Module code: **ES3B2**
Module title: **Digital Systems Design**

Assessment setter:
Dr Eduardo Wächter

Assessment Weighting:
50% of the overall module mark for ES3B2

Presentation/Demonstration of practical design:
Submit the .bit and video files on Tabula by 12 noon (mid-day), Monday, Week 31.

Submission Deadlines for written report:
Submit the design report on Tabula by 12 noon (mid-day), Monday, Week 31.

Target Learning Outcomes:

1. Through the practical use of the Verilog hardware description language (HDL), consolidate understanding of the theory of combinational and sequential circuits and how these combine in the design of digital computing circuits.
2. Devise a testing strategy and design a testbench to evaluate the functional correctness of a circuit using the testing features of the Verilog HDL and a professional standard simulator.

Feedback:
Feedback will be provided on Tabula and a cohort level feedback will be given in term 3.

Overview

The assignment involves design of an interactive game from scratch using the Nexys 4DDR FPGA development board. To do this, you will need to design a VGA controller and additional logic to draw items on screen and manage game logic. Detailed instructions are provided in further lab sheets. The game must have an 'Info box' that is displayed at all times. The Info bar colours you use must be unique to your group. It must be 100 pixels in height and span the width of the display. The Info bar should display the game name and the ID numbers of the group members. The assignment consists of practical design work, undertaken during lab sessions, with supporting work in your own time. Your work will be assessed in two stages, a practical demo of your design followed by a final report. The deadlines for both stages are shown on the cover page above. You will work in pairs for the practical part, and **write reports individually**. Anyone not in a pair by the end of the lab will be paired up.

Presentation/Demonstration of practical design

The practical part of the assignment will be assessed by the deadline shown on the cover page. You will have to submit the **.bit** file of your work and a **maximum 5 minute video**, describing how your game meets the requirements listed below. The video should capture the display only (**do not include code in your demonstration**), extra features used (leds, seven segment display, GPIO, accelerometer etc) and a voice-over describing the design of the game. Up to 50% of the marks will be allocated to this part of the assignment, based on the following breakdown:

- User control of a moving object on screen with respect for screen boundaries: up to 10%
- A map or multiple objects and interactions between them, e.g. collisions: up to 10%
- Info bar: up to 5%
- Extra features like using other board inputs/outputs (leds, seven segment display, GPIO, accelerometer): up to 10%
- Use of sprites from a memory block: up to 10%
- Marks for creative design ideas: up to 5%

Pairs will receive the same mark unless it is clear that one among the pair contributed more to the work, which will be assessed through attendance and work in the lab, and may result in deductions.

Written Report Assessment

The written report must be submitted by the deadlines shown on the cover page.
In this report, you are to describe the design you built in a maximum of 10 pages (**excluding your code, which should be included as appendix**). A good report would have the following template structure:

- Introduction to VGA
- Game idea and logical procedures:
  - Top view of the project with a figure showing how each module is connected to others.
  - Modules design: each module is explained in details separately
  - Extra features

- Testbench and tests
- Conclusion:
  - Reflection

Start from describing the VGA signalling protocol, how you built circuits to generate the correct sync pulses, pixel values and how you designed the info bar. Then, explain how you determined current pixel coordinates, how you drew objects on screen, how they move, collide and interact with each other. You should also discuss how you tested your design. Your report should be written in a formal manner, and include excerpts of code where this would assist discussion. Screen captures may also be useful. Include all your Verilog code in an appendix, clearly stating what each source file is for. Do not paste screenshots of code – **if you want syntax highlighting use an online syntax highlighting tool**. The report should conclude with a reflective section about what you liked and disliked about the project, what you learned or couldn't understand, and suggestions for improvement in the future. The 50% marks for the report will be distributed as follows:

- Introduction and Background discussion on displays/VGA: up to 5%
- Design description: up to 25%
- Testing description: up to 5%
- Code quality: up to 5%
- Presentation, accordance to report template and references: up to 5%
- Reflection section: up to 5%