1 AC-DC Converter Design and Analysis

1.1

$f = 50\,\text{Hz}$
$V_{mains} = 230\,\text{V}_{\text{RMS}}$
$V_{out} = 30\,\text{V}$
$V_{ripple} = 6\,\text{V}$
$I_{out} = 5\,\text{A}$

Firstly, the peak voltage needs to be found to determine what ratio is required for the step-down transformer.

$$\begin{aligned}\hat{V} &= \sqrt{2}V_{RMS} \\ &= \sqrt{2} \cdot 230\,\text{V} \\ &= 325.269\,\text{V}\end{aligned}$$

To find the transformer specifications, the peak voltage can be divided by the desired output plus half the permitted ripple. This returns the ratio of windings.

$$\begin{aligned}N_{ratio} &= \frac{\hat{V}}{V_{out} + \frac{1}{2}V_{ripple}} \\ &= \frac{325.3\,\text{V}}{30\,\text{V} + 3\,\text{V}} \\ &= 9.86\end{aligned}$$

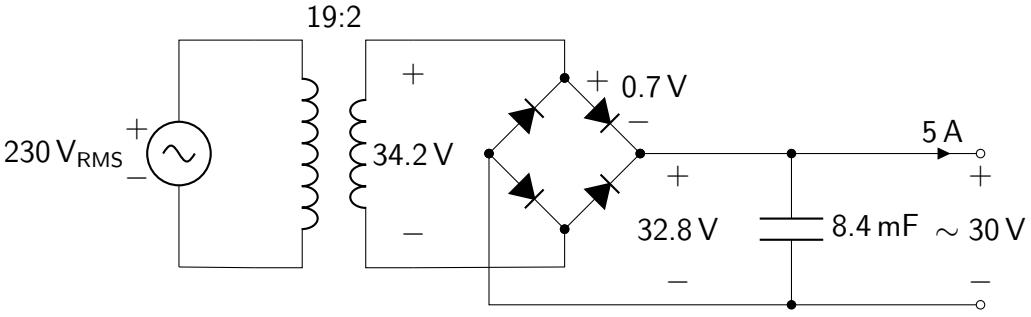
Rounded down to allow some buffer for voltage drops across components during rectification and filtering, it is found that a ratio of 9.5:1 (19:2) provides a voltage of 34.24 V. Each diode must be rated above this to prevent reverse breakdown. Furthermore, the load circuit requires 5 A of current. The diodes must be rated at ten times this ($\sim 50\,\text{A}$) due to peak pulsed current draw by the capacitor.

Full-bridge rectification means that two diodes are conducting each half cycle. Each drops 0.7 V. The peak voltage after rectification is 32.84 V, meaning the voltage across the load should be $29.84 \pm 3.00\,\text{V}$ given correct capacitor choice.

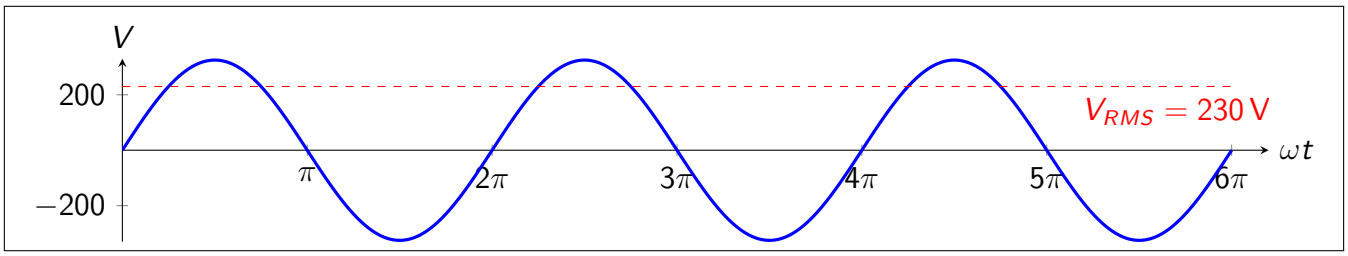
Using only capacitor smoothing, the minimum value can be found:

$$\begin{aligned}C &= \frac{\hat{I}}{2f \cdot \Delta V} \\ &= \frac{5\,\text{A}}{2 \cdot 50\,\text{Hz} \cdot 6\,\text{V}} \\ &= 8.\overline{3}\,\text{mF}\end{aligned}$$

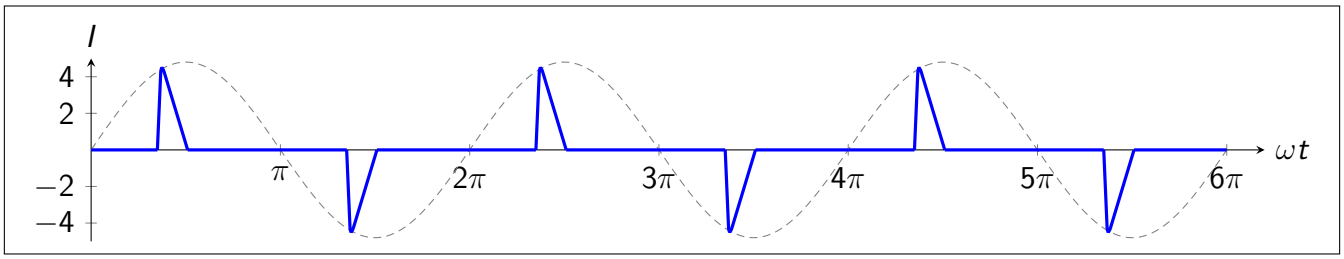
This results in the following circuit:



The voltage and current at the source are demonstrated by the following two graphs:



Source voltage



Source current

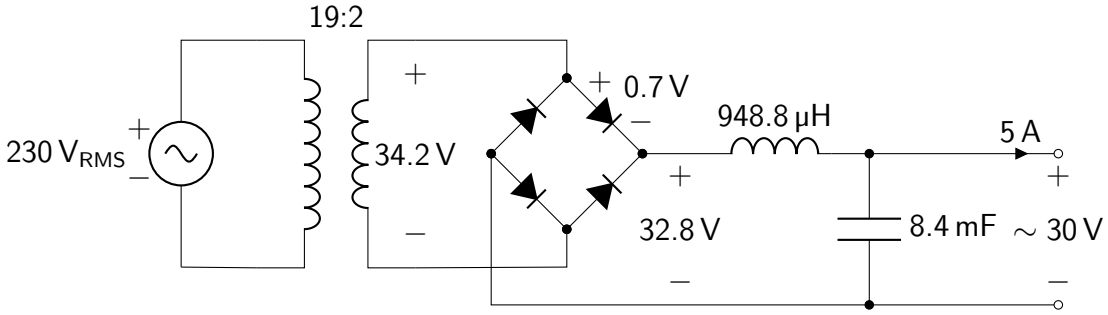
Alternatively, smoothing using an LC filter can be used, but first, the inductor value must be specified.

$$\frac{\Delta V}{V_{out}} = \frac{\sqrt{2}}{3}\left[\frac{1}{(4\pi f)^2 LC - 1}\right]$$

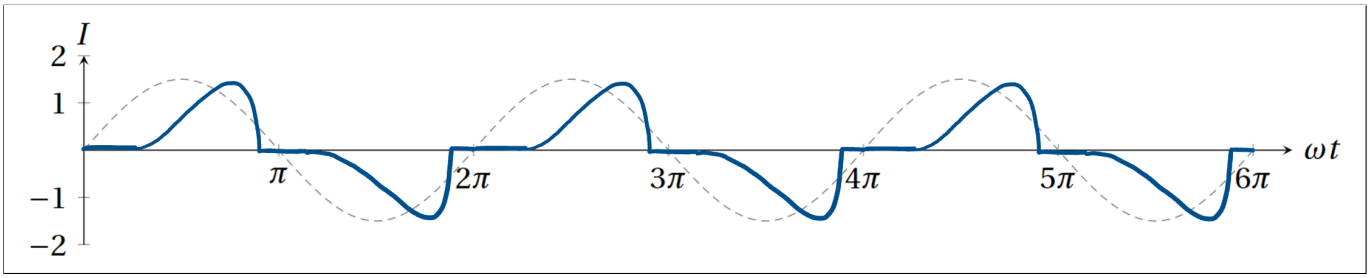
$$\frac{6}{30} = \frac{\sqrt{2}}{3}\left[\frac{1}{(200\pi)^2 L \cdot 8.4\,\text{mF} - 1}\right]$$

$$\implies L = 948.8\,\mu\text{H}$$

The following circuit now has an LC filtering element.



The resultant voltage waveform remains the same at the source (although the load voltage will have reduced slightly without modifications to the windings etc.), however the current waveform appears as follows:



Source current

1.2

2 DC-DC Converter Design and Specifications

$V_{in} = 30\,\text{V}$
$V_{out} = 48\,\text{V}$
$P = 100\,\text{W}$
$\Delta V = 100\,\text{mV}$
$f = 25\,\text{kHz} \implies T = 4 \times 10^{-5}\,\text{s}$

From the parameters above, the peak current can be found. The inductor needs to operate above this. Furthermore, the capacitor needs to operate above V_{out}.

$$\begin{aligned} I_{max} &= \frac{P}{V_{out}} \\ &= \frac{100\,\text{W}}{48\,\text{V}} \\ &= 2.08\overline{3}\,\text{A} \end{aligned}$$

Using this, the duty cycle can be found.

$$\begin{aligned} \rho &= 1 - \frac{V_{out}}{V_{in}} \\ &= 1 - \frac{30\,\text{V}}{48\,\text{V}} \\ &= \frac{3}{8} \end{aligned}$$

Finally, the capacitor and inductor values can be calculated.

$$\begin{aligned} C_{out} &= \frac{I_{max}\rho}{f \cdot \Delta V} \\ &= \frac{2.08\overline{3}\,\text{A} \cdot \frac{3}{8}}{25\,\text{kHz} \cdot 100\,\text{mV}} \\ &= 312\,\mu\text{F} \end{aligned}$$

$$\begin{aligned} L &= \frac{V_{in}\rho T}{2 \cdot I_{max}} \\ &= \frac{30\,\text{V} \cdot \frac{3}{8} \cdot 4 \times 10^{-5}\,\text{s}}{2 \cdot 2.08\overline{3}\,\text{A}} \\ &= 104\,\mu\text{H} \end{aligned}$$

The found capacitor and inductor values are the minimum, therefore the next highest value of the units available need to be used. The 150 µH (rated 6.5 A) inductor and 330 µF (rated 63 V) capacitor are chosen.

3 Boost Convertor Experiment Report

3.1 Abstract

The purpose of this laboratory was to design a DC/DC 30 V-48 V boost converter and experimentally test its performance. The boost convertor designed was subjected to up to a 75 W load in 25 W increments, with measurements taken of various parameters, including output voltage, inductor current, and duty ratios of the converter switching transistor. The circuit was not tested to the designed conditions precisely, and therefore does not perform exactly to specification. For most areas except ripple voltage, the circuit parameters are within reasonable expection.

Furthermore, different switching control systems were used to compare the performance of the circuit under changing conditions. The results show that the circuit performance can be improved for specific metrics, however some trade-offs need to be made. Open-loop control is the simplest to implement and no further power draining circuitry, however suffers from limited flexibility to changing loads. Proportional control introduces extra load on the circuit, but does not manage to make power efficiency improvements to counteract this. It did have the quickest response time. Proportional and integral control showed the best efficiency,however suffered the greatest rise time and may not be suitable in applications where response time is vital.

3.2 Introduction

3.2.1 Aims

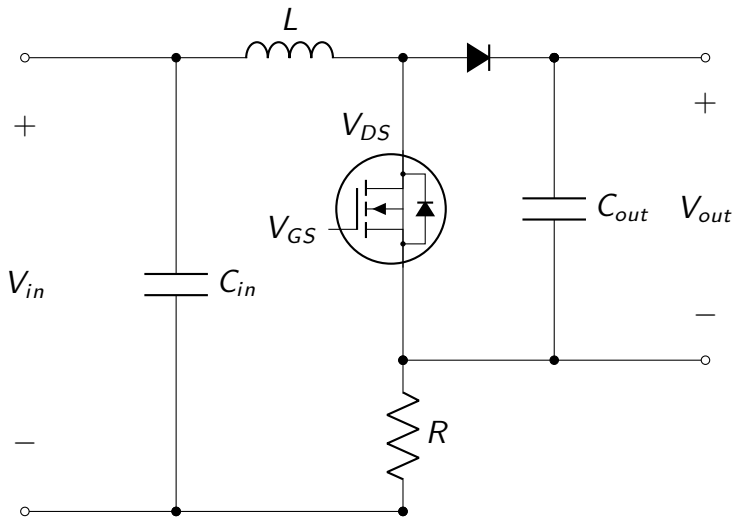
This report will detail the process of experimentally testing the performance of the boost converter, parameters for which specified in Section 2. The experiment additionally tests the converter performance under different control systems: open-loop control, proportional control, and finally proportional and integral control.

The experiment will be used to compare theoretical ideal performance to observed real performance under different conditions.

3.2.2 Theory

A boost converter ensures that the output voltage is higher than the input voltage. It does this by leveraging an inductor's tendency to oppose changes in current by adjusting its voltage.

The following diagram demonstrates a simple boost converter circuit, as will be used in this experiment.



The converter circuit operates in two states depending on whether the MOSFET switch is 'open' (not conducting) or 'closed' (conducting).

Open Current flows to the diode and capacitor, resulting in higher overall circuit impedance. The inductor compensates by developing a voltage in series with the source in order to maintain current from the 'closed' stage. This results in a greater voltage at the output.

Closed Current flows throught the MOSFET as the path of least resistance, effectively closing the circuit off from the diode onwards. The inductor charges its magnetic field during this stage. The output capacitor C_{out} maintains the voltage to the output during this stage, as it was charged to the voltage of the parallel output. The diode prevents backflow from the capacitor.

Continuous mode Continuous mode for a boost converter means the inductor current is continous - in other words, it never drops to 0 or becomes discontinuous. Discontinous conduction can occur if the current ripple is too large (due to insufficient load) or the MOSFET is not switched quickly enough (V_{GS} is pulsed too slowly), allowing the inductor to discharge completely.

Additional components The circuit specified uses two additional components that are not fundamental to an ideal boost converter circuit. Resistor R manages large current discharge through the MOSFET during the 'closed' stage. Capacitor C_{out} smooths the input as the DC signal is not ideally flat.

Control systems The experiment will be performed with three control systems: open-loop, proportional, and proportional and integral control. Open-loop control requires the response of the circuit to be adjusted externally. While the simplest to implement, it requires external input to adjust for any changes in the load. Closed-loop systems, on the other hand, can respond to changing conditions automatically with no external input required. However, reduced steady-state error may come at the cost of greater response time, especially where integral controllers are used. With no differential controller, overshoot is also likely to increase. Many of these drawbacks can be minimised with suitable parameter choices, however this requires complex analysis of the system and its responses, and would likely prove to become more complex than the boost converter circuit itself.

3.3 Method

3.3.1 Equipment

The experiment requires a number of components in order to test the design. The design portion of this experiment involves selecting an inductor and capacitor from an available range.

In addition to these two components, the following equipment is also required:

- ES3E0 experimental test board - comes with:
  - IRFI14110G MOSFET
  - UF5401 diode
  - LM3524 PWM controller
- 36 V capable DC power supply
- Oscilloscope
- 100 W load bank with 25 W increments - caution: may get hot with continuous load; use for minimum time necessary for measurements
- Voltmeter
- Ammeter

3.3.2 Method

Setup

1. Connect the power supply to the experimental test board 0 V and VIN terminals
2. Set the output voltage of the power supply to 30 V
3. Set the current limit to 6 A
4. Ensure VOUT SET is at minimum (turned fully anti-clockwise)
5. Fit the chosen specified capacitor and inductor into the board. Also include an input capcitor as part of the circuit (can be of any appropriate size - 1000 µF suggested)
6. Connect the load bank to the boost converter output (VOUT), including an ammeter in series and a voltmeter in parallel
7. Ensure the load bank is switched off (0 %)
8. With everything set up, enable the power supply

Open-loop system test

Purpose The boost converter is operated in open-loop mode. The VOUT SET potentiometer on the experimental board controls the duty cycle of the MOSFET, thereby manually setting the output voltage of the converter.

The steady-state power losses and output voltage ripples will be measured.

There are two experiments performed to test the open-loop system parameters: steady-state and transient. The steady-state test observes how the converter works under typical use. The transient test observes the converter when it is first powered on with no load.

Steady-state Switch SW1 (LOOP CONTROL) to OPEN and SW4 (STEP INPUT) to OFF. Set the load bank to 50 % by switching on two switches. Set the output voltage to 48 V using the VOUT SET potentiometer. This can be done using the rotating the potentiometer clockwise until the multimeter across the output reads 48 V.
Record:

1. Inductor current
   - Maximum
   - Minimum
   - Period
2. Output voltage ripple
   - Maximum
   - Minimum
   - Period
3. Duty ratio
4. Switching frequency
5. Voltages V_{GS} and V_{DS}
6. Input and output voltages and currents

The power supplied and provided, and subsequently the overall efficiency can then be calculated.

Transient Set the load bank to 25 % by switching on one switch and set VOUT SET to minimum by rotating fully anti-clockwise. Switch STEP INPUT from OFF to STEP 1 to introduce a step input signal. The oscilloscope will need to be set up to record 35 V rising edge transients.
Record:

1. Initial voltage
2. Final voltage
3. Start time
4. End time

Repeat this experiment with the load bank set to 50 % by switching on an additional switch.

Closed-loop system test

Purpose Manually setting the duty cycle suffers from not only limited accuracy but also difficulty maintaining a setpoint where the load varies. Closed-loop system control uses feedback to adjust the duty cycle in order to account for flunctuating load, thereby maintaining the desired setpoint. This can be achieved by using a proportional and integral (PI) controller.

Two tests will be defined - one with proportional control only, and a second with proportional and integral control.

Proportional control Set switch SW1 to PI CTRL, SW2 to Integrator OUT, SW4 to Step input OFF. Ensure the VOUT SET potentiometer is set to minimum (turned fully anti-clockwise). Set load to 25 %. Switch Step Input to STEP 1. Adjust the proportional gain potentiometer (K_P) to give an output of 35 V. Toggle the Step Input switch to measure both transient and steady-state parameters.
Record:

- Transients
    1. Initial voltage
    2. Final voltage
    3. Start time
    4. End time
- Ripple
    1. Maximum voltage
    2. Minimum voltage
    3. Period
- Proportional controller output
- Duty ratio, especially during transient period
- Input and output voltages and currents

Repeat the experiment with the load set to 50 %. Additionally, change the reference voltage to 40 V by switching Step Input from STEP 1 to STEP 2, holding the position to take readings.

Proportional and integral control Set switch SW2 to integrator IN and SW4 STEP INPUT to OFF. Wnsure VOUT SET is at minimum (turned fully anti-clockwise). Reset proportional (K_P) and integrator (K_I) potentiometers to centre. Switch integral capacitor SW3 to 47 nF. Set load to 50 % and STEP INPUT from OFF to STEP 1.
Record:

- Transients
    1. Initial voltage
    2. Final voltage
    3. Start time
    4. End time
- Ripple
    1. Maximum voltage
    2. Minimum voltage
    3. Period
- Proportional and integral controller output
- Duty ratio, especially during transient period
- Input and output voltages and currents

Repeat the experiment with the load set to 75 %.

3.4 Results

3.4.1 Open-loop system tests

Table 1: **Open-loop steady-state inductor current (measured at 50 mV/A)**

Maximum current	Minimum current	Peak-to-peak ripple current	Average current	Period	Frequency
3.58 A	0.22 A	3.36 A	1.9 A	42.40 µs	23.6 kHz

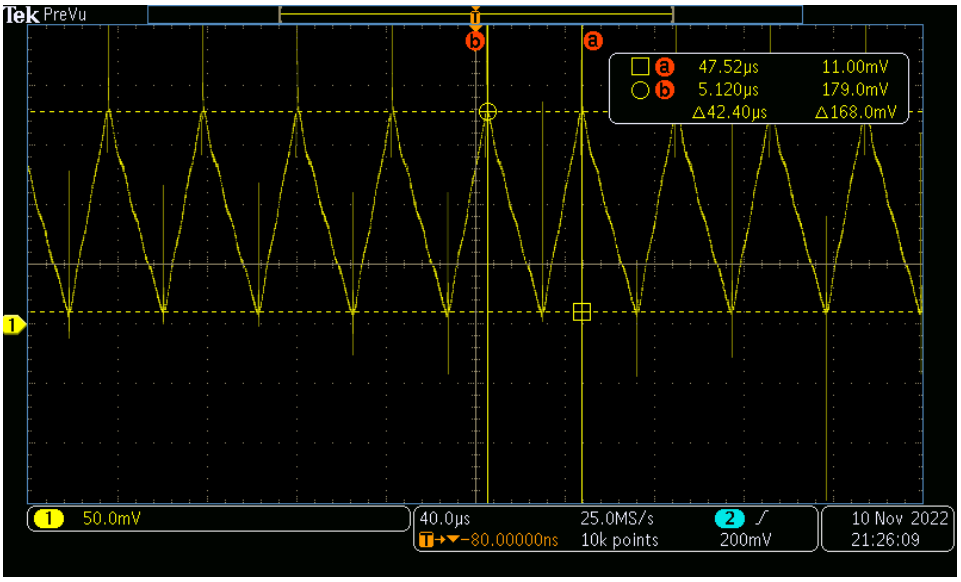


Figure 1: Inductor current (measured at 50 mV/A)

Table 2: **Open-loop steady-state ripple voltage**

Maximum voltage	Minimum voltage	Peak-to-peak ripple voltage	Period	Frequency
254.0 mV	−274.0 mV	528 mV	42.40 µs	23.6 kHz

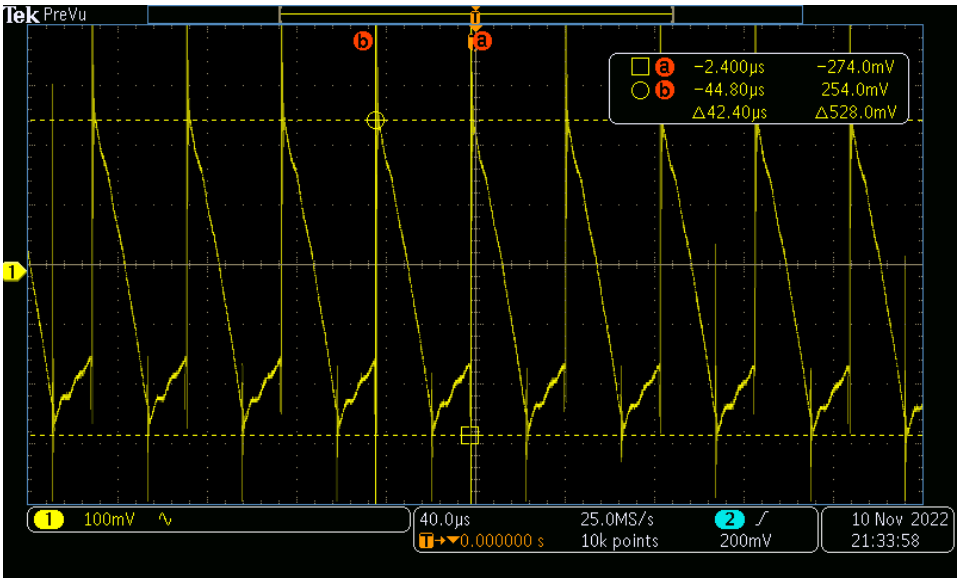
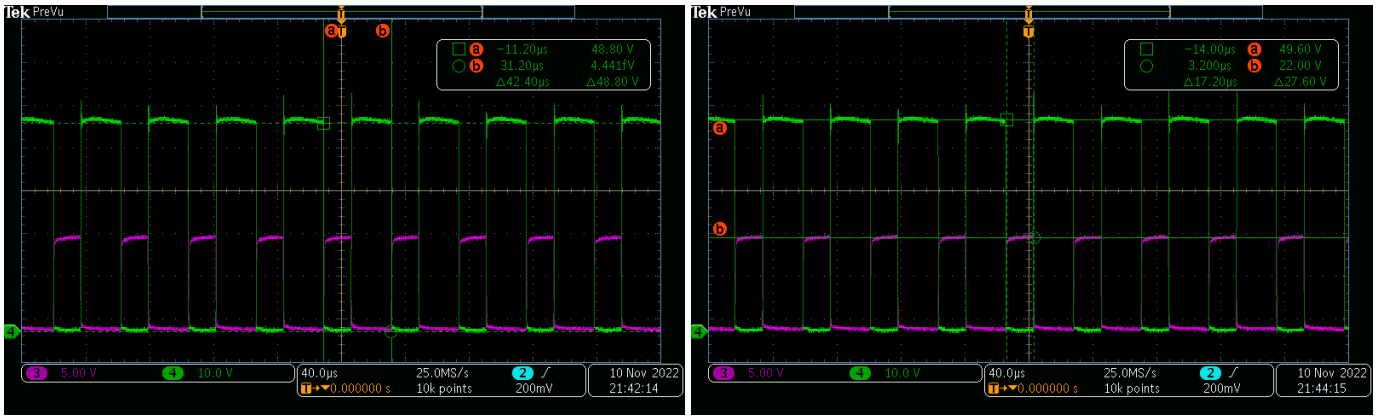


Figure 2: Ripple voltage

Table 3: **Open-loop steady-state switching signals**

Duty ratio	Frequency	V_{GS} voltage	V_{DS} voltage
0.575	23.6 kHz	22.0 V	49.6 V



(a) Duty cycle measurement (b) Terminal voltages V_{GS} and V_{DS}

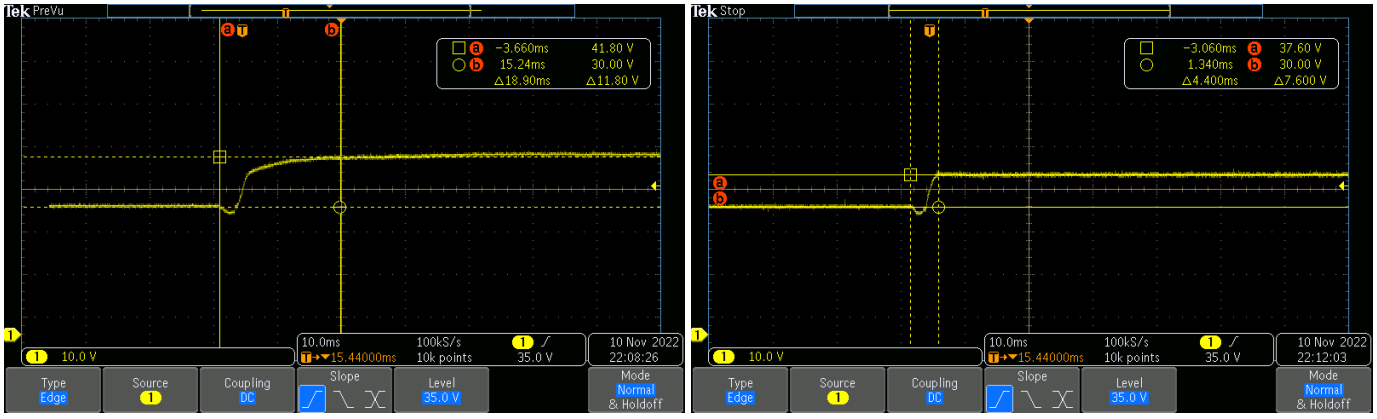
Figure 3: Switching signals

Table 4: **Open-loop steady-state efficiency**

Input current	Output current	Input voltage	Output voltage	Input power	Output power	Efficiency
1.91 A	1.02 A	30 V	48 V	57.3 W	49.0 W	85.5 %

Table 5: **Open-loop transient parameters**

Initial voltage	Final voltage	Start time	End time	Rise time
25 % load				
30 V	41.8 V	−3.66 ms	15.24 ms	18.9 ms
50 % load				
30 V	37.6 V	−3.06 ms	1.34 ms	4.4 ms



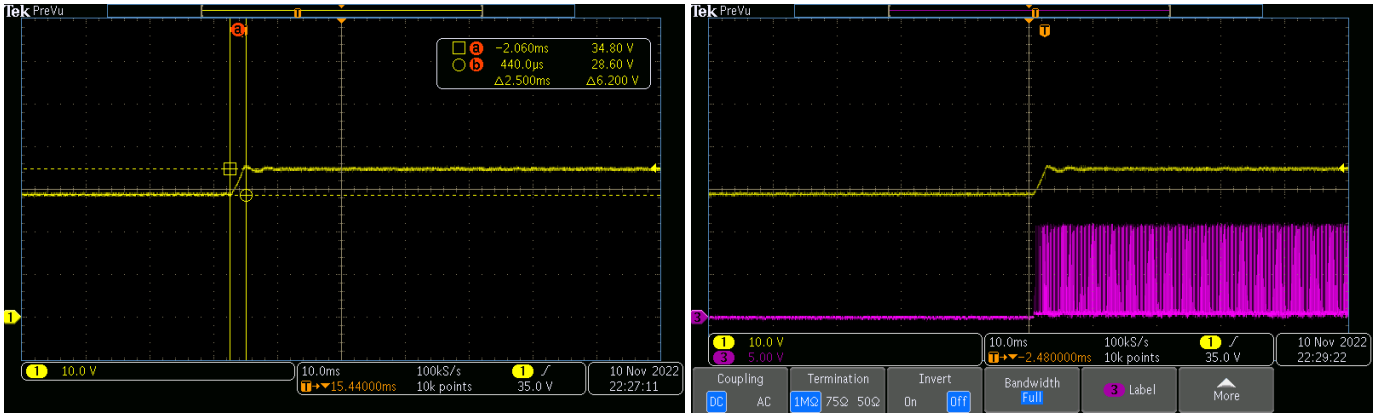
(a) 25 % load (b) 50 % load

Figure 4: Transient parameters

3.4.2 Closed-loop system test

Table 6: **Proportional control transient parameters (25 % load)**

Initial voltage	Final voltage	Start time	End time	Rise time
28.6 V	34.8 V	−2.06 ms	440.0 µs	2.5 ms



(a) Transient capture (b) Proportional controller response

Figure 5: Transient parameters (25 % load)

Table 7: **Proportional control ripple voltage (25 % load)**

Maximum voltage	Minimum voltage	Peak-to-peak ripple	Period	Frequency
180 mV	−48 mV	228.0 mV	42.4 µs	23.6 kHz

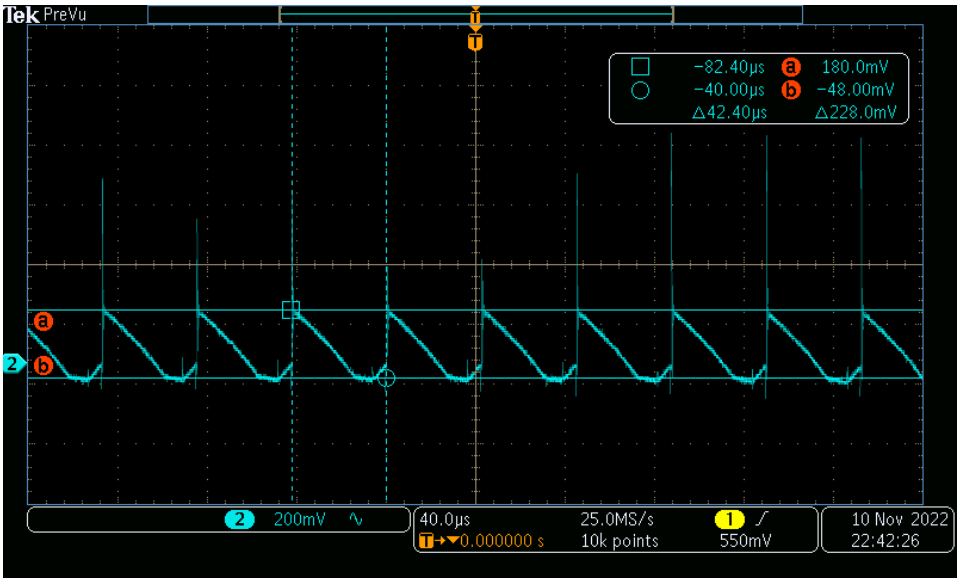


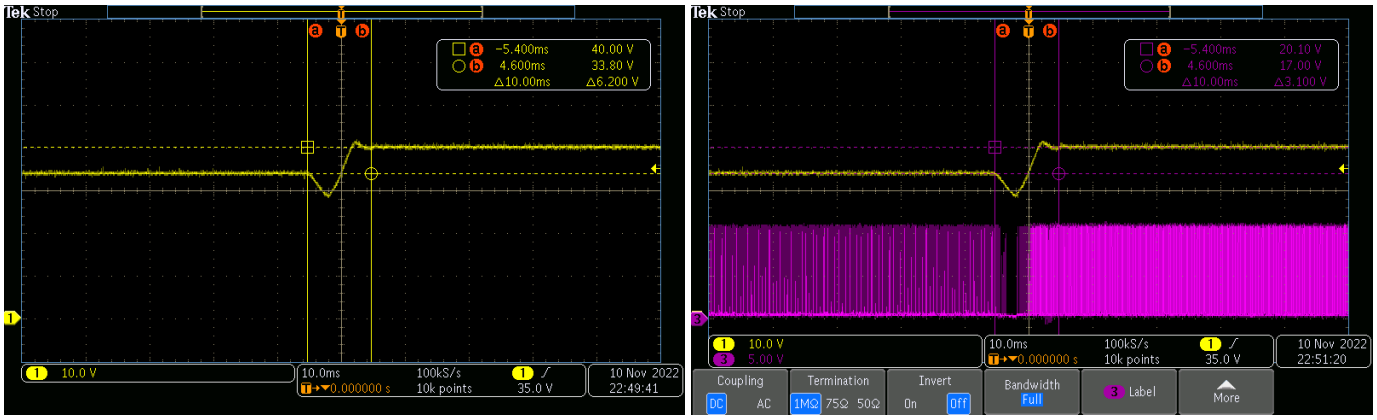
Figure 6: Ripple voltage (25 % load)

Table 8: **Proportional control efficiency (25 % load)**

Input current	Output current	Input voltage	Output voltage	Input power	Output power	Efficiency
0.564 A	0.384 A	30.0 V	35.0 V	16.92 W	13.44 W	79.4 %

Table 9: **Proportional control transient parameters (50 % load)**

Initial voltage	Final voltage	Start time	End time	Rise time
33.8 V	40 V	−5.4 ms	4.6 µs	10 ms

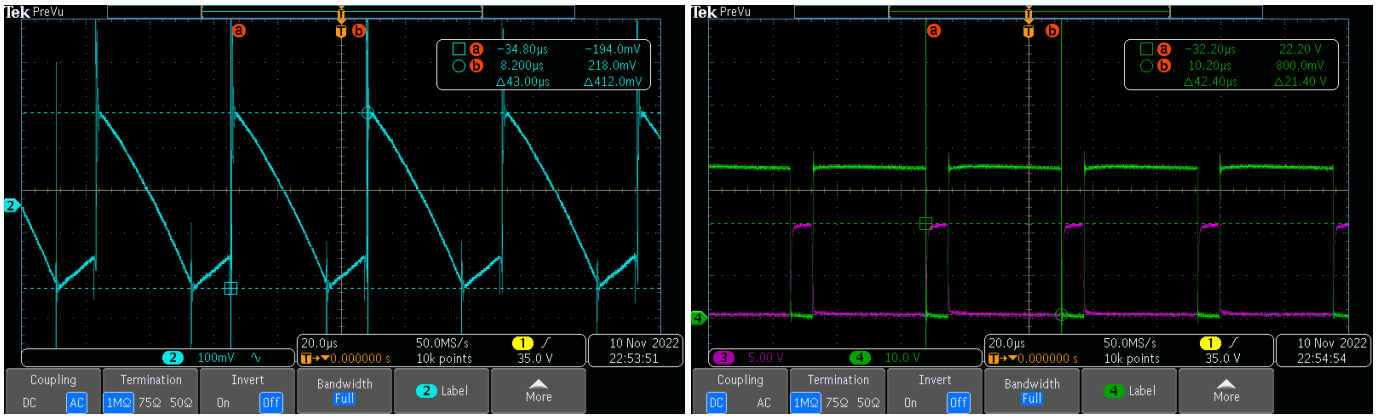


(a) Transient capture (b) P controller response

Figure 7: Transient parameters (50 % load)

Table 10: **Proportional control ripple voltage (50 % load)**

Maximum voltage	Minimum voltage	Peak-to-peak ripple	Period	Frequency
218 mV	−194 mV	412.0 mV	43.0 µs	23.3 kHz



(a) Ripple voltage (50 % load) (b) Duty cycle

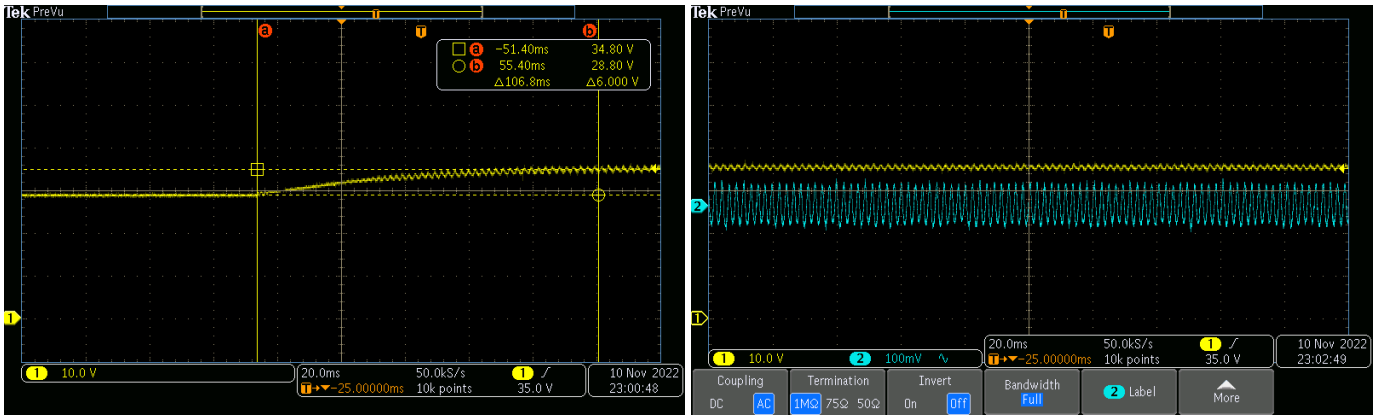
Figure 8: Output captures

Table 11: **Proportional control efficiency (50 % load)**

Input current	Output current	Input voltage	Output voltage	Input power	Output power	Efficiency
1.344 A	0.857 A	30.0 V	40.2 V	40.32 W	34.45 W	85.4 %

Table 12: **Proportional and integral control transient parameters (50 % load)**

Initial voltage	Final voltage	Start time	End time	Rise time
28.8 V	34.8 V	−51.4 ms	55.4 µs	106.8 ms



(a) Transient capture (b) PI controller response

Figure 9: Transient parameters (50 % load)

Table 13: **Proportional and integral control ripple voltage (50 % load)**

Maximum voltage	Minimum voltage	Peak-to-peak ripple	Period	Frequency
710 mV	380 mV	330 mV	42.4 µs	23.6 kHz

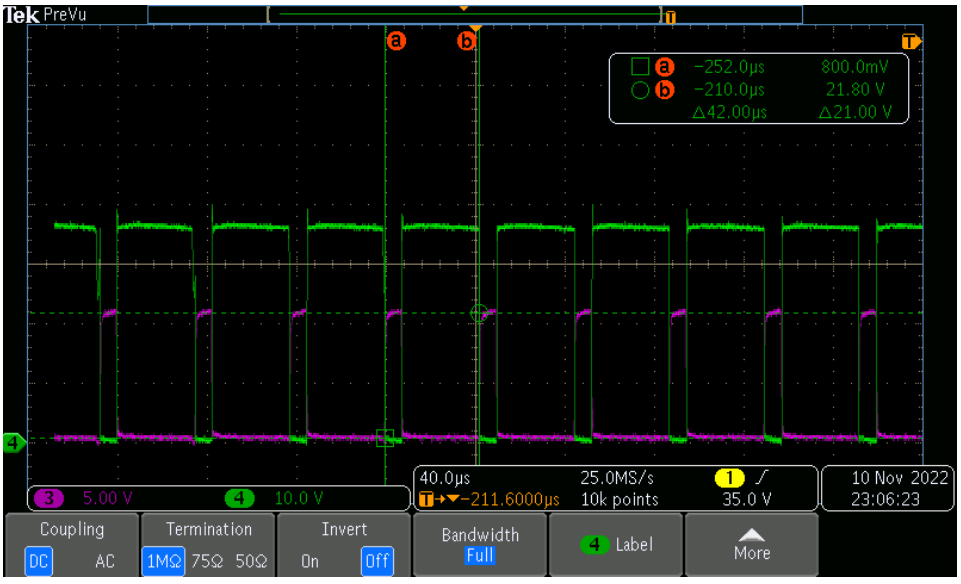


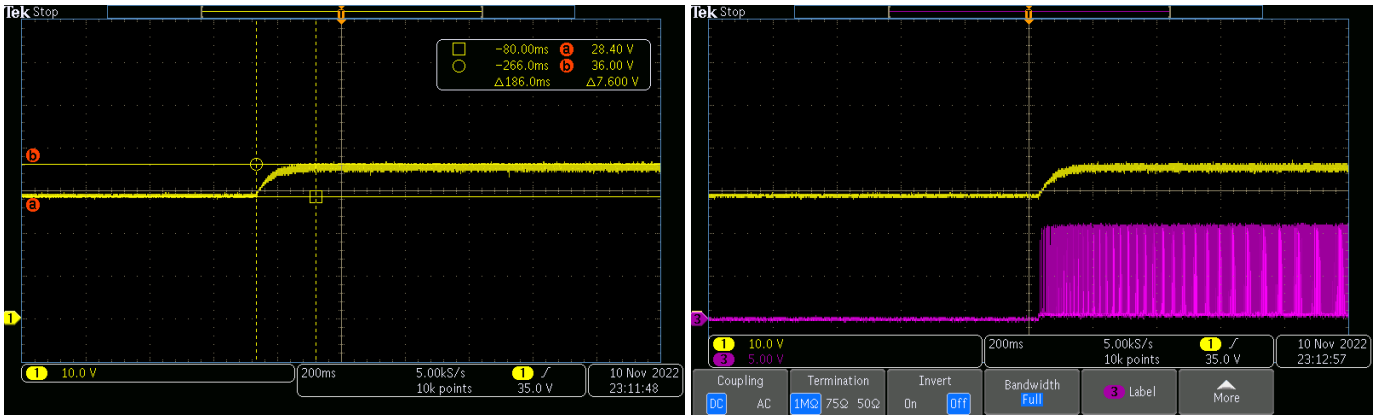
Figure 10: Duty cycle

Table 14: **Proportional and integral control efficiency (50 % load)**

Input current	Output current	Input voltage	Output voltage	Input power	Output power	Efficiency
1.045 A	0.755 A	30.0 V	35.41 V	31.35 W	26.73 W	85.3 %

Table 15: **Proportional and integral control transient parameters (75 % load)**

Initial voltage	Final voltage	Start time	End time	Rise time
28.4 V	36.0 V	−266 ms	−80 µs	186 ms

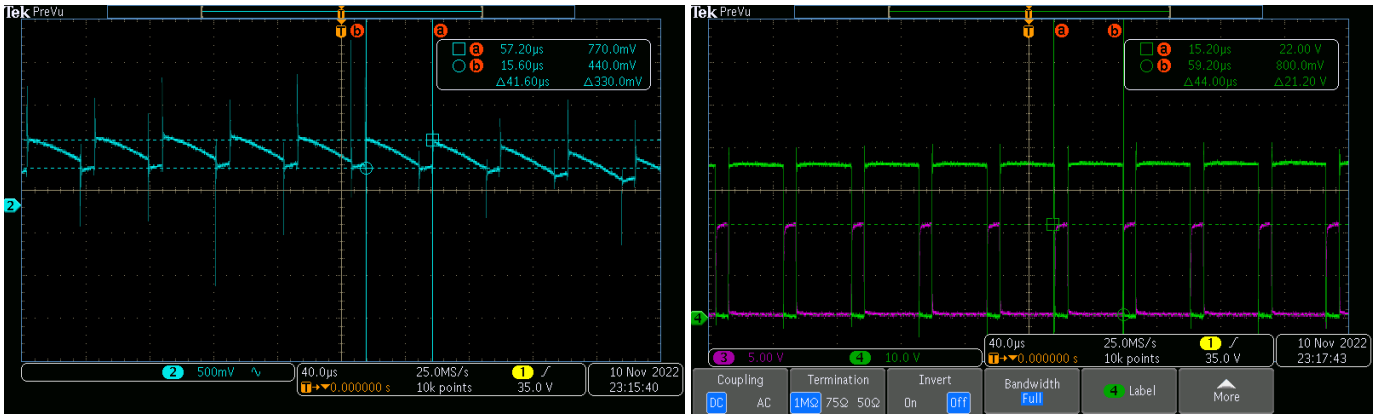


(a) Transient capture (b) PI controller response

Figure 11: Transient parameters (75 % load)

Table 16: **Proportional and integral control ripple voltage (75 % load)**

Maximum voltage	Minimum voltage	Peak-to-peak ripple	Period	Frequency
770 mV	440 mV	330 mV	41.6 µs	24.0 kHz



(a) Ripple voltage (75 % load) (b) Duty cycle

Figure 12: Output captures

Table 17: **Proportional and integral control efficiency (75 % load)**

Input current	Output current	Input voltage	Output voltage	Input power	Output power	Efficiency
1.509 A	1.119 A	30.0 V	35.41 V	45.27 W	39.62 W	87.5 %

3.5 Analysis

Open-loop system

Steady-state The first tests involve an open-loop control system. Here (Table 1), the inductor parameters were observed. The inductor is operating comfortably below its maximum rated current. Conduction is on the threshold of dicontinuity.
The steady-state peak-to-peak ripple voltage voltage (Table 2) reaches 528 mV which is somewhat large, however ultimately 1 % of the output.
The frequency of both signals and transistor switching align, which is expected. The V_{DS} voltage is larger than the output voltage which hints to losses occuring within the circuit.
Efficiency appears at 85.5 %, which is quite good. Power draw is fairly large, but not out of expectation due to the large voltage requirements.

Transient The transient parameters in Table 5 show different responses to increased load. The final voltage is lower than expected, likely due to an error in the experimental procedure where the duty ratio was set with no load. Qualitatively, the output voltage decreases with a greater load, as does the rise time (by a factor of 7.5).

Proportional control

25 % load The initial voltage is slightly below 30 V. The output voltage was set at 35 V which is somewhat smaller which may have led to a quicker rise time of the circuit (2.5 ms). Figure 5 shows the proportional controller begin pulsing rapidly and continuously once the converter is enabled. The peak-to-peak ripple has also reduced to 228 mV, suggesting a smoother circuit. The frequency has as yet remained the same.
Due to the smaller output, the current draw requirements are also smaller, with almost a quarter the current draw of the open-loop circuit. The efficiency has decreased, which suggests that the controller introduces some losses on the circuit.

50 % load The initial voltage is not 30 V due to the experiment being performed with an increase to 50 % from 25 %, rather than from 0 %. This may have reduced the rise time. This is further evidenced by the controller in Figure 7b operating in the 'initial' region. After the load is increased, the controller responds by pulsing more frequently.
The frequency appears to have decreased, however this may be within measurement error as, while the period for the ripple voltage in Table 10 has increased, the period in Figure 8b appears the same as in previous experiments.
Efficiency has increased by six percentage points, which indicates better power management on either higher loads or higher output voltages.

Proportional and integral control

50 % load The initial voltage is slightly below 30 V at 28.8 V. The final voltage is well met, with a deficiency of 0.2 V from the specified 35 V. The rise time is an order of magnitude greater than in previous tests. The ripple voltage in Figure 9a appears greater than in previous tests, however this is likely due to the use of a different timescale. Similarly, the PI controller response appears to have a larger wavelength. Figure 9b does not demonstrate the change in controller response across the rise due to experimental error in the transient capture.
As mentioned, the ripple appears greater than it actually is. As per Table 13, the peak-to-peak ripple is 330 mV, which is smaller than the ripple with proportional control only (412 mV). The frequency 23.6 kHz again.
Efficiency sits at 85.3 %, which indicates similar performance to the proportional controller.

75 % load Initial voltage is slightly below 30 V, which is similar to the 50 % load. The final voltage has risen by 1 V above the specified. Rise time has also increased by almost double the previous.
Ripple voltage has decreased, which may explain the increase in frequency, however it is possible the latter falls within the margin for error as in proportional control ripple (Table 10).
This setup indicates the greatest efficiency yet, at 87.5 %.

3.6 Discussion

The designed parameters were built around predicted use case values - for example, 100 W load. Furthermore, the design called for specific, non-standard values that could not be met in implementation. This is the first of perhaps many reasons why differences exist between the designed values and the observed results with real components.
One of the first assumptions was the peak current, which can more accurately be referred to as the average current. The observed values (1.9 A) was close to the calculated value (2.1 A), however this was at no load. Testing was not performed with a full 100 W load, but the subsequent experiments suggest that the current would be in this region.
While there is consistency here, differences begin to emerge when comparing the duty cycle and frequency of the converter. The frequency across tests was reasonbly consistent but slightly lower than expected by calculation. The duty cycle, on the other hand, appeared to be 0.575 rather than the expected 0.375. The peak-to-peak ripple was also very far out of proportion (over five times as much), however this reduced once greater loads were introduced. The ripple itself may be unsuitable for some applications as it over 0.5 V, which may be too large a variation. For equipment running at 48 V however, this is unlikely (but not a factor to ignore).
Some of these differences may be accounted for by the unideal performance of components in experimentation. The theoretical calculations do not take into account losses in operation, however this is reflected in the observed efficiency of the system at 85.5 %. Overall, this efficiency is quite good, however it may be possible to improve upon this with components that are more energy efficient. As it stands, the circuit lost almost 10 W which is significant enough that it cannot be ignored. It is not recommended to use this circuit without any passive cooling at a minimum, and especially not in and enclosed or compact space without mitigation for the power losses of the converter. The greatest losses likely occured in the MOSFET due to high-frequency switching, and the resistor due to current handling.

The introduction of proportional control appears to have reduced the ripple and rise time. However, this came at the cost of decreased efficiency, likely due to greater power dissipation in the control system circuit. The reduced ripple is within expectations, as the proportional gain should allow the circuit to respond to the ripple and conpensate. Usually, the response takes some time, so it is surprising to see the rise time so low and the frequency remain the same. These findings were reflected in the 50 W test. Direct comparisons are difficult given different output voltages and loads per test, both of which likely impact factors such as the peak-to-peak ripple.

The further addition of integral gain allowed noticeable improvements to the ripple voltage and efficiency. This occurs despite the extra load on the entire circuit with the inclusion of proportional and integral gain circuitry. This rise time was significantly affected adversely, however, and is noticeably slower to switch on to the rated voltage than any other circuit.

A few general trends could also be noticed. Rise times appeared to improve across increased loads with all else the same. Efficiency also seemed to improve with greater output voltages. This may be due to the circuit loading parameters approaching those of the design. Additionally, frequency changes between load changes for both closed-loop controllers can be observed. This may fall within measurement error, however it may also be a result of the controller adapting the frequency to account for the increased load.

References

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