1 Introduction

The logic required for the comparator can be determined using a truth table. There are three expected outputs for 4-bit inputs 'A' and 'B':

- A > B (Greater)
- A = B (Equal)
- A < B (Lesser)

Input				Output		
A_3, B_3	A_2, B_2	A_1, B_1	A_0, B_0	A > B (G)	A = B (E)	A < B (L)
$A_3 > B_3$	X	X	X	1	0	0
$A_3 = B_3$	$A_2 > B_2$	X	X	1	0	0
$A_3 = B_3$	$A_2 = B_2$	$A_1 > B_1$	X	1	0	0
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 > B_0$	1	0	0
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	0	1	0
$A_3 < B_3$	X	X	X	0	0	1
$A_3 = B_3$	$A_2 < B_2$	X	X	0	0	1
$A_3 = B_3$	$A_2 = B_2$	$A_1 < B_1$	X	0	0	1
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 < B_0$	0	0	1

Table 1: Comparator truth table

To simplify the set of equations, the truth table output can be modified such that only G and E need to be considered. L can then be inferred by whether G and E are both 0. This gives the resultant equations:

```
G = A3B3' + A3A2B2' + A2B3'B2' + A3A2A1B1' + A2A1B3'B1' + A3A1B2'B1' + A1B3'B2'B1' +
    A3A2A1A0B0' + A2A1A0B3'B0' + A3A1A0B2'B0' + A1A0B3'B2'B0' + A3A2A0B1'B0' + A2A0B3'B1'B0' +
    A3A0B2'B1'B0' + A0B3'B2'B1'B0'
```

Listing 1: 'A > B' equations

```
E = A3A2A1A0B3B2B1B0 + A3'A2A1A0B3'B2B1B0 + A3A2'A1A0B3B2'B1B0 + A3'A2'A1A0B3'B2'B1B0 + A3A2A1
    'A0B3B2B1'B0 + A3'A2A1'A0B3'B2B1'B0 + A3A2'A1'A0B3B2'B1'B0 + A3'A2'A1'A0B3'B2'B1'B0 +
    A3A2A1A0'B3B2B1B0' + A3'A2A1A0'B3'B2B1B0' + A3A2'A1A0'B3B2'B1B0' + A3'A2'A1A0'B3'B2'B1B0' +
     A3A2A1'A0'B3B2B1'B0' + A3'A2A1'A0'B3'B2B1'B0' + A3A2'A1'A0'B3B2'B1'B0' + A3'A2'A1'A0'B3'B2
    'B1'B0'
```

Listing 2: 'A = B' equations

A schematic can then be designed. To accommodate L, an additional gate is required to evaluate the output of G and E. G and E should not be able to assert at the same time[1], however for the calculation of L it is irrelevant. Therefore, either a NOR or an XNOR gate is appropriate. The choice ultimately falls as to which would be most appropriate for the given design.

G	E	L
0	0	1
X	1	0
1	X	0

Table 2: L truth table

Gate	Inputs	Quantity
NOT	1	9
NAND	2	10
	3	3
NOR	2	1
	3	1

Table 3: Gate usage

In total, four gate types are used for the schematic in fig. 1, shown in table 3, which overall required 86 transistors. However, it is possible to reduce the number of transistors or the number of gate ICs. During research and design, the fewest transistor count determined possible was 70. As this requires a 5-input NAND gate[2], the next most feasible design uses 80 transistors. Both of these designs are reliant on using a non-standard XOR gate in order to determine equality between A and B. While typically an XOR gate requires 8 transistors, the fewest possible is 3 [1], however the output suffers from signal degradation and requires a buffer to clean the output. While this method may reduce the overall die area required, it adds a layer of complexity to both the overall design process, and per component simulation.

[1] It may be important to ensure outputs cannot assert at the same time.

[2] Gates with 4 series transistors begin to suffer delays such that it is better to split the logic across multiple gates.

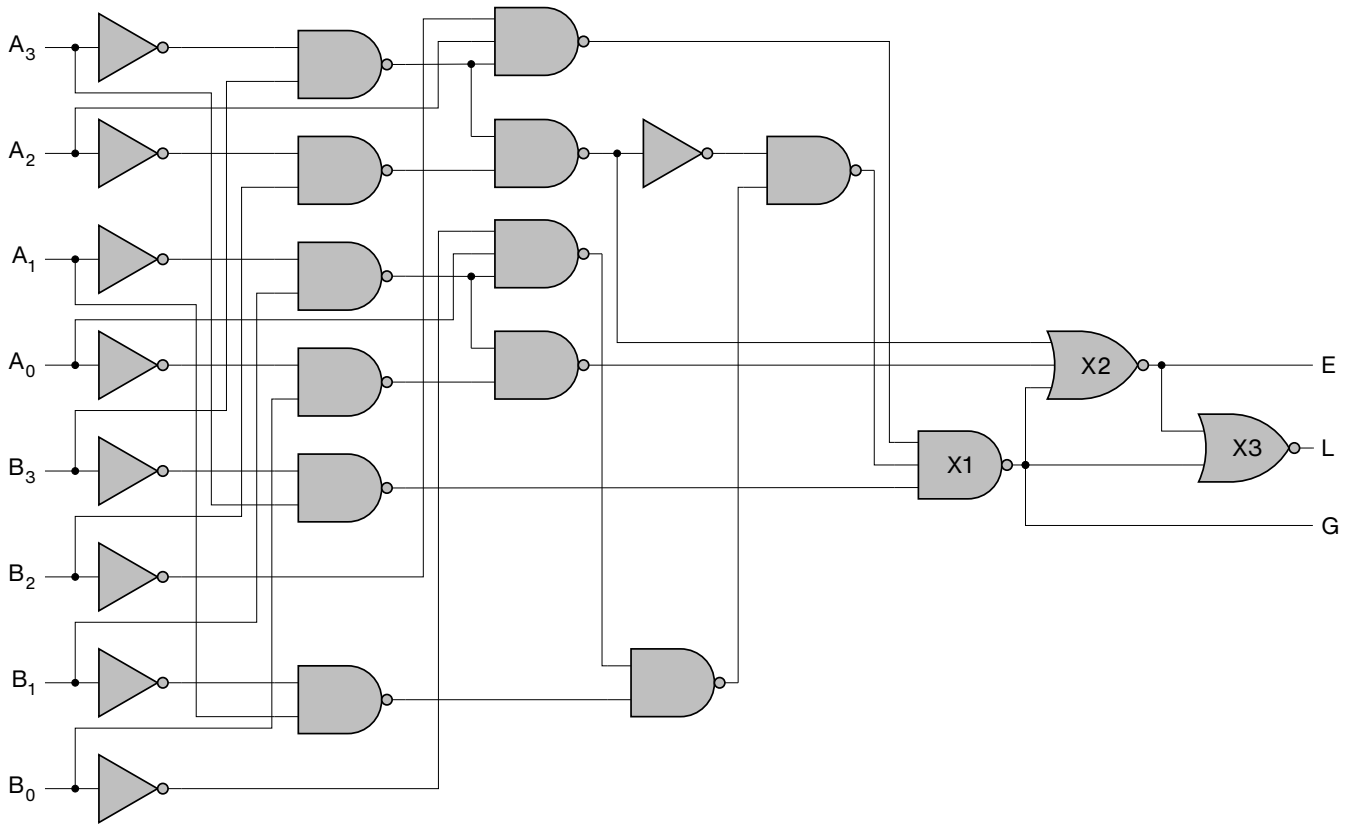
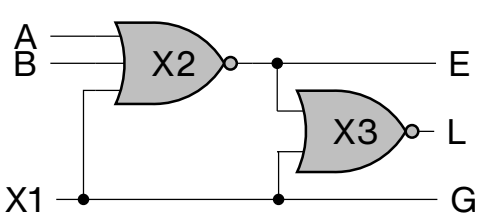
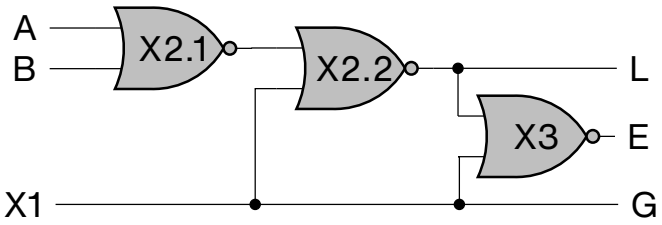


Figure 1: Comparator schematic

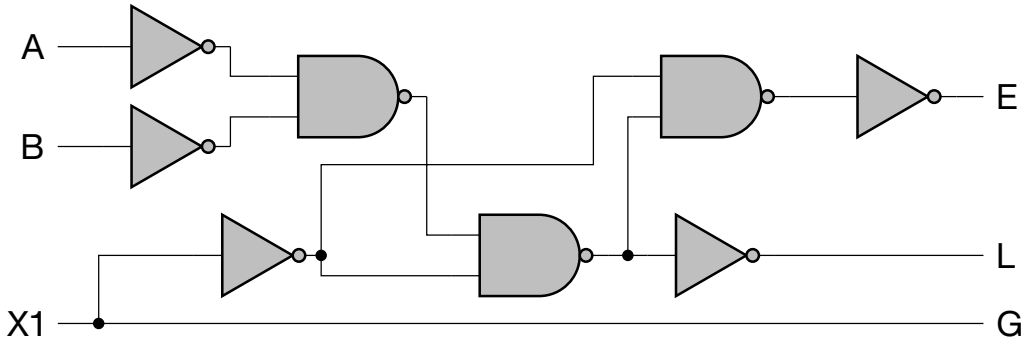
Another notable feature is the use of NOR gates, especially a 3-input NOR. Typically, NOR gates are avoided with a preference for NAND gates. The output circuit following gate X1 in fig. 1 can be redrawn in a number of ways as shown in fig. 2.



(a) NOR-3 circuit



(b) NOR-2 circuit



(c) NAND circuit

Figure 2: Output circuit possibilities

A brief study on the logical effort (table 4) of each circuit indicates how, as the number of paths grow in the alternative circuits, the effort required escalates rapidly. This is due to how path logical effort, $G = \prod g_i$, which quickly grows out of control as branching increases. A NAND-only solution also suffers from a greater number of gate ICs required for the same logic.

Circuit	Path effort	
	g_E	g_L
NOR-3, 2a	$12\frac{19}{27}$	$6\frac{2}{3}$
NOR-2, 2b	$138\frac{8}{9}$	$18\frac{14}{27}$
NAND, 2c	120	$50\frac{22}{27}$

Table 4: Logical effort

1.1 Delay

The overall delay of the comparator can be determined by analysing one of the longest paths.

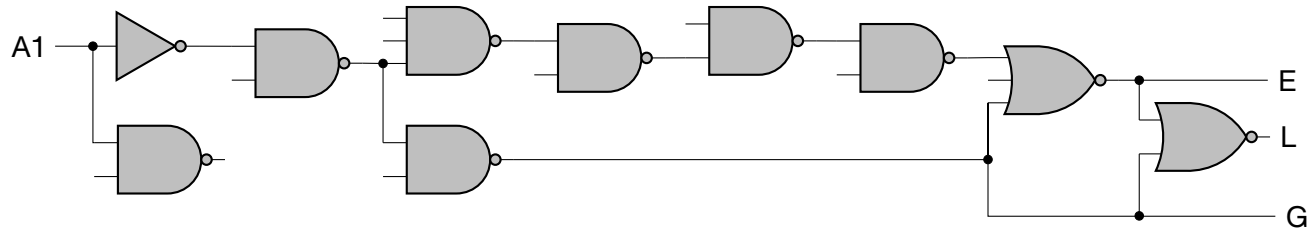


Figure 3: Longest path

The minimum delay, D, of the longest path can be calculated by $N(G \cdot B \cdot H)^{\frac{1}{N}} + P$,

where: N = Number of gates
G = Path logical effort, $\prod g_i$
B = Branching effort, $\prod \frac{C_{on-path}+C_{off-path}}{C_{on-path}}$
H = Electrical effort, $\frac{C_{out}}{C_{in}}$
P = Parasitic delay, $\sum p_i$

In this instance,

$$N = 8$$
$$G = 1 \times \left(\frac{4}{3}\right)^4 \times \left(\frac{5}{3}\right)^2 \times \frac{7}{3} = \frac{44800}{2187}$$
$$B = \frac{3+4}{3} \times \frac{5+4}{5} \times \frac{7+5}{7} = \frac{98}{15}$$
$$H = \frac{6}{3} = 2$$
$$P = 1 + 2 + 3 + 2 + 2 + 2 + 3 + 2 = 17$$
$$\therefore$$
$$D = 33.089$$

The absolute delay, $D_{abs} = D \cdot \tau$, where τ is the process dependent time constant. Assuming $\tau \cong 3$ ps, $D_{abs} = 99.27$ ps.

With all things considered, the proposed design in fig. 1 offers a good balance between size, propagation delay, and overall complexity.

2 Gate development

In total five different gate cells are required. The process of designing a logic gate involves four major steps:

1. Schematic design of transistor circuit.
2. Simulation to verify the schematic is correct for the logic desired.
3. Layout of silicon to produce the fabricable gate.
4. Simulation of the layout to verify it matches the schematic logic.

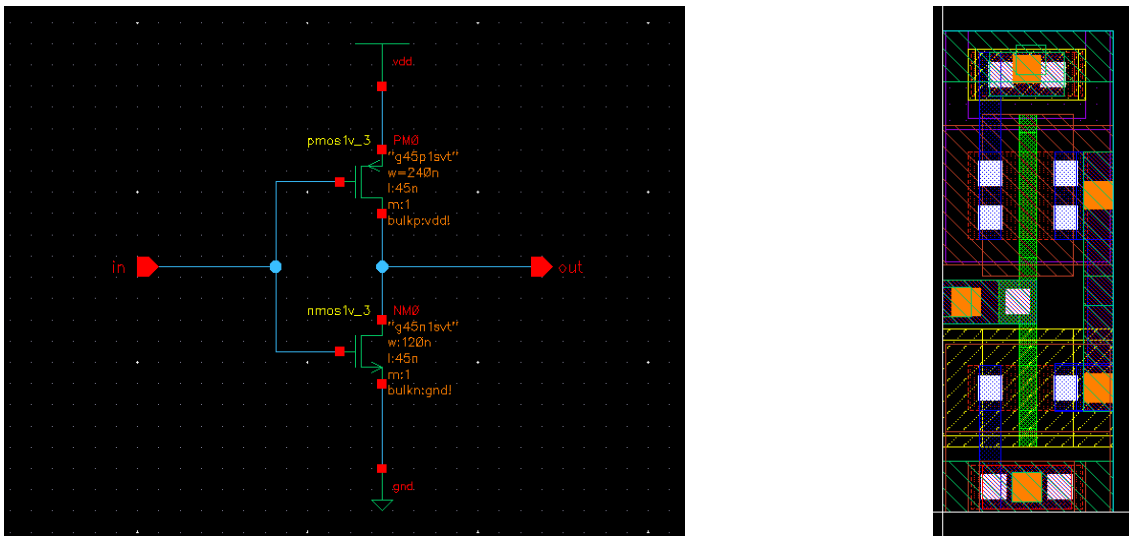
The following section compares the schematic design to the layout, followed by the simulation results, for each gate.

Some general rules were observed during the design, particularly layout, of each gate: In order to manage the complexity of the comparator layout, the gate cells were standardised in height (1.315 µm). They include a VDD rail on the top and GND rail across the bottom, each 0.14 µm tall, extending from body ties created using the module generator. Pins and rails are exposed to metal 3 for top cell routing, with internal routing performed with metal 1 and 2.

2.1 NOT gate

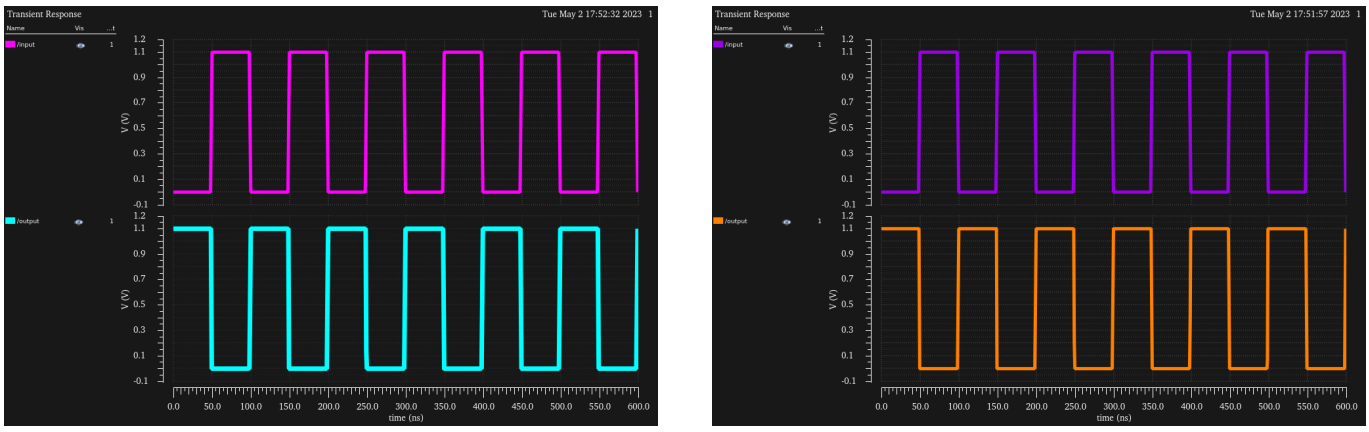
Peak power	Area efficiency	Transistor count
3.828 µW	57.595 %	2

Table 5: NOT gate parameters



(a) Schematic **(b)** Layout

Figure 4: NOT gate circuits



(a) Schematic **(b)** Layout

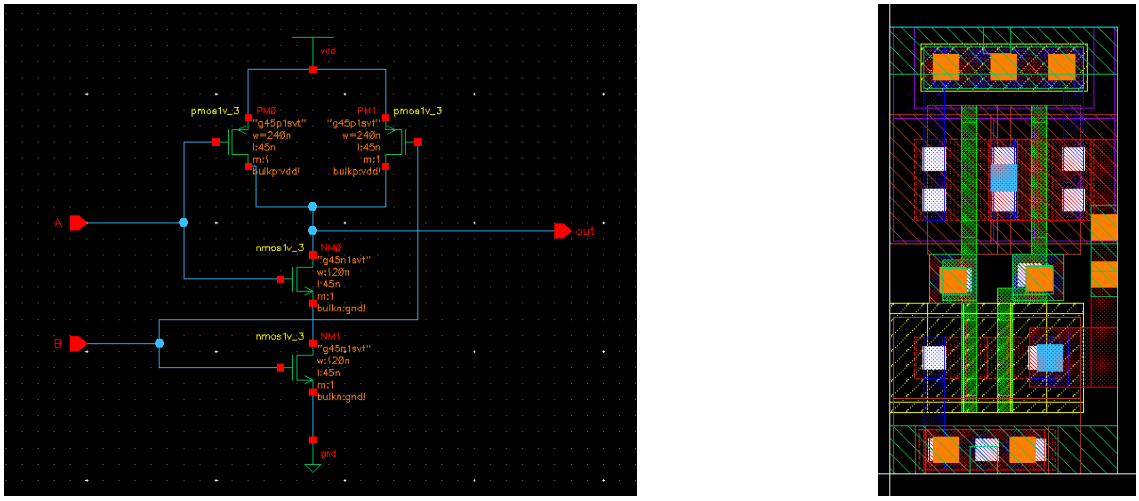
Figure 5: NOT gate input response

2.2 NAND gate

2.2.1 2-input

Peak power	Area efficiency	Transistor count
4.595 µW	66.239 %	4

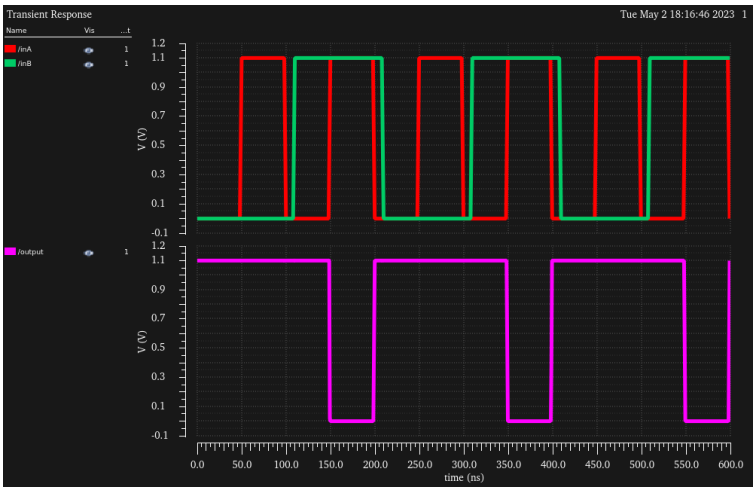
Table 6: 2-input NAND gate parameters



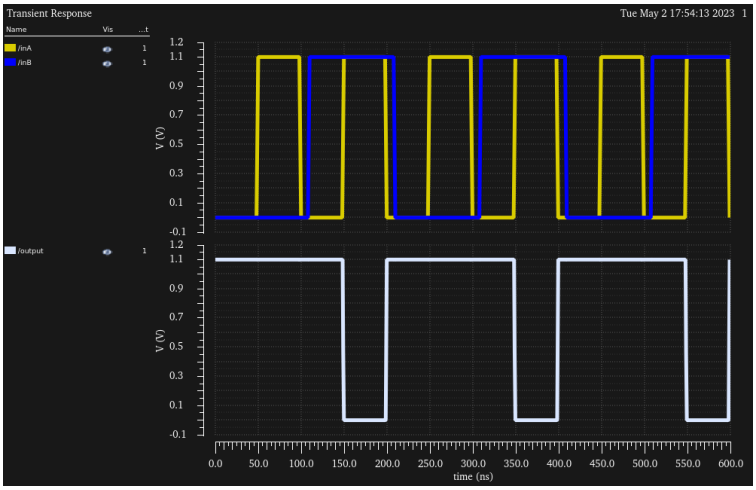
(a) Schematic

(b) Layout

Figure 6: 2-input NAND gate circuits



(a) Schematic



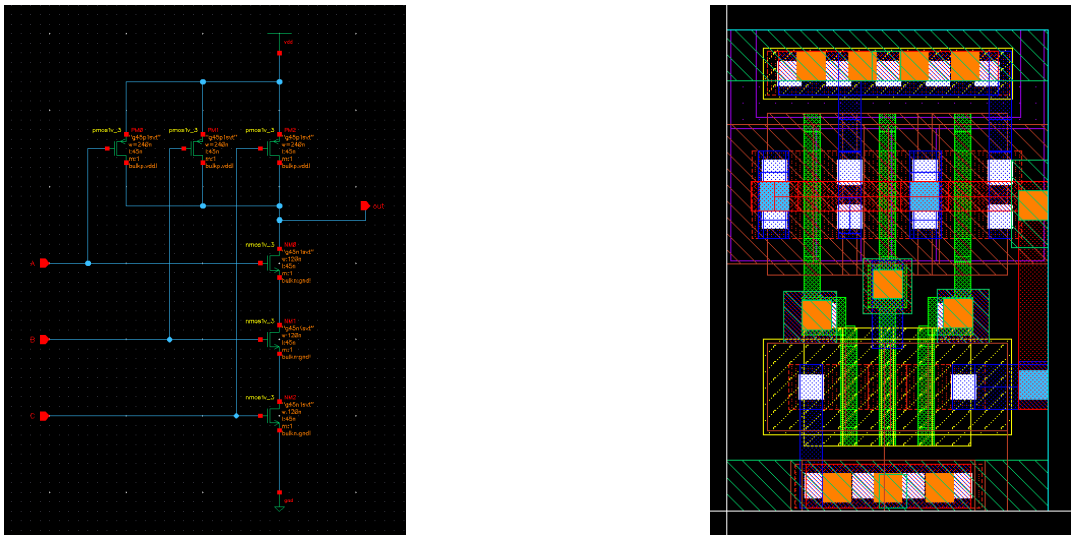
(b) Layout

Figure 7: 2-input NAND gate input response

2.2.2 3-input

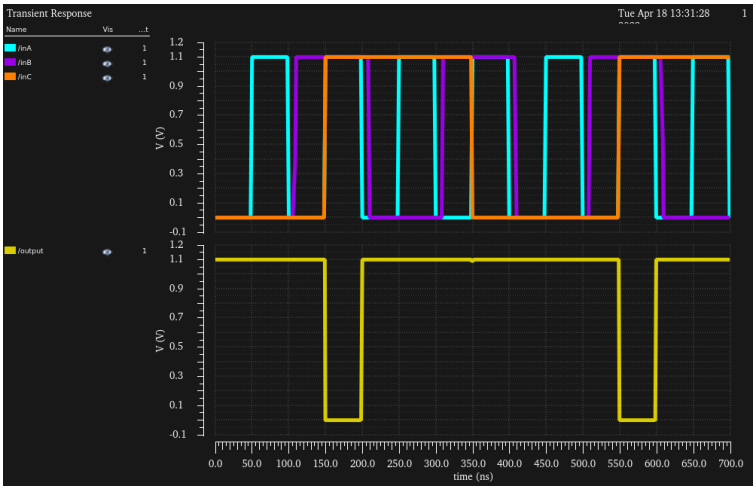
Peak power	Area efficiency	Transistor count
4.173 µW	70.727 %	6

Table 7: 3-input NAND gate parameters

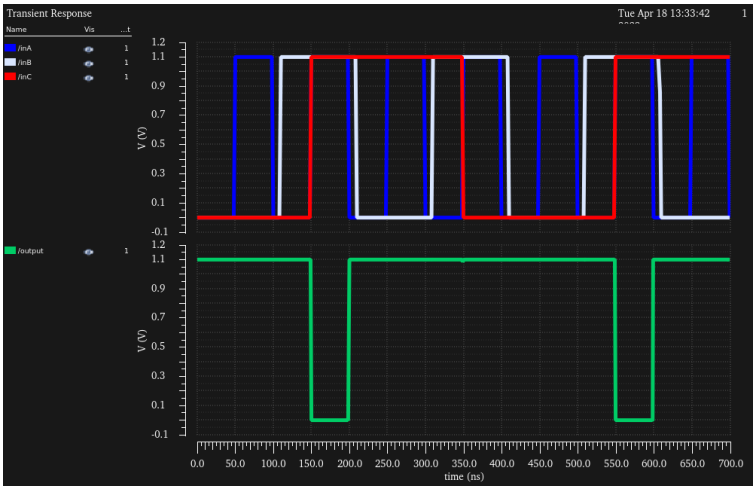


(a) Schematic **(b)** Layout

Figure 8: 3-input NAND gate circuits



(a) Schematic



(b) Layout

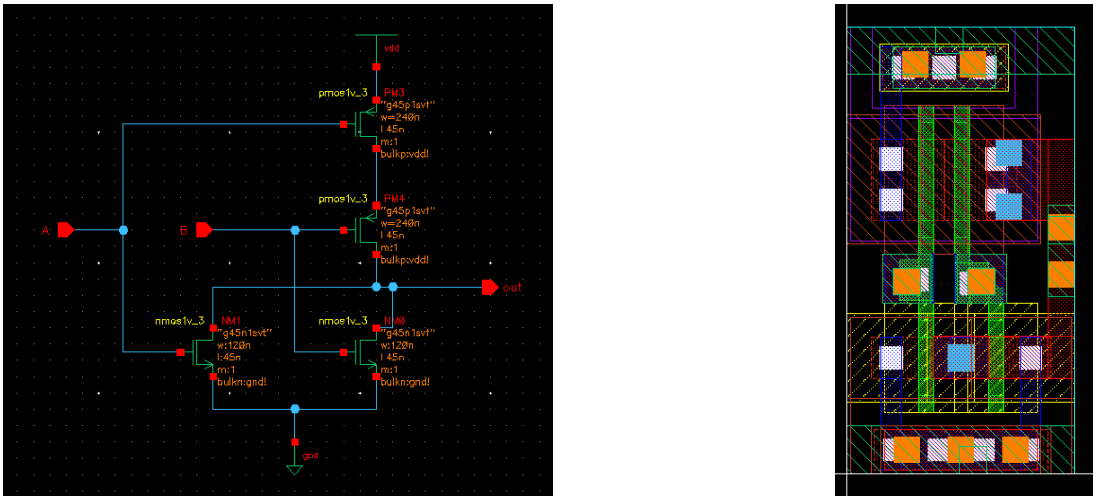
Figure 9: 3-input NAND gate input response

2.3 NOR gate

2.3.1 2-input

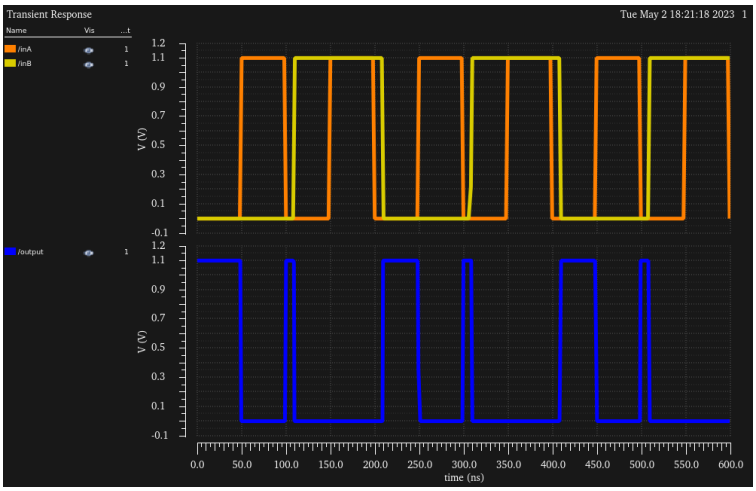
Peak power	Area efficiency	Transistor count
4.329 µW	64.877 %	4

Table 8: 2-input NOR gate parameters

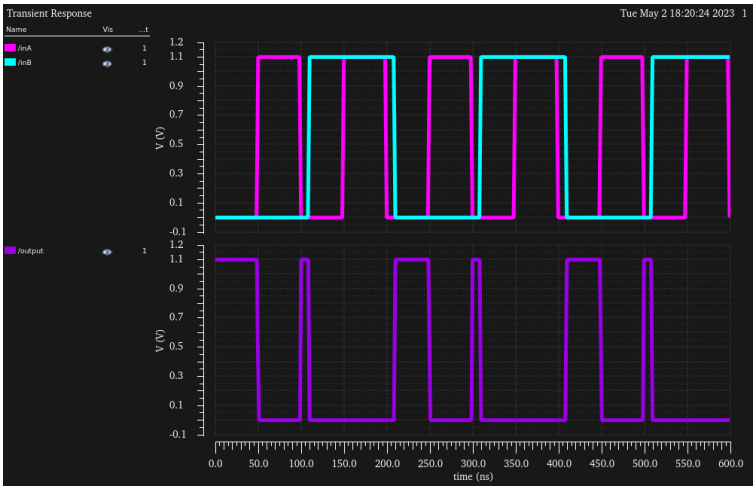


(a) Schematic **(b)** Layout

Figure 10: 2-input NOR gate circuits



(a) Schematic



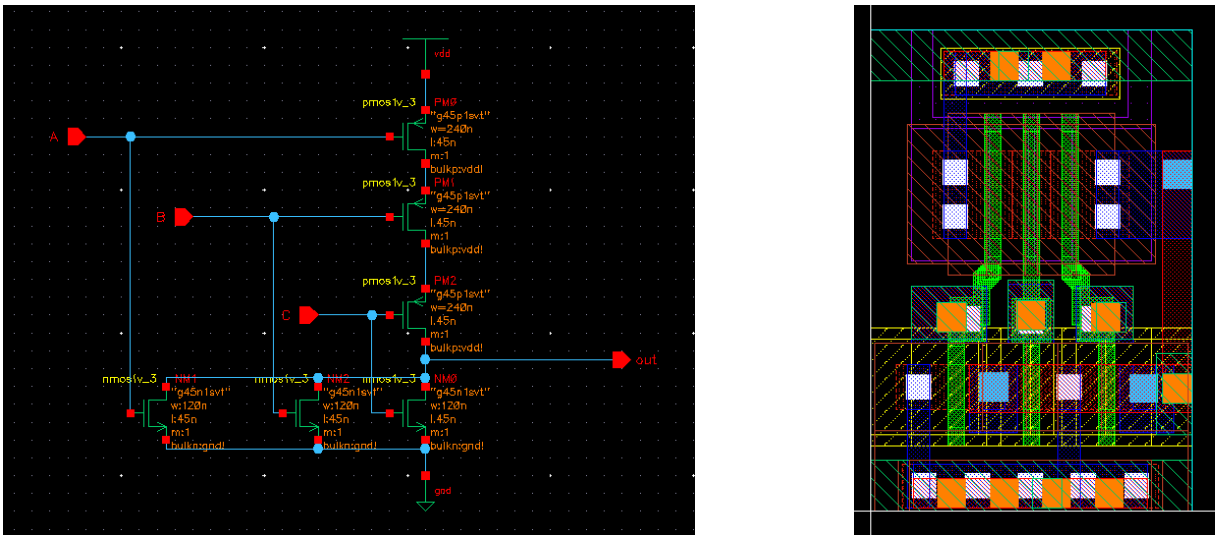
(b) Layout

Figure 11: 2-input NOR gate input response

2.3.2 3-input

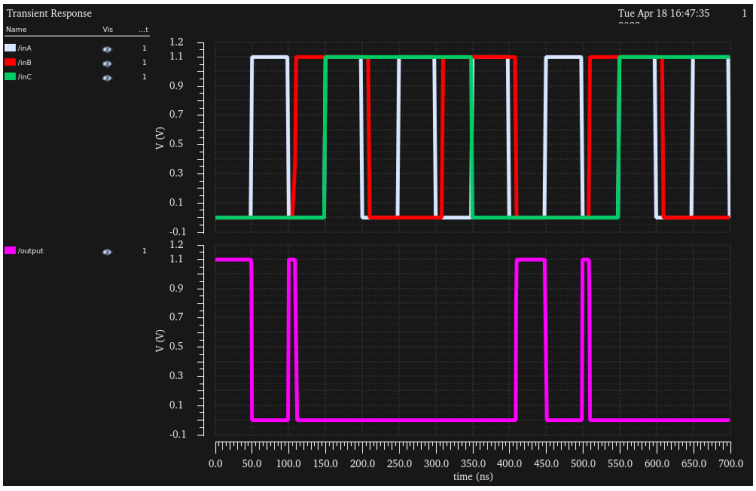
Peak power	Area efficiency	Transistor count
4.911 µW	68.641 %	6

Table 9: 3-input NOR gate parameters

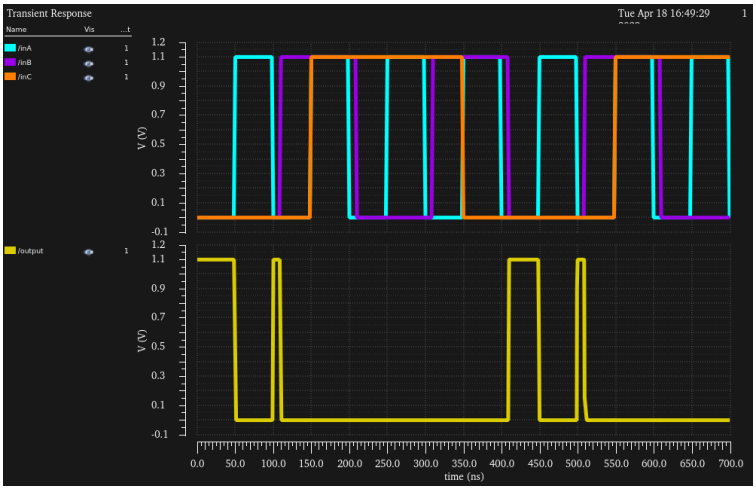


(a) Schematic **(b)** Layout

Figure 12: 3-input NOR gate circuits



(a) Schematic



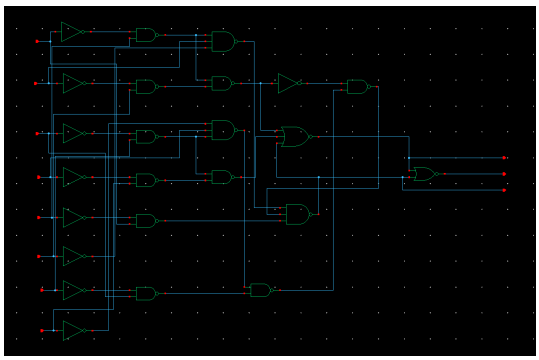
(b) Layout

Figure 13: 3-input NOR gate input response

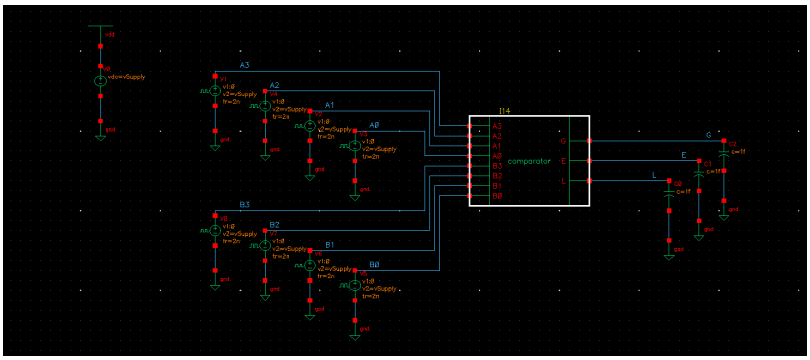
3 Comparator design

3.1 Schematic design

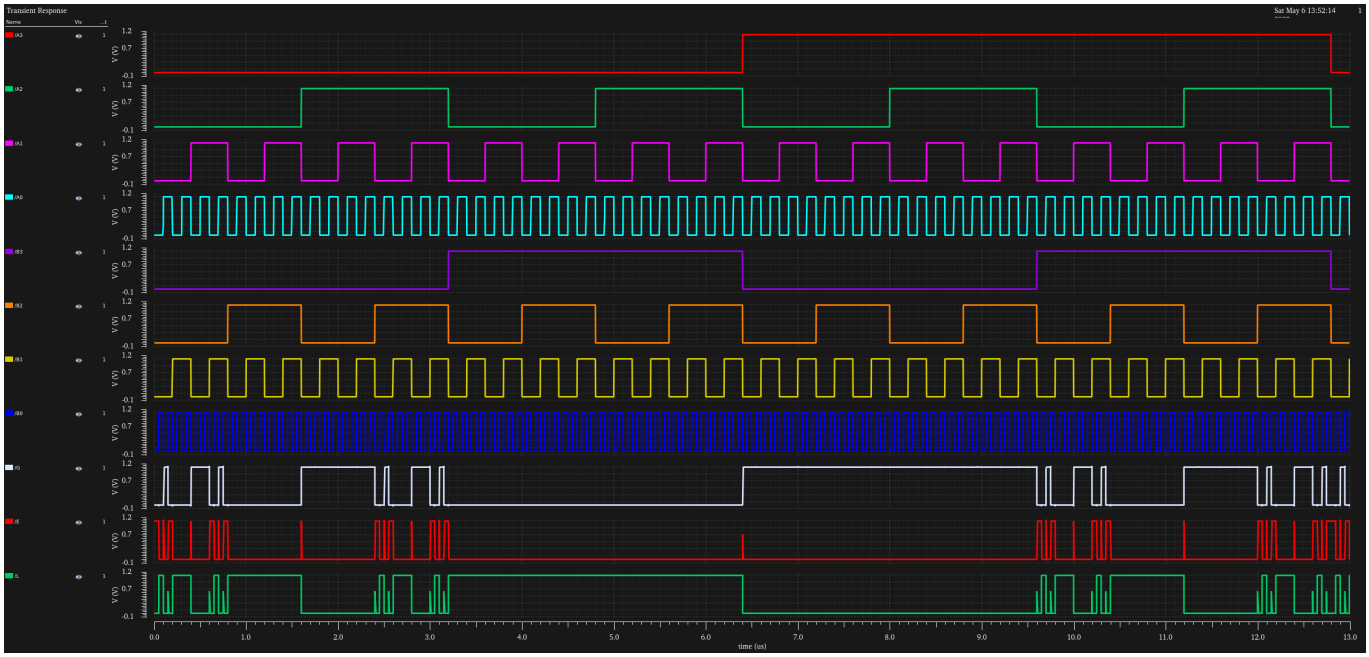
Comparator design commences with reproducing the schematic design in fig. 1 in Virtuoso's schematic editor, and setting up a simulation to verify the schematic functions correctly.



(a) Schematic



(b) Test bench



(c) Simulation

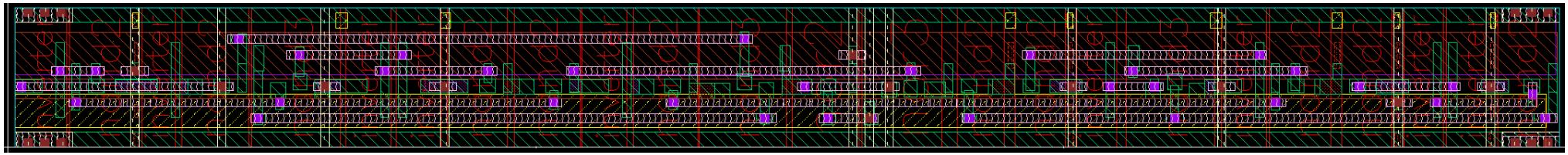
Figure 14: Comparator schematic

The simulation indicates the correct outputs for the given binary inputs. There are many instances in the simulation where transient undesirable outputs occur. For example, output E rises briefly, sometimes not even completely, when G falls and L rises at the same time. This is due to two reasons. In the design, a NOR gate was opted for to select the outputs rather than an XOR. Secondly, the rise and fall of the test bench simulation signals fall within the threshold voltage of the MOSFETs used. To counteract this, enough time for outputs to settle needs to be provided for the outputs to settle, or the comparator output can be latched so the output only updates on the edge of a clock. For the purposes of this design, the settling time will be determined after the layout is complete.

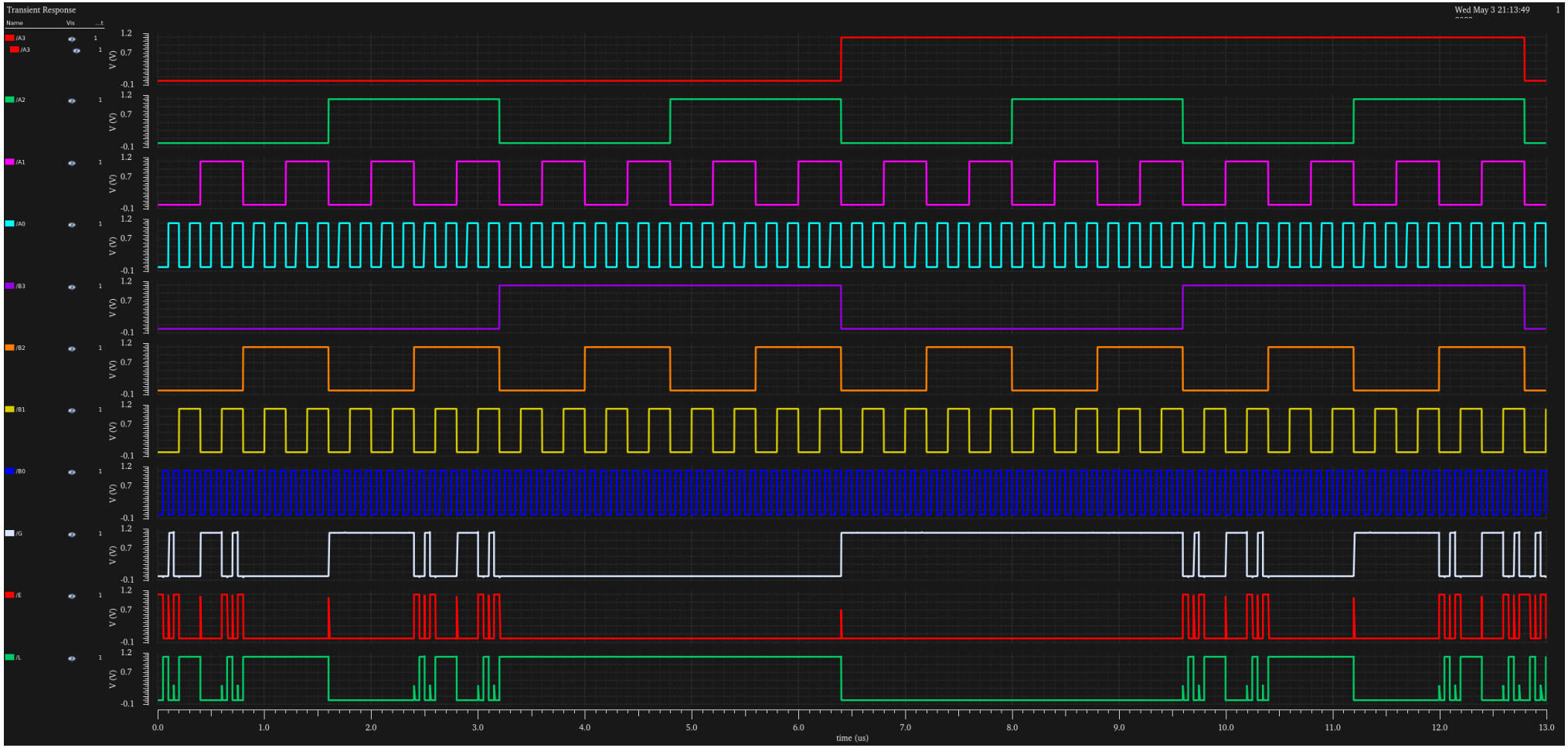
3.2 Layout

The standard cell height allows for efficient routing, with vertical connections within a cell on the metal 3 layer, and horizontal connections between cells on metal 4 layer. Finally, pins and power are exposed on metal 5 layer. The pins run the height of the comparator, so it can be connected from either end. The power rails run on metal 3, and are exposed at each horizontal end to metal 5.

The cells share a well and implants, allowing them to be butted up extremely close; they can even be overlapped. The placement report calculates area efficiency to be 102.233 %, requiring a chip area of 19.365 μm^2.



(a) Layout



(b) Simulation

Figure 15: Comparator layout

3.3 Power

The peak dynamic power dissipation is 68.189 µW and occurs during switching of outputs. There does not appear to be a greater level of dissipation due to all outputs being high simultaneously, suggesting that switching the NOR gate on G and E for an XNOR would have little benefit.

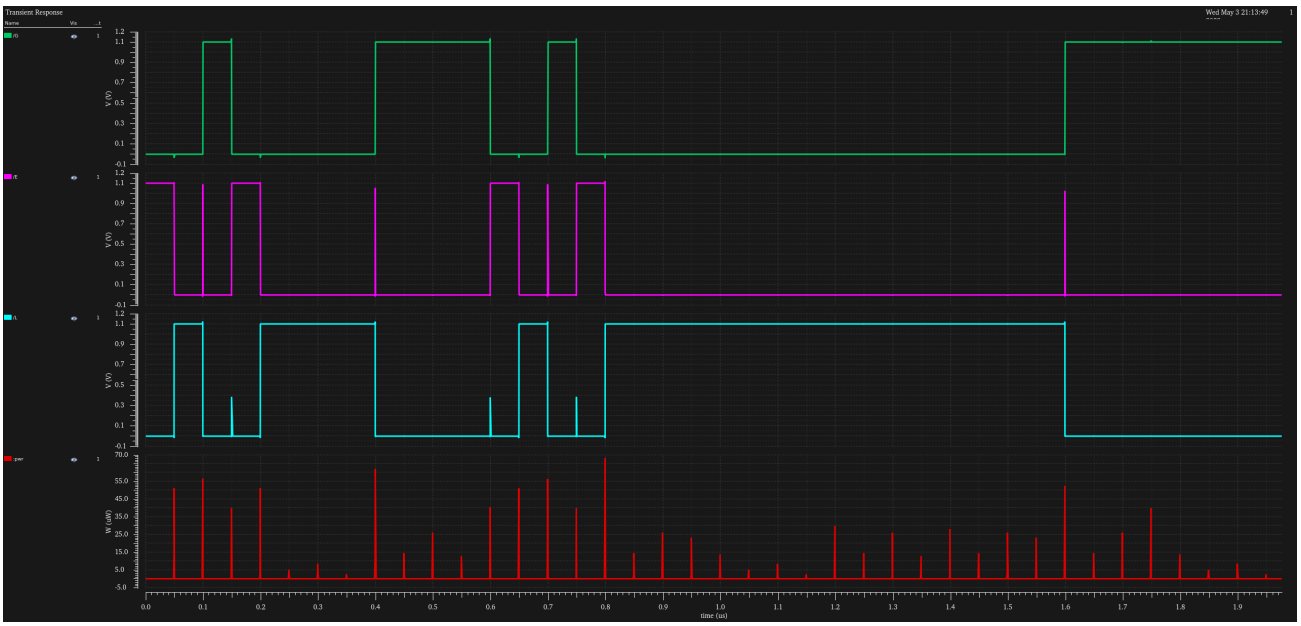


Figure 16: Power dissipation during switching

3.4 Delay

The comparator responds 150 ps after the input reaches 50 % of vSupply (0.55 V), and settles after an additional 200 ps. Considering settling time for transient outputs, readings are available from the comparator after, at earliest 350 ps, or comfortably after 400 ps. This suggests a maximum possible clock speed of 2.857 GHz.

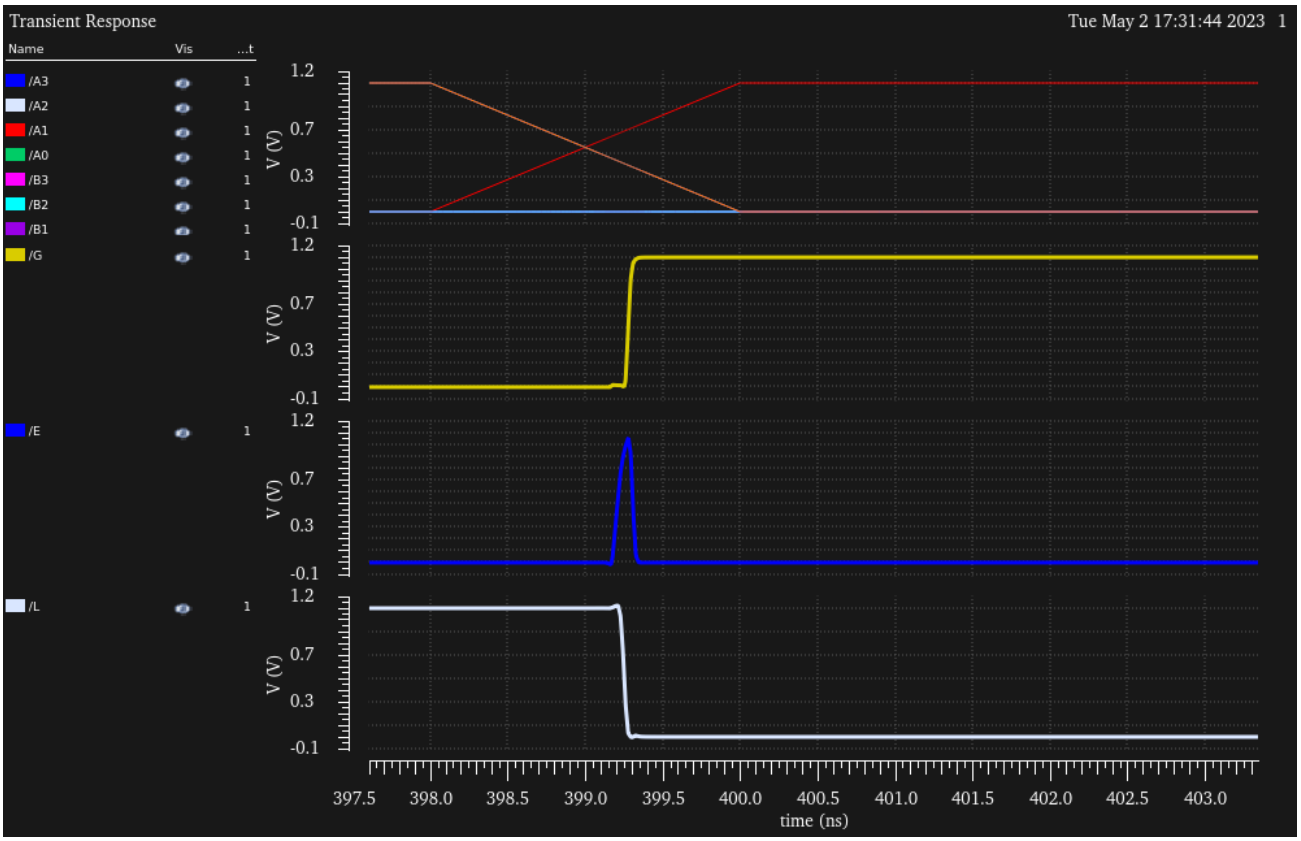


Figure 17: Transient output

4 Evaluation

Peak power	Area efficiency	Chip area	Transistor count	Delay	Recommended clock
68.189 µW	102.233 %	19.365 μm^2	86	400 ps	⩽2.5 GHz

Table 10: Performance metrics

The comparator as a whole appears to function quite well. It responds appropriately and quickly to the input of two 4-bit numbers, A and B, to set the outputs G (greater), E (equal), or L (lesser). Die area is low and utilisation is high, achieved by overlapping standard cells. The design uses a reasonably low number of transistors, at 86, spread across five gate ICs. While designs using fewer transistors are possible, they may introduce complexity when maintaining standardised cells or perform slower.

4.1 Standard cells

The design leverages the use of standard cells to attain the extremely high area efficiency. The cells share a common n-well, implants, and power rails, allowing gates to be overlapped. While each individual gate's area efficiency can be improved, the aim for standardisation allows the top cell to recoup those losses. The large diffusions required may also increase the expense of manufacture. The use of taller cells may allow for this expense to be reduced, however that would have to balanced against the total area used.

A downside of designing in this manner is that it leads to routing with little to no flexibility to accommodate changes. Using the comparator as a standard cell itself may require adjustment of sizing, which may prove difficult.

4.2 Routing

The pins and rails for each cell are exposed on metal 3. Routing on the top cell then uses metal 4 to move horizontally between cells. As the rails are on the same metal layer as the vertical routing, the maximum number of horizontal lines that can be supported is reduced. The comparator falls within the level of complexity that can be supported, however it is close to the limit of what is possible with a single line layout given the maximum number of horizontal tracks (six) is reached.

Routing can be improved by exposing the rails on a different layer to the internal pins (thereby allowing overlapping), and increasing the standard cell height for more complex designs. For particularly complex designs, routing may not be possible across the cells, in which case pins may need to move to be commonly accessible from a routing channel.

4.3 Power dissipation

Compact routing across the cells additionally lead to a low value of power dissipation during switching. Due to the level of complexity of the design, and thereby the total number of transistors used, the static power dissipation is in the region of yW and negligible when analysing the comparator by itself.

4.4 Delay

The minimum delay required was calculated to be 100 ps, which is 3.5 times smaller than the observed minimum delay, 350 ps. This indicates that there may be areas for improvement in the design to minimise this, although managing this without sacrificing on other aspects like area utilisation may be difficult to balance. One such improvement may be to change the NOR gate across G and E for an XNOR, potentially allowing a quicker response by limiting transient outputs.

References

[1] K. Chandra, R. Kumar *et al.*, 'A new design 6t full adder circuit using novel 2t xnor gates', *IOSR Journal of VLSI and Signal Processing (IOSR-JVSP)*, vol. 5, pp. 2319–4197, Apr. 2015. DOI: 10.9790/4200-05316368.

[2] N. H. Weste and D. M. Harris, *CMOS VLSI Design: A Circuits and Systems Perspective*. Addison Wesley, 2011, ISBN: 9780321547743.