VLSI Circuit Design II– EHB 425E

HOMEWORK III

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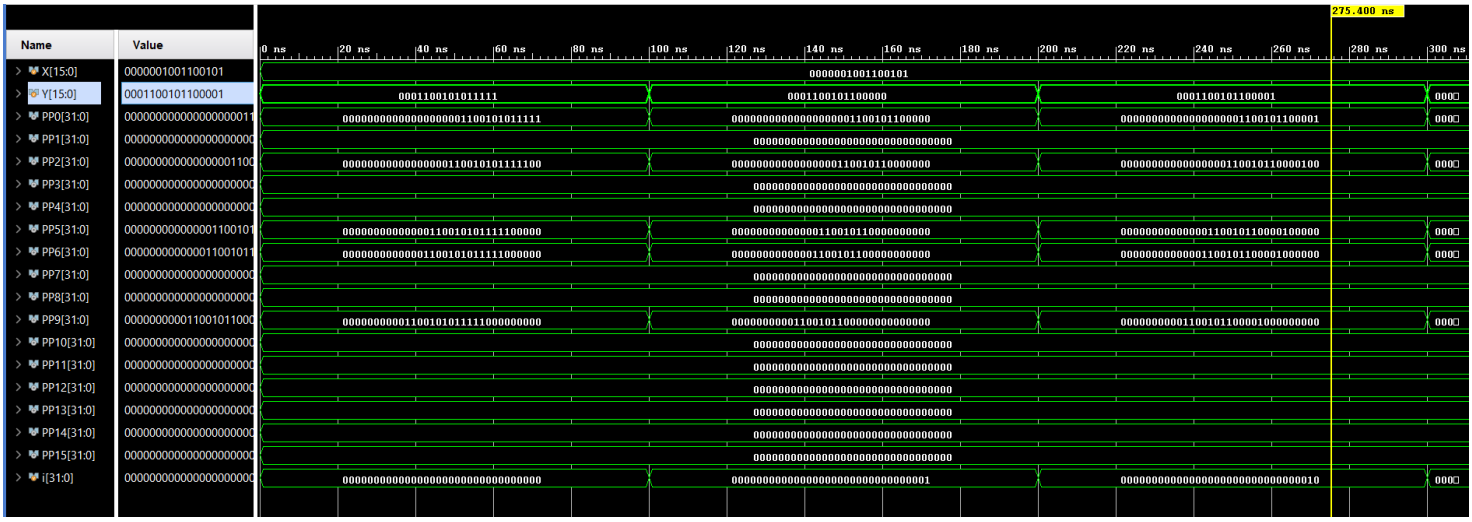
INTRODUCTION

The author of this report has designed a 16-bit multiplier which has 3 main blocks: Partial Product Generator, Partial Product Accumulator, and Final Stage Adder. The HDL codes and dot files will be uploaded to Ninova in a zip file, but they are not included in this report because the dot files are large and some of them did not produce .pdf or .svg files. The author will include all the dot files in the zip file

1- PPG

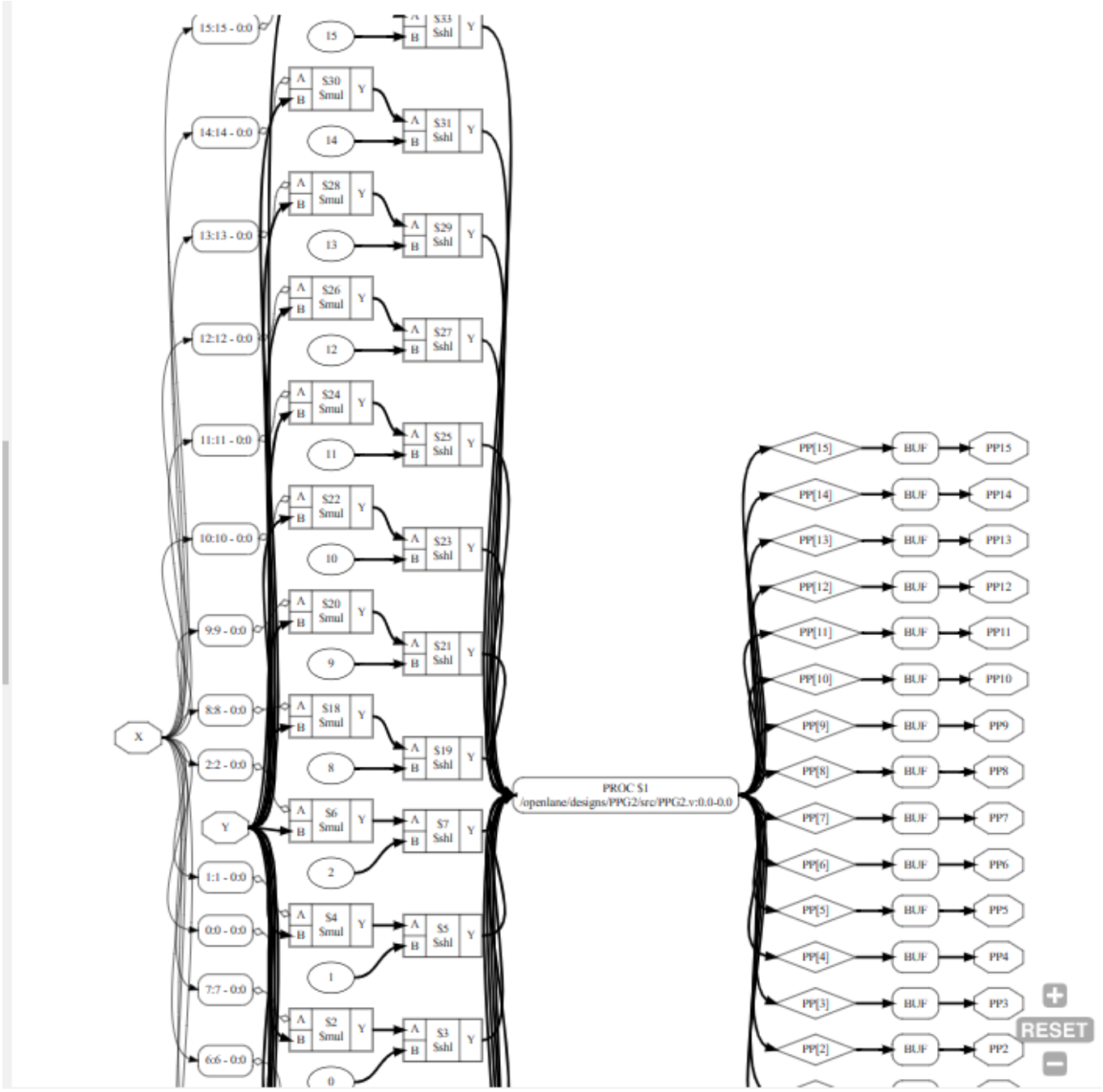
- Behavioral Simulation Results



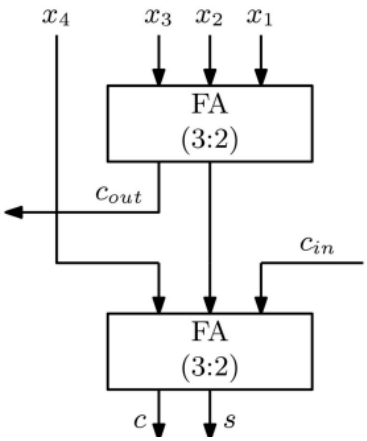
Partial product results are given as seen above. The first bit of X is 1 and accordingly the first PP value must be Y itself. Then the 2nd bit of X is 0, so the 2nd value of PP should be 0. The 3rd bit of X is 1, so its bit must be shifted to the left by 1 minus. In other words, if the 3rd bit is 1, the value of the 3rd element Y of the PP should be written 2 shifted to the left. The pattern continues in this way. The simulation is working correctly.

WHOLE SIMULATION

The hierarchy dot file belonging to PPG is given below. Here, it is seen that the generated wire signals and the generated signals are connected to the output. In the left digit, it is seen that a number is shifted to the left side by increasing gradually.

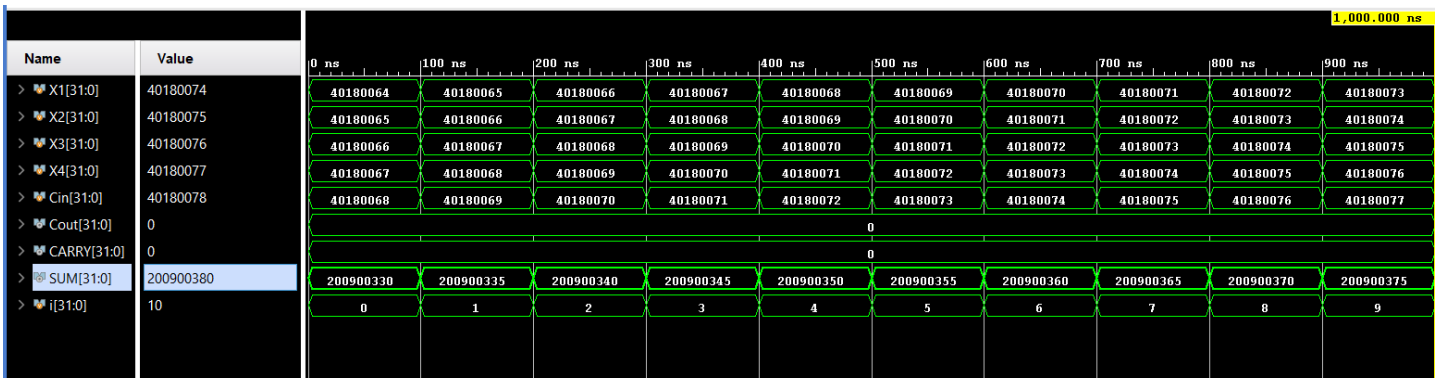


2- 4:2 COMPRESSOR



A basic 4:2 compressor circuit

- Behavioral Simulation Results



$$x_1 + x_2 + x_3 + x_4 + c_{in} = s + 2(c + c_{out})$$

4:2 Compressor Equation

$$\frac{(40180064 + 40180068)}{2} \cdot 5 = 200900330$$

$$\frac{(40180065 + 40180069)}{2} \cdot 5 = 200900335$$

$$\frac{(40180066 + 40180070)}{2} \cdot 5 = 200900340$$

$$\frac{(40180067 + 40180071)}{2} \cdot 5 = 200900345$$

$$\frac{(40180068 + 40180072)}{2} \cdot 5 = 200900350$$

$$\frac{(40180069 + 40180073)}{2} \cdot 5 = 200900355$$

$$\frac{(40180070 + 40180074)}{2} \cdot 5 = 200900360$$

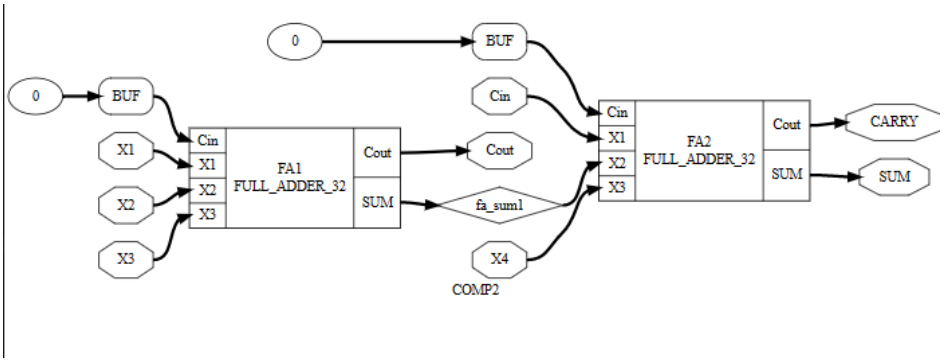
$$\frac{(40180071 + 40180075)}{2} \cdot 5 = 200900365$$

$$\frac{(40180072 + 40180076)}{2} \cdot 5 = 200900370$$

$$\frac{(40180073 + 40180077)}{2} \cdot 5 = 200900375$$

The equation for 4:2 compressor is as stated above. The numbers indicated by the sequential number addition formula were added. When the additions were made, the correctness of the result was verified with the calculator. The calculator results are also shown above.

Below is the output of the .dot file of 4:2 Compressore. Compressore's cin, cout, sum, carry, input signals and also some empty inputs are assigned 0 by giving buf.



3- PPA

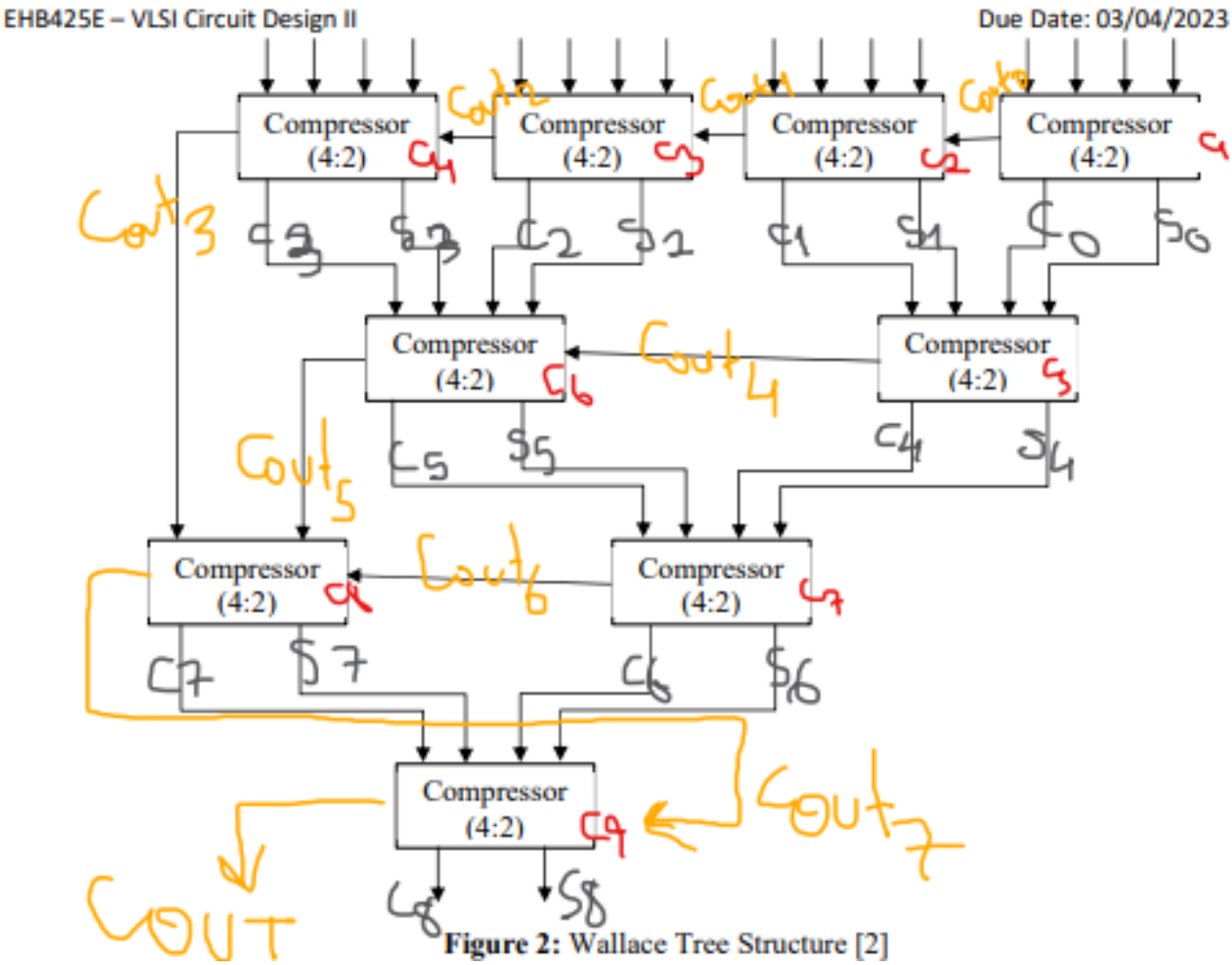
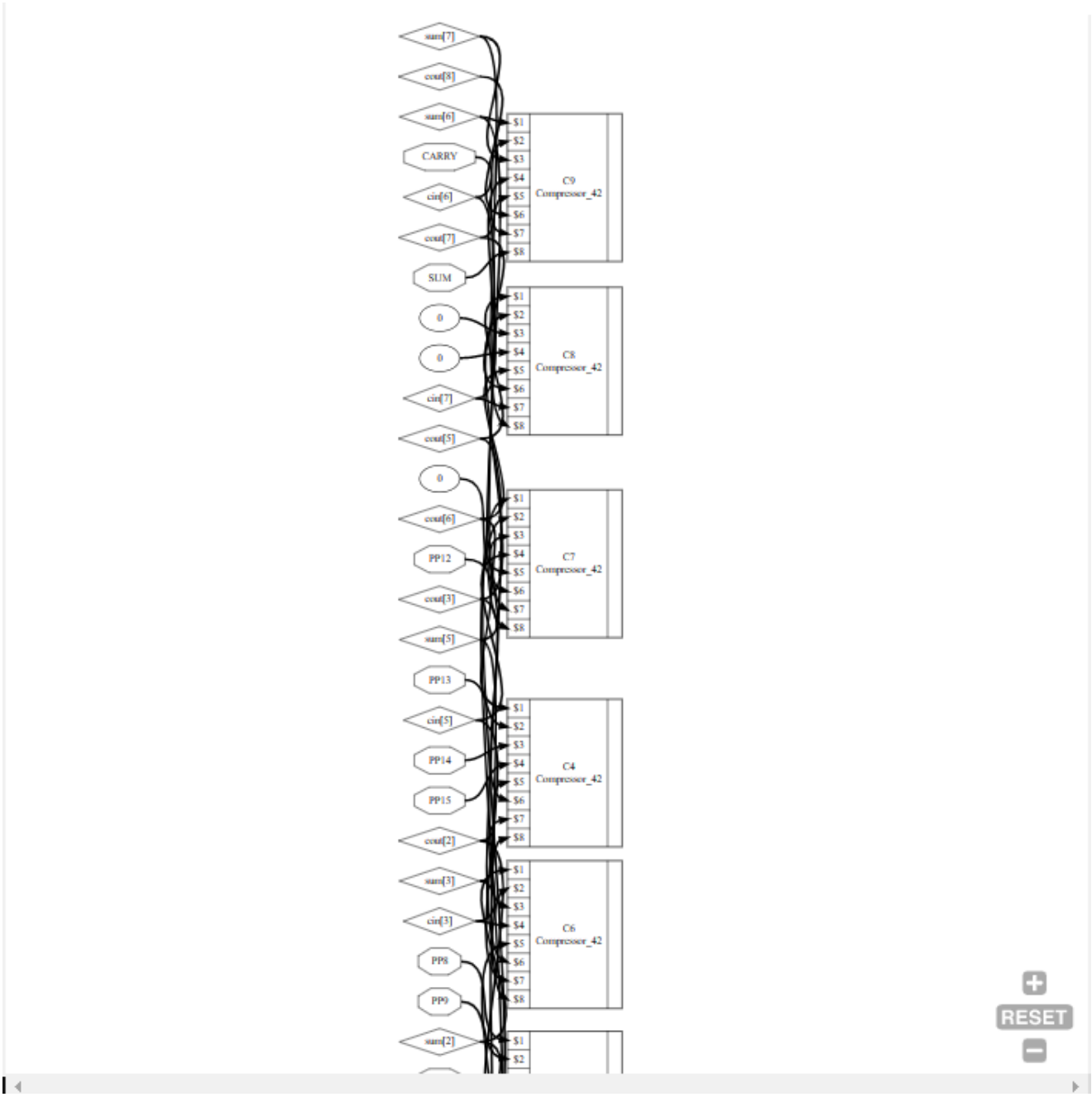


Figure 2: Wallace Tree Structure [2]

Above is the block from which the PPA was derived with the 4:2 Compressor. Verilog code is written and tested by simulation. The simulation results are mentioned below.

In the dot extension hierarchy file, Compressors cin, cout, sum and input signals are displayed as connected to each other. I have outlined part of the circuit below when the image is too large.



- Behavioral Simulation Results

$$\frac{(40180063 + 40180078)}{2} \cdot 16 = 642881128$$

$$\frac{(40180064 + 40180079)}{2} \cdot 16 = 642881144$$

$$\frac{(40180065 + 40180080)}{2} \cdot 16 = 642881160$$

$$\frac{(40180066 + 40180081)}{2} \cdot 16 = 642881176$$

$$\frac{(40180067 + 40180082)}{2} \cdot 16 = 642881192$$

$$\frac{(40180068 + 40180083)}{2} \cdot 16 = 642881208$$

$$\frac{(40180069 + 40180084)}{2} \cdot 16 = 642881224$$

$$\frac{(40180070 + 40180085)}{2} \cdot 16 = 642881240$$

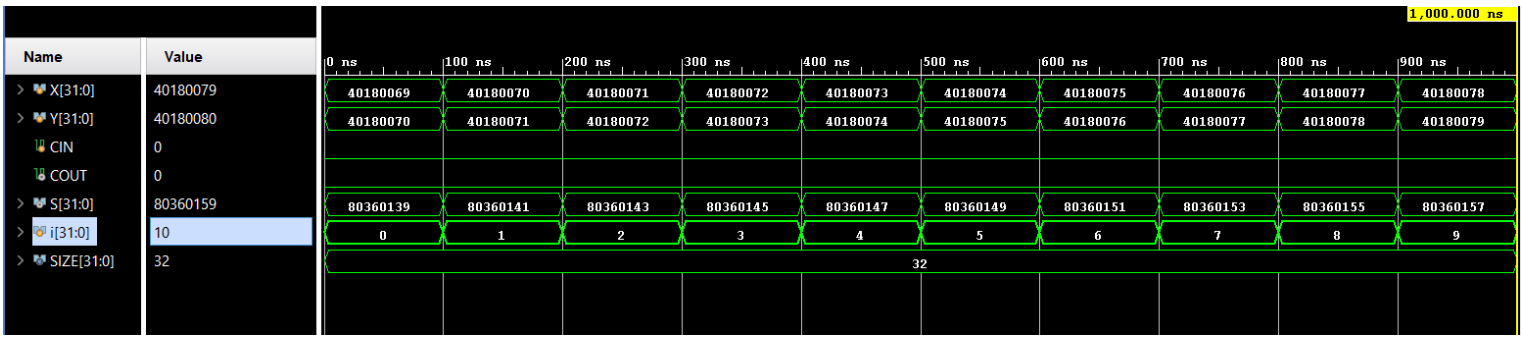
$$\frac{(40180071 + 40180086)}{2} \cdot 16 = 642881256$$

$$\frac{(40180072 + 40180087)}{2} \cdot 16 = 642881272$$

The PPA circuit shown above is a circuit that shows the sum of the PP values. The results of the simulation are compared with the results of the calculator. It has been verified that the circuit is working correctly.

4- RCA

- Behavioral Simulation Results

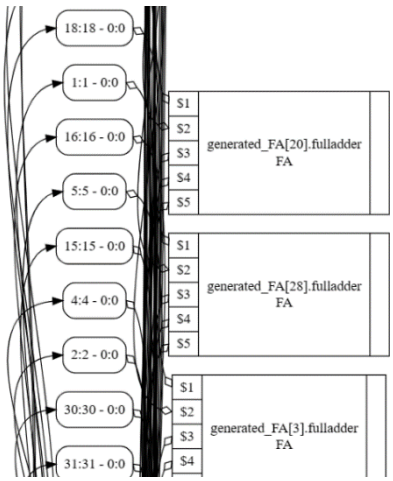


40180069 + 40180070	= 80360139
40180069 + 40180070 + 2	= 80360141
40180069 + 40180070 + 4	= 80360143
40180069 + 40180070 + 6	= 80360145
40180069 + 40180070 + 8	= 80360147
40180069 + 40180070 + 10	= 80360149

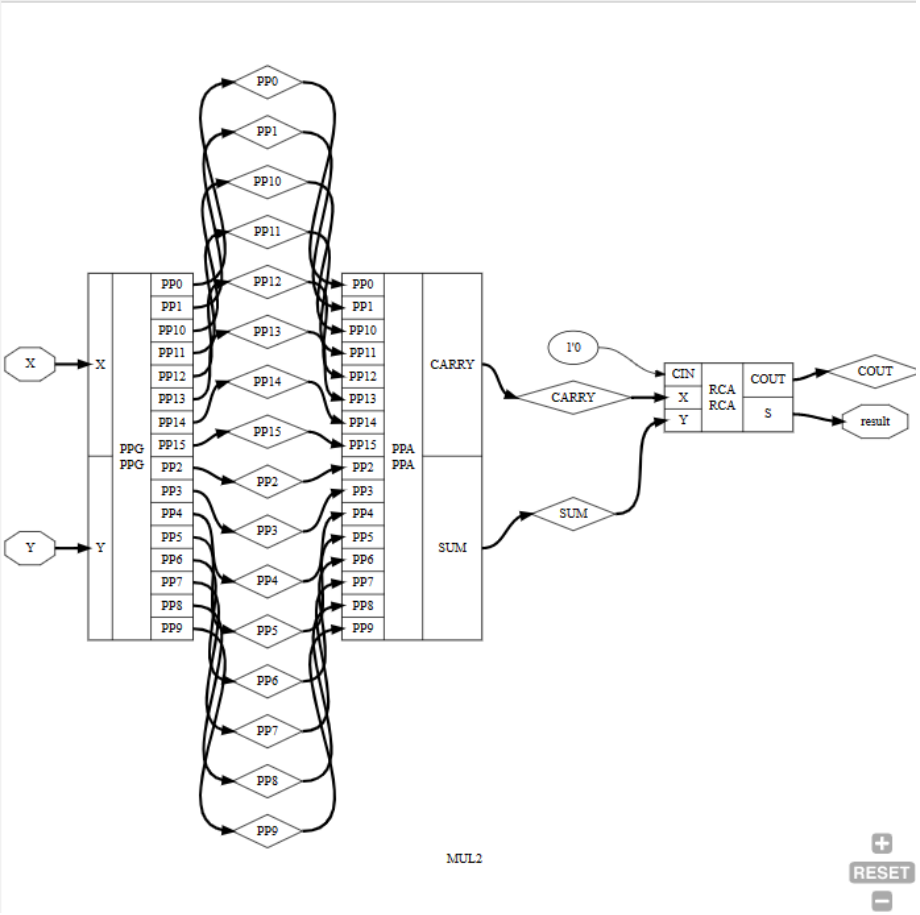
40180069 + 40180070 + 12	= 80360151
40180069 + 40180070 + 14	= 80360153
40180069 + 40180070 + 16	= 80360155
40180069 + 40180070 + 18	= 80360157

RCA is a summation circuit. Behavioral simulation results of the designed 32-bit RCA circuit are shown above. Both entries were collected from the desmos calculator to verify the results. Collection results are mentioned above. When the summation results and the simulation results of the circuit are compared, it is seen that 1 to 1 correct results are obtained. Thus, it has been verified that the circuit works correctly

In the .dot file the generated FULL adders in the 32bit RCA circuit and the inputs connected to them are seen. For detailed view, you can see the dot file in the folder. I have outlined part of the circuit below when the image is too large.



5- MUL



- Behavioral Simulation Results (iVerilog)

```
Y =     1, X =     0, result =         0, expected result=         0
Y =     2, X =  1235, result =      2470, expected result=      2470
Y =     1, X = 12373, result =     12373, expected result=     12373
Y =    10, X =   151, result =      1510, expected result=      1510
Y =  1000, X =  1235, result =   1235000, expected result=   1235000
Y = 12137, X = 12373, result = 150171101, expected result= 150171101
Y =     7, X =    18, result =       126, expected result=       126
Y =     3, X =    19, result =        57, expected result=        57
Y = 12324, X =     2, result =     24648, expected result=     24648
Y =  4095, X =  4095, result =  16769025, expected result=  16769025
```

- Post Synthesis Results (iVerilog)

```
Y =     1, X =     0, result =         0, expected result=         0
Y =     2, X =  1235, result =      2470, expected result=      2470
Y =     1, X = 12373, result =     12373, expected result=     12373
Y =    10, X =   151, result =      1510, expected result=      1510
Y =  1000, X =  1235, result =   1235000, expected result=   1235000
Y = 12137, X = 12373, result = 150171101, expected result= 150171101
Y =     7, X =    18, result =       126, expected result=       126
Y =     3, X =    19, result =        57, expected result=        57
Y = 12324, X =     2, result =     24648, expected result=     24648
Y =  4095, X =  4095, result =  16769025, expected result=  16769025
```

Both simulations work correctly.

Extra Note:

Since the post_tech.dot files are too large and do not fit on the page, I archived them and put them in the folders I uploaded in the assignment. When I view it, there are lots of AND OR NORs.

I've imaged the NAND and XOR gates. They were both very small in resolution and outnumbered.