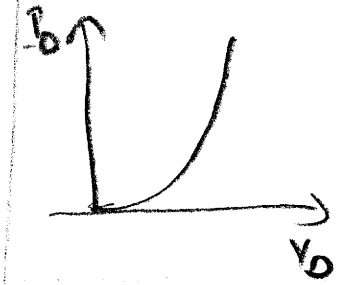
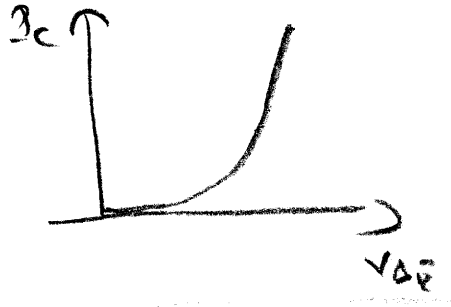
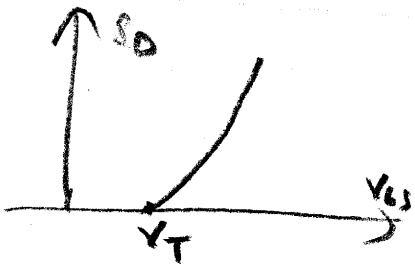
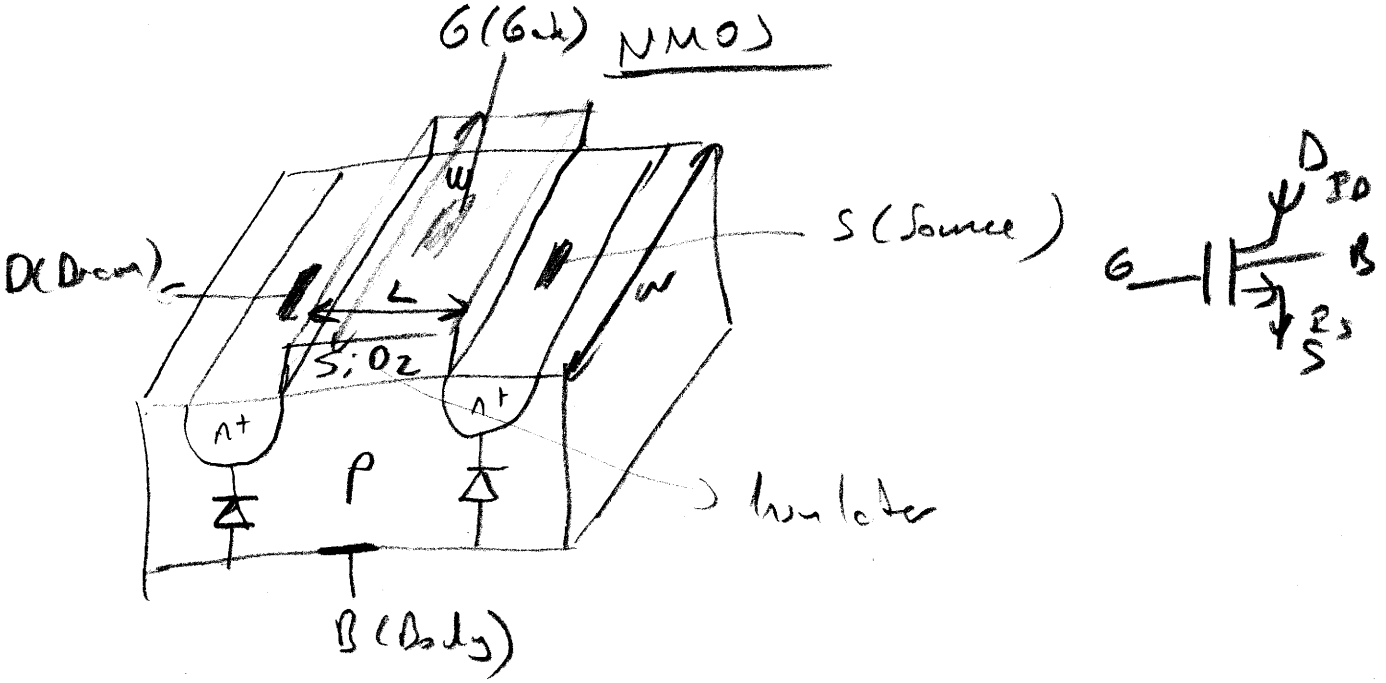
# EHB 322E Digital Electronic Circuits
## SPRING 2015

## Devices for digital circuits

| | Diode | BJT | MOSFET |
|---|---|---|---|
| | + $V_D$ − <br> Anode, Cathode | Collector, Base, Emitter <br> $I_B$, $I_C$, $I_E$, $V_{BE}$ | Drain, Gate, Body, Source <br> $I_D$, $I_S$ |
| # of terminals | 2 | 3 terminal | 4 terminal |
| I vs. V <br> ideal |   |   |   |
| V-I Models | $I_D = I_S(e^{V_D/V_T} - 1)$ | $I_C = I_S(e^{V_{BE}/V_T} - 1)$ <br> $I_B = \frac{I_C}{\beta}$ $(\beta > 40)$ <br> $I_E = (\beta+1) I_B$ | $I_D = K(V_{GS} - V_T)^2$ <br> $I_S = I_D$ <br> $I_G = 0$ <br> $I_B = 0$ |
| Can be a switch | X | ✓ | ✓ |
| Speed | | Best | |
| Power | | | Best |
| Area / Integration | | | Best |

# NMOS, PMOS, and CMOS Structures



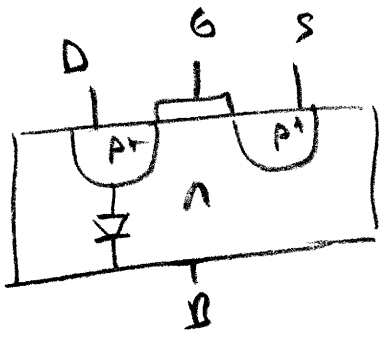

- Symmetric
- $SiO_2$ is an insulator → $I_G = 0$
- $I_B$ should be zero (How?
  + Connect B to the most negative (minimum) voltage node in the circuit.

- If $I_G = 0$ and $I_S = 0$ then

  $I_D = I_S$

- If $V_{GS}$ exceeds a threshold value $V_T$ then there is current flowing between S and D. Electrons are majority carriers
- W ↑ $I_D$ ↑ ; L ↑ $I_D$ ↓

# PMOS

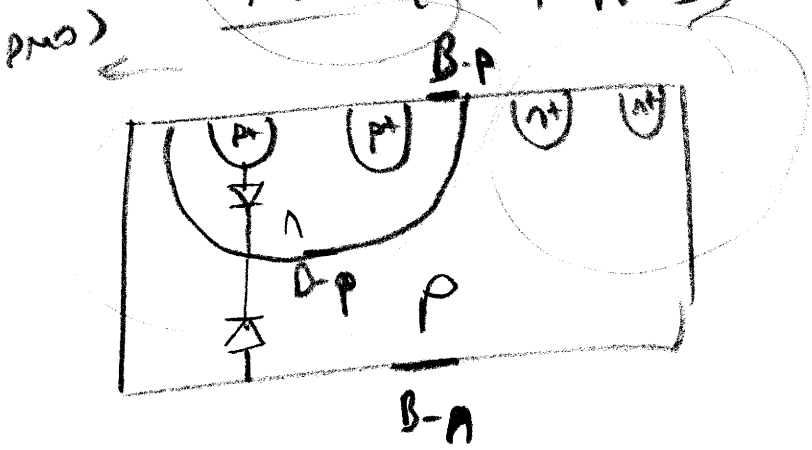




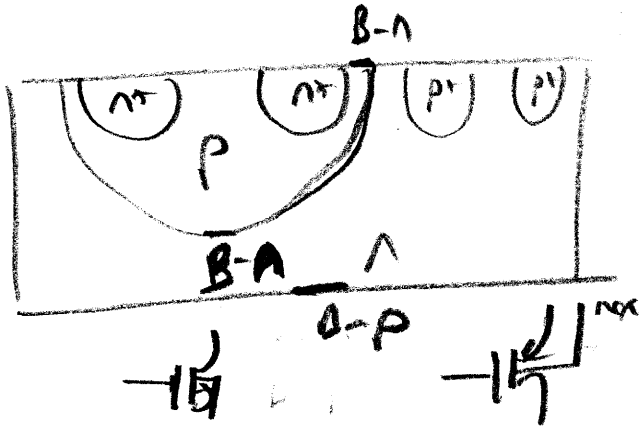
- To make $I_D = 0$ B is connected to the maximum voltage node in the circuit.
- $I_D = I_S$, Holes are majority carriers
- W ↑ $I_D$ ↑, L ↑

## CMOS (Complementary MOS)
(In the same substrate)

Nwell (More preffered) NMOS — why?




Pwell

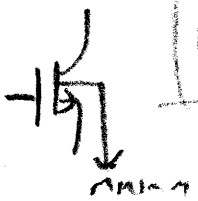





- B-n to S-n
- B-P to the maximum

- Connect B-p (Body of PMOS) to S-p (Source of PMOS)

- Connect B-n (Body of NMOS) to the minimum voltage node

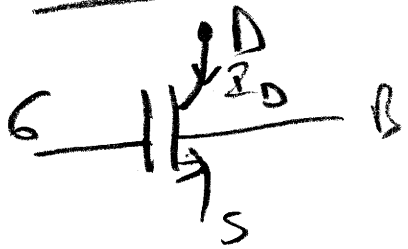


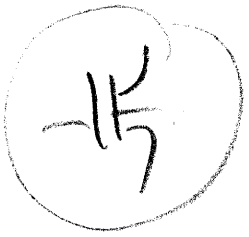

$|V_{BS}|$ ↑ $(|V_T|$ ↑

$V_{SS} = 0$ is the best

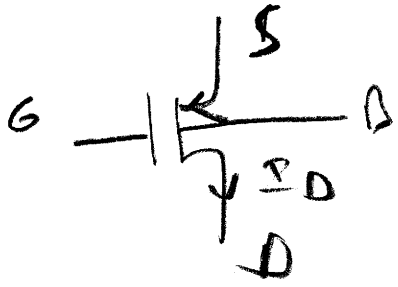
# I-V Models for NMOS and PMOS

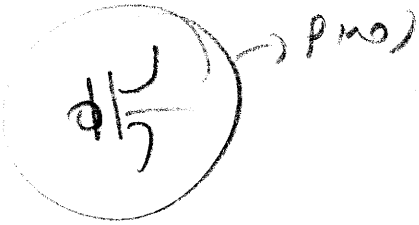
NMOS



PMOS




| Region | Condition | I-V relation |
|---|---|---|
| Cut-off | $\lvert V_{GS}\rvert < \lvert V_T\rvert$ | $I_D = 0$ |
| Linear | $\lvert V_{GS}\rvert \geq \lvert V_T\rvert$<br>$\lvert V_{GS} - V_T\rvert > V_{DS}$ | $I_D = K\left[2(V_{GS}-V_T)V_{DS} - V_{DS}^2\right]$ |
| Saturation | $\lvert V_{GS}\rvert \geq \lvert V_T\rvert$<br>$\lvert V_{GS}-V_T\rvert \leq \lvert V_{DS}\rvert$ | $I_D = K\left\{(V_{GS}-V_T)^2\right\}\left(1 + \frac{V_{DS}}{V_A}\right)$ |

Early effect or channel length modulation

NMOS

- In conduction
  - $I_D > 0$
  - $V_{GS} > 0$
  - $V_{DS} > 0$
  - $V_A > 0$
  - $V_T > 0$
  - $K > 0$

$K = K_n = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}$ → $k_n'$

PMOS

- In conduction
  - $I_D > 0$
  - $V_{GS} < 0$
  - $V_{DS} < 0$
  - $V_A < 0$
  - $V_T < 0$
  - $K > 0$

$K = K_p = \frac{1}{2}\mu_p C_{ox}\frac{W}{L}$ → $k_p'$

- In most cases $|V_A| \gg |V_{DS}|$, so Early effect is neglected

$V_A \approx 40$ $V_{DS} = 1$ $\left(1 + \frac{1}{40}\right) \approx (1)$

- Body effect

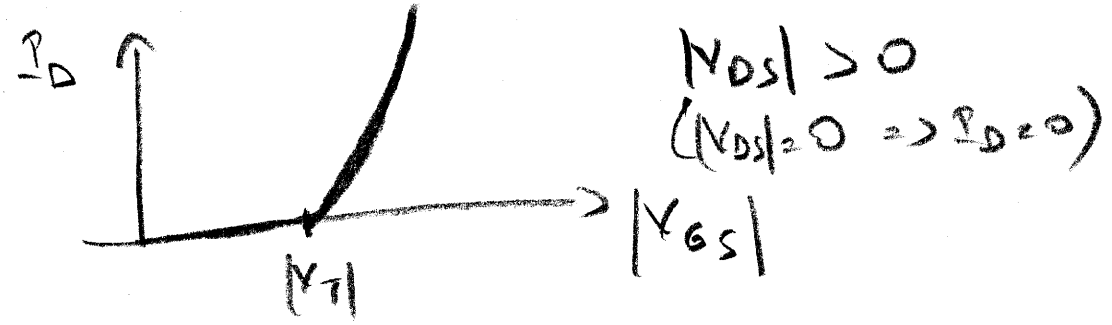
$$V_{TN} = V_{TO} + \gamma\left(\sqrt{|V_{SB} + 2\phi_F|} - \sqrt{|2\phi_F|}\right)$$

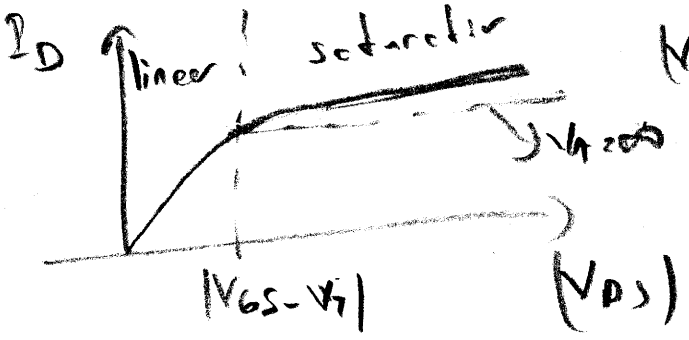
$\phi_F$ : surface potential

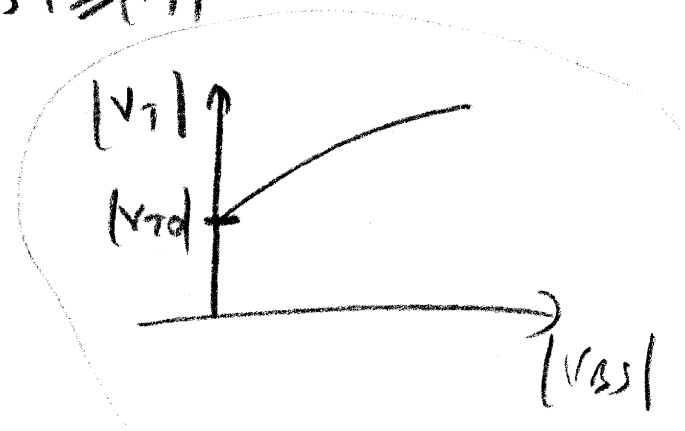
$\gamma$ : body effect parameter

$|V_{SB}| \uparrow$ $|V_T| \uparrow$ $V_{SB} = 0$ is the best

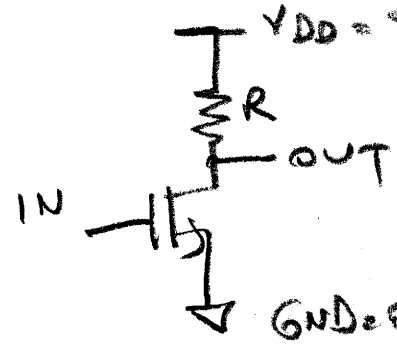
Graphs



Ex-1




Neglect Early Effect (needless here)

$k_n' = \mu_n C_{ox} = 25\ \mu A/V^2$

$V_T = 2V$

$W = 8\mu$

$L = L_{min} = 1\mu$

$R = 1k$

① If IN = 0V OUT = ?

② If IN = 5V OUT = ?

① IN = 0V

$I_D = 0 \Rightarrow$ OUT = 5V

② IN = 5V

linear ↙ ↘ saturation

Suppose that the transistor is in saturation

$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T)^2$

$I_D = \frac{1}{2} 25\mu \cdot 8 \cdot (5-2)^2 = 0.9\ mA$

OUT = $5 - 1k \cdot 0.9m = 4.1V \geq (V_{GS} - V_T) = 3V$ saturation ✓

Suppose that R is not known
For which values of R the transistor is in saturation and linear?

If $R \geq 2{,}22\,k$ then Linear

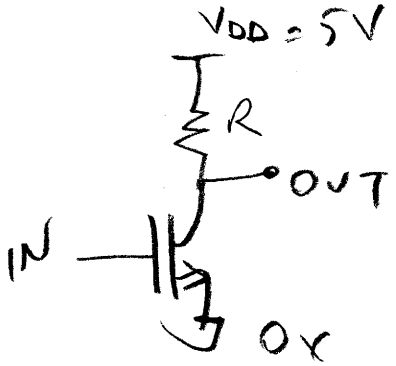
If $R < 2{,}22\,k$ then S-duration

I want to implement an inverter, but the previous circuit can not be used as an inverter

| IN | OUT | |
|---|---|---|
| 0 V | 5 V | → logic 1 |
| 5 V | 4,1 V | → can not be logic 0 |

logic 0 ← 0 V
logic 0 ← 5 V

Ex-2




$k'_1 = 25\,\mu A/V^2$, $R = 48\,k$
$V_T = 2V$, $L_{min} = 1\mu$

Design an inverter using the circuit shown below. The inverter should meet the specifications shown below

| IN | OUT |
|---|---|
| 0 V | 5 V |
| 5 V | < 0,2 V |

$L_{min}$ ? $W_{min}$ ?

If IN = 5V and OUT = 0.2

then $V_{GS} - V_T > V_{DS}$ → linear region

$5 - 2 > 0.2$

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} \left[ 2(V_{GS} - V_T) V_{DS} - V_{DS}^2 \right]$$

$$I_D = I_R = (V_{DD} - V_{out}) / R = \frac{4.8}{48k} = 0.1mA$$

$$\Rightarrow 0.1mA = \frac{1}{2} 25\mu \left(\frac{W}{L}\right) \left\{ 2(3)(0.2) - (0.2)^2 \right\}$$

$$\Rightarrow \frac{W}{L} = \frac{8}{1.16} = 6.896$$

We can select $W = 7\mu$

$L = 1\mu$

If IN = 5V,

$\frac{W}{L}$ ↑ OUT ↓

R ↑ OUT ↓

# Stedre power (SP)

Prof

| IN | OUT | ID | Stedre Power |
|---|---|---|---|
| 0V | 5V | 0 A | 0 |
| 5V | 4,1 | 0,9mA | 5.0,9 = 4,5mW |

Lv-2

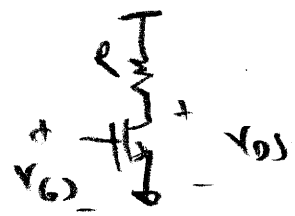
| IN | OUT | ID | Stedre Power ( |
|---|---|---|---|
| 0V | 5V | 0 | 0 |
| 5V | 0,2V | 0,1mA | 5.0,1 = 0,5mW |

## I ↑ SP ↑

$$I = \frac{V_{DD} - V_{DS}}{R} \quad , \quad I = K\left\{2(V_{GS} - V_T)V_{DS} - V_{DS}^2\right\}$$

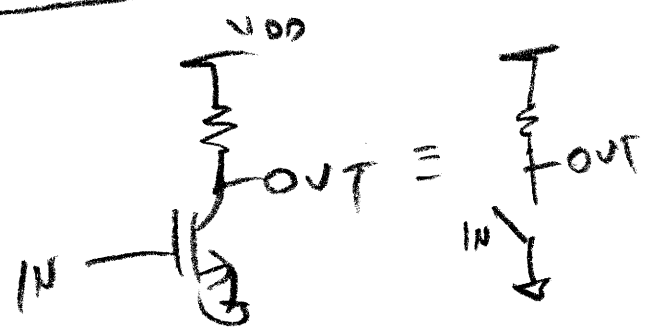
↓ $\frac{W}{L}$ • R ↑ $V_{DS}$ ↓ SP ↓

↓ $\frac{W}{L}$ ↑ L • $V_{DS}$ ↓ SP ↑



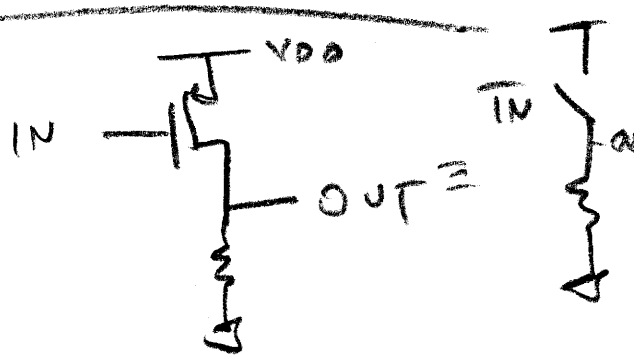
# Inverters

## NMOS Inverter



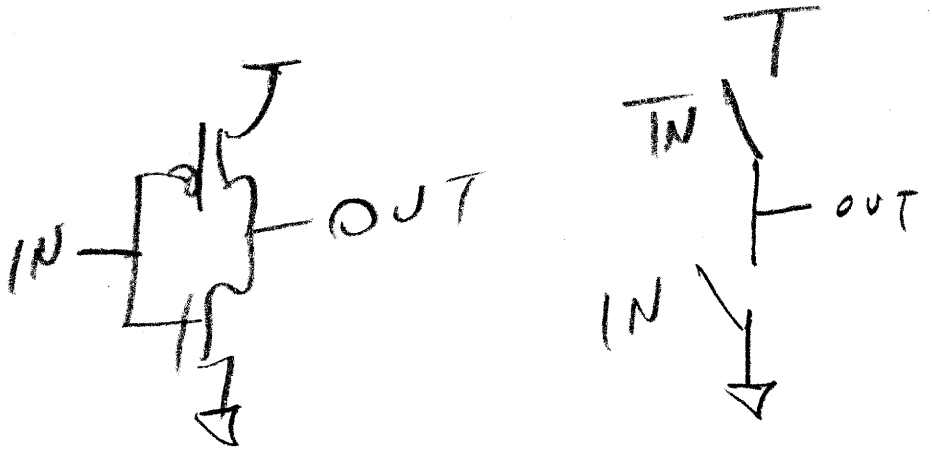

Consumes static power when IN = VDD

## PMOS Inverter




Consumes static power when IN = 0V

## CMOS Inverter




No static power

| IN | OUT |
|---|---|
| 0V | 5V |
| 5V | 0V |