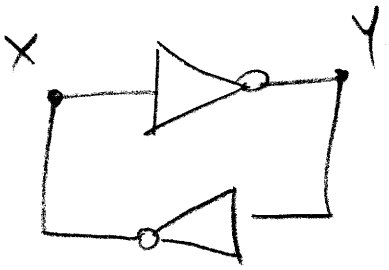
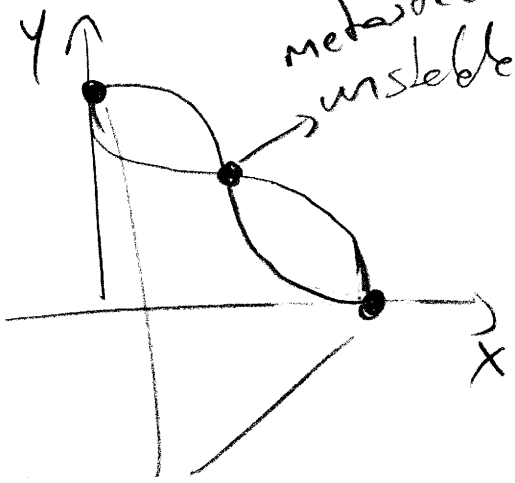
EHB 322E Digital Electronic Circuits
SPRING 2015

Digital Circuits

- Combinational (Uses only the present)
- Sequential (Remembers the past) (stores the present)

- Latches or flip-flops are the basic building block of sequential circuits.
- Flip-flops have 2 stable states.





bistability

metastable states tend to shift to stable states.
- small changes in X or Y make X=0 Y=VDD or X=VDD Y=0

Flip-Flops

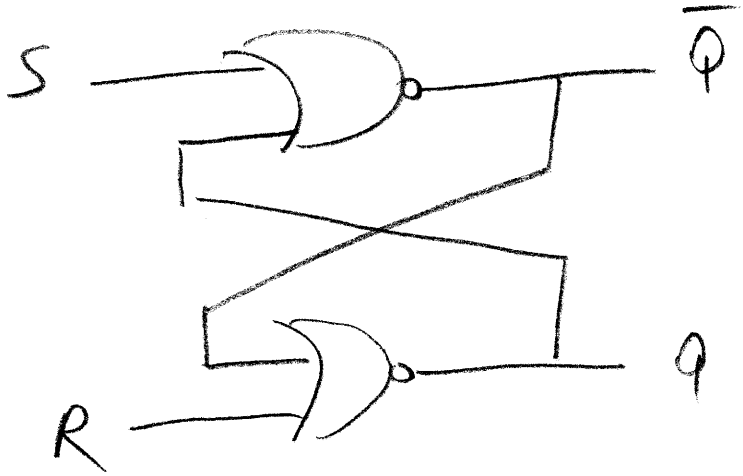
- Static
- Dynamic (CLK)

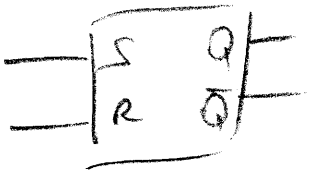
Static flip-flops

S-R flip-flop

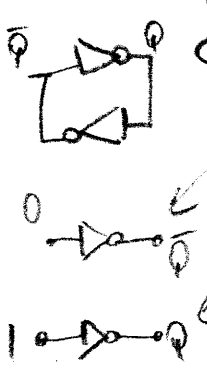
S → set
R → reset

(1) NOR-based

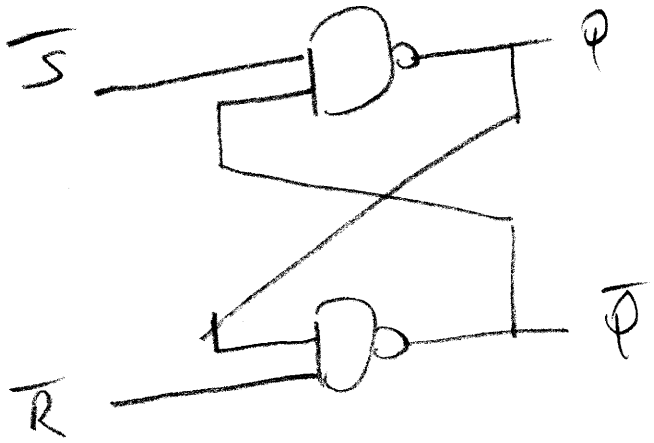




INPUTS		OUTPUTS		
S	R	Q	Q̄	
0	0	Q_{pre}	$\bar{Q}_{pre}$	H (HOLD)
0	1	0	1	R (RESET)
1	0	1	0	S (SET)
1	1	0	0	NA (NOT ALLOWED)



(2) NAND-based



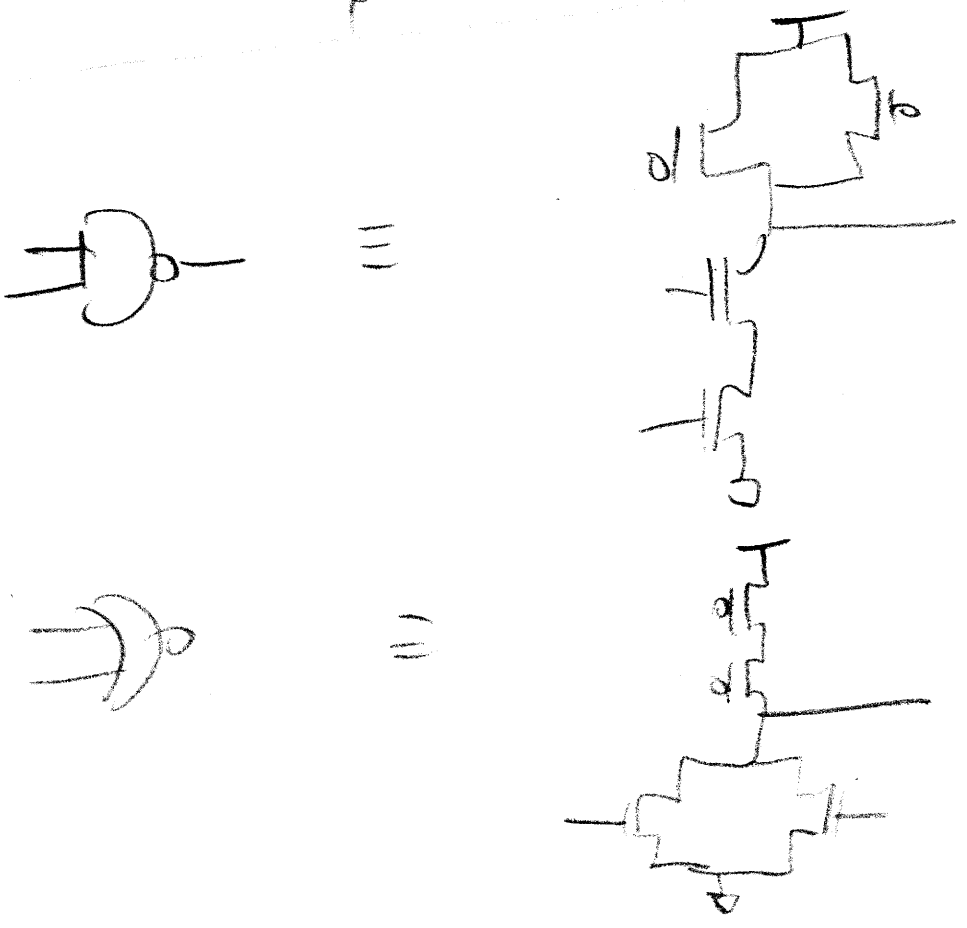
$\bar{S}$	$\bar{R}$	Q	$\bar{Q}$	
0	0	1	1	NA
0	1	1	0	S
1	0	0	1	R
1	1	Q_{pre}	$\bar{Q}_{pre}$	H

NOR

$$Q = S\bar{R} + \bar{S}\bar{R}\,Q_{pre}$$
$$Q = S\bar{R} + \bar{R}\,Q_{pre}$$

NAND

$$Q = SR + S\bar{R} + \bar{S}\bar{R}\,Q_{pre}$$
$$Q = S + \bar{R}\,Q_{pre}$$



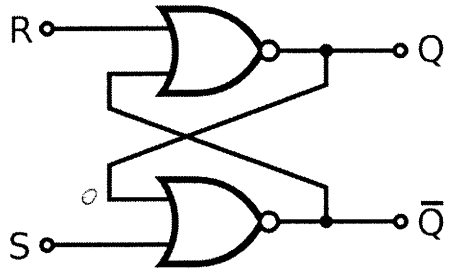
NAND-based
8 tran.

NOR-based
8 tran

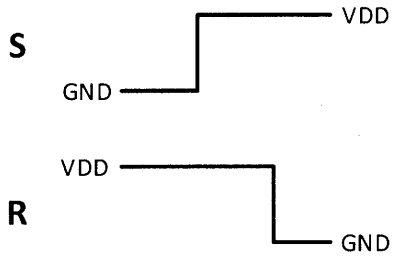
(4)

Consider an S-R flip-flop consisting of two identical CMOS NOR gates, shown below. Suppose that load capacitors of **1pF** are connected to the outputs Q and $\bar{Q}$. Neglect all internal MOS capacitors.

Equivalent resistor for an NMOS transistor: R_N**= (12kΩ) / (W/L)**$_N$
Equivalent resistor for a PMOS transistor: R_P**= (24kΩ) / (W/L)**$_P$
Transistor dimensions for all transistors: $W_P = W_N = L_P = L_N$**=1u**



An S-R Flip-Flop

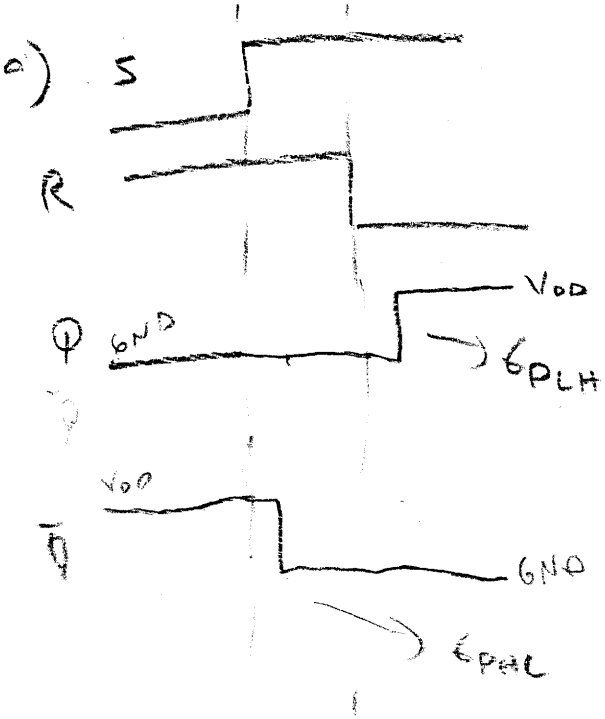


Input Signals

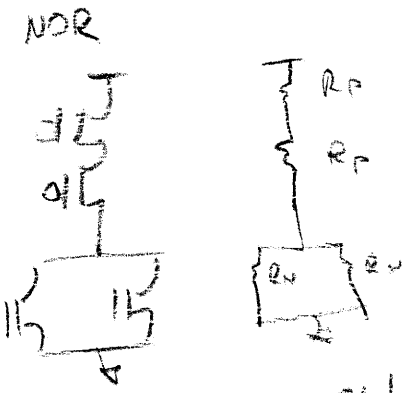
a) Sketch the **waveforms** at the outputs Q and $\bar{Q}$ if the input signals shown above are applied to the flip-flop.

b) Calculate the **total propagation delays** at the outputs Q and $\bar{Q}$ if the input signals shown above are applied to the flip-flop.

a)



b)



$R_P = 24k / 1 = 24k$

$R_N = 12k / 1 = 12k$

Delay $t_Q = 0,69(2k_P)C_L$

$= 0,69\ 48k\ 1p = 33,1ns$

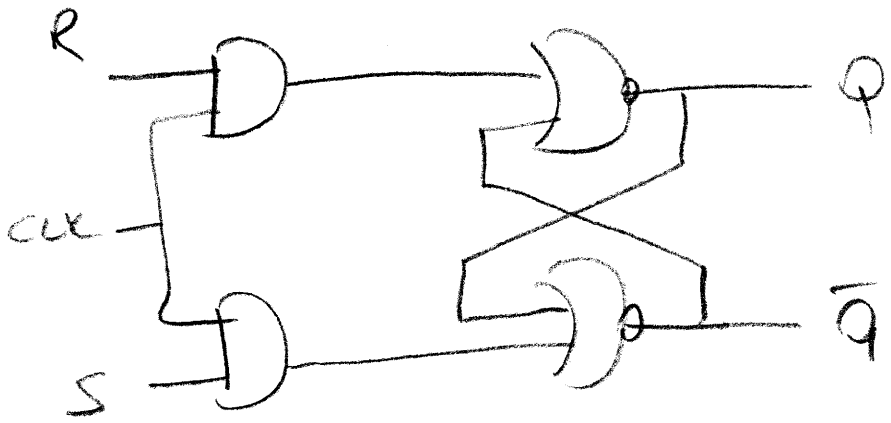
Delay $t_{\bar{Q}} = 0,69(R_N)C_L$

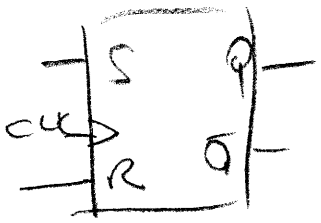
$= 0,69\ 12k\ 1p = 8,3ns$

Since 1 NMOS transistor

Dynamic flip-flops

S-R dynamic flip-flop





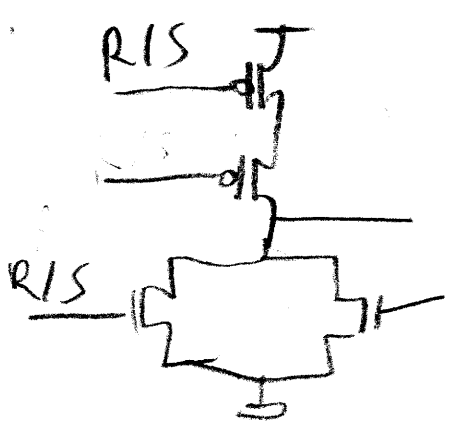
CLK = 0 HOLD

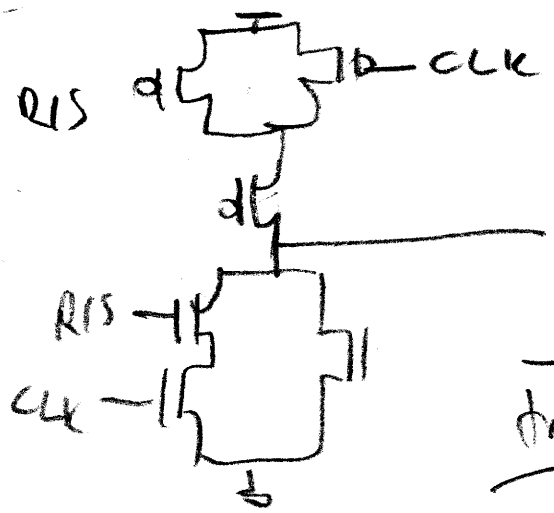
CLK = 1 Save ⇒ static

needs 20 transistors!

Simpler implementation (CMO)

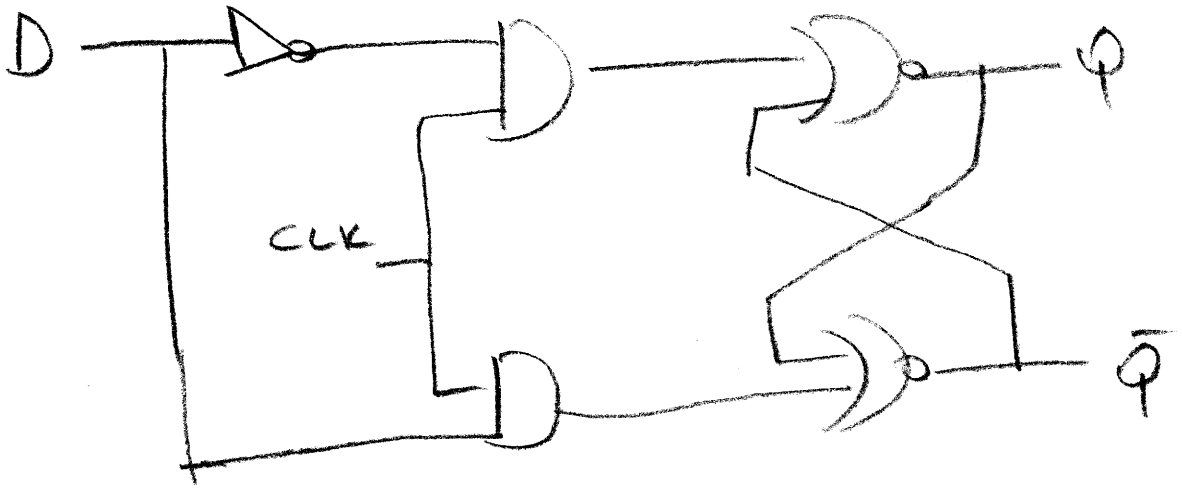
Replace R with R.CLK in NOR-based static FF
S with S.CLK





12 transistors

D flip-flop



CLK	D	Q	$\bar{Q}$	
0	0, 1	Q_{pre}	$\bar{Q}_{pre}$	HOLD
1	0	0	1	RESET
1	1	1	0	SET

10 transistors