06/04/2015 - WED

EHB 322E Digital Electronic Circuits

SPRING 2015

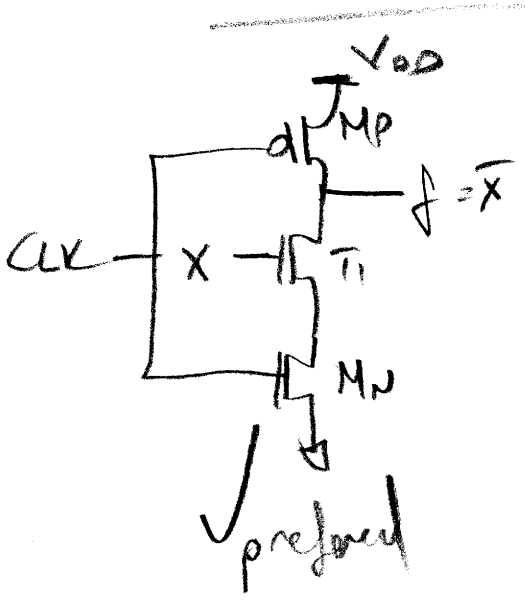
Dynamic (CMOS) Logic

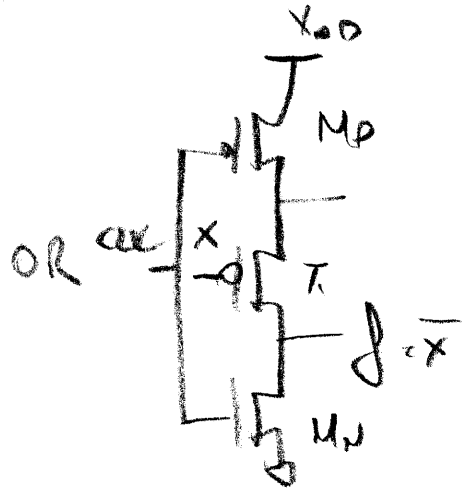
Dynamic : changes over time
Static : stabilizes over time

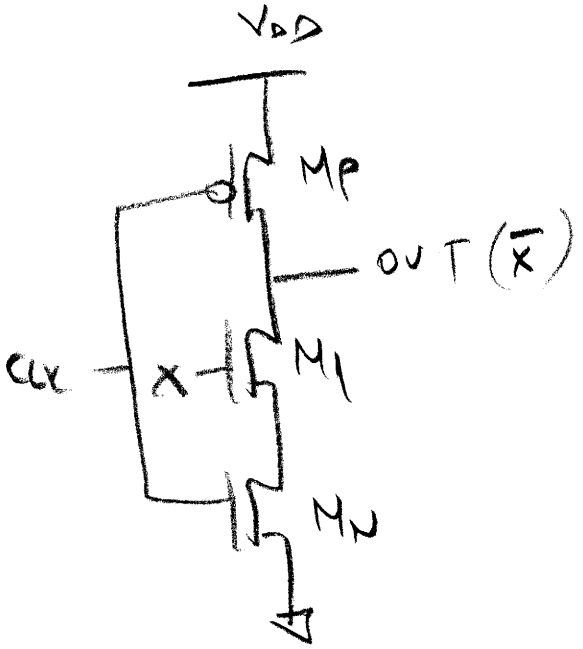
Goals
1) No resistors
2) No static power
3) Fewer transistors compared to CMOS
4) Faster than CMOS and PTL

Drawbacks
1) Extra clock signal is needed
2) Design is much more difficult compared to CMOS
3) Output is floating (open) in some cases worsening signal quality

Inverter with a Dynamic Logic







If CLK = 0V (Precharging)

OUT is VDD

If CLK = VDD (Evaluation)

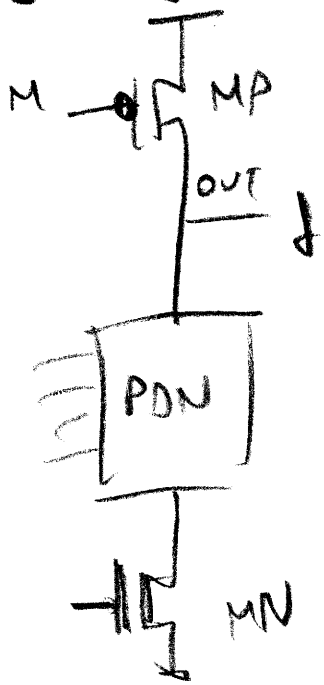
OUT is $V_{DD} - V_x$ ($f = \bar{x}$)

$$OUT = \overline{CLK} + CLK(\bar{x})$$

f (target function)

General Dynamic Logic

Given a target function f to be implemented



$OUT = \overline{CLK} + CLK(f)$

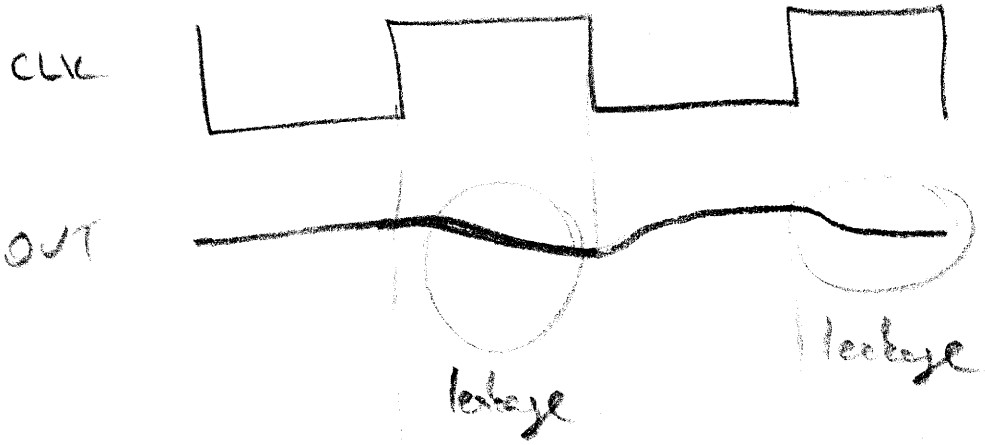
If f has a literal count $\underline{\underline{n}}$ in factored form

$\underline{\underline{n+2}}$ transistors are needed in Dynamic Logic

Problems in Dynamic Logic (when OUT is floating)

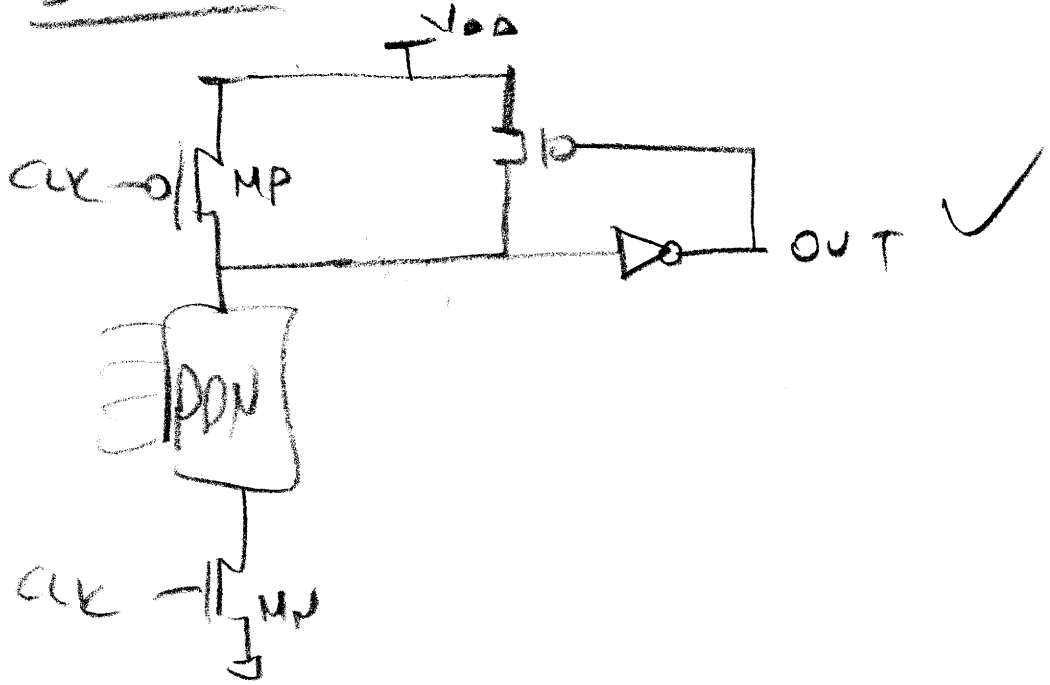
(1) Charge leakage problem

Supposed that $f_{clk} = 1$



OUT is open

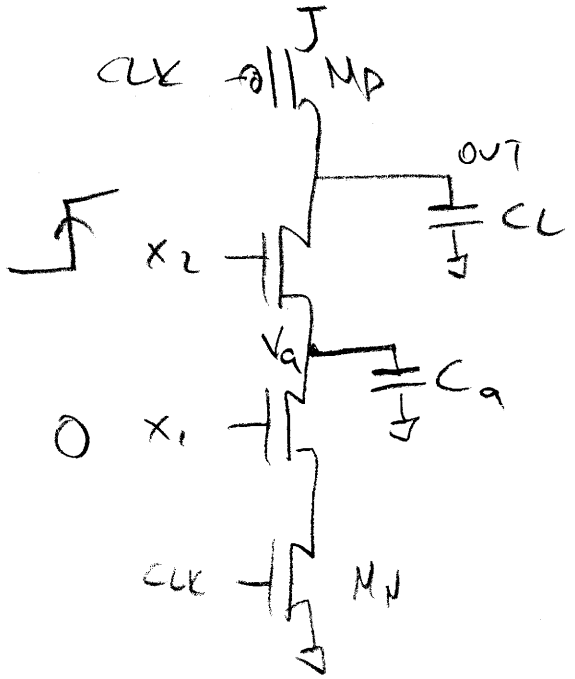
Solution

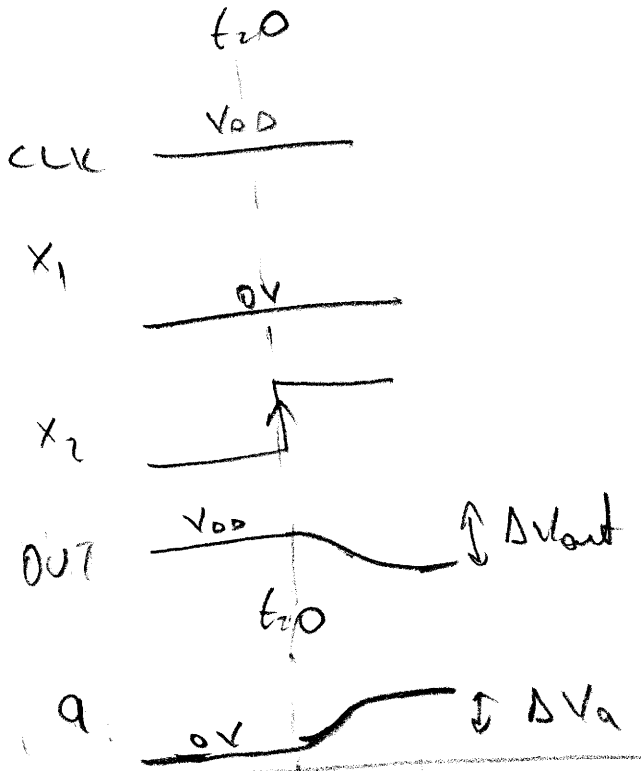


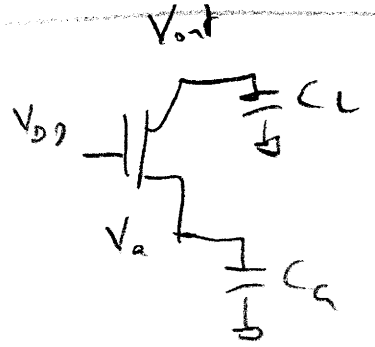
② Charge-Sharing Problem

Suppose that $\phi = 1$, $CLK = 1$, $X_1 = 0$, $X_2 = 0 \to 1$

, $V_{a\text{-initial}} = 0$







$$C_L \left|\frac{dV_{out}}{dt}\right| \simeq C_a \left|\frac{dV_a}{dt}\right| \quad (|I_{C_L}| = |I_{C_a}|)$$

$$\Rightarrow C_L \frac{\Delta V_{out}}{\Delta t} \simeq C_a \frac{\Delta V_a}{\Delta t}$$

$$\Rightarrow \boxed{C_L \cdot \Delta V_{out} \simeq C_a \Delta V_a}$$

$V_{out\text{-}initial}(t=0) = V_{DD}$ $V_{a\text{-}initial}(t=0) = 0V$

Two cases to stop current flow

(1) $V_{out\text{-}final} \geq V_{DD} - V_{TN}$ $\Delta V_{out} \leq V_{TN}$

$V_{a\text{-}final} = V_{DD} - V_{TN}$ $\Delta V_a = V_{DD} + V_{TN}$

$$\frac{C_L}{C_a} = \frac{\Delta V_a}{\Delta V_{out}} \Rightarrow \boxed{\frac{C_L}{C_a} \geq \frac{V_{DD} - V_{TN}}{V_{TN}}}$$

should be satisfied

(2) $V_{out\text{-}final} < V_{DD} - V_{TN}$ $\Delta V_{out} > V_{TN}$

$V_{a\text{-}final} = V_{out\text{-}final}$ $\Delta V_a = V_{DD} - \Delta V_{out}$

$$\frac{C_L}{C_a} > \frac{\Delta V_a}{\Delta V_{out}} \Rightarrow \boxed{\frac{C_L}{C_a} = \frac{V_{DD} - \Delta V_{out}}{\Delta V_{out}}}$$

$$\Rightarrow \boxed{V_{out\text{-}final} = \frac{V_{DD} \cdot C_a}{C_a + C_L}}$$

should be avoided

Ex $C_a = 1pF$ $V_{DD} = 5V$ $V_{TN} = 1V$

Determine $V_{out\text{-}final}$ if

a) $C_L = 5pF$

b) $C_L = 3pF$

Check if $\frac{C_L}{C_q} \geq \frac{V_{DD}-V_{TN}}{V_{TN}}$ is satisfied

a) $\frac{5}{1} \geq \frac{4}{1}$ ✓ $\Rightarrow$ $\Delta V_q = V_{DD} - V_{TN} = 4V$

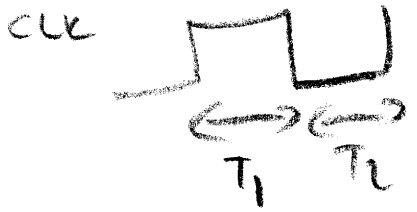
$\Rightarrow$ $\Delta V_{out} = \frac{\Delta V_q}{5} = 4/5 = 0,8V$

$\Rightarrow$ $V_{out\text{-}final} = 4,2V$

b) $\frac{3}{1} \geq 4$ ✗ $\Rightarrow$ $V_{out\text{-}final} = \frac{5.1}{4} = 1,25V$

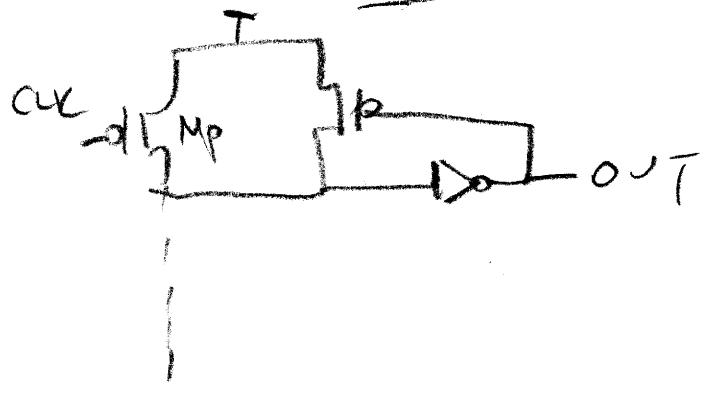
(too small)

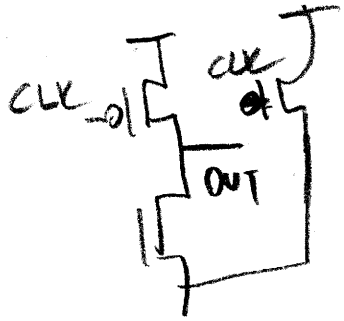
— $V_{out\text{-}final}$ can not be seen if T_1 is not large enough



— $V_{out\text{-}Inibel}$ might not be V_{DD} if T_2 is not large enough

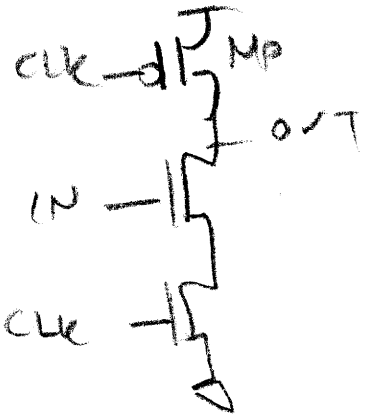
2 Solutions

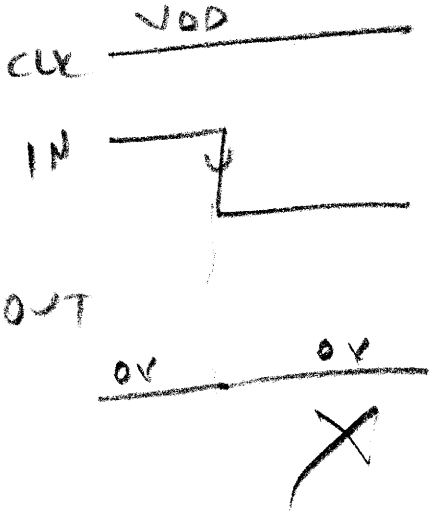




Delays in Dynamic Logic

- Inputs should be switched during the precharge (CLK=0) operation.



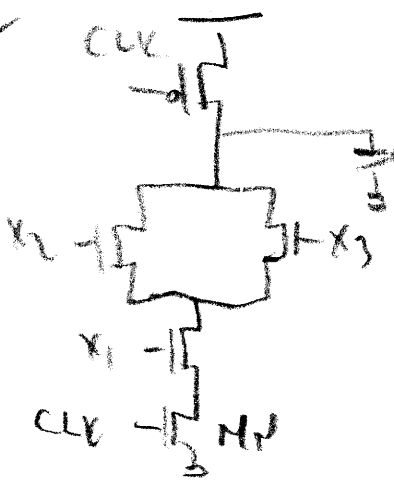


- t_{PLH} is determined by a single transistor

  Mp

- t_{PHL} is determined by PDN and MN

Ex



$f = \bar{x}_2 \bar{x}_3 + \bar{x}_1$

$C = 1p$ $R_N = 1k$ $R_p = 2k$

Neglect Internal MOS cap

Best case and Worst case Delays?

$t_{PLH(WC,BC)} = 0.69\ (2k)\ (1p)$

$t_{PHL(WC)} = 0.69\ (3k)\ (1p)$ $t_{PHL(BC)} = 0.69\ (2.5k)\ (1p)$