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EHB322E Digital Electronic Circuits

Quiz 2

Duration: 30 Minutes; Grading: 1) 40%, 2) 60%,

Quiz is in closed-notes and closed-books format; calculators are allowed

For your answers please use the space provided in the exam sheet

GOOD LUCK!

- Suppose that all NMOS transistors are identical and all PMOS transistors are identical.
Equivalent resistor for an NMOS transistor: $R_N = (12\text{k}\Omega) / (W/L)_N$
Equivalent resistor for a PMOS transistor: $R_P = (24\text{k}\Omega) / (W/L)_P$
 - Suppose that each circuit node (including outputs) has a capacitance value of **10pF**.
- 1) Consider a Boolean function $f = x_1 \overline{x_3} + \overline{x_1} \overline{x_2} x_3 + x_2 \overline{x_3}$ to be implemented. Find the minimum values of $[(W/L)_P + (W/L)_N]$ if f is implemented with “NMOS and PMOS (CMOS) Pass Transistor Logic” and worst case propagation delays $t_{PLH} = t_{PHL} = 82,8\text{ns}$ ($120 \times 0,69 = 82,8$) should be achieved.

- 2) Consider an approximate adder shown below. Derive Boolean expressions for outputs **Sum** and **Cout** in terms of inputs **A**, **B**, and **Cin**. Calculate worst case propagation delays t_{PLH} and t_{PHL} if $(W/L)_P = (W/L)_N=1$ for all transistors.

