Very Large Scale Integration II - VLSI II

Introduction to Digital World

Prof. Dr. Berna ÖRS

Araş. Gör. Fırat Kula

ITU VLSI Laboratories

Istanbul Technical University

Syllabus (Tentative)

- Week 1
  - Introduction to Digital World
  - Digital Design Methodology
  - Verilog Basics
- Week 2
  - Verilog Basics
- Week 3
  - Full Custom gate design
- Week 4
  - Design example using Verilog
  - Behavioral Simulation Using Xcellium
- Week 5
  - Synthesis Using GENUS
  - Place and Route Using Encounter
- Week 6
  - Signout
  - Verilog and Full Custom Design Integration
- Week 7
  - Instruction Set Architecture
  - RISCV Instruction Set Architecture
- Week 8
  - Memory Structures
  - Cache Hierarchies
- Week 9
  - Hardware Arithmetic

Syllabus (Tentative)

- Week 10
  - RF & Datapath & Single Cycle Control
- Week 11-12
  - Basic Pipelining
  - Hazard Handling
- Week 13-14
  - Q&A

Text Books

- Morris Mano, Charles Kime, Tom Martin, Logic and Computer Design Fundamentals, Pearson Education Limited, 5th Edition, 2015.
- John L. Hennessy, David A. Patterson, Computer Architecture: A Quantitative Approach, Morgan Kaufmann, 6th Edition, 2017.
- Frank Vahid, Digital Design with RTL Design, Verilog and VHDL, Wiley, 2nd Edition, 2010.
- Frank Vahid, Tony Givargis, Embedded System Design: A Unified Hardware/Software Introduction, John Wiley & Sons, 2002.

Time Table (Tentative)

- 1st Homework
  - Reseach about available Technologies
- 2nd Homework
  - Custom gate design and implementation
- 3rd Homework
  - Combinational circuit design and implementation
- 4th Homework
  - Finite state machine design and implementation
- 5th Homework
  - Memory design for your processor
  - Research about RISC-V ISA
- 6th Homework
  - ALU design for your processor
- 7th Homework
  - Datapath design for your processor
  - Controlpath design for your processor
  - Single cycle control processor design
- 8th Homework
  - Pipeline design for your processor
  - Hazard handler design for your processor
  - Testing your processor
- 9th Homework
  - Documentation of your processor

Grading

- Average of first 6 homeworks will be grade for midterm
- Average of last 3 will be grade for final
- Term grade=midterm*0,6+final*0,4

Outline

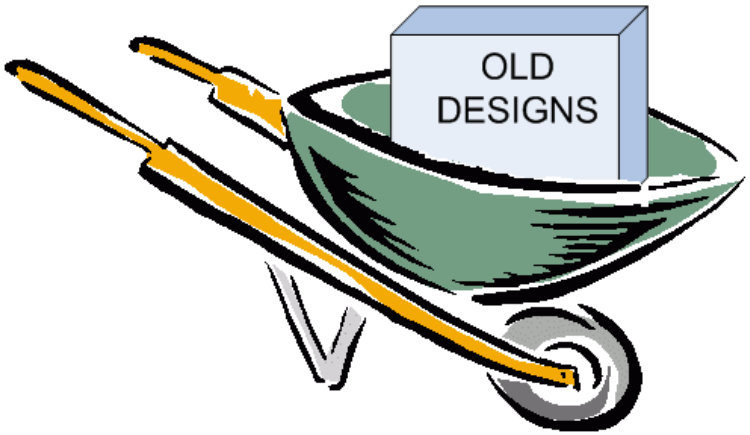
- Why Digital?
- Why NOT Digital?
- Considerations of Digital Technology
- Limitations of Digital Technology

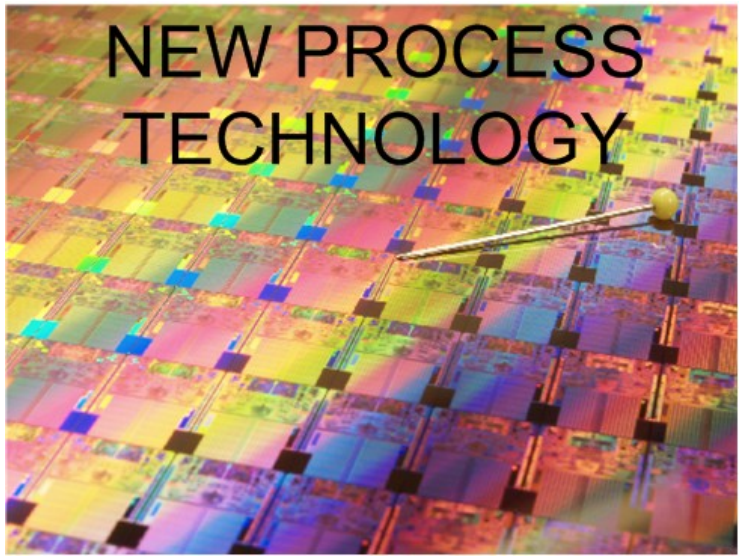
Why Digital?

- Ease of Design
  - Low Idea-to-Product Time

Why Digital?

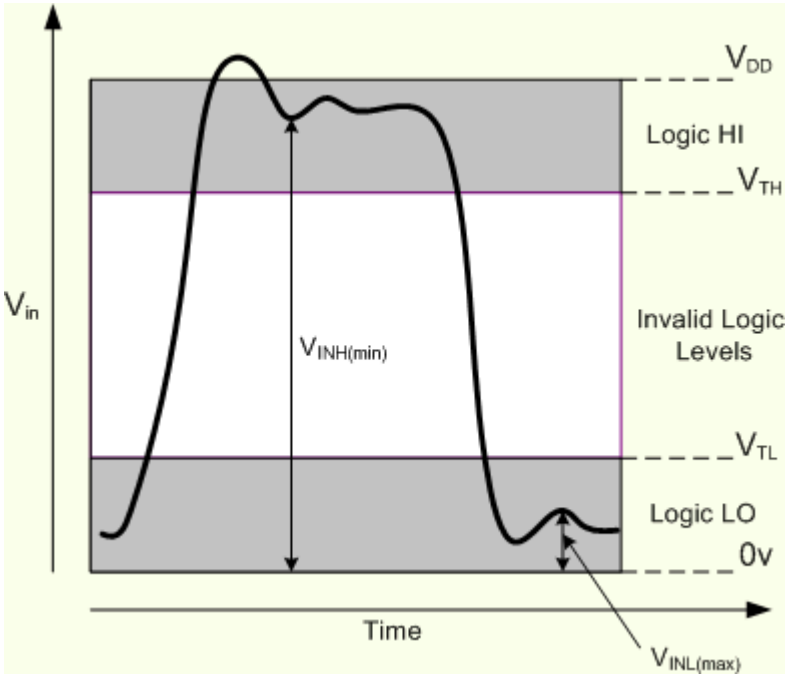
- Ease of Design
  - Portability





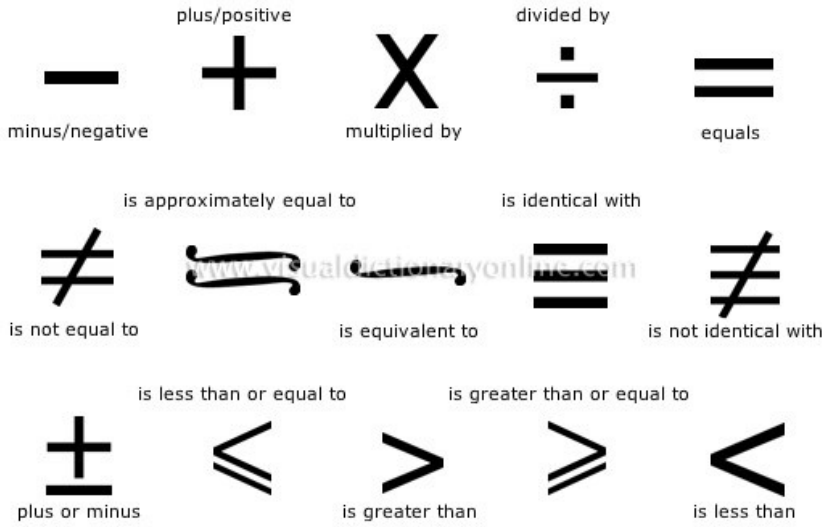
Why Digital?

- Ideal World
  - Immunity to Noise



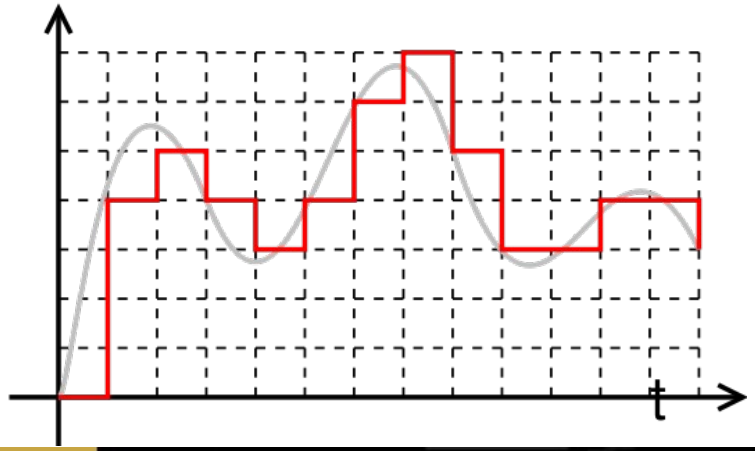
Why Digital?

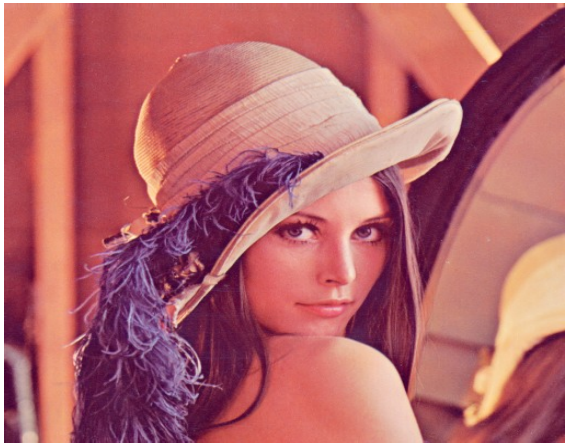
- Ideal World
  - Only mathematical and logical operations
    - Zero error for some operations
    - Customizable precision



Why Digital?

- Ideal World
  - Easy Signal Processing



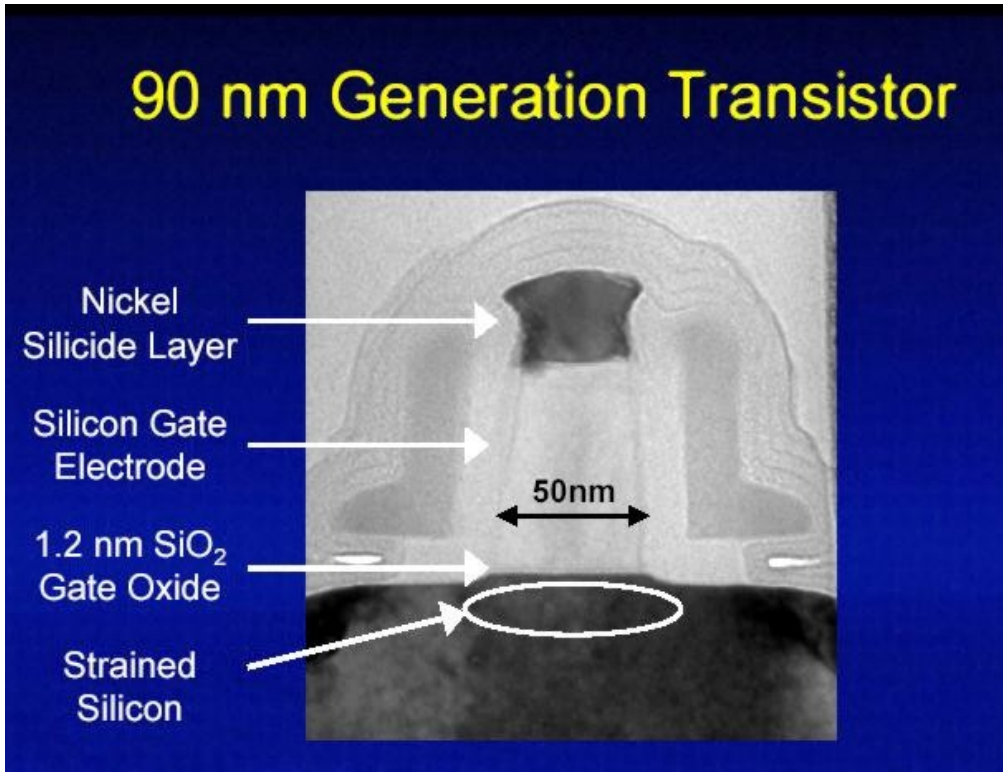


Why Digital?

- Programmability
  - Can be programmable on the fly
  - Can change the behavior completely

Why Digital?

- Technology (scaling) driven

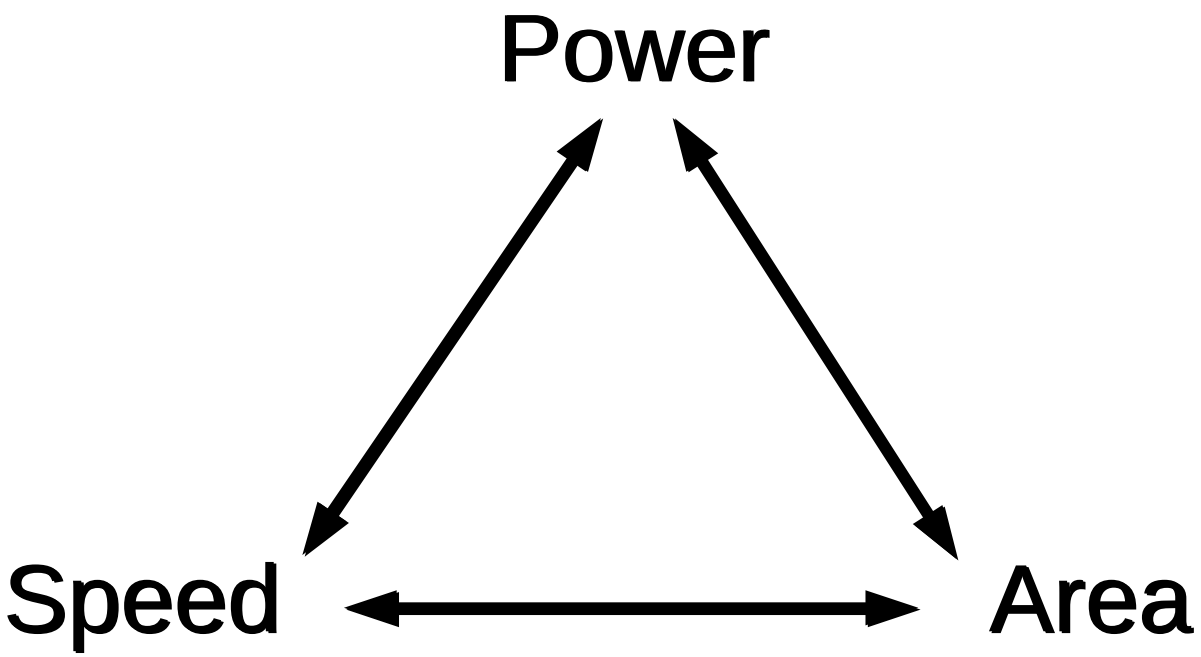


Why NOT Digital?

- Sound
- Electromagnetic Waves
  - Light etc.
- All other sensory data
  - Pressure
  - Temperature
  - Humidity etc.
- Short, The World is **ANALOG**

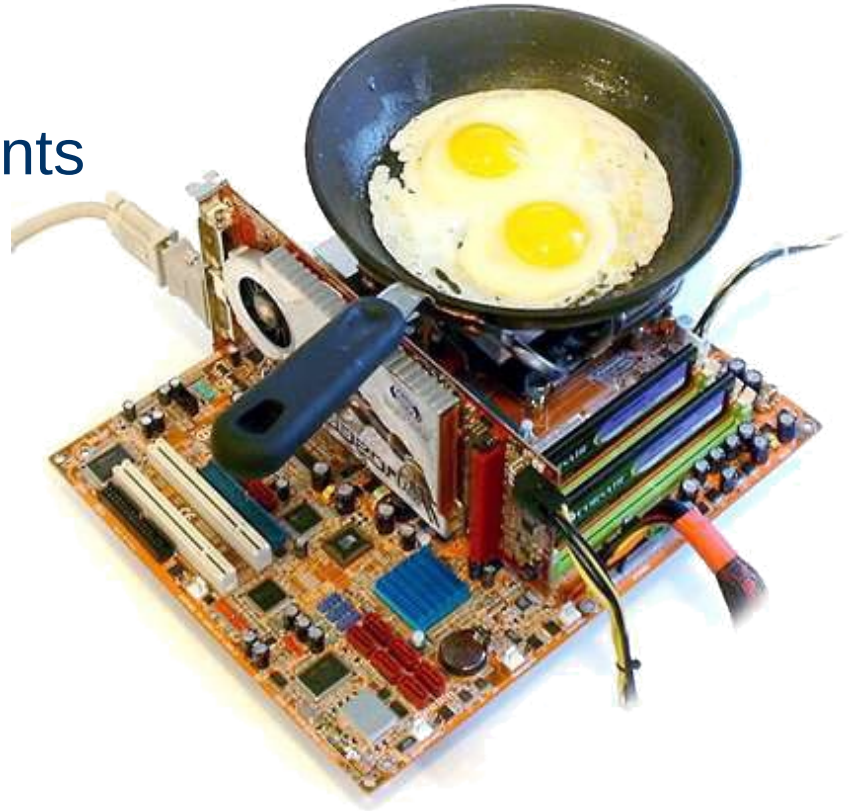
Considerations of Digital Technology

Trade-off Triangle



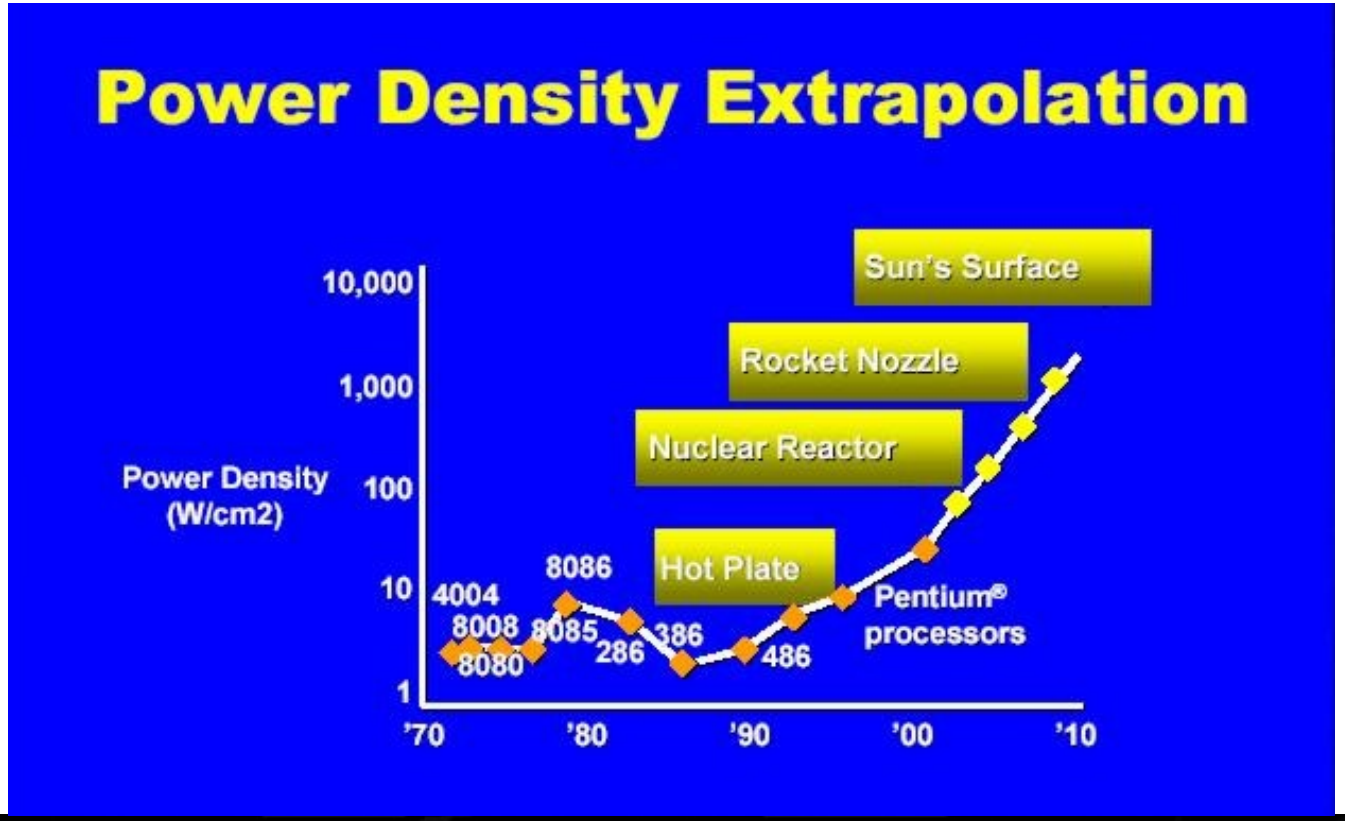
Limitations of Digital Technology

- Total Power = Dynamic Power + Static Power
- Dynamic Power → $C.f.V_{DD}^2$
- Static Power → Leakage Currents



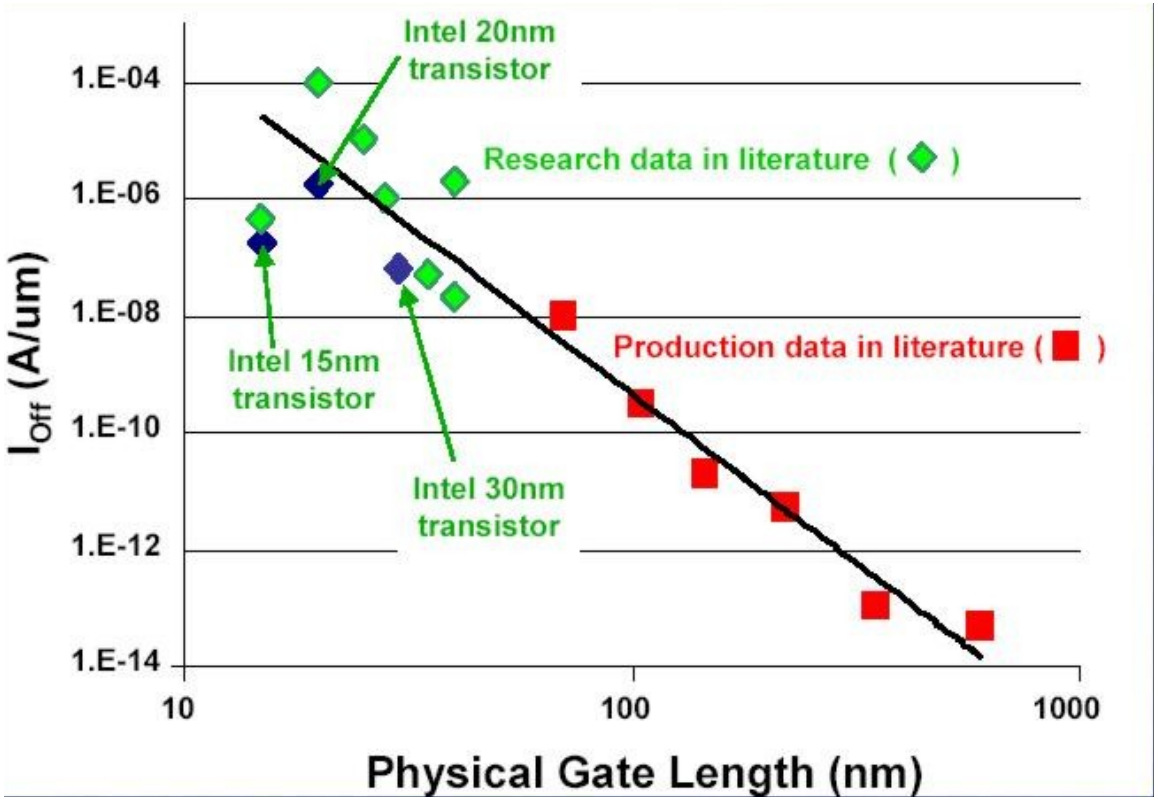
Limitations of Digital Technology

- Power Density = Power Consumption per Unit Area



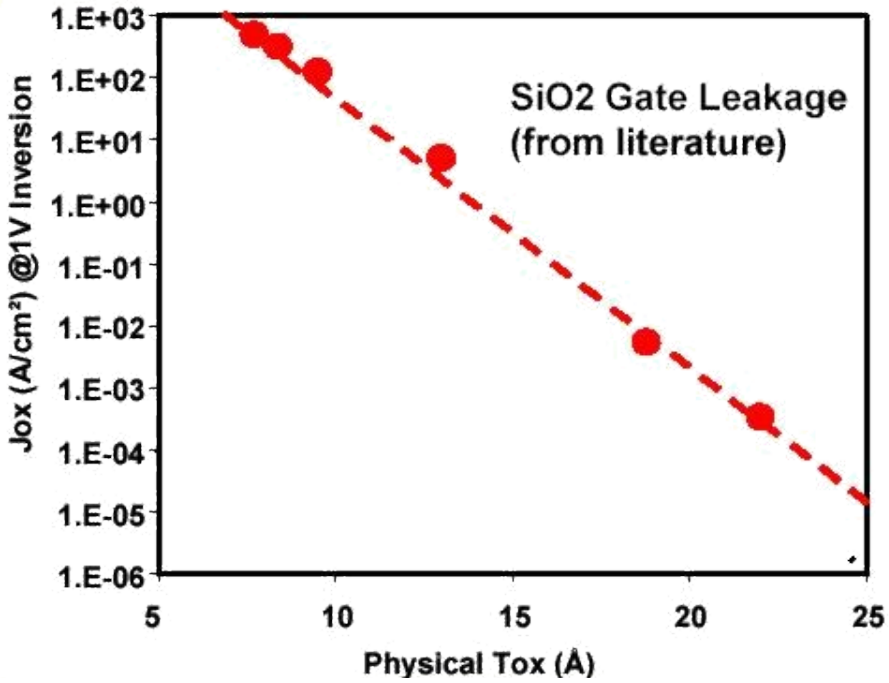
Limitations of Digital Technology

- Subthreshold Leakage Currents



Limitations of Digital Technology

- Gate Leakage
  - Thinner gates → faster transistors but more leakage



Homework I

- Do a literature research on logic families
  - Keywords (not limited to): ECL, CMOS, Domino, NORA, Zipper, Pass-transistor Logic

References

- http://download.intel.com/pressroom/kits/45nm/pin.jpg
- http://www.clipartheaven.com/show/clipart/tools_&_hardware/wheelbarrow-gif.html
- http://www.topnews.in/health/files/Aircraft-noise.jpg
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