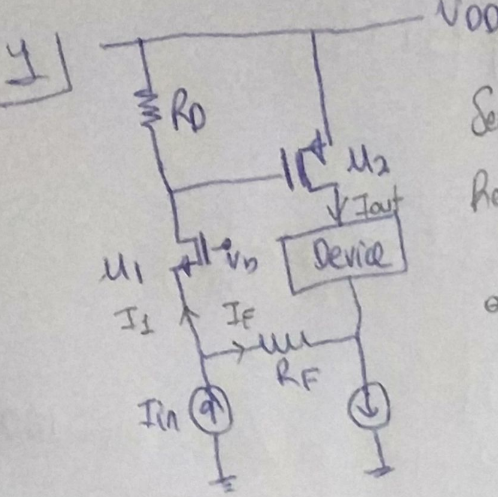
– EHB 335E – ANALOG ELECTRONICS – 11219 –

SERDEN SAIT ERANIL

040170025

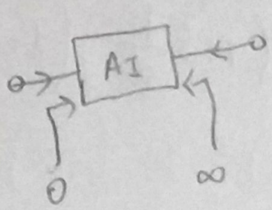
EHB 335E HW6

1)

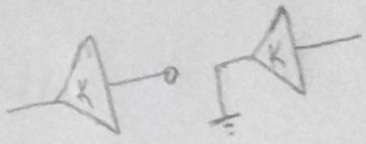


Sense : Current
Return : Current

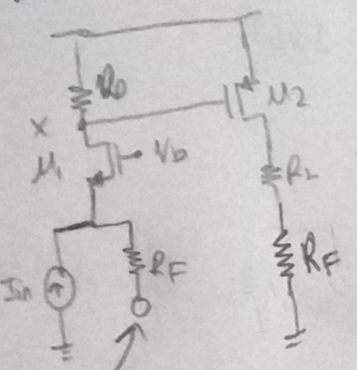
$\Rightarrow$ CL Amplifier $\Rightarrow$ Shunt-Series Amplifier



$\Rightarrow$



When we break the loop, the new circuit is

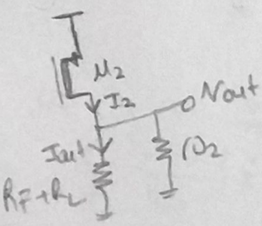


since $\lambda_1 = 0$, and DC current source is open in AC analysis

$v_x = I_{in} R_D$ (All current flows into the transistor)

However $\lambda_2 \neq 0$

$$V_{out} = -g_{m2}\left[(R_L+R_F) \parallel r_{O2}\right] v_x$$



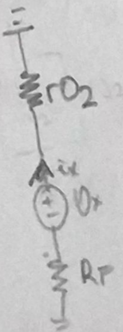
$$I_2 = \frac{V_{out}}{\left[(R_L+R_F) \parallel r_{O2}\right]} = -g_{m2} v_x$$

$$I_{out} = \frac{r_{O2}}{R_F+R_L+r_{O2}} I_2 = -\frac{g_{m2} r_{O2}}{R_F+R_L+r_{O2}} v_x$$

Simple Current Division

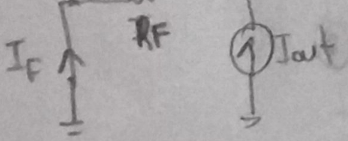
$$\Rightarrow A_I = \frac{I_{out}}{I_{in}} = -\frac{g_{m2} r_{O2} R_D}{R_F+R_L+r_{O2}}$$

$\Rightarrow R_{in} = \frac{1}{g_{m1}}$; $R_{out} =$



$\Rightarrow \frac{v_x}{i_x} = R_{out} = r_{O2} + R_F$

Let us determine K-factor



$\Rightarrow K = \frac{I_F}{I_{out}} = -1 \Rightarrow$

$$A_{I,CL} = \frac{A_I}{1+KA_I} = \frac{-\frac{g_{m2} r_{O2} R_D}{R_F+R_L+r_{O2}}}{1+(-1)\left(-\frac{g_{m2} r_{O2} R_D}{R_F+R_L+r_{O2}}\right)}$$

- $A_{I,CL} = -\frac{g_{m2} r_{O2} R_D}{R_F+R_L+r_{O2}+g_{m2} r_{O2} R_D}$

- $R_{in,CL} = \frac{R_{in}}{1+KA_I} = \frac{1/g_{m1}}{1+\frac{g_{m2} r_{O2} R_D}{R_F+R_L+r_{O2}}}$

- $R_{out,CL} = (1+KA_I) R_{out} = \left(1+\frac{g_{m2} r_{O2} R_D}{R_F+R_L+r_{O2}}\right)\left[r_{O2}+R_F\right]$

2) $A_0 = 10^4 \left(\frac{V}{V}\right)$

$f_1 = 10^5\ Hz$

$f_2 = 3.16 \times 10^5\ Hz$ $\Rightarrow A(s) = \dfrac{A_0}{\left(1+\frac{jf}{f_1}\right)\left(1+\frac{jf}{f_2}\right)\left(1+j\frac{f}{f_3}\right)}$

$f_3 = 10^6\ Hz$

$$A(s) = \frac{10^4}{\left(1+j\frac{f}{10^5}\right)\left(1+j\frac{f}{3.16\times10^5}\right)\left(1+j\frac{f}{10^6}\right)}$$

$$\angle A(s) = -\left[\tan^{-1}\left(\frac{f}{10^5}\right) + \tan^{-1}\left(\frac{f}{3.16\times10^5}\right) + \tan^{-1}\left(\frac{f}{10^6}\right)\right]$$

we want a phase margin of $45°$, $PM = \angle A(s) + 180° \Rightarrow \angle A(s) = PM - 180°$

$\Rightarrow \angle A(s) = 45° - 180° = -135°$

$$\Rightarrow \left[\tan^{-1}\left(\frac{f_1}{10^5}\right) + \tan^{-1}\left(\frac{f_1}{3.16\times10^5}\right) + \tan^{-1}\left(\frac{f_1}{10^6}\right)\right] = 135°$$

By using Wolfram Alpha we find $f_1 \approx 3.16 \times 10^5\ Hz$

$$A(jw_1) = \frac{10^4}{\left(1+j\frac{3.16\times10^5}{10^5}\right)\left(1+j\frac{3.16\times10^5}{3.16\times10^5}\right)\left(1+j\frac{3.16\times10^5}{10^6}\right)} \Rightarrow |A(jw_1)| = 2034.25 \left(\frac{V}{V}\right)$$

$|A(jw_1)|\ (dB) = 20\log_{10}(2034.25) \approx 66.17\ dB$ (open-loop gain)

Since at gain-crosover frequency loop gain is 0 dB. We can calculate β -

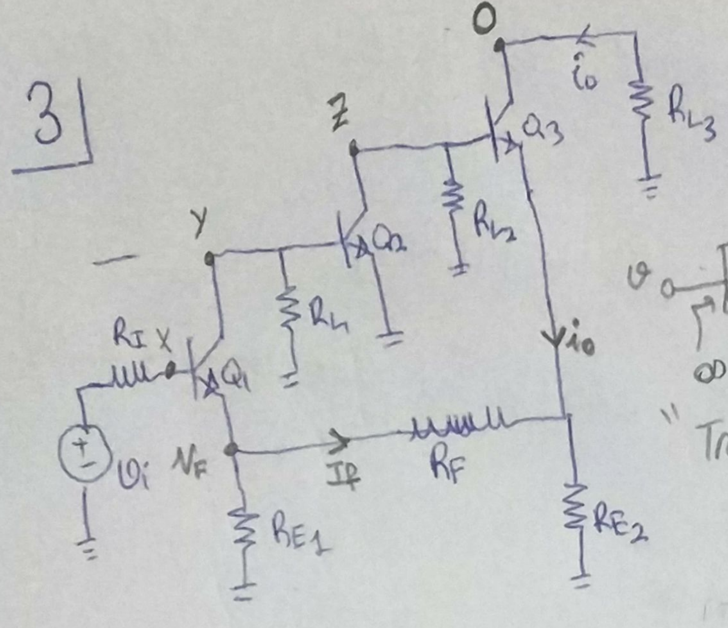
$\beta_{(dB)} \cong -66.17\ dB \Rightarrow 20\log_{10}\beta = -66.17 \Rightarrow \beta = 10^{-\frac{66.17}{20}} \approx 4.91\times10^{-4}$

Then, we can calculate the closed-loop gain by the formula $A_f = \dfrac{A_0}{1+KA_0}$

$$\Rightarrow A_{fo} = \frac{10^4}{1+(4.91\times10^{-4})(10^4)} = \frac{10^4}{5.91} = 1.69\times10^3 \left(\frac{V}{V}\right)$$

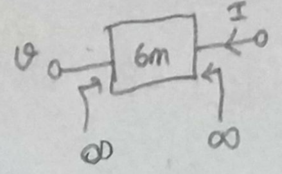
$$\Rightarrow A_{fo\,(dB)} = 20\log(1.69\times10^3) = 64.56\ dB$$

3]

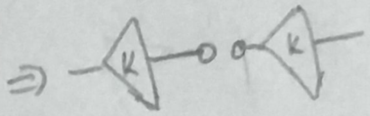


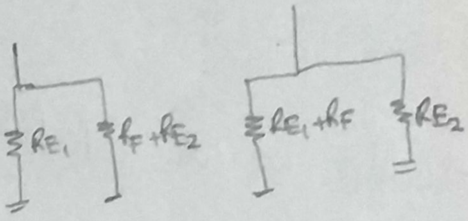
→ we are sensing current

→ and returning voltage (υ_{be} subtractor)



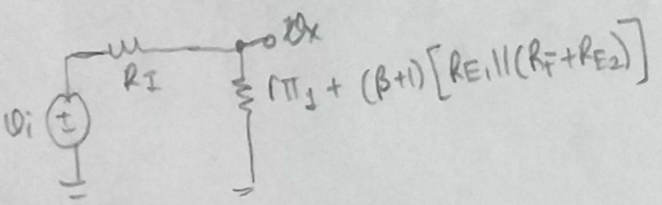
"Transconductance Amplifier"





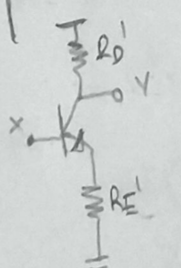
$$\frac{i_o}{\upsilon_i}=\frac{\upsilon_x}{\upsilon_i}\cdot\frac{\upsilon_y}{\upsilon_x}\cdot\frac{\upsilon_z}{\upsilon_y}\cdot\frac{i_o}{\upsilon_z}$$ ⇒ Let's calculate these gains seperately

$$\frac{\upsilon_x}{\upsilon_i}=\frac{(\beta+1)\left[R_{E1}\,||\,(R_F+R_{E2})\right]+r_{\pi_1}}{(\beta+1)\left[R_{E1}\,||\,(R_F+R_{E2})\right]+r_{\pi_1}+R_I}$$



" Voltage Divider"

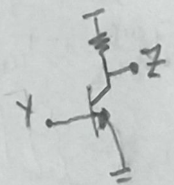
$$\frac{\upsilon_y}{\upsilon_x}=-\frac{g_{m_1}\left[R_{L1}\,||\,r_{\pi_2}\right]}{1+g_{m_1}\left[R_{E1}\,||\,(R_F+R_{E2})\right]}$$



$R_E' = R_{E1}\,||\,(R_F+R_{E2})$

$R_D' = R_{L1}\,||\,r_{\pi_2}$

"Emitter Degenerated CE stage with $g_m' = \dfrac{g_m}{1+g_mR_E'}$"



"Simple CE stage"

$$\frac{\upsilon_z}{\upsilon_y}=-g_{m_2}\left\{R_{L2}\,||\left[r_{\pi_3}+(\beta+1)\left[(R_{E1}+R_F)\,||\,R_{E2}\right]\right]\right\}$$

"emitter degenerated CE stage"

$$\frac{i_o}{\upsilon_z}=\frac{g_{m_3}}{1+g_{m_3}\left[(R_{E1}+R_F)\,||\,R_{E2}\right]}$$

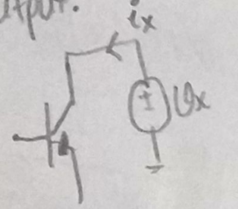
Then, the open loop gain $G_{m,OL}$ (We have assumed that collector and emitter currents are the same for Q_3)

$$G_{m,OL}=\underbrace{\frac{(\beta+1)\left[R_{E1}||(R_F+R_{E2})\right]+r_{\pi_1}}{(\beta+1)\left[R_{E1}||(R_F+R_{E2})\right]+r_{\pi_1}+R_I}}_{\frac{\upsilon_x}{\upsilon_i}}\cdot\underbrace{\frac{g_{m_1}\left[R_{L1}||r_{\pi_2}\right]}{1+g_{m_1}\left[R_{E1}||(R_F+R_{E2})\right]}}_{\frac{\upsilon_y}{\upsilon_x}}\cdot\underbrace{g_{m_2}\left\{R_{L2}||\left[r_{\pi_3}+(\beta+1)\left[(R_{E1}+R_F)||R_{E2}\right]\right]\right\}}_{\frac{\upsilon_z}{\upsilon_y}}\cdot\underbrace{\frac{g_{m_3}}{1+g_{m_3}\left[(R_{E1}+R_F)||R_{E2}\right]}}_{\frac{i_o}{\upsilon_z}}$$

→ We can calculate open-loop input resistance simply by looking into the base of the Q1. That is,

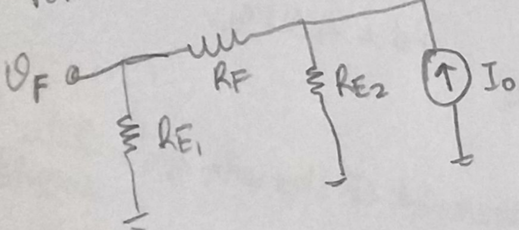
$$R_{in,OL} = r_{\pi_1} + (\beta+1)\left[(R_F+R_{E_2}) \parallel R_{E_1}\right]$$

→ Also, we can calculate the Rout by adding a test source in series to the output.



$$\Rightarrow R_{out,OL} = \frac{v_x}{i_x} = \infty$$

→ Now, we can calculate, the feedback factor **K** in order to find closed-loop parameters



$$\Rightarrow K = \frac{v_f}{I_o} = \frac{R_{E2}}{R_{E_1}+R_{E2}+R_F} \cdot R_{E1}$$

→ CLOSED-LOOP PARAMETERS

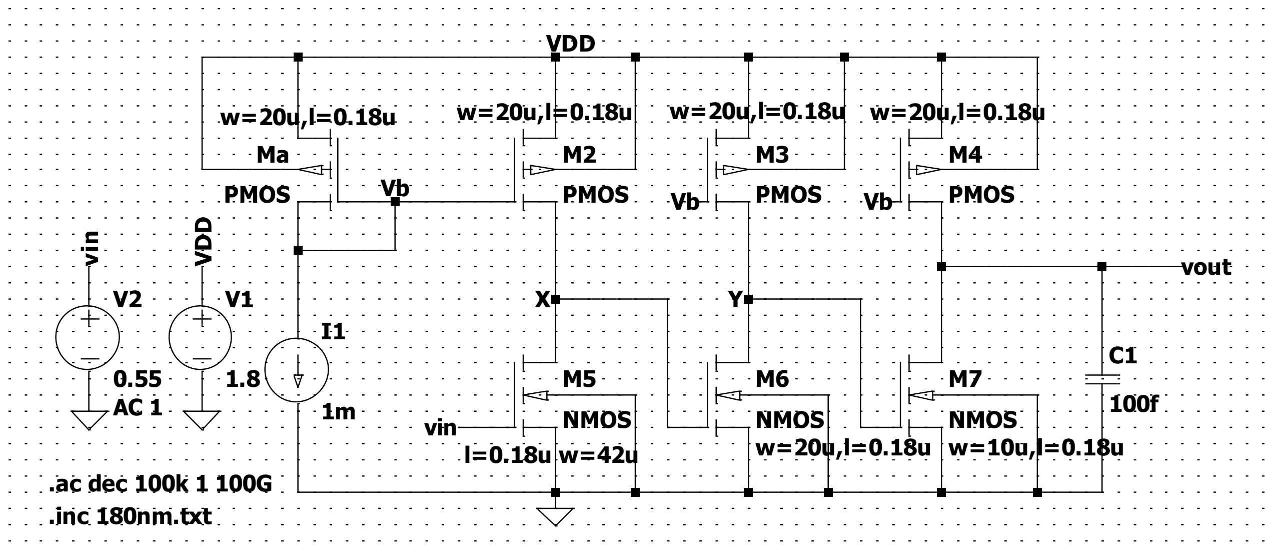
- $$G_{m,CL} = \frac{G_{m,OL}}{1+K\,G_{m,OL}}$$

- $$R_{in,CL} = R_{in,OL}\left(1+K.G_{m,OL}\right)$$

- $$R_{out,CL} = R_{out,CL}\left(1+K.G_{m,OL}\right)$$

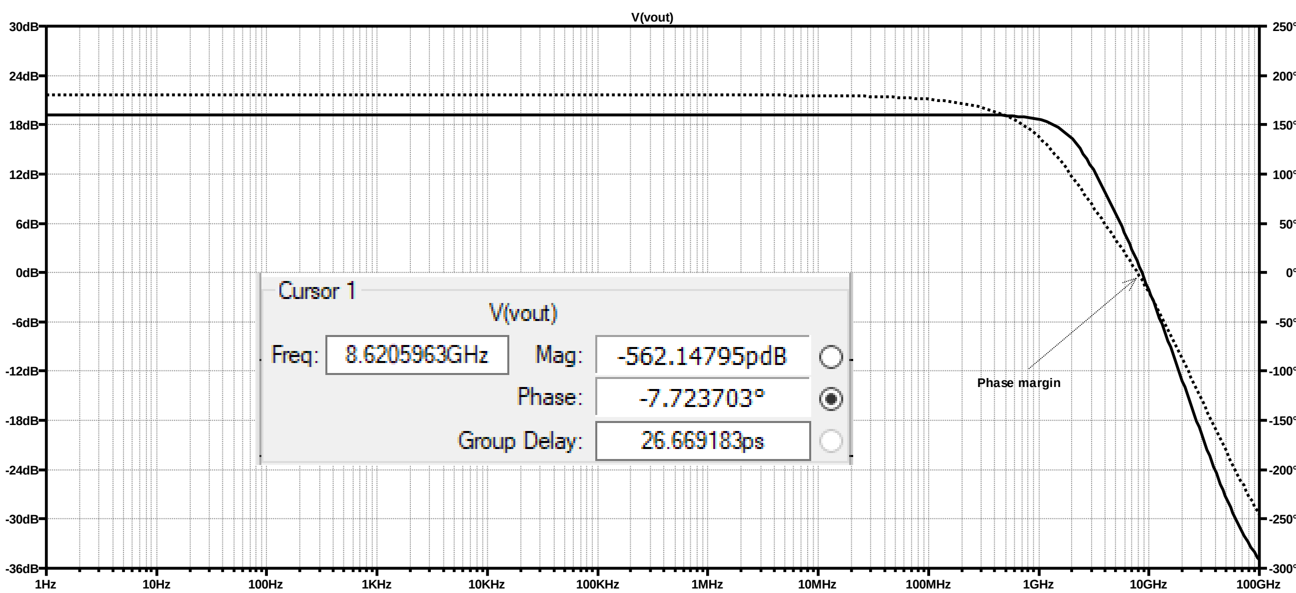
4TH QUESTION IS REALIZED USING THE LTSPICE SIMULATION PROGRAM

First of all, let us draw the circuit in the ltspice given in the question.



Then, include the models by creating a 180nm.txt file in the same directory with the circuit.asc file. Copy the given model codes into this txt file and include these models by using the .inc 180nm.txt spice directive.

a-) we are asked to find the phase margin. In order to find phase margin, let us do ac analysis.

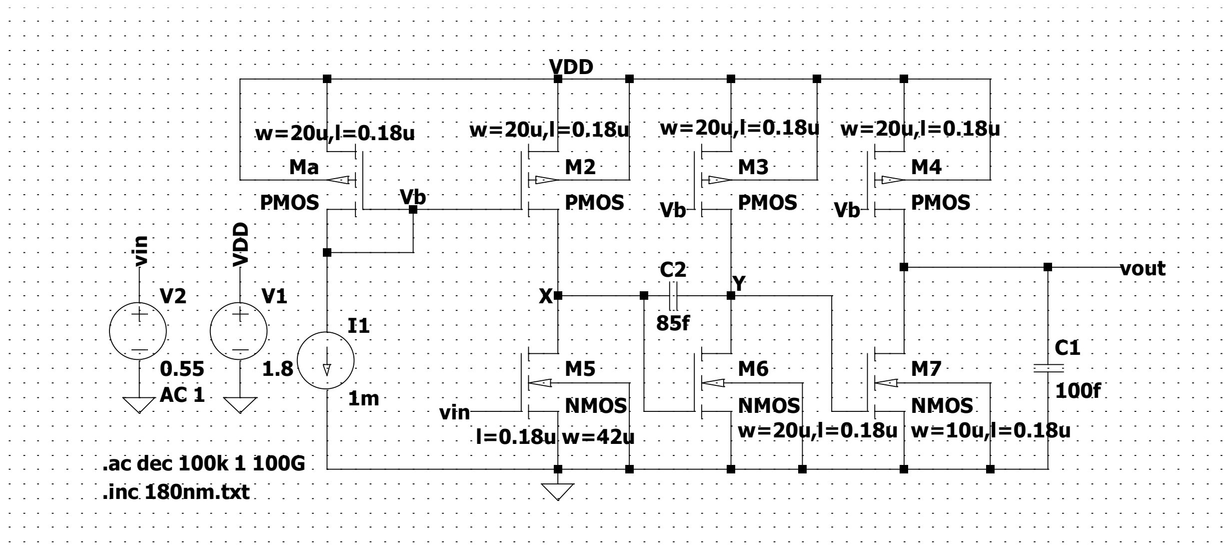


As it can be seen from the simulation results, phase margin which makes the gain 0 dB is approximately -7.72 °

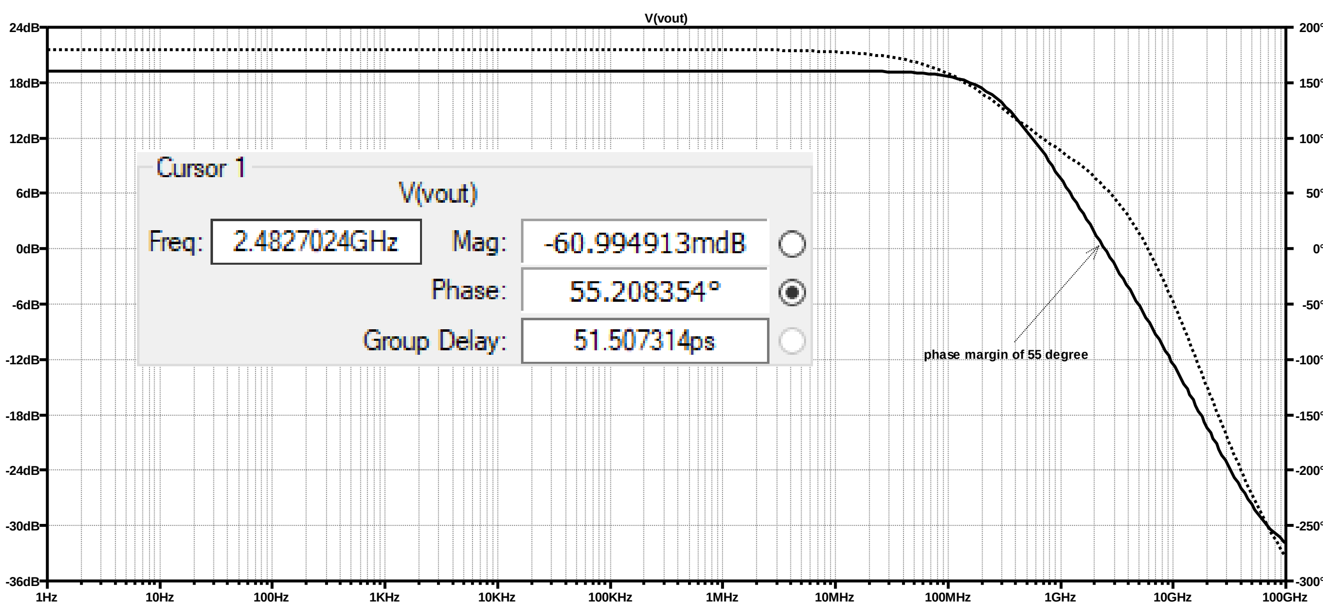
PHASE MARGIN = -7.72 °

b-) Now we apply the same procedure after we place a capacitor between node X and node Y. We select a capacitor value such that our phase margin becomes 55°.

First, let us draw the new circuit



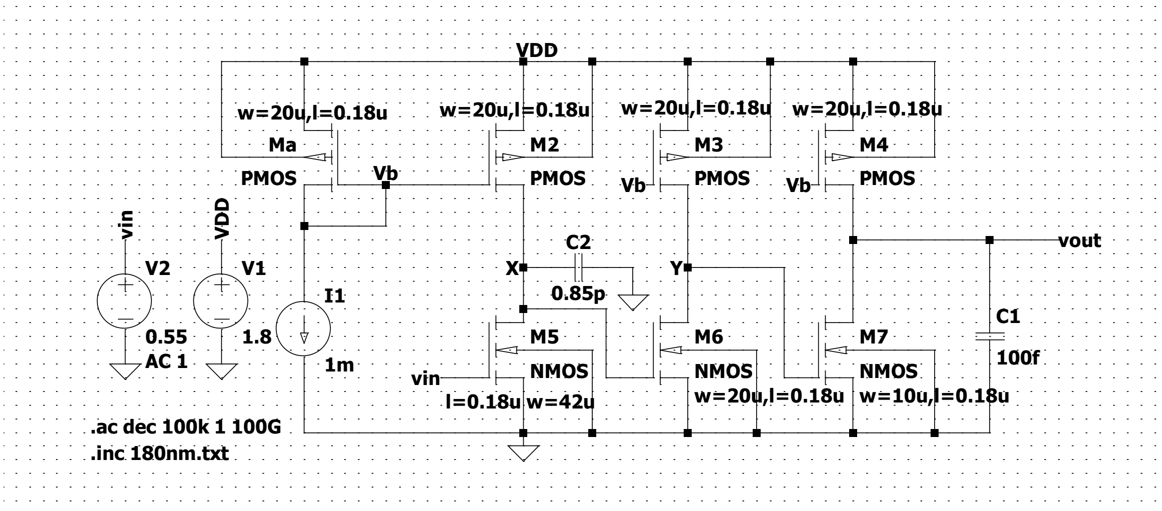
By trying some values for the capacitor value, we find that for C2 = 85 fF, a phase margin of 55° is obtained. It can be seen from the simulation results



FOR C2 = 85 fF

PHASE MARGIN = 55 ° ; UNITY GAIN BANDWIDTH = 2.48 GHz c-) Now we remove the capacitor between the nodes X and Y and place another capacitor between node X and ground. Now are in the search of a capacitor value that creates 55° of phase margin.

In order to determine capacitor value again let us draw the circuit diagram.



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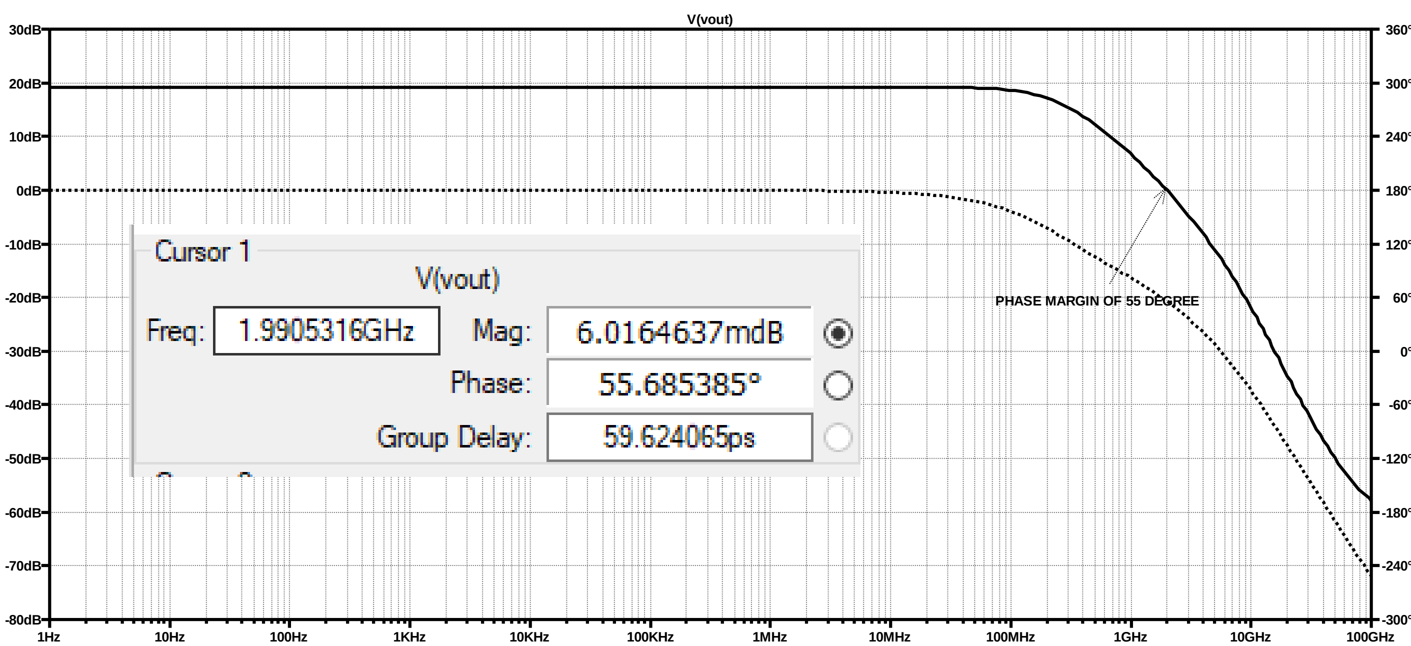

FOR C2 = 0.85 pF

PHASE MARGIN = 55 °

UNITY GAIN BANDWIDTH = 2 GHz