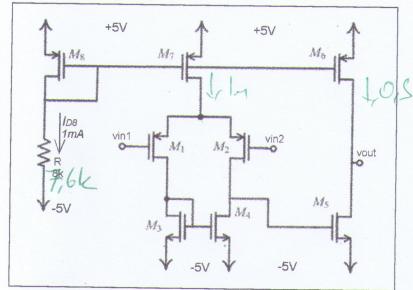
ELECTRONICS II NAME: SUMMER-2019 Final 03.08.2019 Number:

**P1** For the transistors in the figure,  $k_p$ '= $\mu_p c_{ox}$ = $40\mu A/V^2$ ,  $k_n$ '= $\mu_n c_{ox}$ = $100\mu A/V^2$ ,  $V_{An}$ =60V,  $V_{Ap}$ =40V,  $V_{Th,p}$ =-0.8V,  $V_{Th,n}$ =0.6V are given. Vin1=Vin2=0 for DC case

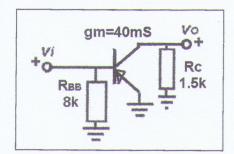
|    | L(um) | W(um) |
|----|-------|-------|
| M1 | 0.7   | 17:5  |
| M2 | 0.7   | 17.5  |
| МЗ | 0.7   | 7     |
| M4 | 0.7   | 7     |
| M5 | 0.7   | 7     |
| M6 | 0.7   | 8.75  |
| M7 | 0.7   | 17.5  |
| M8 | 0.7   | 17.5  |
|    |       |       |

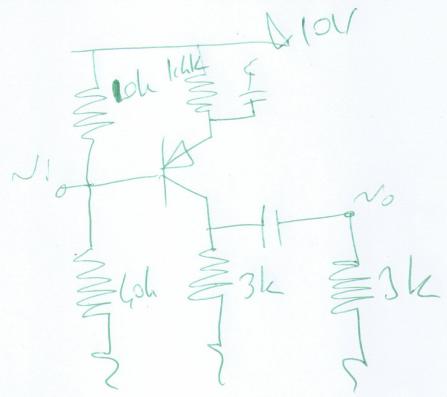
a) Find the differential gain of the circuit (vout/(vin1-vin2)).



b) Find the CMMR value.

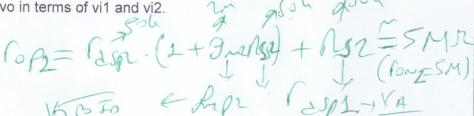
P2 The circuit, ac case of which is given in the figure has a DC source of 10V.  $\beta_F$ =100,  $N_{BB}$ =0.6V and  $N_A$ = $\infty$  are given for the PNP transistor. In DC case  $V_{BQ}$   $\approx$  8V and  $V_{CQ}$   $\approx$  3V. In ac case,  $R_{BB}$  = 8k,  $R_c$  = 1.5kand  $g_m$  = 40mS (V<sub>T</sub>=25mV). The circuit has one PNP transistor, four bias-resistors, two capacitors and one load-resistor. Design and sketch the circuit.

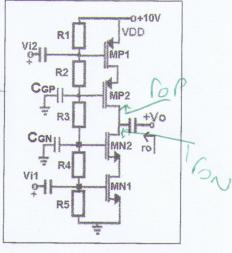




**P3** β=2mA/V<sup>2</sup>,  $|V_{TH}|$ =1V and  $V_A$ =50V are given for the all transistors in the Figure. R1=R5=200k, R2=R4=250k, R3=100k.

Find vo in terms of vi1 and vi2.





JOME = FON = FON = FON = FON = 2m (2-1) = /mA NAPI - NAPI = -9mps. /Ampr. 9mps (Cop/16. NO = NANI VENZ = - LINI - FINI PUNI ( POP/MON)

No = - 5 K(NIL+Nh)