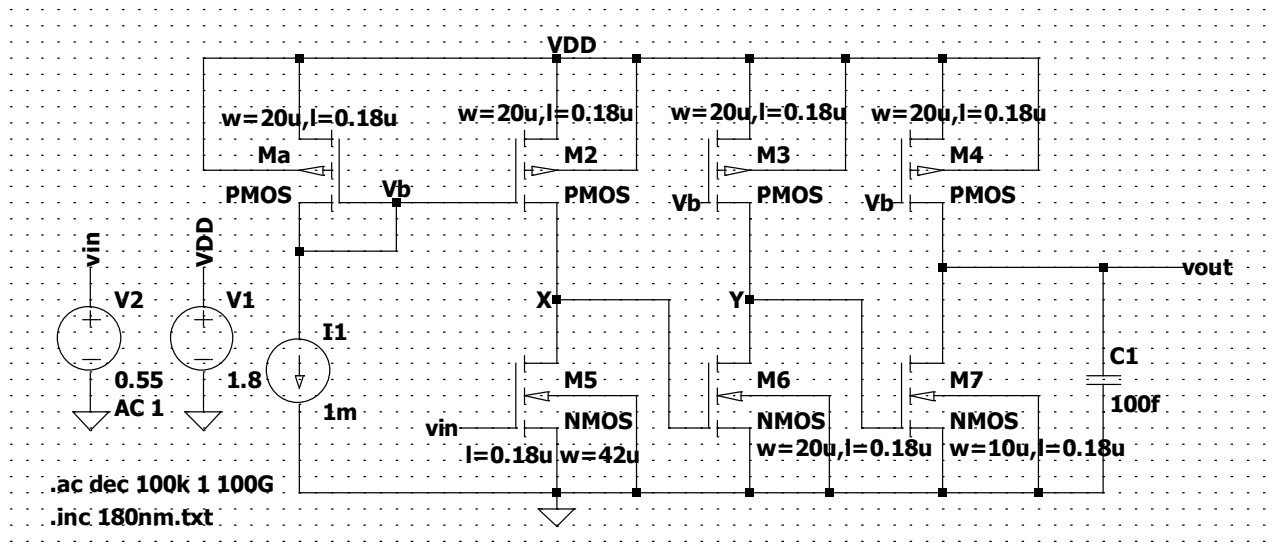# 4$^{TH}$ QUESTION IS REALIZED USING THE LTSPICE SIMULATION PROGRAM

First of all, let us draw the circuit in the ltspice given in the question.



Then, include the models by creating a 180nm.txt file in the same directory with the circuit.asc file. Copy the given model codes into this txt file and include these models by using the .inc 180nm.txt spice directive.

a-) we are asked to find the phase margin. In order to find phase margin, let us do ac analysis.
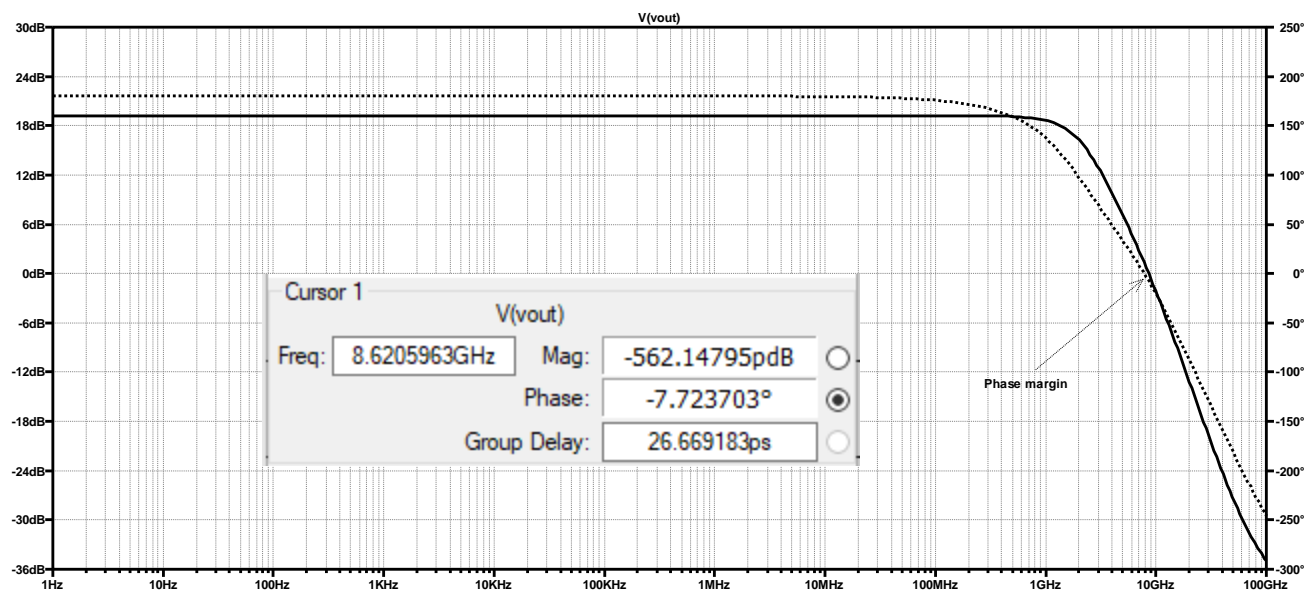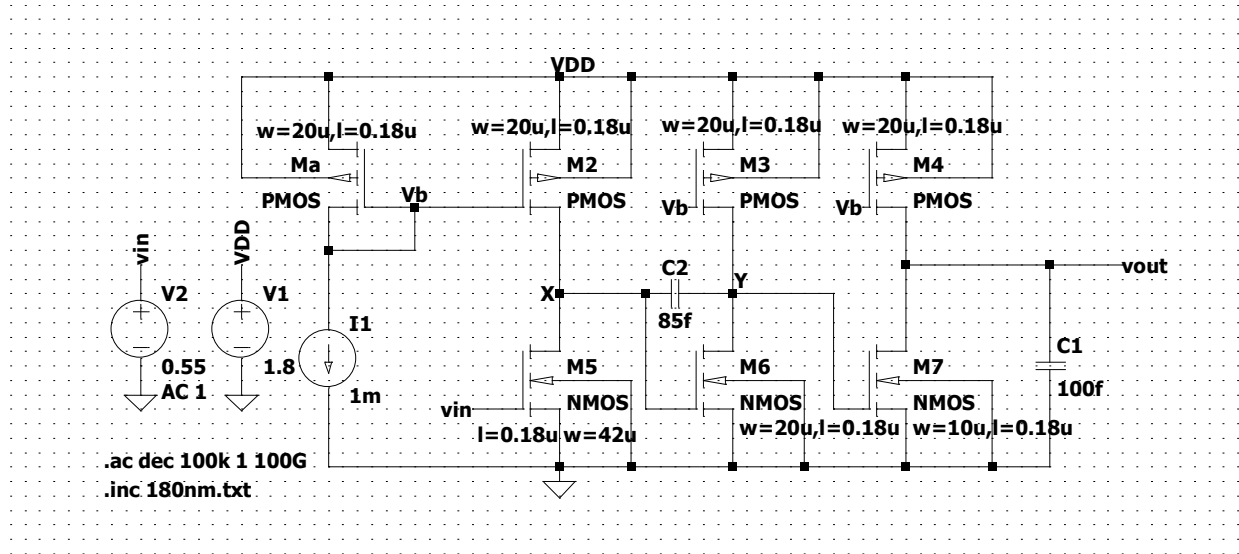


As it can be seen from the simulation results, phase margin which makes the gain 0 dB is approximately -7.72 °
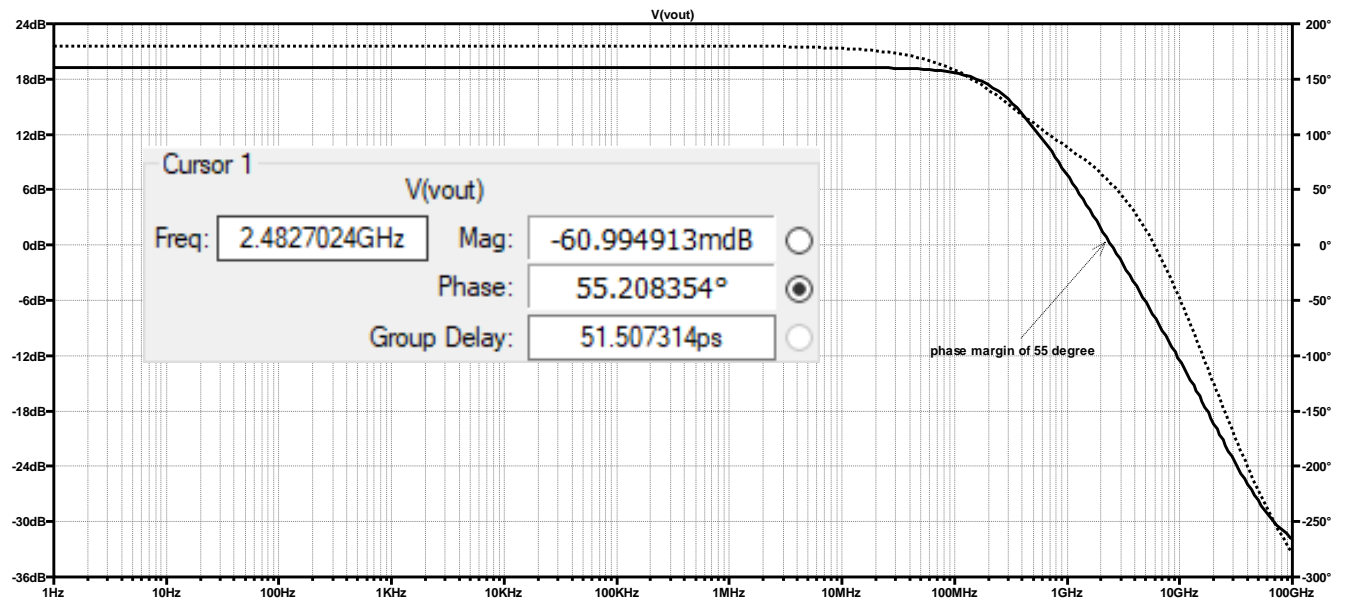
PHASE MARGIN = -7.72 °

b-) Now we apply the same procedure after we place a capacitor between node X and node Y.  We select a capacitor value such that our phase margin becomes 55°.

First, let us draw the new circuit



By trying some values for the capacitor value, we find that for C2 = 85 fF, a phase margin of 55° is obtained. It can be seen from the simulation results
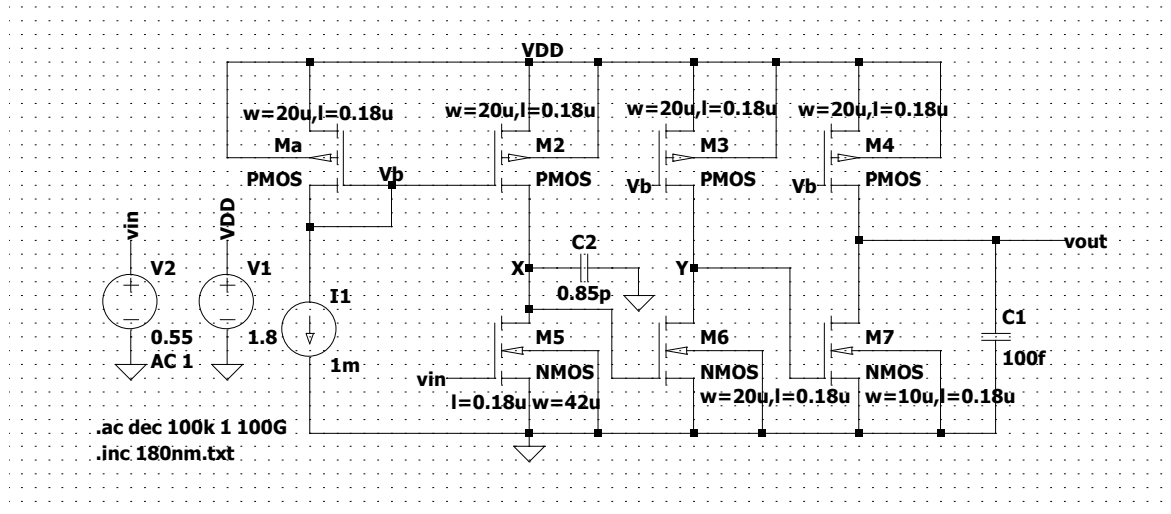


FOR C2 = 85 fF

PHASE MARGIN = 55 ° ; UNITY GAIN BANDWIDTH = 2.48 GHz

c-) Now we remove the capacitor between the nodes X and Y and place another capacitor between node X and ground. Now are in the search of a capacitor value that creates 55° of phase margin.

In order to determine capacitor value again let us draw the circuit diagram.



By trying some values for the capacitor value, we find that for C2 = 85 fF, a phase margin of 55° is obtained. It can be seen from the simulation results
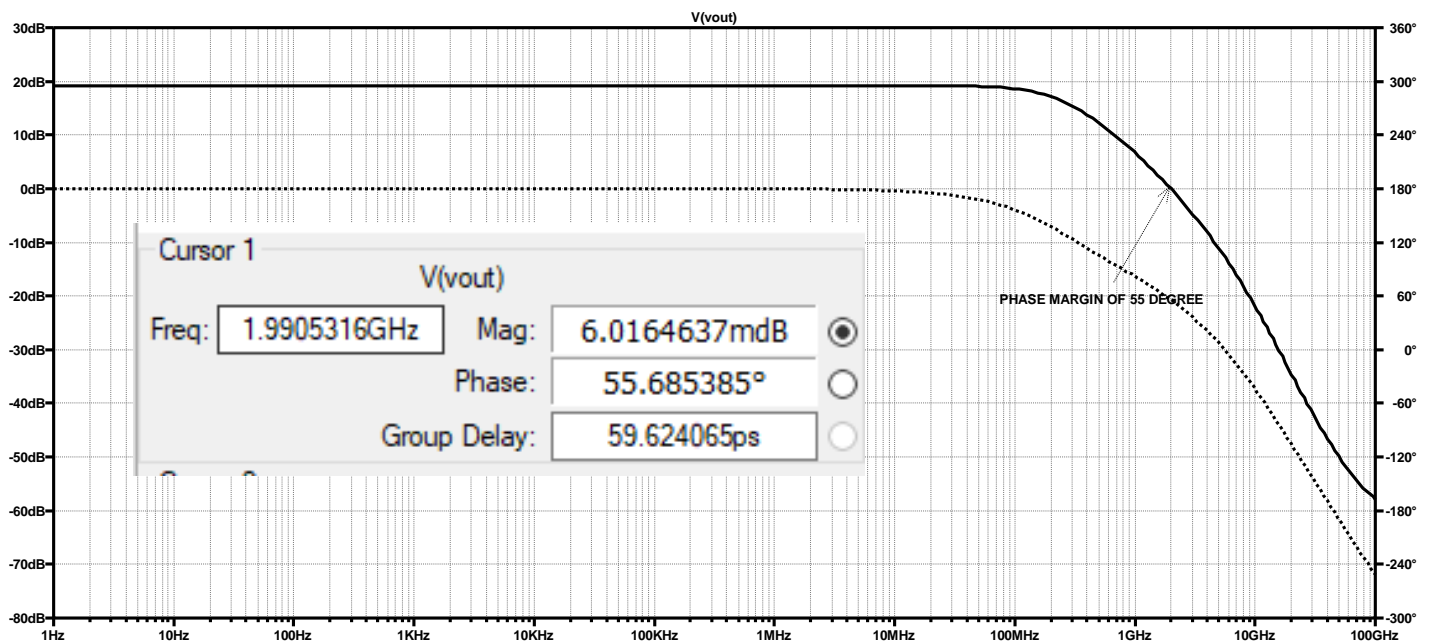


FOR C2 = 0.85 pF

PHASE MARGIN = 55 °

UNITY GAIN BANDWIDTH = 2 GHz