VLSI Circuit Design II– EHB 425E

HOMEWORK II

Yiğit Bektaş GÜRSOY

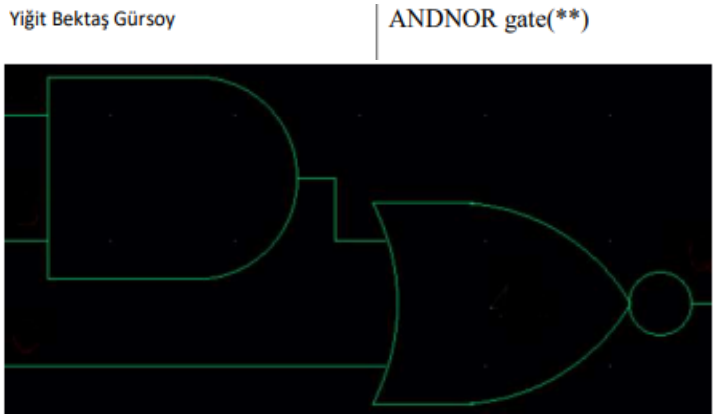
040180063

Class Lecturer: Sıddıka Berna Örs Yalçın

Class Assistant:
Yasin Fırat Kula

1- Circuit in Homework

As stated in the assignment 2 file, my circuit consists of 1 AND and 1 NOR gate.



The individual truth tables for these gates are shown below.

AND

INPUT		OUTPUT
A	B	
0	0	0
1	0	0
0	1	0
1	1	1

NOR

INPUT		OUTPUT
A	B	
0	0	1
1	0	0
0	1	0
1	1	0

In order to create a truth table of the circuit shown, x, y and z inputs are given respectively as a representation. The value coming out of the AND gate is "xy" and the inputs entering the NOR gate are xy and z. The value to be output at the NOR gate is (x'+y')z'=x' + y'z'. The truth table resulting from this boolean equation is also given below.

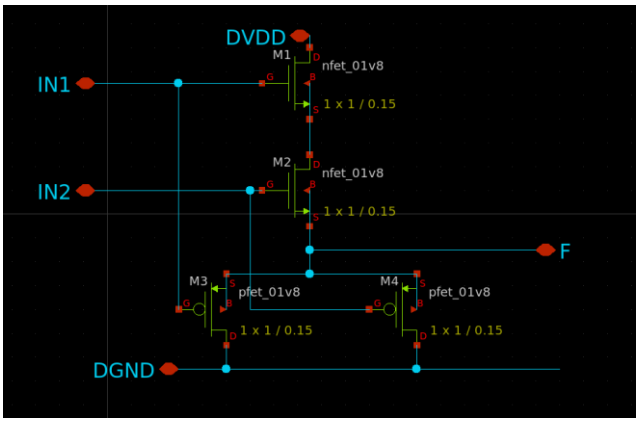
X,Y **(AND)** XY
XY,Z **(NOR)** (XY+Z)'=(X'+Y')Z'= X'Z'+Y'Z'

Truth Table

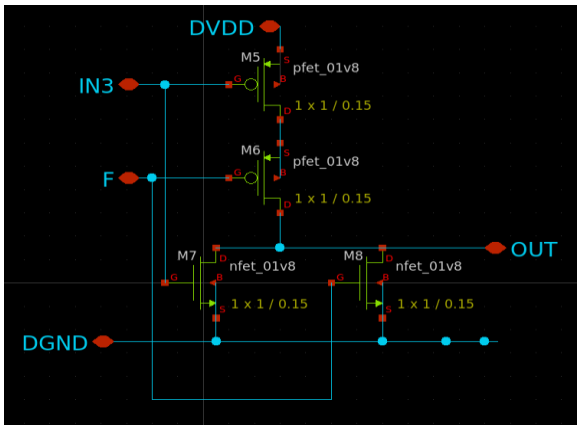
	A	B	C	Y
0	0	0	0	1
1	0	0	1	0
2	0	1	0	1
3	0	1	1	0
4	1	0	0	1
5	1	0	1	0
6	1	1	0	0
7	1	1	1	0

2- Designing Process

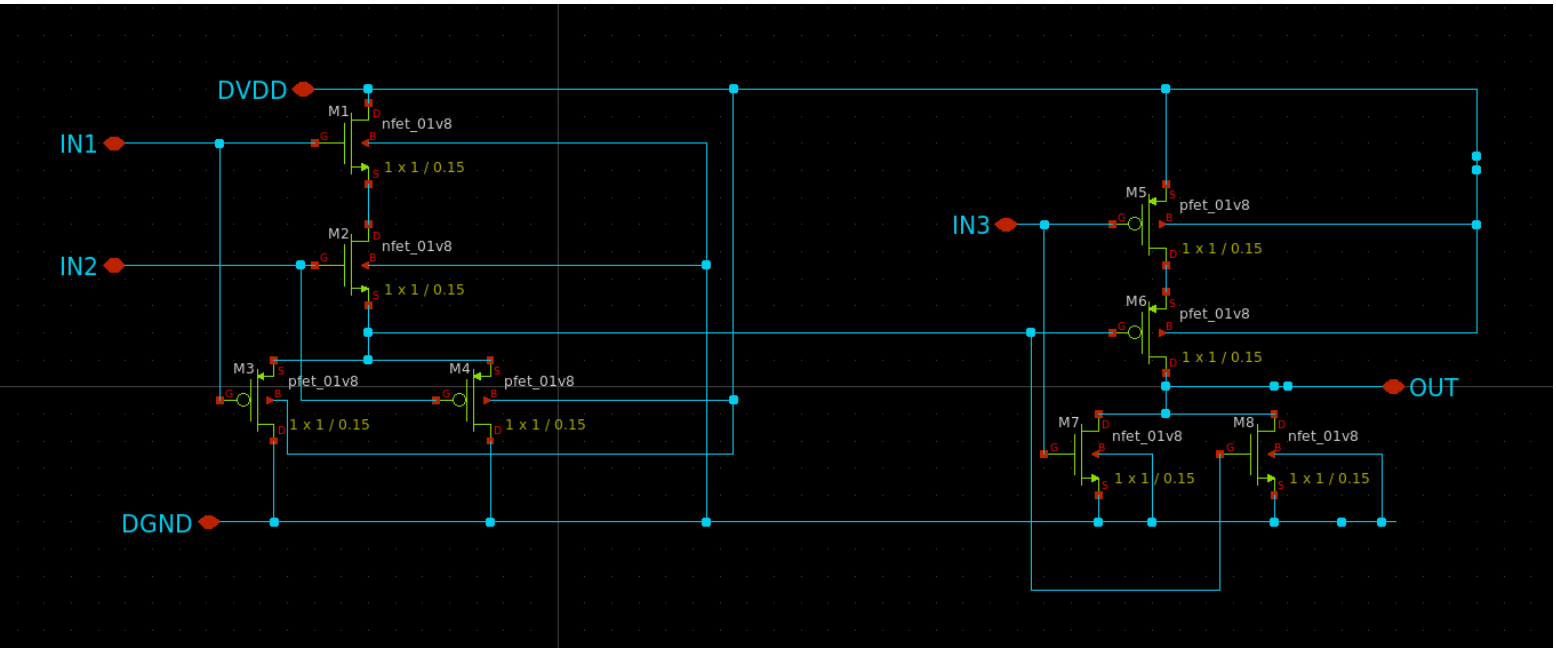
Using pmos and nmos symbols in xschem program, AND and NOR gates were implemented as follows. The inputs are listed as IN1, IN2 and IN3. DVDD is specified as the power source and DGND is specified as the ground. "F", which is the output from the AND gate, is determined as an input of the other gate.



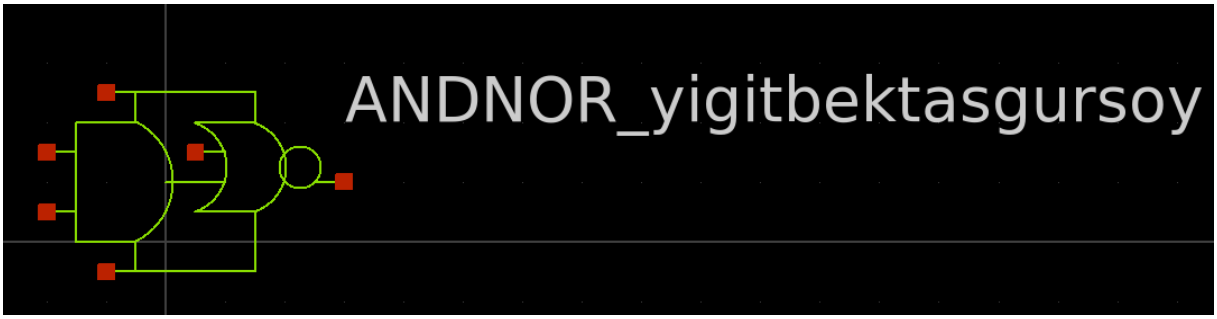
AND GATE



NOR GATE

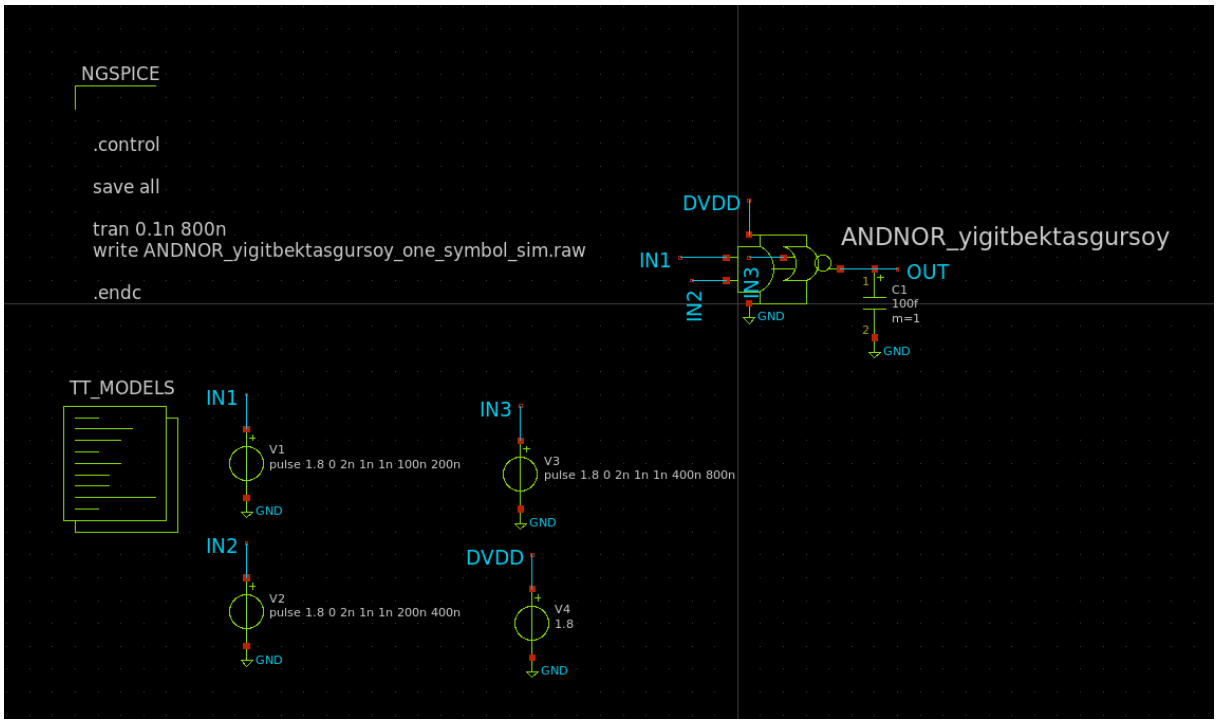


ANDNOR GATE



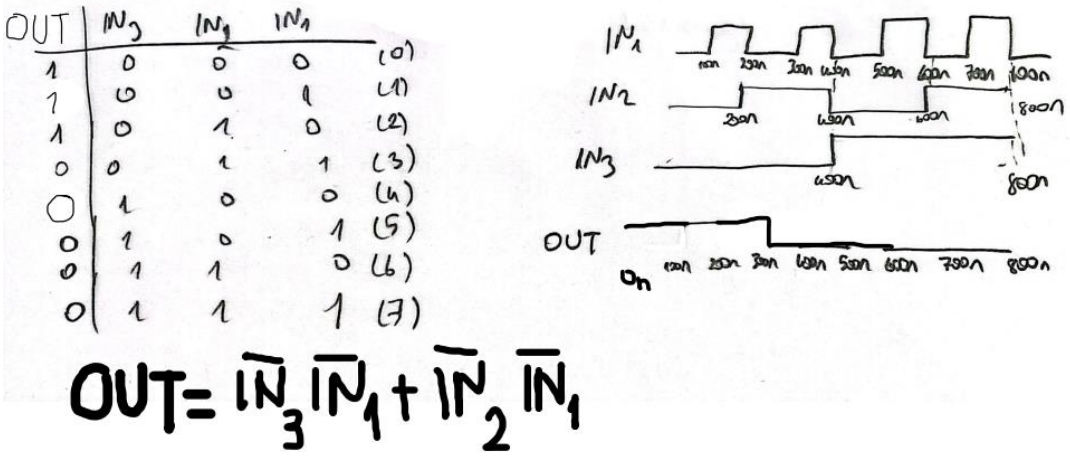
ANDNOR GATE SYMBOL

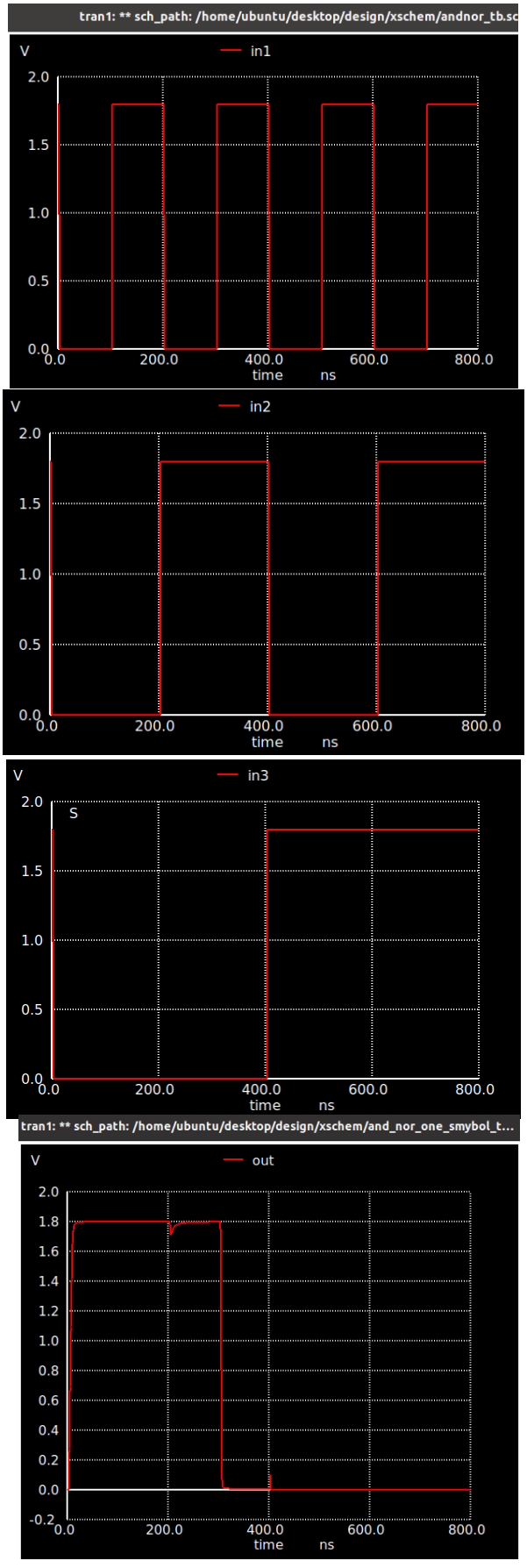
Above, representative symbols for properly connecting the gates to each other have been drawn and put into a single schematic. Then, source and ground are connected to the relevant places to simulate the circuit. After entering the appropriate values for ngspice, the simulation was performed by clicking the "**Netlist**" button and then the "**Simulation**" button. The relevant schematic and related results are given below.

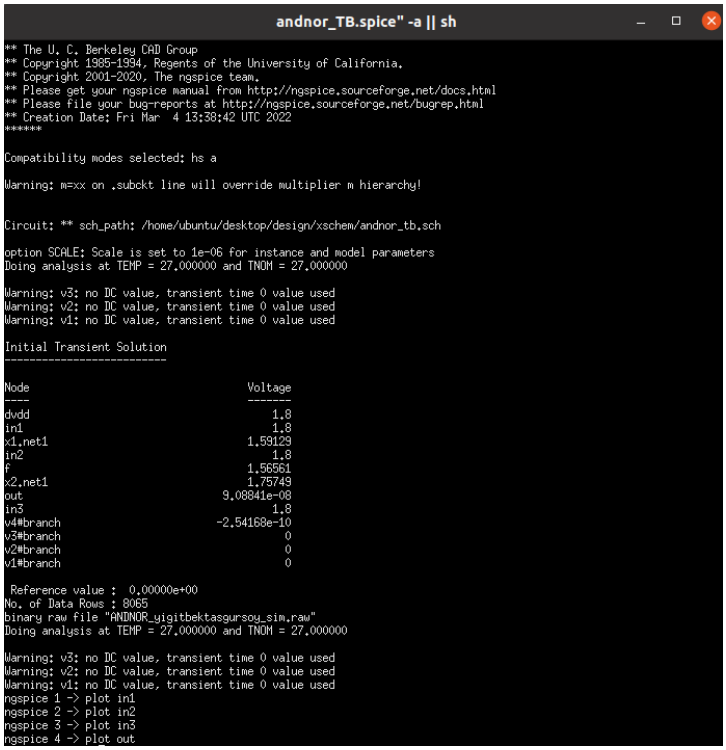


3- Simulation Process

In order to match the hand results with the simulation results, the boolean function of the circuit was extracted and the logic signals were drawn. The simulation results then need to be compared with ngspice simulations to validate.

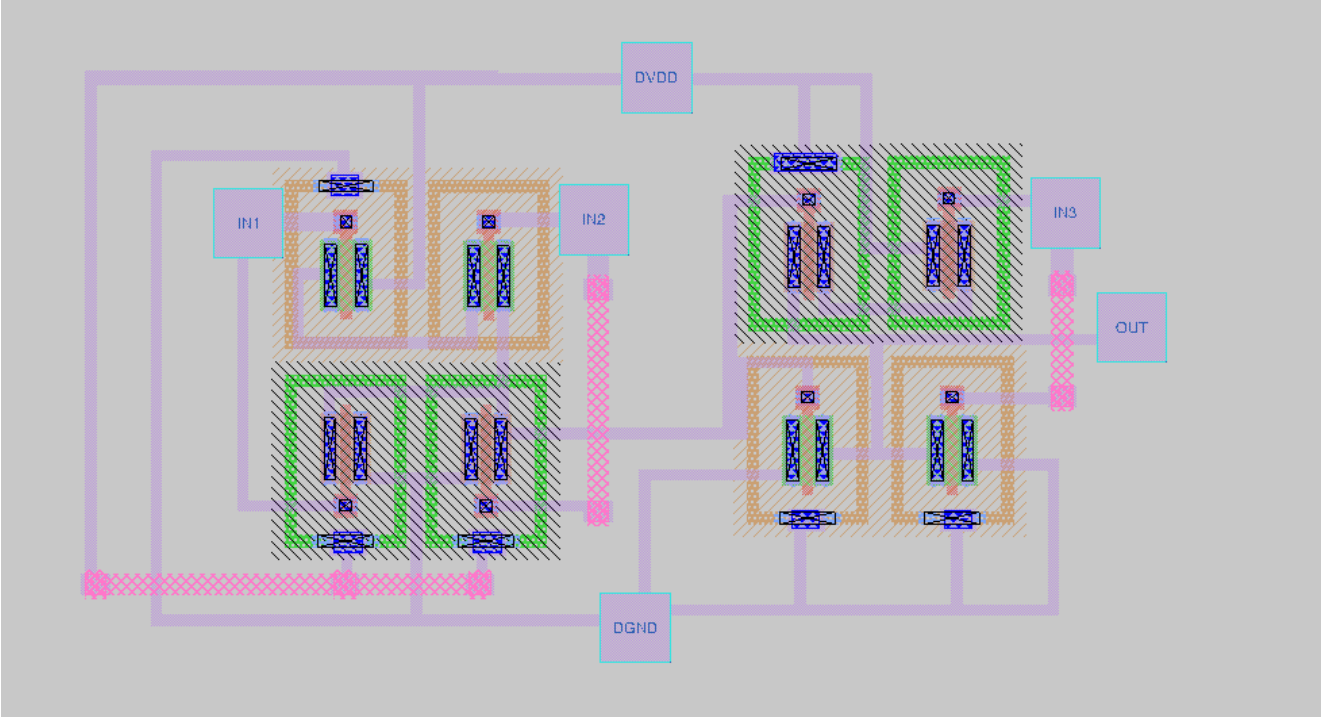




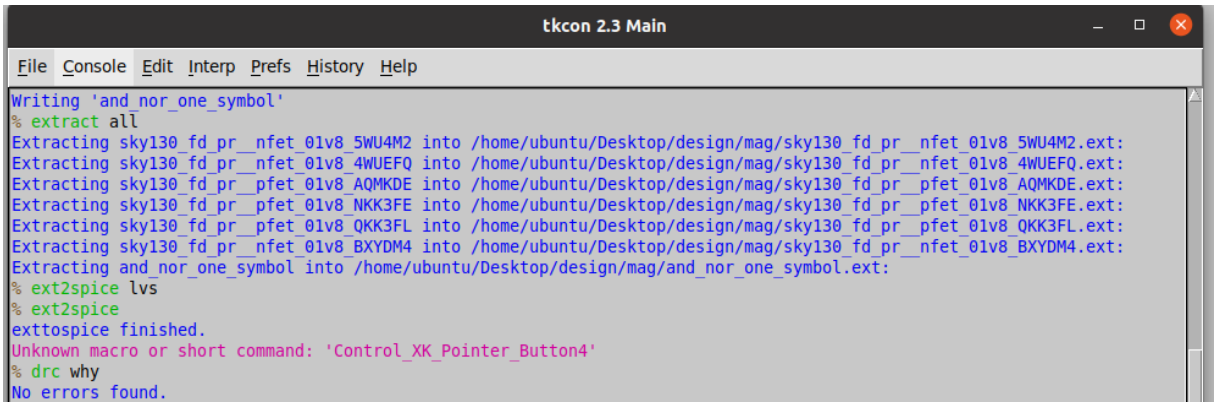


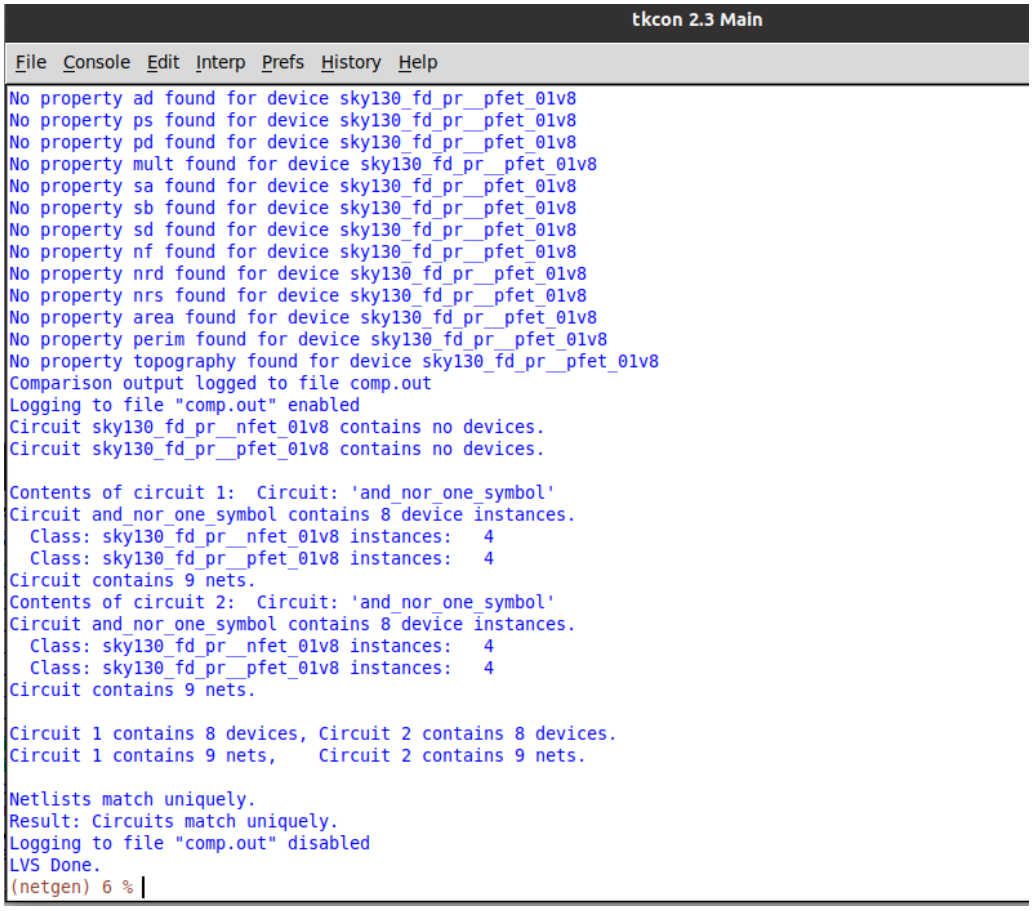
First, as shown in the image above, IN1, IN2, IN3 and OUT signals were plotted, respectively. All possible situations are given at 100ns intervals and 100fF capacite load is added to the circuit. Then it was put on the same scale and compared with the previously found results. The simulation results were matched with the above mentioned truth table and the drawn waveform. The circuit is working correctly.

The layout of the given circuit was created by taking help from the TUTEL pdf files in the class files in Ninova and using the magic program. The layout is as follows.

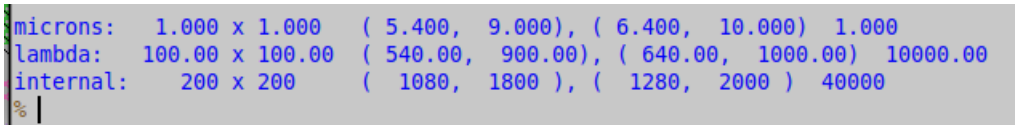


The necessary commands were written to confirm the correctness of the extracted layout, and a file was created for testing on netgen. Then it was tested. No errors were found in the tests, the layout and the circuit match each other exactly. The relevant results are given below. (DRC and LVS are clean)

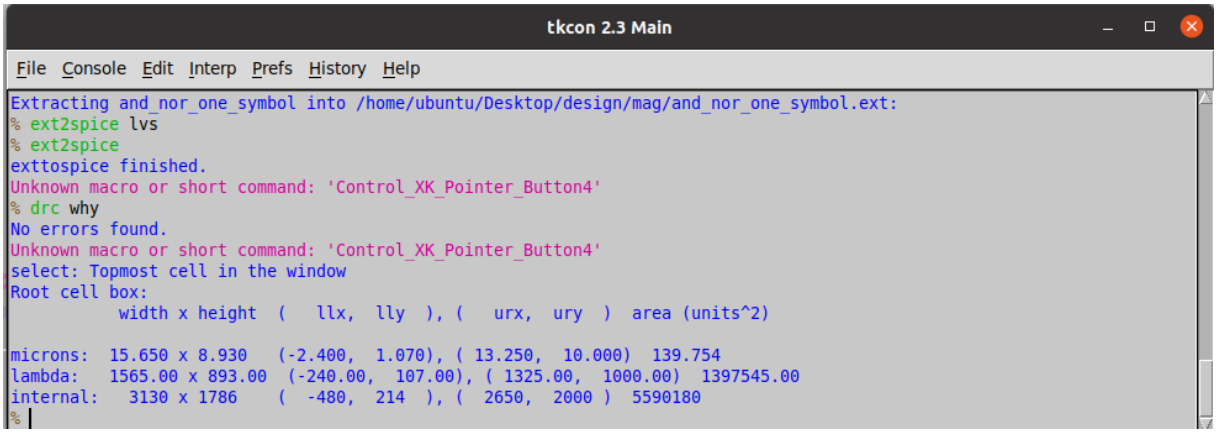




DVDD/DGND values are as shown below. It came out as given in the assignment.



The area occupied by the designed layout is as follows.



4- Parasitic Extraction

After the layout operations, the steps in the TUTEL 5.pdf file placed in the class files were followed. The results (out) and the circuit are as follows. The results gave the same results as in the first simulation. The working logic of the circuit is still the same.