

of inputs = $2^3 = 8$

of outputs = 3

CPU
22665

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Fig 1

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x_7	x_6	x_5	x_4	x_3	x_2	x_1	x_0	y_2	y_1	y_0
1	0	0	0	0	0	0	0	1	1	1
0	1	0	0	0	0	0	0	1	1	0
0	0	1	0	0	0	0	0	1	0	1
0	0	0	1	0	0	0	0	1	0	0
0	0	0	0	1	0	0	0	0	1	1
0	0	0	0	0	1	0	0	0	1	0
0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	0	0	1	0	0	0

$$y_2 = \sum m(128, 64, 32, 16, 64, 128)$$

$$y_1 = \sum m(128, 64, 8, 4)$$

$$y_0 = \sum m(128, 32, 8, 2)$$

$$y_2 = x_7 \bar{x}_6 \bar{x}_5 \bar{x}_4 \bar{x}_3 \bar{x}_2 \bar{x}_1 \bar{x}_0 + \bar{x}_7 x_6 \bar{x}_5 \bar{x}_4 \bar{x}_3 \bar{x}_2 \bar{x}_1 \bar{x}_0$$

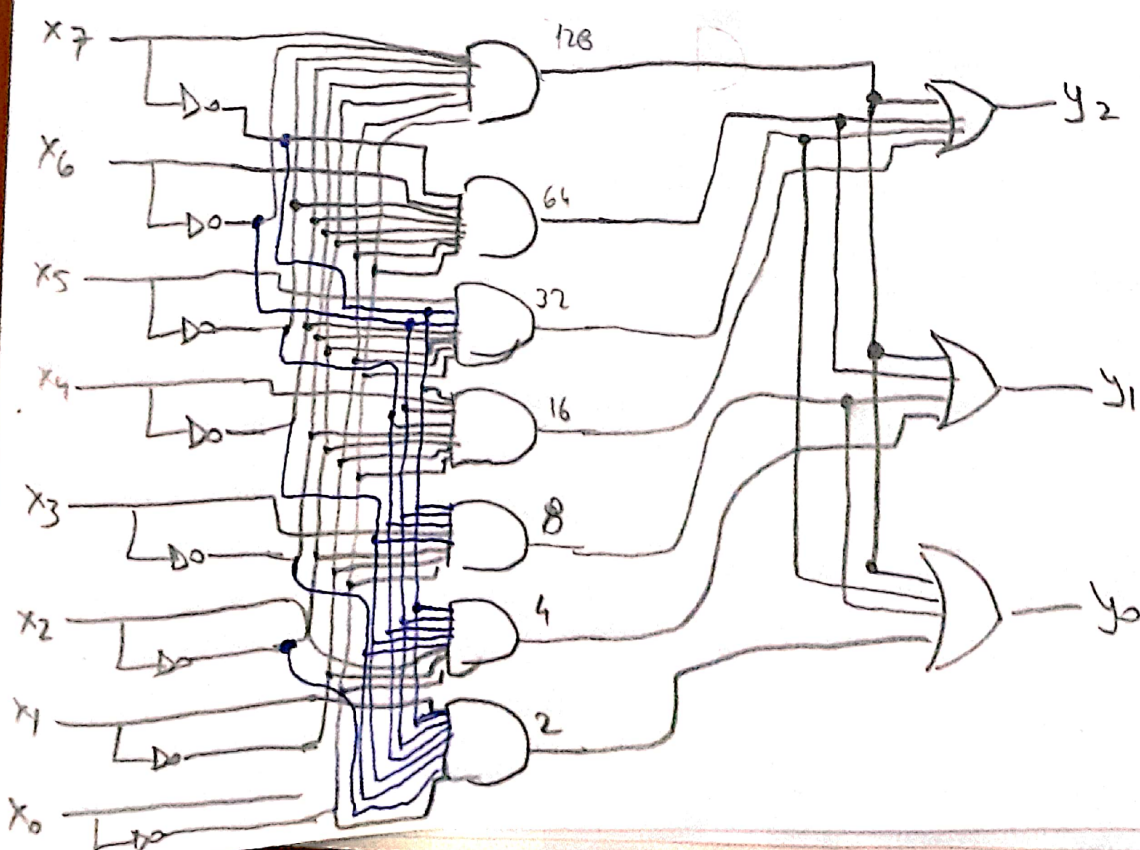
$$+ \bar{x}_7 \bar{x}_6 x_5 \bar{x}_4 \bar{x}_3 \bar{x}_2 \bar{x}_1 \bar{x}_0 + \bar{x}_7 \bar{x}_6 \bar{x}_5 x_4 \bar{x}_3 \bar{x}_2 \bar{x}_1 \bar{x}_0$$

$$y_1 = x_7 \bar{x}_6 \bar{x}_5 \bar{x}_4 \bar{x}_3 \bar{x}_2 \bar{x}_1 \bar{x}_0 + \bar{x}_7 x_6 \bar{x}_5 \bar{x}_4 \bar{x}_3 \bar{x}_2 \bar{x}_1 \bar{x}_0$$

$$+ \bar{x}_7 \bar{x}_6 \bar{x}_5 \bar{x}_4 x_3 \bar{x}_2 \bar{x}_1 \bar{x}_0 + \bar{x}_7 \bar{x}_6 \bar{x}_5 \bar{x}_4 \bar{x}_3 x_2 \bar{x}_1 \bar{x}_0$$

$$y_0 = x_7 \bar{x}_6 \bar{x}_5 \bar{x}_4 \bar{x}_3 \bar{x}_2 \bar{x}_1 \bar{x}_0 + \bar{x}_7 x_6 \bar{x}_5 \bar{x}_4 \bar{x}_3 \bar{x}_2 \bar{x}_1 \bar{x}_0 + \bar{x}_7 \bar{x}_6 \bar{x}_5 \bar{x}_4 x_3 \bar{x}_2 \bar{x}_1 \bar{x}_0$$

$$+ \bar{x}_7 \bar{x}_6 \bar{x}_5 \bar{x}_4 \bar{x}_3 x_2 \bar{x}_1 \bar{x}_0$$

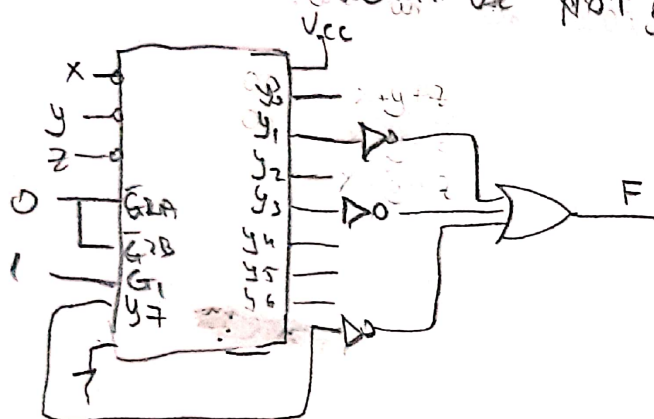


EXP 3

$$F = x'y'z + yz$$

$$F = x'y'z + (x+x')yz = x'y'z + xyz + x'y z$$

active 0 decoder \Rightarrow outputs are maxterms
to have minterms we will use NOT gates at output



$$\begin{aligned} y_0 &= x + y + z \\ y_1 &= x + y + \bar{z} \\ y_2 &= x + \bar{y} + z \\ y_3 &= x + \bar{y} + \bar{z} \\ y_4 &= \bar{x} + y + z \\ y_5 &= \bar{x} + y + \bar{z} \\ y_6 &= \bar{x} + \bar{y} + z \\ y_7 &= \bar{x} + \bar{y} + \bar{z} \end{aligned}$$

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a)

A	B	C	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

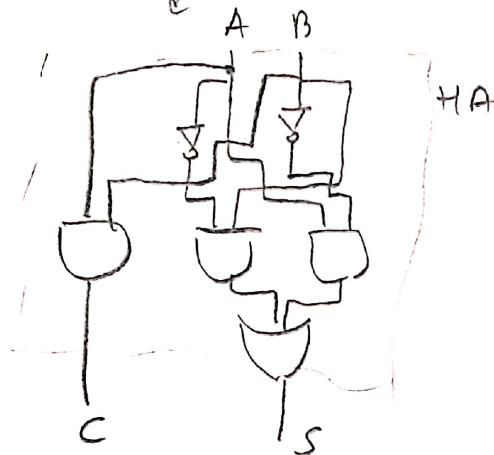
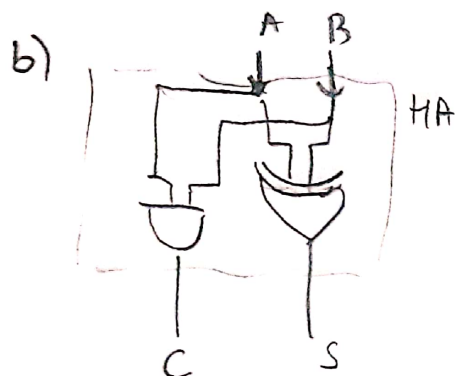
$$C = \sum m(3)$$

$$C = AB$$

$$S = \sum m(1, 2)$$

$$S = \bar{A}B + A\bar{B} \quad (\text{SOP representation})$$

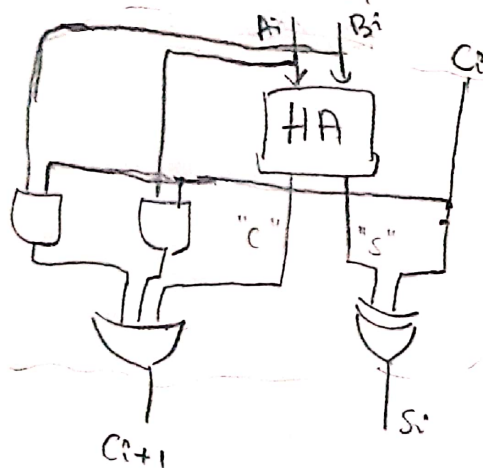
$$S = A \oplus B \quad (\text{using 1cm gates})$$



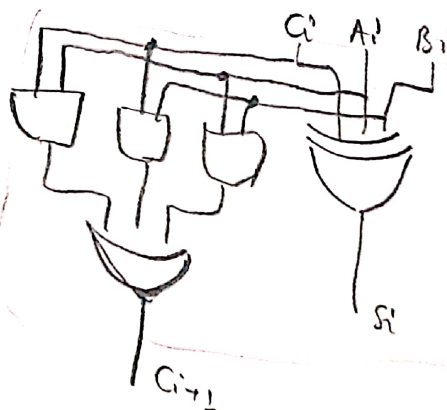
c) Full Adder

$$S_i = A_i \oplus B_i \oplus C_i$$

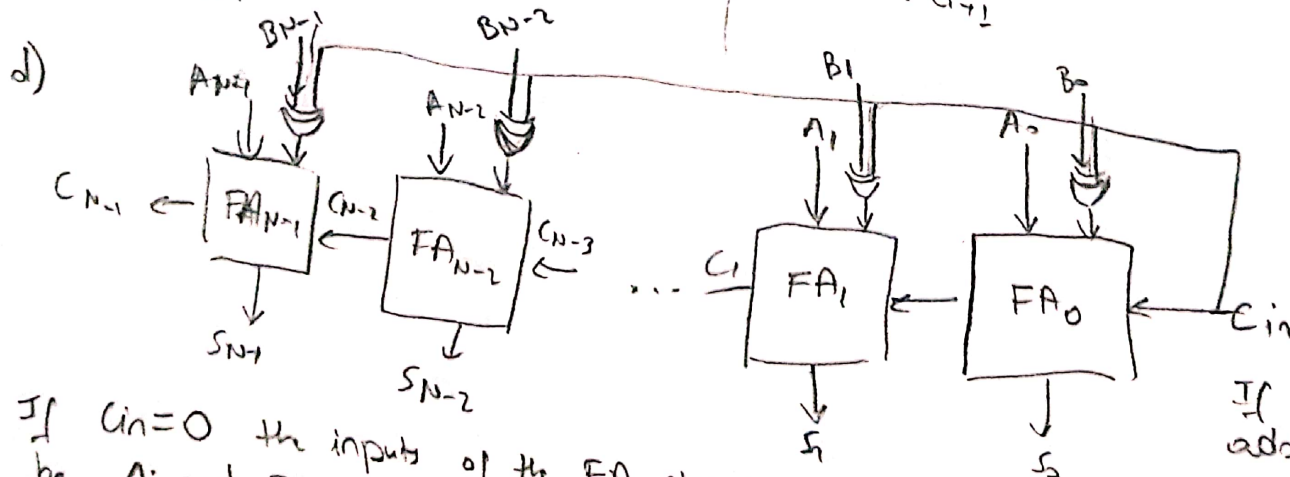
$$C_{i+1} = A_i B_i + A_i C_i + B_i C_i$$



FA
using
HA



FA
(not using
HA)
directly



If $C_{in} = 0$ the inputs of the FA circuit will be A_i and $B_i \Rightarrow$ we will have a basic adder
If $C_{in} = 1$ the inputs will be A_i and \bar{B}_i so we will have a subtractor

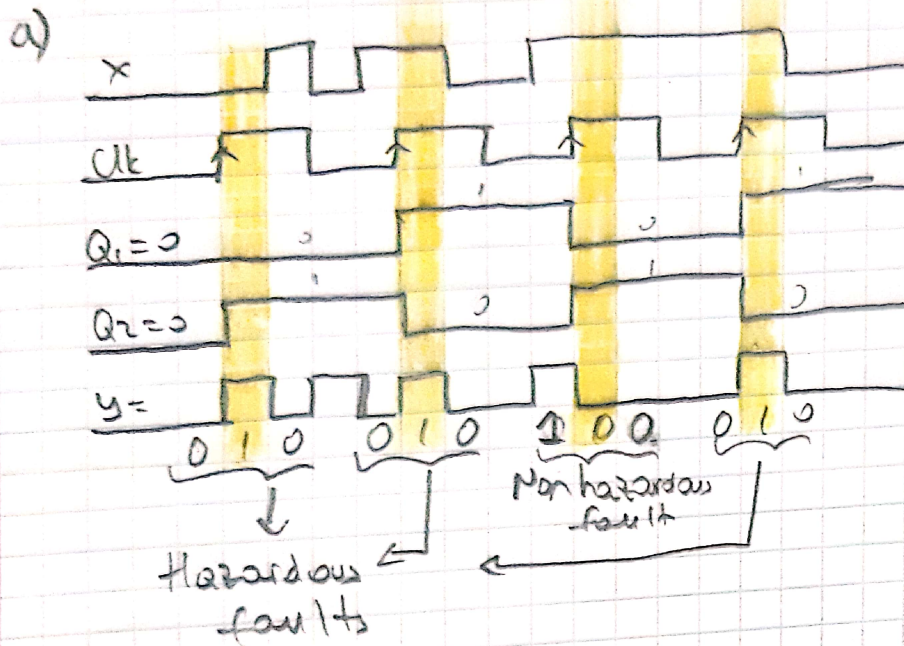
If we want
adder
If $C_{in} = 0$
If we want
subtractor
 $C_{in} = 1$

If $B_i = 1 \quad 1 \oplus 1 = 0 = \bar{1} = \bar{B}_i$
If $B_i = 0 \quad 0 \oplus 1 = 1 = \bar{0} = \bar{B}_i$

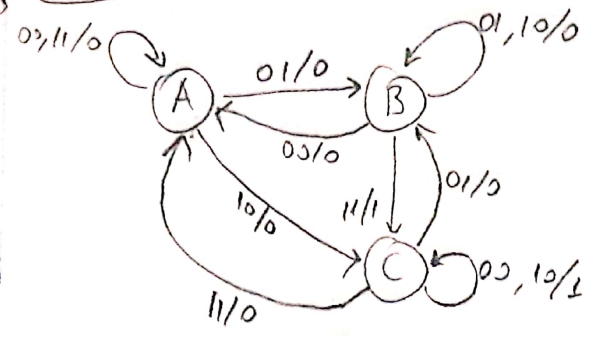
\hookrightarrow because of XOR gate

Maximizing ←

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Pg 4



b) This circuit is a Mealy machine since we have such faults at output and output value depends on both the present state and current input values



a) 3 states
↓
2 bits are enough
to encode them

A → 00
B → 01
C → 10

b)

x	y	q ₁	q ₂	Q ₁	Q ₂	J ₁	K ₁	J ₂	K ₂	z
0	0	0	0	0	0	0	k	0	k	0
0	0	0	1	0	0	0	k	k	1	0
0	0	1	0	1	0	k	0	0	k	1
0	0	1	1	k	k	k	k	k	k	k
0	1	0	0	0	1	0	k	1	k	0
0	1	0	1	0	1	0	k	k	0	0
0	1	1	0	0	1	k	1	1	k	0
0	1	1	1	k	k	k	k	k	k	k
1	0	0	0	1	0	1	k	0	k	0
1	0	0	1	0	1	0	k	k	0	0
1	0	1	0	1	0	k	0	0	k	1
1	0	1	1	k	k	k	k	k	k	k
1	1	0	0	0	0	0	k	0	k	0
1	1	0	1	1	0	1	k	k	1	1
1	1	1	0	0	0	k	1	0	k	0
1	1	1	1	k	k	k	k	k	k	k

JK FF

$$Q = Jq' + K'q$$

00 → 0k
11 → k0
01 → 1k
10 → k1

xy \ q ₁ q ₂	00	01	11	10
00	0	0	k	1
01	0	0	k	0
11	0	1	k	0
10	0	0	k	1

z = $\bar{y}q_1 + xyq_2$

c)

xy \ q ₁ q ₂	00	01	11	10
00	0	0	k	k
01	0	0	k	k
11	0	1	k	k
10	1	0	k	k

J₁ = $x\bar{y}q_2 + xyq_2$

xy \ q ₁ q ₂	00	01	11	10
00	1	k	k	0
01	k	k	k	1
11	k	k	k	1
10	k	k	k	0

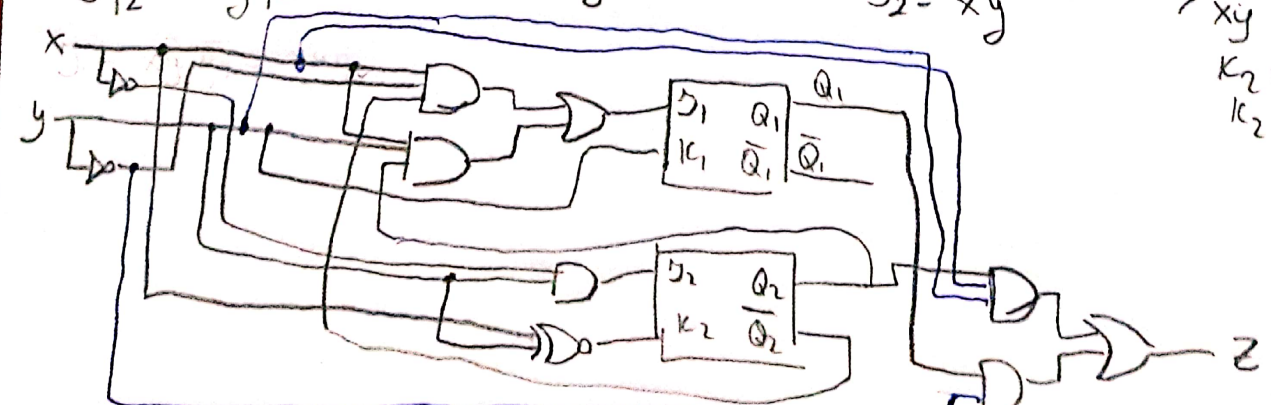
K₁ = y

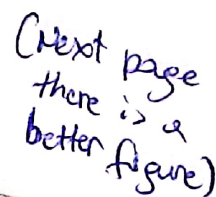
xy \ q ₁ q ₂	00	01	11	10
00	0	k	k	0
01	1	k	k	1
11	0	k	k	0
10	0	k	k	0

J₂ = $\bar{x}y$

xy \ q ₁ q ₂	00	01	11	10
00	k	1	k	k
01	k	0	k	k
11	k	1	k	k
10	k	0	k	k

K₂ = $\bar{x}\bar{y} + xy$
K₂ = $x \oplus y$





After 15 we will need the 2nd IC to represent our numbers in binary.

Unless RCO_2
p.s. 1, then clp
should be g active
A = 1
use clp to
the IC₂ restar.
each time)
1

Then QA should stay like that for 15 Pk pulses. (We use IC_2 to make QA = 1 to each pulse)
and QB should become 0 and QC should become 1
Then IC1 should stay like that for 2 pulses where IC1 counts from 0 to 2
IC1 should restart again from 3. (We use IC_2 to make IC1 = 3 to each pulse)

load of IC_1 and IC_2 \rightarrow $Q_{B_2} Q_{A_1}$

When it reaches 15 using AND gate it "tells" \odot IC₂ to start counting
QA₂ stays 1 for 15 pulses since I'm making Clr₂ command active by applying
RCO₁ there
when counter reaches 31 IC₂ loads 0010 and IC₁ counts from 0 to 1
we reach 33 ($Q_{B2}=1, Q_{A1}=1$) we load 3 at IC₁ and restart
from there.

When counter reaches 15 using AND gate it "tells" IC₂ to start counting. Q_{A2} stays 1 for 15 pulses since I'm making Cln₂ command active by applying RCO₁ there. When counter reaches 31 IC₂ loads 0010 and IC₁ counts from 0 to 1. We reach 33 (Q_{B2}=1, Q_{A1}=1) we load 3 at IC₁ and restart from there.

EXP 7

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EXP 7 (pg 7)

3 to 33 counter

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Circuit

