VLSI Circuit Design II– EHB 425E

HOMEWORK VII

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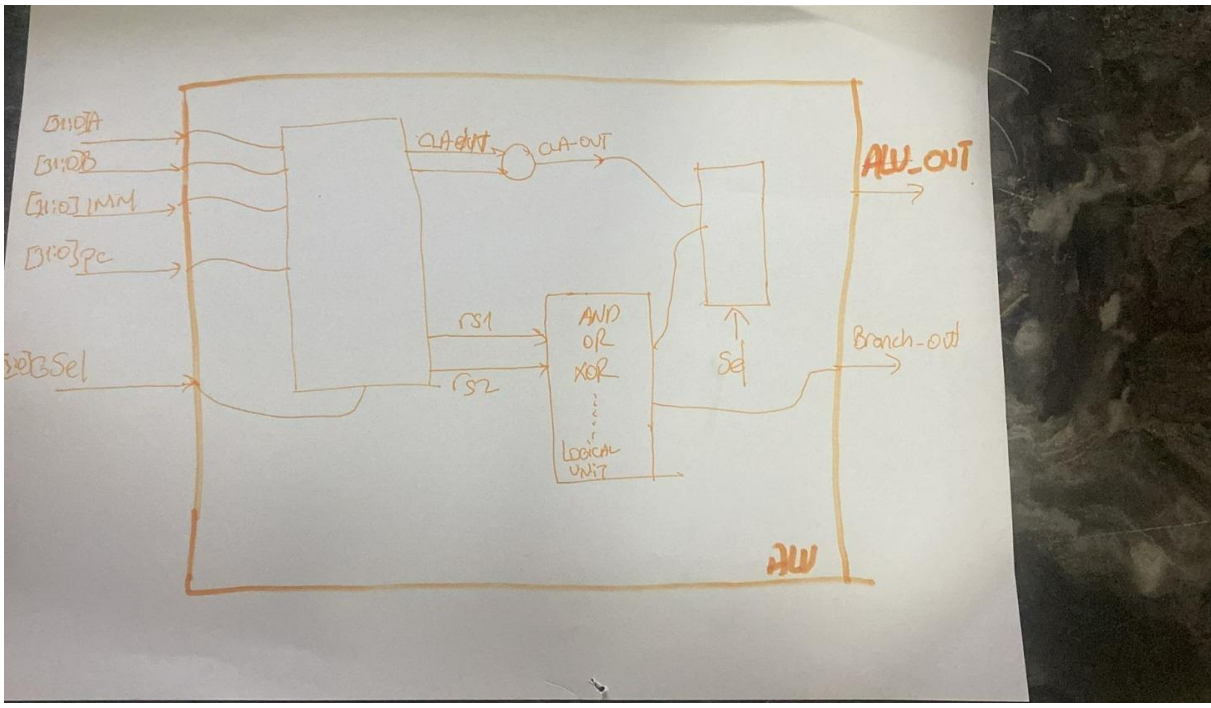
1- ALU Design

a)



b) Selection Signals

1- GSel (4 bits) [3:0]: This is the main selection signal used to control the operation of the ALU. The bits of GSel serve different purposes:
GSel[0]: This bit is used to select between using the B input or the immediate value (imm) as the second operand for the ALU operation.
- If GSel[0] is 1, the immediate value is used as the second operand.
- If GSel[0] is 0, the B input is used as the second operand.

GSel[3:1]: These 3 bits are used to select the specific operation to be performed by the ALU. The following cases are defined:

- 3'b000: AND operation
- 3'b001: OR operation
- 3'b010: XOR operation
- 3'b011: ADD/SUB operation
- 3'b100: Unsigned comparison and branch operations, or jump operations (JAL and JALR)
- 3'b101: Signed comparison and branch operations

2- branch_in (3 bits) [2:0]: This signal is used when GSel[3:1] is set to 3'b100 (unsigned branch) or 3'b101 (signed branch). It is responsible for selecting a specific branch operation based on its value:
- 3'b000: Branch if less than (BLT)
- 3'b001: Branch if greater than or equal (BGE)
- 3'b010: Branch if equal (BEQ)

- 3'b011: Branch if not equal (BNE)
- 3'b100: Set less than (SLT)

3- JAL: This signal indicates a Jump and Link operation, used for branching to a new location and saving the return address.

4- JALR: This signal indicates a Jump and Link Register operation, used for branching to a new location based on the value in a register and saving the return address.

5- sub: This signal is used to indicate whether the ALU should perform an addition or a subtraction operation when GSel[3:1] is set to 3'b011 (ADD/SUB operation). If 'sub' is 1, the ALU performs subtraction; if 'sub' is 0, the ALU performs addition.

These selection signals are essential for controlling the functionality of the ALU, allowing it to perform a wide range of arithmetic, logic, and branching operations based on the input operands and the desired operation specified by the control signals.

c) Status Signals

1- CO (Carry Out): This signal represents the carry-out generated during an addition or subtraction operation. It is set when there is a carry or borrow generated in the most significant bit (MSB) of the result. In unsigned arithmetic, this signal can be used to detect overflow.

2- V (Overflow): This signal indicates when an overflow occurs during a signed arithmetic operation (addition or subtraction). An overflow occurs when the result of the operation is too large (positive overflow) or too small (negative overflow) to be represented within the given bit-width (32 bits in this case).

3- C (Carry): This signal represents the carry generated during an addition or subtraction operation. It is set when there is a carry or borrow generated in the most significant bit (MSB) of the result. In unsigned arithmetic, this signal can be used to detect overflow. Note that the 'C' signal is functionally similar to the 'CO' signal, but is used in different contexts within the module.

4- N (Negative): This signal is set when the result of the ALU operation is negative, i.e., when the most significant bit (MSB) of the result is 1. It helps to determine the sign of the result for signed operations.

5- Z (Zero): This signal is set when the result of the ALU operation is zero. The ZERO_DETECT module checks if all bits of the ALU output (G) are zero, and if so, it sets the 'Z' signal. This signal is useful for conditional branch instructions, such as BEQ (Branch if Equal) and BNE (Branch if Not Equal).

These status signals provide essential information about the outcome of the ALU operation, helping the control unit make decisions based on the result. They are used in various instructions like conditional branches, comparisons, and arithmetic operations to determine the flow of the program or to set the necessary flags in the processor's status register.

d) Purposes Sub-Blocks

1- AND: This sub-block performs a bitwise AND operation on the input operands (rs1 and rs2). It takes two inputs and produces an output where each bit is the result of a bitwise AND between the corresponding bits of the input operands. The AND operation is selected when GSel[3:1] is set to 3'b000.

2- OR: This sub-block performs a bitwise OR operation on the input operands (rs1 and rs2). It takes two inputs and produces an output where each bit is the result of a bitwise OR between the corresponding bits of the input operands. The OR operation is selected when GSel[3:1] is set to 3'b001.

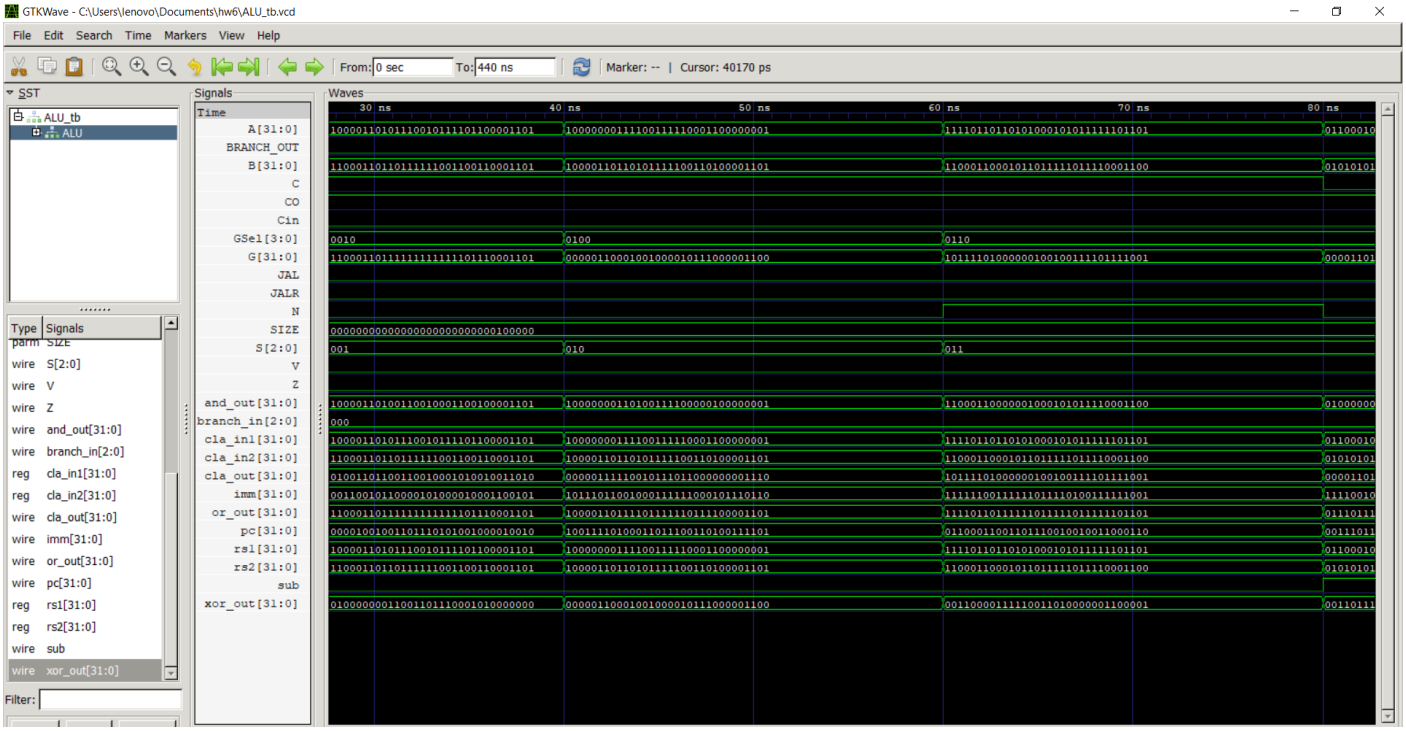
3- XOR: This sub-block performs a bitwise XOR (exclusive OR) operation on the input operands (rs1 and rs2). It takes two inputs and produces an output where each bit is the result of a bitwise XOR between the corresponding bits of the input operands. The XOR operation is selected when GSel[3:1] is set to 3'b010.

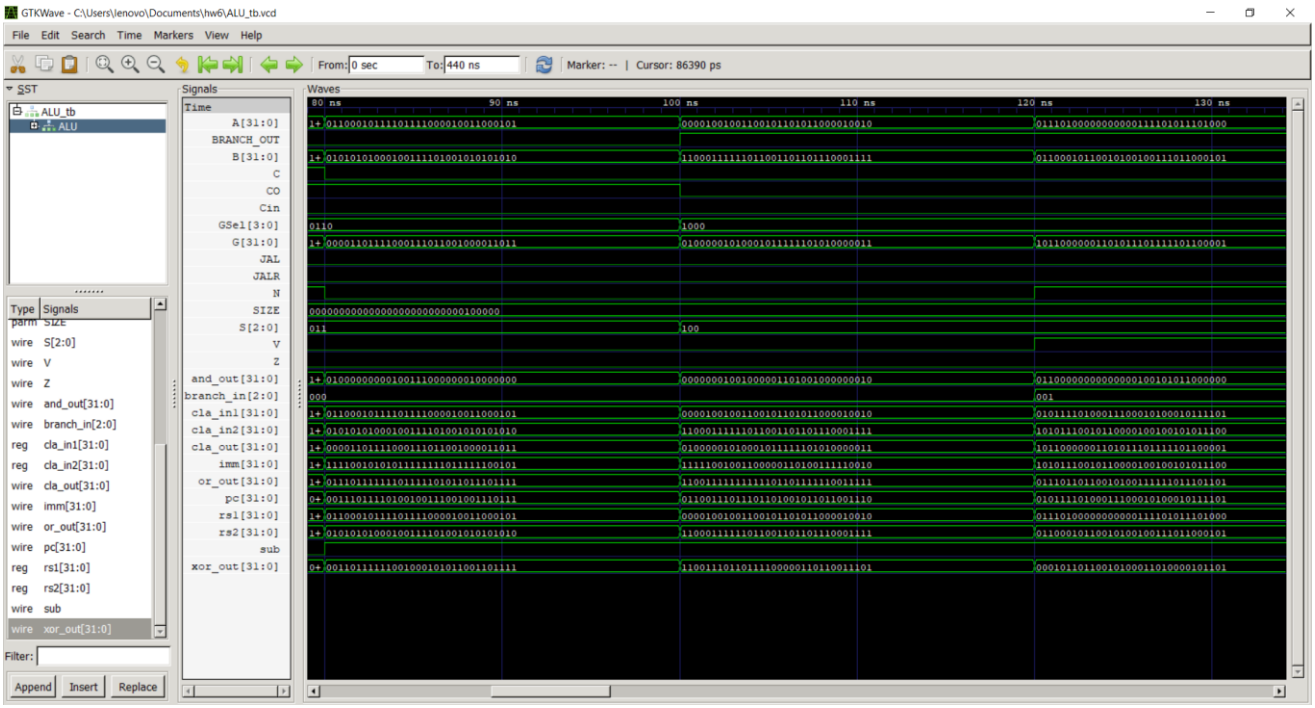
4- CLA (Carry Lookahead Adder): This sub-block performs addition or subtraction on the input operands (cla_in1 and cla_in2) based on the 'sub' signal. The carry lookahead adder is an efficient implementation of an adder that can quickly propagate carry bits through the adder, reducing the overall delay. When GSel[3:1] is set to 3'b011, the CLA is used for ADD/SUB operations. In addition, the CLA is involved in executing branch and jump instructions (when GSel[3:1] is set to 3'b100 or 3'b101) as it calculates the new program counter (PC) value. The CLA sub-block also generates the status signals CO, V, C, and N.

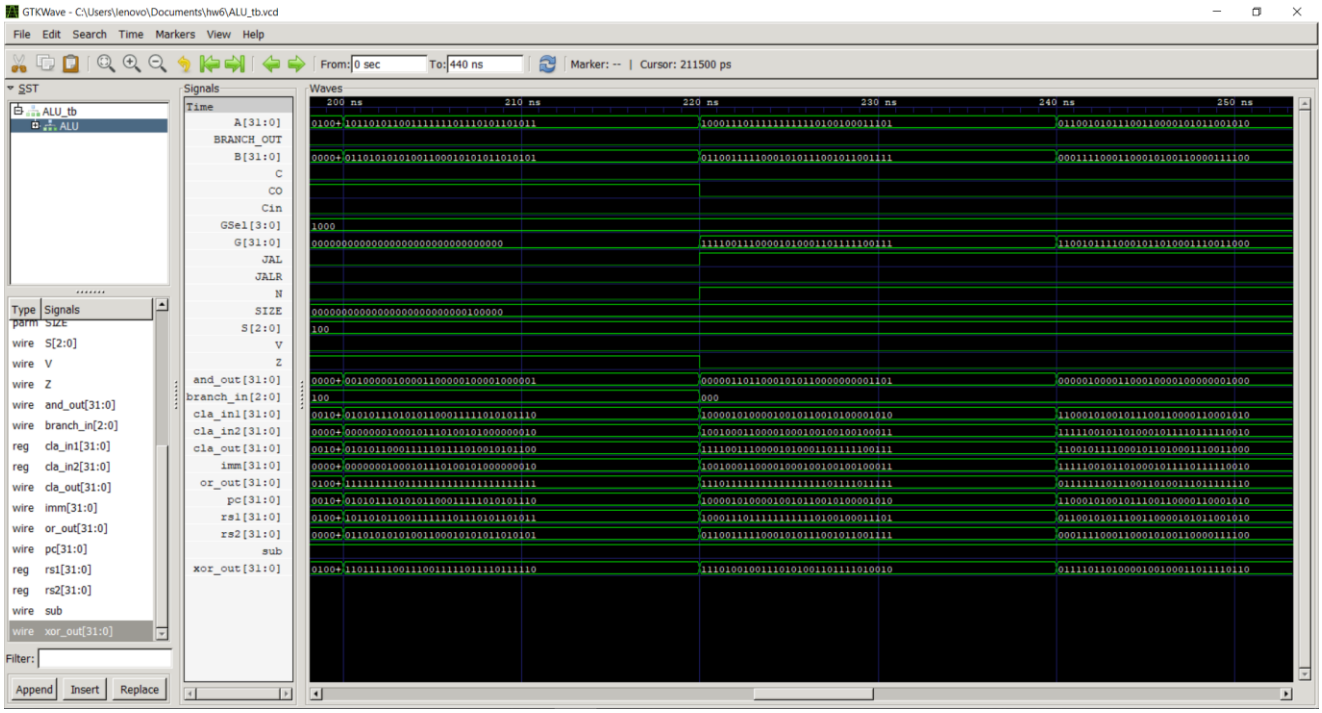
5- ZERO_DETECT: This sub-block checks if the result of the ALU operation (G) is zero. If all bits of the ALU output are zero, the 'Z' (Zero) status signal is set. The ZERO_DETECT sub-block is involved in the execution of conditional branch instructions like BEQ (Branch if Equal) and BNE (Branch if Not Equal), as well as other instructions where the zero flag needs to be updated.

2- ALU

I. Behavioral Simulation Results







ALU block in testbench respectively AND, OR , XOR, ADDER, SUBSTRACTOR, branch A<B, branch A>=B, branch A=B, branch A!=B, G = (rs1 < rs2) ? 32'd1 : 32'd0, branch rs1<rs2 , branch rs1<rs2, JAL||JALR , branch, $signed(A) < $signed(B), $signed(A) >= $signed(B), G= ($signed(rs1) < $signed(rs2)) ? 32'd1 : It returns 32'd0. Looking at the graph and checking TCL from the console, it seems that all transactions are working correctly.

Constant_in	Branch_in	JAL	JALR	GSel	Function	Operation
0	00	0	0	0000	ADD	A+B
0	00	0	0	1000	SUB	A-B
1	00	0	0	0000	ADDI	A+IMM
0	00	0	0	0001	XOR	A^B
1	00	0	0	0001	XORI	A^IMM
0	00	0	0	0010	OR	A|B
1	00	0	0	0010	ORI	A|IMM
0	00	0	0	0011	AND	A&B
1	00	0	0	0011	ANDI	A&IMM
0	00	0	0	0101	SLT	IF A<B, SET 1
1	00	0	0	0101	SLTI	IF A<IMM, SET1
0	00	0	0	0100	SLTU	IF A<B(UNSIGNED), SET 1
1	00	0	0	0100	SLTIU	IF A<IMM(UNSIGNED), SET 1
0	01	0	0	0000	BEQ	IF A == B, PC += IMM
0	10	0	0	0000	BNE	IF A != B, PC += IMM
0	01	0	0	0101	BLT	IF A < B, PC += IMM
0	01	0	0	0100	BLTU	IF A < B (UNSIGNED), PC += IMM
0	10	0	0	0101	BGE	IF A ≥ B, PC += IMM
0	10	0	0	0100	BGEU	IF A ≥ B (UNSIGNED), PC += IMM
0	00	1	0	0000	JAL	JUMP, PC += IMM
0	00	0	1	0000	JALR	JUMP, PC += IMM

- OpenLane Results

```
[STEP 35]
[INFO]: Running OpenROAD Antenna Rule Checker (log: designs/ALU/runs/run/logs/signoff/35-antenna.log)...
[STEP 36]
[INFO]: Running Circuit Validity Checker ERC (log: designs/ALU/runs/run/logs/signoff/36-erc_screen.log)...
[INFO]: Saving current set of views in 'designs/ALU/runs/run/results/final'...
[INFO]: Saving runtime environment...
[INFO]: Generating final set of reports...
[INFO]: Created manufacturability report at 'designs/ALU/runs/run/reports/manufacturability.rpt'.
[INFO]: Created metrics report at 'designs/ALU/runs/run/reports/metrics.csv'.
[WARNING]: There are max fanout violations in the design at the typical corner. Please refer to 'designs/ALU/runs/run/reports/signoff/25-rcx_sta.slew.rpt'.
[INFO]: There are no hold violations in the design at the typical corner.
[INFO]: There are no setup violations in the design at the typical corner.
[SUCCESS]: Flow complete.
[INFO]: Note that the following warnings have been generated:
[WARNING]: There are max fanout violations in the design at the typical corner. Please refer to 'designs/ALU/runs/run/reports/signoff/25-rcx_sta.slew.rpt'.
```

Cell Usage & Estimated Area

```
59. Printing statistics.

=== ALU ===

   Number of wires:               1610
   Number of wire bits:           1801
   Number of public wires:          16
   Number of public wire bits:     176
   Number of memories:               0
   Number of memory bits:            0
   Number of processes:              0
   Number of cells:               1564
     $_ANDNOT_                     496
     $_AND_                          7
     $_MUX_                        358
     $_NAND_                        11
     $_NOR_                         44
     $_NOT_                        102
     $_ORNOT_                       65
     $_OR_                         285
     $_XNOR_                        14
     $_XOR_                        149
     sky130_fd_sc_hd__dlxtn_1       33
```

Estimated Area

Open — 2-syn_sta.area.rpt — ~/OpenLane/designs/ALU/runs/run/reports/synthesis

```
 report_design_area
Design area 7264 u^2 100% utilization.
```

Power Consumption

Open — 2-syn_sta.power.rpt — ~/OpenLane/designs/ALU/runs/run/reports/synthesis

```
 report_power
Group                  Internal  Switching    Leakage      Total
                          Power      Power      Power      Power (Watts)
----------------------------------------------------------------
Sequential             1.24e-05   2.41e-05   2.68e-10   3.65e-05  21.6%
Combinational          7.73e-05   5.55e-05   2.60e-09   1.33e-04  78.4%
Macro                  0.00e+00   0.00e+00   0.00e+00   0.00e+00   0.0%
Pad                    0.00e+00   0.00e+00   0.00e+00   0.00e+00   0.0%
----------------------------------------------------------------
Total                  8.97e-05   7.96e-05   2.87e-09   1.69e-04 100.0%
                          53.0%      47.0%       0.0%
```

Fanout Report

Open — 2-syn_sta.slew.rpt
~/OpenLane/designs/ALU/runs/run/reports/synthesis

```
1
2 ===========================================================================
3  report_check_types -max_slew -max_cap -max_fanout -violators
4 ===========================================================================
5 max fanout
6
7 Pin                                   Limit Fanout  Slack
8 ------------------------------------------------------------
9 _1095_/X                                10     35    -25 (VIOLATED)
10
11
12 ===========================================================================
13 max slew violation count 0
14 max fanout violation count 1
15 max cap violation count 0
16 ===========================================================================
```

Clock Report

Open — 2-syn_sta.worst_slack.rpt
~/OpenLane/designs/ALU/runs/run/reports/synthesis

```
1
2 ===========================================================================
3  report_worst_slack -max (Setup)
4 ===========================================================================
5 worst slack 3.31
6
7 ===========================================================================
8  report_worst_slack -min (Hold)
9 ===========================================================================
10 worst slack 10.18
```

Critical Path Delay

Open — 2-syn_sta.rpt
~/OpenLane/designs/ALU/runs/run/reports/synthesis

```
1
2 ===========================================================================
3 report_checks -unconstrained
4 ===========================================================================
5 Startpoint: branch_in[1] (input port clocked by clk)
6 Endpoint: C (output port clocked by clk)
7 Path Group: clk
8 Path Type: max
9
10 Fanout     Cap    Slew   Delay    Time   Description
11 ---------------------------------------------------------------------------
12                   0.00    0.00    0.00   clock clk (rise edge)
13                           0.00    0.00   clock network delay (ideal)
14                           5.00    5.00 v input external delay
15                   0.03    0.02    5.02 v branch_in[1] (in)
16      7    0.01                           branch_in[1] (net)
17                   0.03    0.00    5.02 v _0786_/A (sky130_fd_sc_hd__or4_2)
18                   0.09    0.67    5.69 v _0786_/X (sky130_fd_sc_hd__or4_2)
19      1    0.00                           _0011_ (net)
20                   0.09    0.00    5.69 v _0787_/A (sky130_fd_sc_hd__buf_1)
21                   0.12    0.19    5.89 v _0787_/X (sky130_fd_sc_hd__buf_1)
22      7    0.02                           _0012_ (net)
23                   0.12    0.00    5.89 v _0788_/C (sky130_fd_sc_hd__or3_2)
24                   0.12    0.52    6.41 v _0788_/X (sky130_fd_sc_hd__or3_2)
25      6    0.02                           _0013_ (net)
26                   0.12    0.00    6.41 v _0796_/S (sky130_fd_sc_hd__mux2_2)
27                   0.08    0.35    6.76 v _0796_/X (sky130_fd_sc_hd__mux2_2)
28      3    0.01                           _0021_ (net)
29                   0.08    0.00    6.76 v _0813_/C (sky130_fd_sc_hd__or3_2)
30                   0.09    0.45    7.21 v _0813_/X (sky130_fd_sc_hd__or3_2)
31      3    0.01                           _0038_ (net)
32                   0.09    0.00    7.21 v _0830_/B (sky130_fd_sc_hd__or4_2)
33                   0.13    0.72    7.93 v _0830_/X (sky130_fd_sc_hd__or4_2)
34      2    0.01                           _0055_ (net)
35                   0.13    0.00    7.93 v _0839_/A (sky130_fd_sc_hd__nor2_2)
36                   0.13    0.18    8.11 ^ _0839_/Y (sky130_fd_sc_hd__nor2_2)
37      2    0.01                           _0064_ (net)
38                   0.13    0.00    8.11 ^ _0847_/A (sky130_fd_sc_hd__inv_2)
39                   0.04    0.05    8.17 v _0847_/Y (sky130_fd_sc_hd__inv_2)
40      2    0.01                           _0072_ (net)
41                   0.04    0.00    8.17 v _0849_/A (sky130_fd_sc_hd__or3_2)
42                   0.12    0.56    8.72 v _0849_/X (sky130_fd_sc_hd__or3_2)
43      4    0.02                           _0074_ (net)
44                   0.12    0.00    8.72 v _0874_/A (sky130_fd_sc_hd__or3_2)
45                   0.09    0.54    9.27 v _0874_/X (sky130_fd_sc_hd__or3_2)
46      3    0.01                           _0099_ (net)
47                   0.09    0.00    9.27 v _0893_/A (sky130_fd_sc_hd__or3_2)
```

Open

2-syn_sta.rpt
~/OpenLane/designs/ALU/runs/run/reports/synthesis

```
1
2 ===========================================================================
3 report_checks -unconstrained
4 ===========================================================================
5 Startpoint: branch_in[1] (input port clocked by clk)
6 Endpoint: C (output port clocked by clk)
7 Path Group: clk
8 Path Type: max
9
10 Fanout     Cap    Slew   Delay    Time   Description
11 ---------------------------------------------------------------------------
12                  0.00    0.00    0.00   clock clk (rise edge)
13                          0.00    0.00   clock network delay (ideal)
14                          5.00    5.00 v input external delay
15                  0.03    0.02    5.02 v branch_in[1] (in)
16      7    0.01                        branch_in[1] (net)
17                  0.03    0.00    5.02 v _0786_/A (sky130_fd_sc_hd__or4_2)
18                  0.09    0.67    5.69 v _0786_/X (sky130_fd_sc_hd__or4_2)
19      1    0.00                        _0011_ (net)
20                  0.09    0.00    5.69 v _0787_/A (sky130_fd_sc_hd__buf_1)
21                  0.12    0.19    5.89 v _0787_/X (sky130_fd_sc_hd__buf_1)
22      7    0.02                        _0012_ (net)
23                  0.12    0.00    5.89 v _0788_/C (sky130_fd_sc_hd__or3_2)
24                  0.12    0.52    6.41 v _0788_/X (sky130_fd_sc_hd__or3_2)
25      6    0.02                        _0013_ (net)
26                  0.12    0.00    6.41 v _0796_/S (sky130_fd_sc_hd__mux2_2)
27                  0.08    0.35    6.76 v _0796_/X (sky130_fd_sc_hd__mux2_2)
28      3    0.01                        _0021_ (net)
29                  0.08    0.00    6.76 v _0813_/C (sky130_fd_sc_hd__or3_2)
30                  0.09    0.45    7.21 v _0813_/X (sky130_fd_sc_hd__or3_2)
31      3    0.01                        _0038_ (net)
32                  0.09    0.00    7.21 v _0830_/B (sky130_fd_sc_hd__or4_2)
33                  0.13    0.72    7.93 v _0830_/X (sky130_fd_sc_hd__or4_2)
34      2    0.01                        _0055_ (net)
35                  0.13    0.00    7.93 v _0839_/A (sky130_fd_sc_hd__nor2_2)
36                  0.13    0.18    8.11 ^ _0839_/Y (sky130_fd_sc_hd__nor2_2)
37      2    0.01                        _0064_ (net)
38                  0.13    0.00    8.11 ^ _0847_/A (sky130_fd_sc_hd__inv_2)
39                  0.04    0.05    8.17 v _0847_/Y (sky130_fd_sc_hd__inv_2)
40      2    0.01                        _0072_ (net)
41                  0.04    0.00    8.17 v _0849_/A (sky130_fd_sc_hd__or3_2)
42                  0.12    0.56    8.72 v _0849_/X (sky130_fd_sc_hd__or3_2)
43      4    0.02                        _0074_ (net)
44                  0.12    0.00    8.72 v _0874_/A (sky130_fd_sc_hd__or3_2)
45                  0.09    0.54    9.27 v _0874_/X (sky130_fd_sc_hd__or3_2)
46      3    0.01                        _0099_ (net)
47                  0.09    0.00    9.27 v _0893_/A (sky130_fd_sc_hd__or3_2)
```

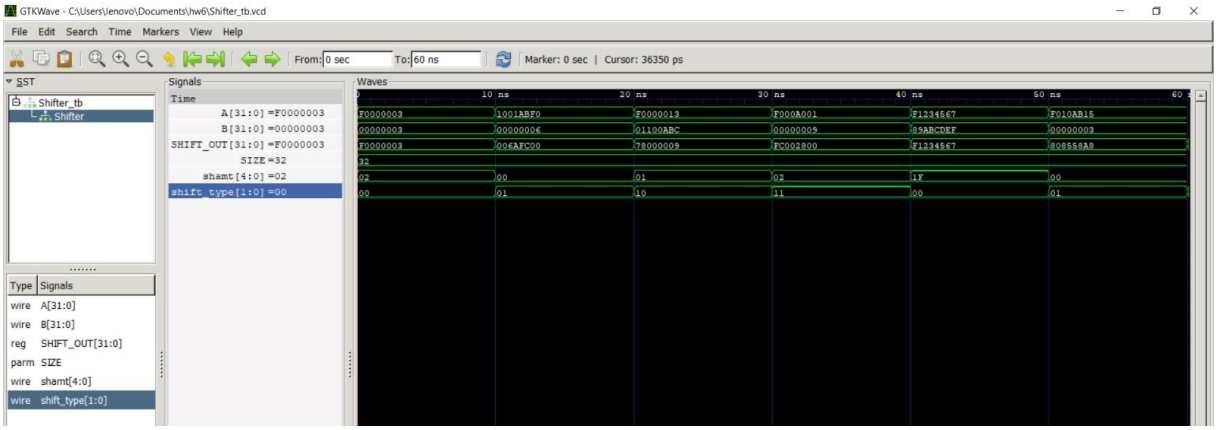
3- SHIFTER

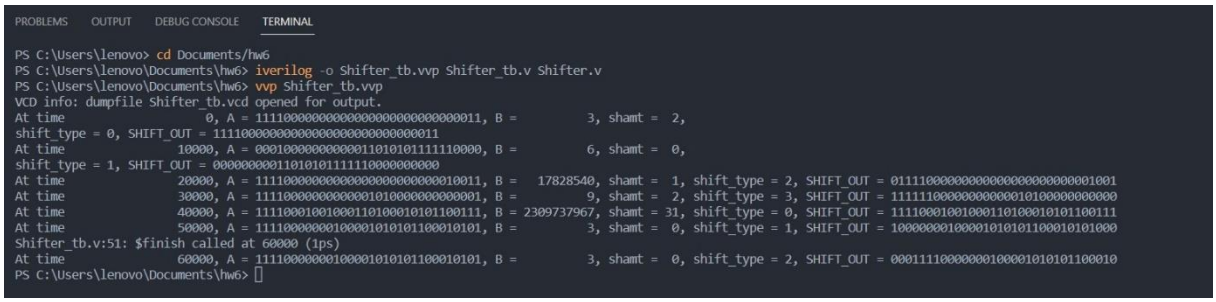
- Purposes of control signals and selection signals
  1- input [SIZE-1:0] A: This input signal represents the first operand, which will be shifted by the specified amount.
  2- input [SIZE-1:0] B: This input signal represents the second operand, which can be used as the shift amount in some cases.
  3- input [4:0] shamt: This input signal, short for "shift amount," specifies the number of positions to shift the operand A. This signal is used when an immediate value is provided for the shift amount.
  4- input [1:0] shift_type: This input signal is a 2-bit control signal that selects the type of shift operation to be performed. The shift operations and their corresponding shift_type values are as follows:
    - 2'b00: No operation (default)
    - 2'b01: Shift Left Logical (SLL) / Shift Left Logical Immediate (SLLI)
    - 2'b10: Shift Right Logical (SRL) / Shift Right Logical Immediate (SRLI)
    - 2'b11: Shift Right Arithmetic (SRA) / Shift Right Arithmetic Immediate (SRAI)

  These control signals are used in the always block to determine the type of shift operation to perform on the input operands A and B. The shift_type input signal is crucial in selecting the appropriate operation based on its value. The shamt input signal provides the shift amount, and depending on the value of shamt, the shift amount will either come from shamt or the lower 5 bits of input B.

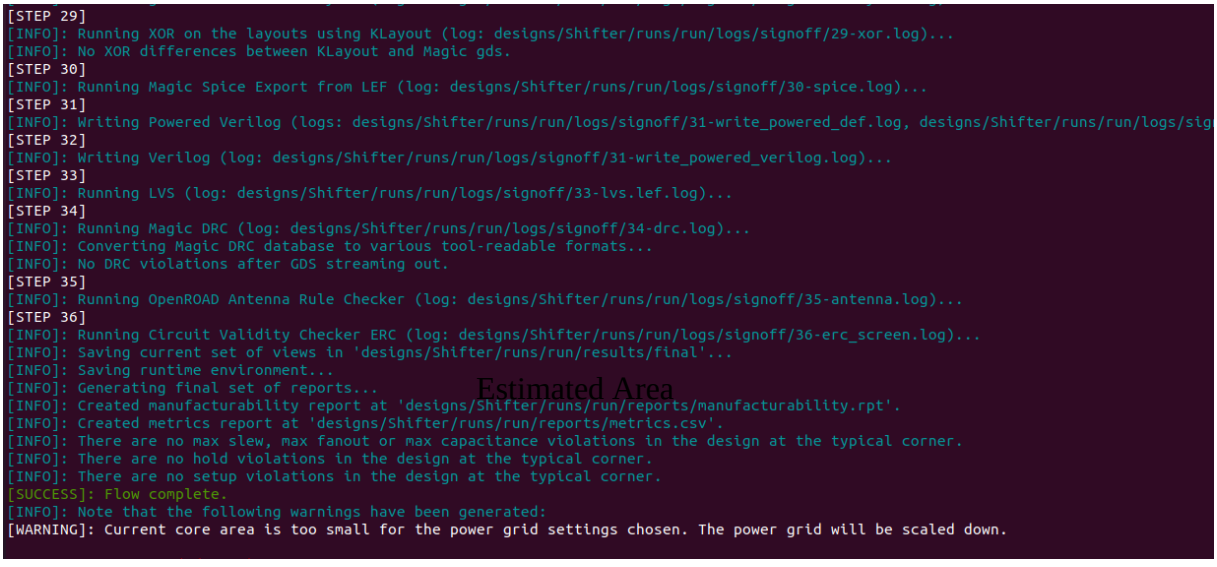
SLL	Shift Left Logical	rd ← rs1 << rs2[4:0]	R-TYPE
SLLI	Shift Left Logical Immediate	rd ← rs1 << shamt	I-TYPE
SRL	Shift Right Logical	rd ← rs1 >> rs2[4:0]	R-TYPE
SRLI	Shift Right Logical Immediate	rd ← rs1 >> shamt	I-TYPE
SRA	Shift Right Arithmetic	rd ← rs1 >>> rs2[4:0]	R-TYPE
SRAI	Shift Right Arithme	rd ← rs1 >>> shamt	I-TYPE

- Behavioral Simulation
  As you can see, the shifter block is working successfully. First, shift_type is selected, then if there is a shamt signal, that shift type is applied as much as the decimal value of the shamt, otherwise it is applied as the decimal value of the B value. Console output is given above. SLL shifts left, SRL shifts right, and SRA shifts arithmetically to the right, then fills in as much space as the most significant bit is.





- Openlane results



Estimated Area

Estimated Area

Open — 2-syn_sta.area.rpt
~/OpenLane/designs/Shifter/runs/run/reports/synthesis

```
1
2 ===========================================================================
3  report_design_area
4 ===========================================================================
5 Design area 6723 u^2 100% utilization.
```

Cell Usage

Open

```
1
2 61. Printing statistics.
3
4 === Shifter ===
5
6    Number of wires:                699
7    Number of wire bits:            797
8    Number of public wires:           5
9    Number of public wire bits:     103
10   Number of memories:               0
11   Number of memory bits:            0
12   Number of processes:              0
13   Number of cells:                726
14     sky130_fd_sc_hd__a211o_2       26
15     sky130_fd_sc_hd__a21bo_2        1
16     sky130_fd_sc_hd__a21o_2        41
17     sky130_fd_sc_hd__a21oi_2       28
18     sky130_fd_sc_hd__a221o_2        2
19     sky130_fd_sc_hd__a22o_2        16
20     sky130_fd_sc_hd__a2bb2o_2       8
21     sky130_fd_sc_hd__a31o_2        10
22     sky130_fd_sc_hd__a32o_2         6
23     sky130_fd_sc_hd__a32oi_2        1
24     sky130_fd_sc_hd__a41o_2         4
25     sky130_fd_sc_hd__and2_2         9
26     sky130_fd_sc_hd__and2b_2        1
27     sky130_fd_sc_hd__and3_2         6
28     sky130_fd_sc_hd__buf_1         63
29     sky130_fd_sc_hd__inv_2         33
30     sky130_fd_sc_hd__mux2_2       320
31     sky130_fd_sc_hd__mux4_2         3
32     sky130_fd_sc_hd__nand2_2       14
33     sky130_fd_sc_hd__nor2_2        33
34     sky130_fd_sc_hd__nor2b_2        1
35     sky130_fd_sc_hd__nor3_2         2
36     sky130_fd_sc_hd__o211a_2       30
37     sky130_fd_sc_hd__o21a_2         1
38     sky130_fd_sc_hd__o21ai_2       12
39     sky130_fd_sc_hd__o221a_2        7
40     sky130_fd_sc_hd__o221ai_2       1
41     sky130_fd_sc_hd__o22a_2         7
42     sky130_fd_sc_hd__o2bb2a_2       1
43     sky130_fd_sc_hd__o31a_2         3
44     sky130_fd_sc_hd__o31ai_2        1
45     sky130_fd_sc_hd__o32a_2         3
46     sky130_fd_sc_hd__or2_2         24
47     sky130_fd_sc_hd__or2b_2         1
```

```
1
2 53. Printing statistics.
3
4 === Shifter ===
5
6    Number of wires:                618
7    Number of wire bits:            716
8    Number of public wires:           5
9    Number of public wire bits:     103
10   Number of memories:               0
11   Number of memory bits:            0
12   Number of processes:              0
13   Number of cells:                645
14     $_ANDNOT_                      38
15     $_AND_                         26
16     $_MUX_                        522
17     $_NAND_                         1
18     $_NOR_                          5
19     $_NOT_                         39
20     $_ORNOT_                        2
21     $_OR_                          12
22
```

Clock Report

Open — 2-syn_sta.worst_slack.rpt
~/OpenLane/designs/Shifter/runs/run/reports/synthesis

```
1
2 ===========================================================================
3  report_worst_slack -max (Setup)
4 ===========================================================================
5 worst slack 2.16
6
7 ===========================================================================
8  report_worst_slack -min (Hold)
9 ===========================================================================
10 worst slack 4.09
```

Critical Path

```
68
69 Startpoint: shift_type[1] (input port clocked by clk)
70 Endpoint: SHIFT_OUT[13] (output port clocked by clk)
71 Path Group: clk
72 Path Type: max
73
74 Fanout     Cap    Slew   Delay    Time   Description
75 ---------------------------------------------------------------------------
76                    0.00    0.00    0.00   clock clk (rise edge)
77                            0.00    0.00   clock network delay (ideal)
78                            2.00    2.00 ^ input external delay
79                    0.05    0.04    2.04 ^ shift_type[1] (in)
80      4    0.01                            shift_type[1] (net)
81                    0.05    0.00    2.04 ^ _0770_/B (sky130_fd_sc_hd__and2_2)
82                    0.03    0.13    2.17 ^ _0770_/X (sky130_fd_sc_hd__and2_2)
83      1    0.00                            _0053_ (net)
84                    0.03    0.00    2.17 ^ _0771_/A (sky130_fd_sc_hd__buf_1)
85                    0.28    0.25    2.42 ^ _0771_/X (sky130_fd_sc_hd__buf_1)
86      9    0.02                            _0054_ (net)
87                    0.28    0.00    2.42 ^ _0772_/C (sky130_fd_sc_hd__and3_2)
88                    0.04    0.22    2.64 ^ _0772_/X (sky130_fd_sc_hd__and3_2)
89      1    0.00                            _0055_ (net)
90                    0.04    0.00    2.64 ^ _0773_/A (sky130_fd_sc_hd__buf_1)
91                    0.36    0.31    2.95 ^ _0773_/X (sky130_fd_sc_hd__buf_1)
```

```
92      8    0.03                            _0056_ (net)
93                    0.36    0.00    2.95 ^ _0780_/A2 (sky130_fd_sc_hd__a21o_2)
94                    0.11    0.26    3.21 ^ _0780_/X (sky130_fd_sc_hd__a21o_2)
95      6    0.02                            _0063_ (net)
96                    0.11    0.00    3.21 ^ _0803_/A (sky130_fd_sc_hd__buf_1)
97                    0.38    0.34    3.55 ^ _0803_/X (sky130_fd_sc_hd__buf_1)
98     10    0.03                            _0086_ (net)
99                    0.38    0.00    3.55 ^ _0844_/S (sky130_fd_sc_hd__mux2_2)
100                   0.05    0.40    3.95 v _0844_/X (sky130_fd_sc_hd__mux2_2)
101     2    0.00                            _0126_ (net)
102                   0.05    0.00    3.95 v _1056_/A1 (sky130_fd_sc_hd__mux2_2)
103                   0.05    0.28    4.23 v _1056_/X (sky130_fd_sc_hd__mux2_2)
104     2    0.00                            _0334_ (net)
105                   0.05    0.00    4.23 v _1212_/A1 (sky130_fd_sc_hd__mux2_2)
106                   0.05    0.27    4.50 v _1212_/X (sky130_fd_sc_hd__mux2_2)
107     1    0.00                            _0482_ (net)
108                   0.05    0.00    4.50 v _1214_/A2 (sky130_fd_sc_hd__o211a_2)
109                   0.04    0.23    4.73 v _1214_/X (sky130_fd_sc_hd__o211a_2)
110     1    0.00                            _0484_ (net)
111                   0.04    0.00    4.73 v _1218_/A (sky130_fd_sc_hd__or3_2)
112                   0.07    0.47    5.21 v _1218_/X (sky130_fd_sc_hd__or3_2)
113     1    0.00                            _0488_ (net)
114                   0.07    0.00    5.21 v _1219_/B1 (sky130_fd_sc_hd__a2bb2o_2)
115                   0.12    0.37    5.58 v _1219_/X (sky130_fd_sc_hd__a2bb2o_2)
116     1    0.03                            SHIFT_OUT[13] (net)
117                   0.12    0.00    5.58 v SHIFT_OUT[13] (out)
118                           5.58    data arrival time
119
120                   0.00   10.00   10.00   clock clk (rise edge)
121                          0.00   10.00   clock network delay (ideal)
122                         -0.25    9.75   clock uncertainty
123                          0.00    9.75   clock reconvergence pessimism
124                         -2.00    7.75   output external delay
125                                 7.75    data required time
126 -----------------------------------------------------------------------------
127                                 7.75    data required time
128                                -5.58    data arrival time
129 -----------------------------------------------------------------------------
130                                 2.17    slack (MET)
131
```

Power consumptioon

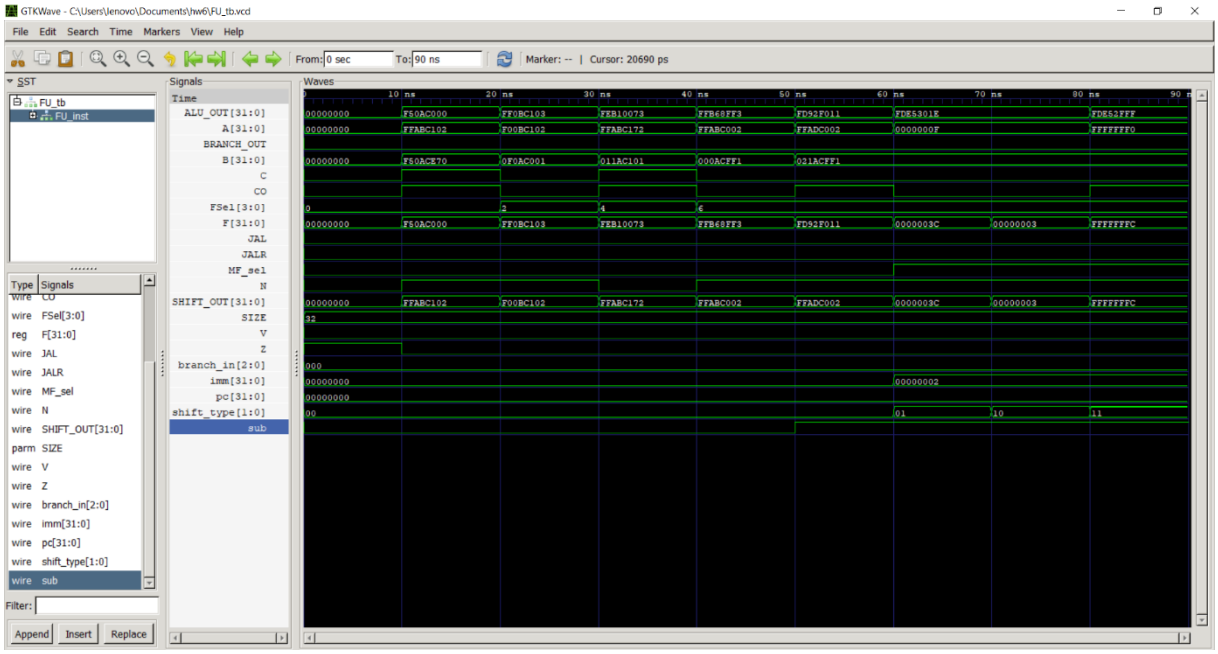
Open — 2-syn_sta.power.rpt
~/OpenLane/designs/Shifter/runs/run/reports/synthesis

```
1
2 ========================================================================
3  report_power
4 ========================================================================
5 Group                  Internal  Switching    Leakage      Total
6                           Power      Power      Power      Power (Watts)
7 ----------------------------------------------------------------
8 Sequential             0.00e+00   0.00e+00   0.00e+00   0.00e+00   0.0%
9 Combinational          2.14e-04   1.57e-04   2.48e-09   3.71e-04 100.0%
10 Macro                 0.00e+00   0.00e+00   0.00e+00   0.00e+00   0.0%
11 Pad                   0.00e+00   0.00e+00   0.00e+00   0.00e+00   0.0%
12 ----------------------------------------------------------------
13 Total                 2.14e-04   1.57e-04   2.48e-09   3.71e-04 100.0%
14                          57.7%      42.3%       0.0%
```

4- FU

ALU module and shifter module are connected in this module. A and B inputs are similar, by defining one lot at the end of the house, it is aimed to leave the output of the ALU or to give the output of the shifter.
MUX 1'b0: ALU_OUT
MUX 1'b1: SHIFT_OUT

- Behavioral Simulation
  As seen below, both shifter output and ALU output can be given. Shifter module and ALU module are connected here. As seen in the simulation, all operators are working successfully. Console output is given below.




```
PS C:\Users\lenovo\Documents\hw6> iverilog -o FU_tb.vvp FU_tb.v  FU.v ALU.v OR.v AND.v CLA.v CLG.v XOR.v ZERO_DETECT.v Shifter.v
PS C:\Users\lenovo\Documents\hw6> vvp FU_tb.vvp
VCD info: dumpfile FU_tb.vcd opened for output.
Testing ALU operations
AND: 11111111101010111100000100000010 & 11110101000010101100111001110000 = 11110101000010101100000000000000, V: 0, C: 1, N: 1, Z: 0
OR: 11110000000010111100000100000010 | 00001111000010101100000000000001 = 11111111000010111100000100000011, V: 0, C: 0, N: 1, Z: 0
XOR: 11111111101010111100000101110010 ^ 00000001000110101100000100000001 = 11111110101100010000000001110011, V: 0, C: 1, N: 0, Z: 0
ADD: 4289445890 &     708593 = 4290154483, V: 0, C: 0, N: 1, Z: 0
SUB: 4289576962 &   35311601 = 4254265361, V: 0, C: 0, N: 1, Z: 0
Testing Shifter operations
SLL: 00000000000000000000000000001111 <<          2 = 00000000000000000000000000111100, V: 0, C: 0, N: 1, Z: 0
SRL: 00000000000000000000000000001111 >>          2 = 00000000000000000000000000000011, V: 0, C: 0, N: 1, Z: 0
SRA: 11111111111111111111111111110000 >>>         2 = 11111111111111111111111111111100, V: 0, C: 0, N: 1, Z: 0
Testbench completed.
FU_tb.v:102: $finish called at 90000 (1ps)
PS C:\Users\lenovo\Documents\hw6>
```

- Openlane Results

Estimated Area

Open — 25-rcx_sta.area.rpt — ~/OpenLane/designs/FU/runs/run/reports/signoff

```
1
2 ===========================================================================
3  report_design_area
4 ===========================================================================
5 Design area 13968 u^2 52% utilization.
```

Power Consumption

Open — 25-rcx_sta.power.rpt — ~/OpenLane/designs/FU/runs/run/reports/signoff

```
1
2 ===========================================================================
3  report_power
4 ===========================================================================
5 Group                  Internal  Switching    Leakage      Total
6                           Power      Power      Power      Power (Watts)
7 ----------------------------------------------------------------
8 Sequential             1.14e-05   7.46e-06   2.60e-10   1.89e-05   4.9%
9 Combinational          1.42e-04   2.26e-04   8.61e-09   3.68e-04  95.1%
10 Macro                 0.00e+00   0.00e+00   0.00e+00   0.00e+00   0.0%
11 Pad                   0.00e+00   0.00e+00   0.00e+00   0.00e+00   0.0%
12 ----------------------------------------------------------------
13 Total                 1.54e-04   2.33e-04   8.87e-09   3.87e-04 100.0%
14                          39.7%      60.3%       0.0%
```

Fanout Report

Open — 25-rcx_sta.slew.rpt — ~/OpenLane/designs/FU/runs/run/reports/signoff

```
1
2 ===========================================================================
3  report_check_types -max_slew -max_cap -max_fanout -violators
4 ===========================================================================
5 max fanout
6
7 Pin                                   Limit Fanout  Slack
8 ------------------------------------------------------
9 _1810_/X                                10     13     -3 (VIOLATED)
10 _1812_/X                               10     12     -2 (VIOLATED)
11 _1861_/X                               10     12     -2 (VIOLATED)
12 _1780_/X                               10     11        (VIOLATED)
13 _1886_/X                               10     11        (VIOLATED)
14 input12/X                              10     11        (VIOLATED)
15
16
17 ===========================================================================
18 max slew violation count 0
19 max fanout violation count 6
20 max cap violation count 0
21 ===========================================================================
```

Clock Report

Open — 25-rcx_sta.worst_slack.rpt — ~/OpenLane/designs/FU/runs/run/reports/signoff

```
1
2 ===========================================================================
3  report_worst_slack -max (Setup)
4 ===========================================================================
5 worst slack 4.59
6
7 ===========================================================================
8  report_worst_slack -min (Hold)
9 ===========================================================================
10 worst slack 10.50
```

Critical Path Delay

Open — 25-rcx_sta.max.rpt — ~/Desktop/FU_signoff — Save

```
                          0.00   25.00   clock network delay (ideal)
                         -0.25   24.75   clock uncertainty
                          0.00   24.75   clock reconvergence pessimism
                         -5.00   19.75   output external delay
                                 19.75   data required time
---------------------------------------------------------------------------
                                 19.75   data required time
                                -10.17   data arrival time
---------------------------------------------------------------------------
                                  9.58   slack (MET)


Startpoint: imm[2] (input port clocked by clk)
Endpoint: F[2] (output port clocked by clk)
Path Group: clk
Path Type: max

Fanout     Cap    Slew   Delay    Time   Description
---------------------------------------------------------------------------
                  0.00    0.00    0.00   clock clk (rise edge)
                          0.00    0.00   clock network delay (ideal)
                          5.00    5.00 v input external delay
                  0.01    0.01    5.01 v imm[2] (in)
     1    0.00                           imm[2] (net)
                  0.01    0.00    5.01 v input97/A (sky130_fd_sc_hd__buf_4)
                  0.12    0.21    5.21 v input97/X (sky130_fd_sc_hd__buf_4)
     9    0.09                           net97 (net)
                  0.12    0.01    5.23 v _2153_/A (sky130_fd_sc_hd__or4_1)
                  0.12    0.63    5.85 v _2153_/X (sky130_fd_sc_hd__or4_1)
     1    0.01                           _1396_ (net)
                  0.12    0.00    5.85 v _2154_/C (sky130_fd_sc_hd__nor3_4)
                  0.38    0.35    6.21 ^ _2154_/Y (sky130_fd_sc_hd__nor3_4)
     6    0.03                           _1397_ (net)
                  0.38    0.00    6.21 ^ _2159_/A (sky130_fd_sc_hd__and2_1)
                  0.05    0.19    6.40 ^ _2159_/X (sky130_fd_sc_hd__and2_1)
     1    0.00                           _1402_ (net)
                  0.05    0.00    6.40 ^ _2160_/A (sky130_fd_sc_hd__clkbuf_4)
                  0.15    0.23    6.63 ^ _2160_/X (sky130_fd_sc_hd__clkbuf_4)
     5    0.05                           _1403_ (net)
                  0.15    0.00    6.63 ^ _2161_/A2 (sky130_fd_sc_hd__a21oi_2)
                  0.10    0.12    6.75 v _2161_/Y (sky130_fd_sc_hd__a21oi_2)
     5    0.02                           _1404_ (net)
                  0.10    0.00    6.76 v _2162_/A (sky130_fd_sc_hd__clkbuf_4)
                  0.11    0.24    7.00 v _2162_/X (sky130_fd_sc_hd__clkbuf_4)
    10    0.05                           _1405_ (net)
                  0.11    0.00    7.00 v _2205_/S (sky130_fd_sc_hd__mux2_1)
```

Open — 25-rcx_sta.max.rpt — ~/Desktop/FU_signoff

```
    10    0.05                           _1405_ (net)
                  0.11    0.00    7.00 v _2205_/S (sky130_fd_sc_hd__mux2_1)
                  0.07    0.36    7.36 v _2205_/X (sky130_fd_sc_hd__mux2_1)
     2    0.01                           _0070_ (net)
                  0.07    0.00    7.36 v _2392_/A1 (sky130_fd_sc_hd__mux2_1)
                  0.06    0.32    7.69 v _2392_/X (sky130_fd_sc_hd__mux2_1)
     1    0.00                           _0255_ (net)
                  0.06    0.00    7.69 v _2393_/A1 (sky130_fd_sc_hd__mux2_1)
                  0.07    0.34    8.02 v _2393_/X (sky130_fd_sc_hd__mux2_1)
     1    0.01                           _0256_ (net)
                  0.07    0.00    8.02 v _2394_/A1 (sky130_fd_sc_hd__mux2_1)
                  0.08    0.35    8.37 v _2394_/X (sky130_fd_sc_hd__mux2_1)
     1    0.01                           _0257_ (net)
                  0.08    0.00    8.37 v _2395_/B (sky130_fd_sc_hd__or2_1)
                  0.05    0.23    8.59 v _2395_/X (sky130_fd_sc_hd__or2_1)
     1    0.00                           _0258_ (net)
                  0.05    0.00    8.59 v _2396_/B1 (sky130_fd_sc_hd__o211a_1)
                  0.05    0.14    8.73 v _2396_/X (sky130_fd_sc_hd__o211a_1)
     1    0.00                           _0259_ (net)
                  0.05    0.00    8.73 v _2416_/B1 (sky130_fd_sc_hd__a211o_1)
                  0.08    0.32    9.05 v _2416_/X (sky130_fd_sc_hd__a211o_1)
     1    0.01                           _0279_ (net)
                  0.08    0.00    9.05 v _2417_/B1 (sky130_fd_sc_hd__a2bb2o_1)
                  0.05    0.29    9.35 v _2417_/X (sky130_fd_sc_hd__a2bb2o_1)
     1    0.00                           _0280_ (net)
                  0.05    0.00    9.35 v _2419_/A1 (sky130_fd_sc_hd__mux2_1)
                  0.17    0.44    9.79 v _2419_/X (sky130_fd_sc_hd__mux2_1)
     1    0.03                           _0282_ (net)
                  0.17    0.00    9.79 v _2420_/A (sky130_fd_sc_hd__clkbuf_1)
                  0.03    0.15    9.94 v _2420_/X (sky130_fd_sc_hd__clkbuf_1)
     1    0.00                           net165 (net)
                  0.03    0.00    9.94 v output165/A (sky130_fd_sc_hd__buf_2)
                  0.09    0.18   10.12 v output165/X (sky130_fd_sc_hd__buf_2)
     1    0.03                           F[2] (net)
                  0.09    0.00   10.12 v F[2] (out)
                                 10.12   data arrival time

                  0.00   25.00   25.00   clock clk (rise edge)
                          0.00   25.00   clock network delay (ideal)
                         -0.25   24.75   clock uncertainty
                          0.00   24.75   clock reconvergence pessimism
                         -5.00   19.75   output external delay
                                 19.75   data required time
---------------------------------------------------------------------------
                                 19.75   data required time
                                -10.12   data arrival time
---------------------------------------------------------------------------
```