EHB 335E HW#4

Due: 6 December 2020 @22 o'clock – **No late homework will be accepted.**

1) Consider the BiCMOS follower circuit shown in Figure 1a. The BJT transistor parameters are $V_{BE,on} = 0.7V$, $V_{CE,sat} = 0.2V$, $V_A = \infty$, and the depletion mode n-MOSFET parameters are $V_{TH} = -1.8V$, $k_n = 12mA/V^2$, $\lambda = 0$ (You can treat depletion mode MOSFETS as regular MOSFETS).
   a. Determine the maximum and minimum values of output voltage and the corresponding input voltages for the circuit to operate in the linear region (i.e., Class-A operation) for (a) $R_L = \infty$ and (b) $R_L = 500\Omega$.
   b. What is the smallest value of R_L possible if a 2 V peak sine wave is produced at the output?
   c. What is the corresponding power conversion efficiency?
2) Consider the class-AB output stage in Figure 1b. Assume that all transistors are matched, with parameters $V_+ = -V_- = 12\ V$ and $\beta = 40$, $V_{BE}(npn) = V_{BE}(pnp) = 0.7\ V$, $R_1 = R_2 = 250\ \Omega$, $R_3 = R_4 = 0\ \Omega$, $R_L = 8\ \Omega$. Hint: You can practically assume that $i_{E3} = i_O$.
   a. For $v_I = 0\ V$, determine i_{E1}, i_{E2}, i_{B1}, and i_{B2}.
   b. For $v_I = 5\ V$, determine i_O,i_{E1}, i_{E2}, i_{B1}, i_{B2}, and i_I.
   c. Using the results of part (b), determine the current gain of the output stage.
3) Consider the class-AB MOSFET output stage, shown in Figure 2a. The circuit parameters are $I_{Bias} = 0.2mA$, $R_L = 1k\Omega$. The transistor parameters are $V_{TH,n} = 0.8V$, $k_n' = 100\mu A/V^2$, $V_{TH,p} = -0.8V$, $k_p' = 40\mu A/V^2$. For the quiescent condition, assume $V_{GS,3} = V_{SG,4}$ and $V_{GS,1} = V_{GS,2}$. Assume $\lambda = 0$ for all transistors.
   a. If $V_i = -1.5V$, $V_O = 0V$, and $i_{D1} = i_{D2} = 0.5mA$, determine the W/L ratio of each transistor.
   b. Assuming a voltage drop across I_{Bias} of 0.2 V and $V_i = -1.5V$, find the maximum and minimum limits of V_O.
4) Using SPICE, plot the input/output characteristic of the circuit shown in Figure 2b for −2 V < V_{in} < +2 V. Also, plot the output waveform for an input sinusoid having a peak amplitude of 2 V. How do these results change if the load resistance is raised to 16 Ω? Use 2N2222 npn and 2N2907 pnp transistors in LTSpice.

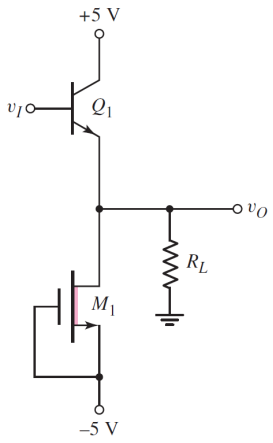

Fig 1a. The figure of Question 1

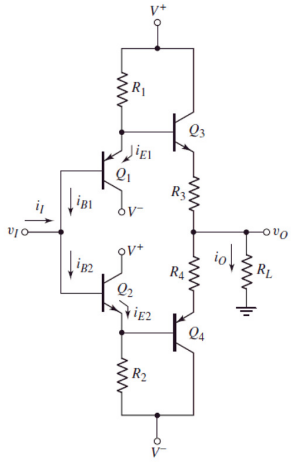

Fig 1b. The figure of Question 2

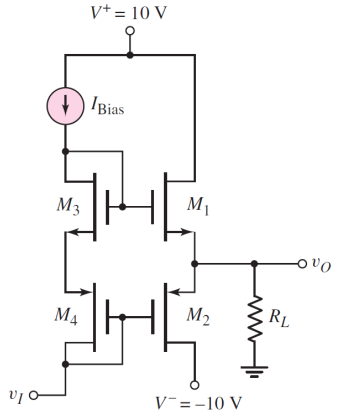

Fig 2a. The figure of Question 3

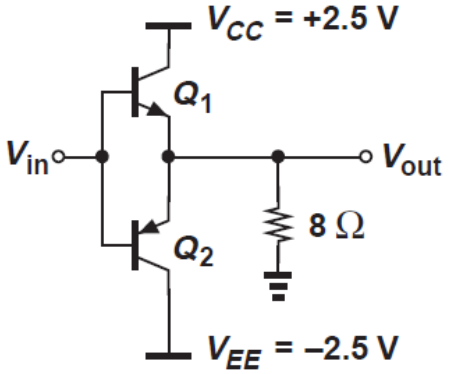

Fig 2b. The figure of Question 4