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EHB342E LOGIC DESIGN LABORATORY
Final Exam

- Students will solve the final exam version corresponding to their last digit of their ITU Student ID Number as explained below:
  - last digit of Student ID Number **0** → Final Exam Version **0**
  - last digit of Student ID Number **1** → Final Exam Version **1**
  - last digit of Student ID Number **2** → Final Exam Version **2**
  - last digit of Student ID Number **3** → Final Exam Version **3**
  - last digit of Student ID Number **4** → Final Exam Version **4**
  - last digit of Student ID Number **5** → Final Exam Version **5**
  - last digit of Student ID Number **6** → Final Exam Version **6**
  - last digit of Student ID Number **7** → Final Exam Version **7**
  - last digit of Student ID Number **8** → Final Exam Version **8**
  - last digit of Student ID Number **9** → Final Exam Version **9**

- If a student submit solutions for a wrong final exam version based on the last digit of the Student ID Number, his/her final exam will be invalid.
- The exam is open-book and open-lecture notes. Exams are exclusive to students and they are expected to work on the solutions on their own.
- The students are expected to abide with the ITU Honor Code http://www.sis.itu.edu.tr/tr/yonetmelik/AkademikOnurSozuEsaslar.html
- Solutions in PDF format are required to be uploaded to the Ninova system before the exam period ended. There will not be extra time for uploading the solutions.
- Each question should be solved on a different page, each page of the solution papers has to be numbered and should have name, last name and Student ID number on top right corner.
- The lecturer will open a Zoom session at the beginning of the exam for announcements and questions about the exam. The Zoom session will end at the end of exam period.
- By uploading the solutions, students here confirm that they have understood the instructions and will act accordingly.

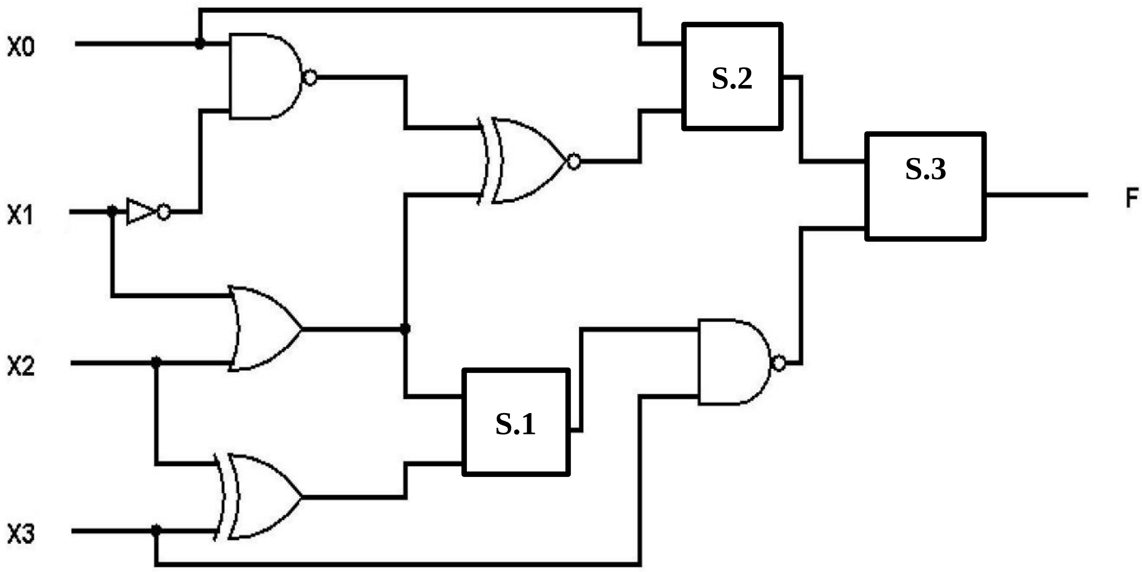
FINAL EXAM 0
This final exam will be solved by only the students with a Student ID number ending with 0.

Experiment 1

Use the gates mentioned in the following table for the square boxes shown in the following figure.

S.1	**S.2**	**S.3**
EXOR	OR	EXNOR

a) Find the **truth table** of circuit.
b) Find the **minimal sum of product representation of the output function F** of the circuit.



Experiment 2

a) Find the minimal sum of product representation of the Boolean functions of the outputs x and y given in the following truth table by using Karnaugh Maps.
b) Draw the circuits using minimum number of gates

a	b	c	d	x	y
0	0	0	0	1	1
0	0	0	1	0	1
0	0	1	0	1	X
0	0	1	1	0	0
0	1	0	0	X	X
0	1	0	1	1	1
0	1	1	0	X	0
0	1	1	1	0	0
1	0	0	0	X	X
1	0	0	1	0	1
1	0	1	0	1	1
1	0	1	1	0	X
1	1	0	0	X	1
1	1	0	1	1	1
1	1	1	0	X	0
1	1	1	1	0	X

Experiment 3

Draw the schematic diagram of circuit which realizes function **F=x′y′z′+xy** by using **3 input active-0 output DECODER** and necessary **AND**, **OR**, **EXOR** and **NOT** gates.

Experiment 4

a) Find the optimum sum of product representation of the Boolean functions for the carry, C and sum, S outputs of a half adder (HA) which is used for adding 2 1-bit numbers and defined by the following truth table.
b) Draw the HA circuit by using the optimal Boolean function that you found in (a).
c) Draw the circuit for a Full Adder (FA) which is used for adding 3 1-bit numbers by using the HA from (b) and neccesary other logic gates.

A	B	C	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Experiment 5

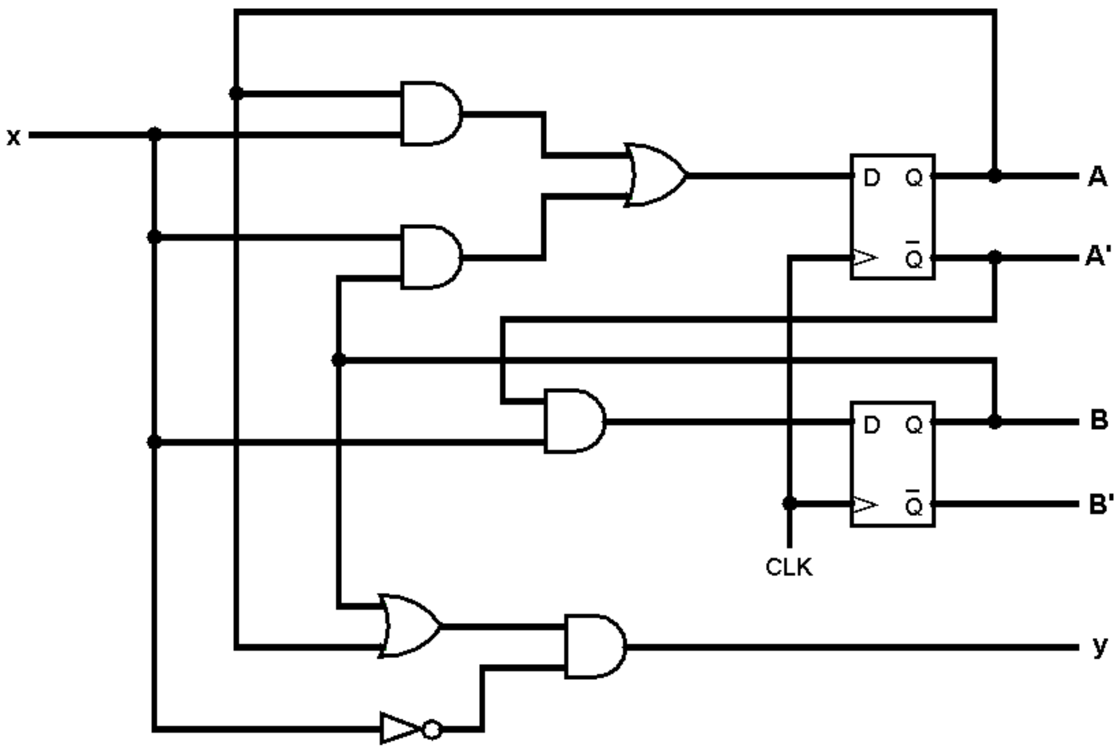


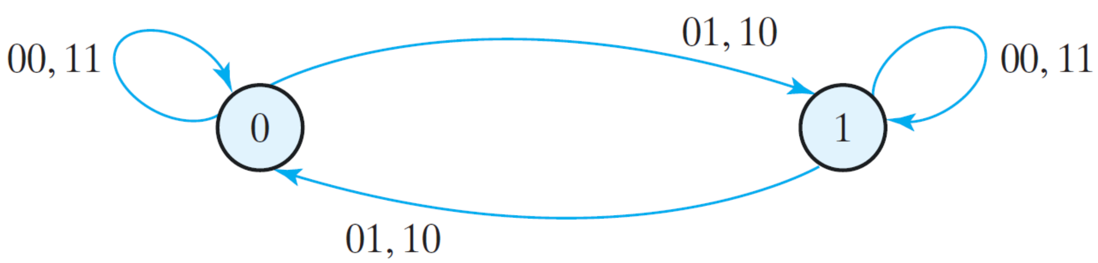
Figure 1

a) Determine the flip-flop input (D1, D2) and output (y) functions that given in Figure 1.
b) Find the state equations by using D-type flip-flop's characteristic equations.
c) Fill the state transition table of the circuit.

Experiment 6

We wish to design a synchronous sequential circuit whose state diagram is shown below. You will use JK-type flip-flops in your design.

a) Encode the states
b) Obtain the state transition table
c) Draw the circuit



Experiment 7

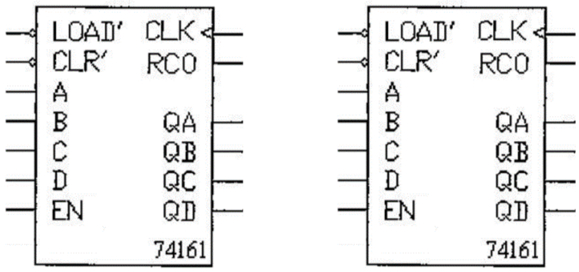


Figure 2

a) Design a 9 to 99 counter by using two 74161 IC (synchronous counter) as shown in the figure. You are allowed to use all the logic gates.
b) Explain the circuit operation briefly.