EHB 335E HW#3

Due: 22 November 2020 @ 22 o'clock – **No late homework will be accepted.**

1) In the circuit below left, the input is applied to the gate of M_1, and the output is taken from the source of M_1. By using the open-circuit time constants method, find an expression for the upper corner (–3 dB) frequency. Assume that the input source has a resistance R_{sig}, and the output is loaded with R_L. Consider C_{GS}, C_{GD}, C_{DB}, and C_{SB}, as well as, $\lambda > 0$ for both transistors.

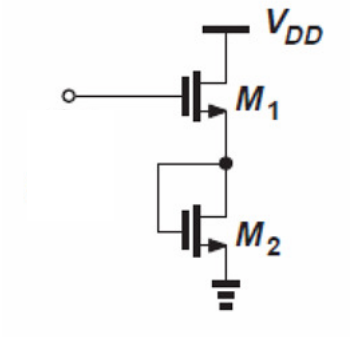

Figure of Question 1

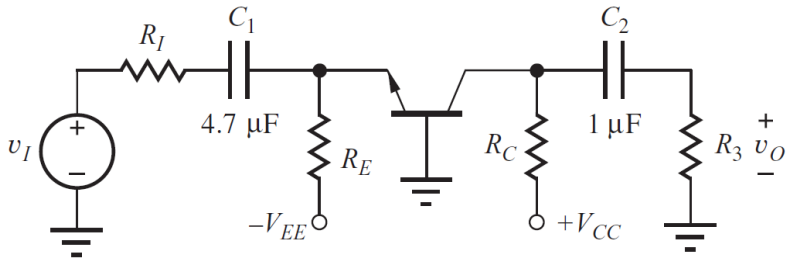

Figure of Question 2

2) Consider the common-base amplifier in the figure above right. Assuming $V_A < \infty$, and neglecting C_1 and C_2, which are coupling capacitors, determine an expression for the upper corner (–3 dB) frequency by using the open-circuit time constants method.

3) Consider the cascade amplifier shown in the figure below left. By using the Miller's theorem, find expressions for the poles of the circuit. Consider C_{GS}, C_{GD}, C_{DB}, and C_{SB}, as well as, $\lambda > 0$ for both transistors. For simplicity, you can assume $1/g_{m2} \ll r_{o2}$.

4) In the two-stage amplifier shown below right, W / L = 10 µm / 0.18 µm for M_{10}-M_{13}. This is a simulation problem, so there is no need for hand calculations.
(a) Select the input DC level for M_{13} to obtain an output dc level of 0.74 V.
(b) Simulate the frequency response. Highlight the low-frequency gain and the –3 dB bandwidth in the plots.

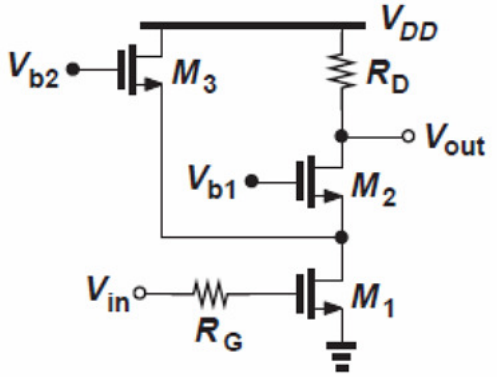

Figure of Question 3

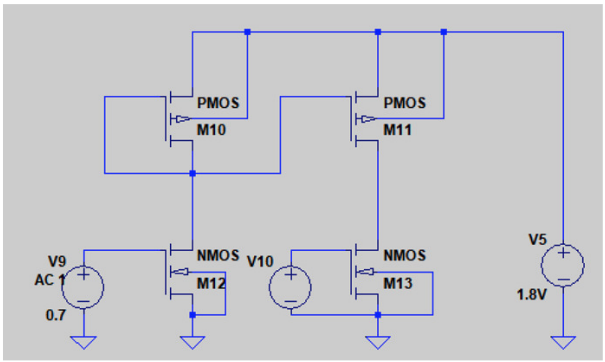

Figure of Question 4

For this HW, you will use the following NMOS and PMOS models. You can import them into LTSpice or your favorite SPICE simulator. One helpful link regarding LTSpice is provided below.

Models: http://ptm.asu.edu/modelcard/180nm_bulk.txt

Incorporation of the models into LTSPICE: http://www.linear.com/solutions/1083