

Due: 3 December 2018 @17:00 – **No late homework will be accepted.**

- 1) Determine the polarity of the feedback for the amplifier in Fig 1a. Clearly explain your reasoning.
- 2) An amplifier has a dc gain of  $10^4$  and poles at  $10^5$  Hz,  $3.16 \times 10^5$  Hz, and  $10^6$  Hz. Find the value of  $\beta$ , and the corresponding closed-loop gain, for which a phase margin of  $45^\circ$  is obtained.

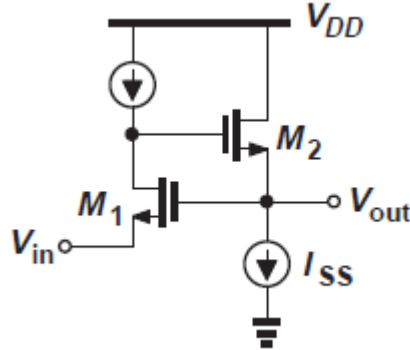


Fig 1a. Figure of Question 1

- 3) Assuming  $V_A = \infty$ , determine the closed-loop gain and I/O impedances of the amplifier in Fig 2a. The output resistance is defined as the resistance looking into the collector of  $Q_3$ .

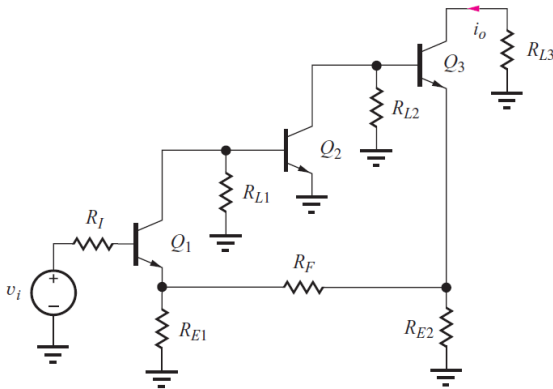


Fig 2a. Figure of Question 3

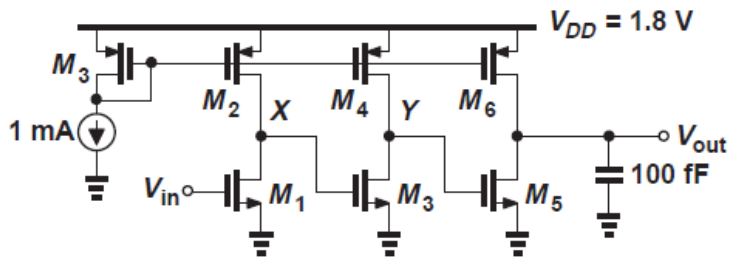


Fig 2b. Figure of Question 4

- 4) In the three-stage amplifier of Fig 2b., all transistors except  $M_1$  and  $M_5$  have  $W/L = 20 \mu\text{m} / 0.18 \mu\text{m}$ . For  $M_1$  use  $W/L = 42 \mu\text{m} / 0.18 \mu\text{m}$  and for  $M_5$  use  $W/L = 10 \mu\text{m} / 0.18 \mu\text{m}$ . Employ the transistor models provided in the last homework for Spice simulations. Assume a DC input level of 0.55 V.
  - a. Determine the phase margin.
  - b. Place a capacitor between nodes X and Y so as to obtain a phase margin of 55 degrees. What is the unity-gain bandwidth under this condition?
  - c. Repeat (b) if the compensation capacitor is tied between X and ground and compare the results.