## Due: 14 November 2018 @9:00 am – No late homework will be accepted.

- 1) Consider the BiCMOS follower circuit shown in Figure 1a. The BJT transistor parameters are  $V_{BE,on}=0.7V$ ,  $V_{CE,sat}=0.2V$ ,  $V_A=\infty$ , and the depletion mode n-MOSFET parameters are  $V_{TH}=-1.8V$ ,  $k_n=12mA/V^2$ ,  $\lambda=0$  (You can treat depletion mode MOSFETS as regular MOSFETS).
  - a. Determine the maximum and minimum values of output voltage and the corresponding input voltages for the circuit to operate in the linear region (i.e. Class-A operation) for (a)  $R_L=\infty$  and (b)  $R_L=500\Omega$ .
  - b. What is the smallest value of  $R_L$  possible if a 2 V peak sine wave is produced at the output?
  - c. What is the corresponding power conversion efficiency?
- 2) Consider the class-AB output stage in Figure 1b. The diodes and transistors are matched, with parameters  $I_S = 6 \times 10^{-12} A$ , and  $\beta = 40$ .
  - a. Determine  $R_1$  such that the minimum current in the diodes is 25 mA when  $V_0=24V$ . Find  $i_N$  and  $i_P$  for this condition.
  - b. Using the results of part (a), determine the diode and transistor currents when  $V_0 = 0$ .
- 3) Consider the class-AB MOSFET output stage shown in Figure 2a. The circuit parameters are  $I_{Bias}=0.2mA$ ,  $R_L=1k\Omega$ . The transistor parameters are  $V_{TH,n}=0.8V$ ,  $k_n=100\mu A/V^2$ ,  $V_{TH,p}=-0.8V$ ,  $k_p=40\mu A/V^2$ . For the quiescent condition, assume  $V_{GS,3}=V_{SG,4}$  and  $V_{GS,1}=V_{GS,2}$ . Assume  $\lambda=0$  for all transistors.
  - a. If  $V_i = -1.5V$ ,  $V_O = 0V$ , and  $i_{D1} = i_{D2} = 0.5mA$ , determine the W/L ratio of each transistor.
  - b. Assuming a voltage drop across  $I_{Bias}$  of 0.2 V and no voltage drop across  $V_i$ , find the maximum and minimum limits of  $V_O$ .
- 4) Using SPICE, plot the input/output characteristic of the circuit shown in Figure 2b for  $-2 \text{ V} < V_{in} < +2 \text{ V}$ . Also, plot the output waveform for an input sinusoid having a peak amplitude of 2 V. How are these results changed if the load resistance is raised to 16  $\Omega$ ? Use 2N2222 npn transistor in LTSpice.

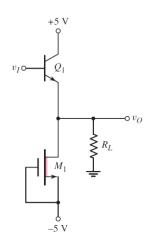


Fig 1a. Figure of Question 1

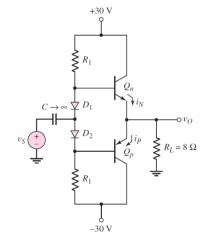


Fig 1b. Figure of Question 2

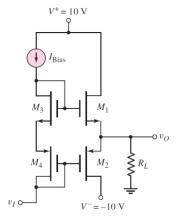


Fig 2a. Figure of Question 3

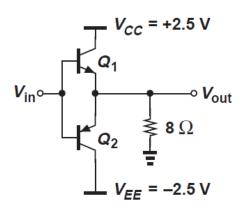


Fig 2b. Figure of Question 4