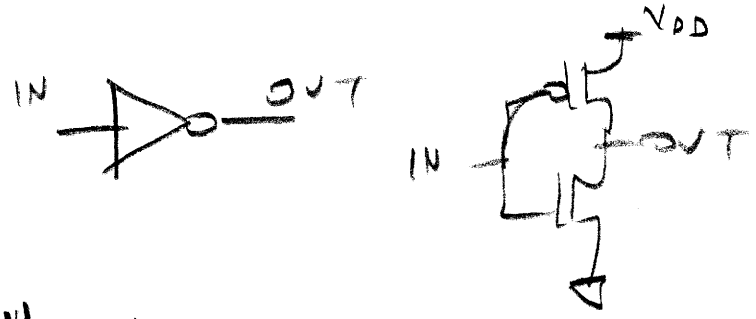
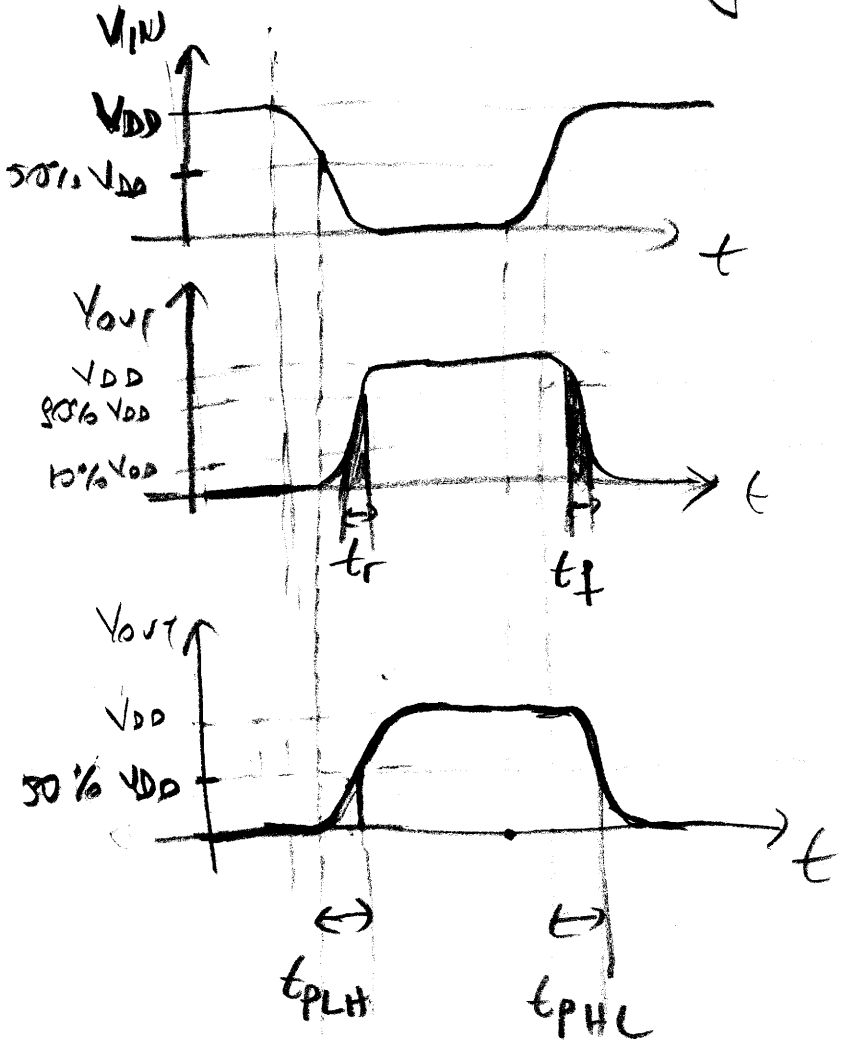
EHB 322E Digital Electronic Circuits

SPRING 2015

Delay in CMOS Inverters





t_r : rise time

t_f : fall time

$$t_p = \frac{t_{PLH} + t_{PHL}}{2}$$

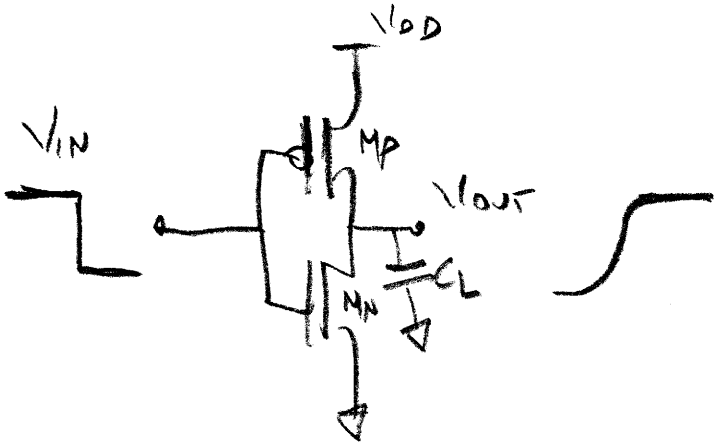
t_p : Average propagation delay

t_{PLH} : Propagation delay when the output switches from low to high

t_{PHL} : Propagation delay when the output switches from high to low

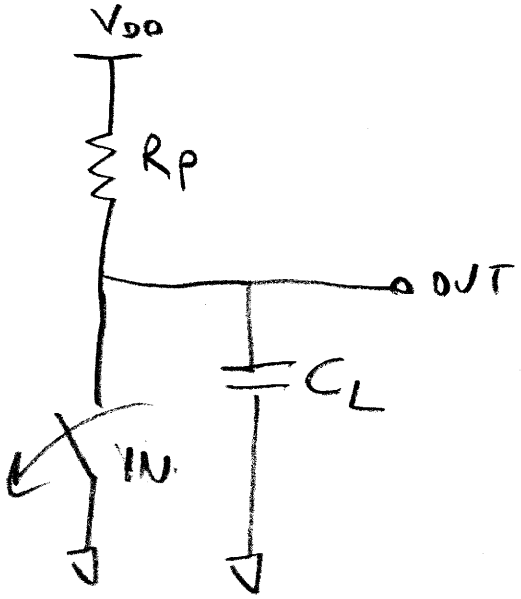
Calculating Propagation Delays

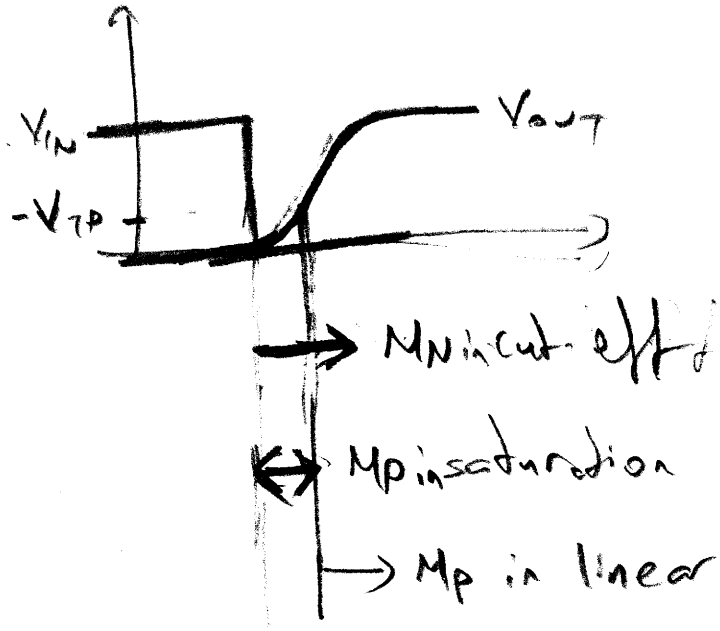
① t_{PLH} : output is charging



C_L is the equivalent output capacitor.

Charging Model





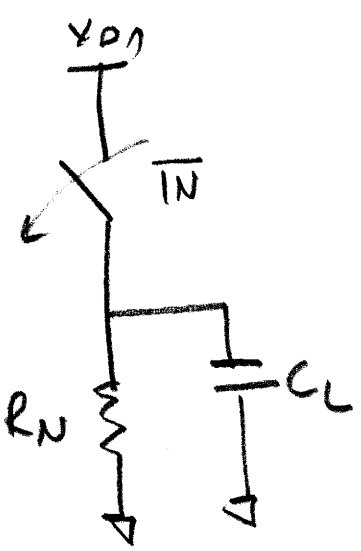
- Pull-up network (M_P) is modeled as a resistor (I_{DP}-V_{DSP} relation is not linear)
- Pull-down network (M_N) is modeled as open switch

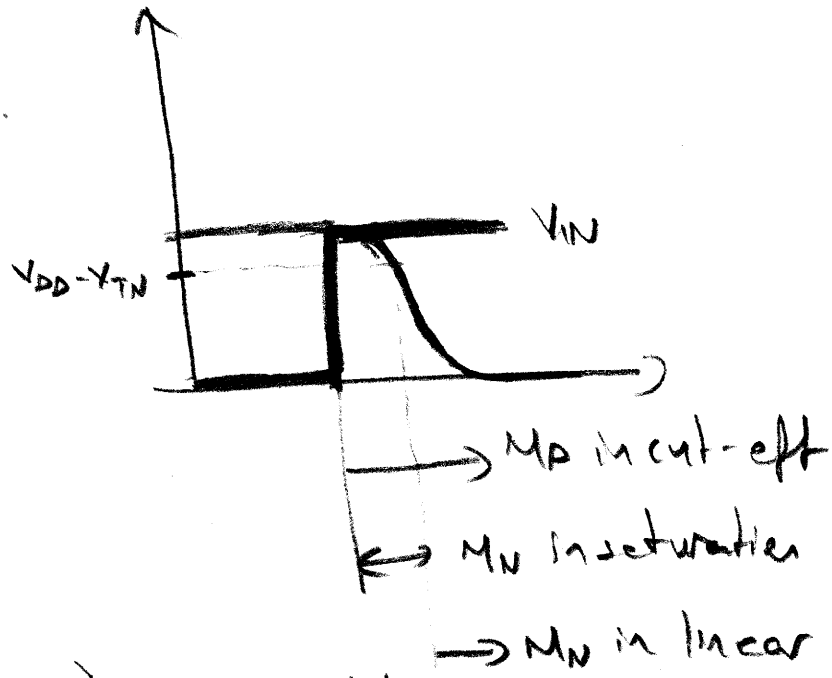
$$t_{PLH} = -\ln(1-0,5)\, R_P C_L = 0,69\, R_P C_L$$

50% of output

② t_{PHL} : output is discharging

Discharging Model





- Pull-up network (M_P) is modeled as an open switch
- Pull-down network (M_N) is modeled as a resistor

$$t_{PHL} = -\ln(1-0,5) R_N C_L = 0,69 R_N C_L$$

How to decrease t_{PHL} and t_{PLH}?

① $W_N \uparrow$ $\frac{\Delta V_{DSN}}{\Delta I_{DN}} \downarrow$ $R_N \downarrow$ $(\propto \frac{1}{W})$ $C_{GDN} \uparrow$ $(\propto W)$ $C_L \uparrow$ $(C_{Dot..})$ $t_{PHL} \downarrow$

② $W_P \uparrow$ $\frac{\Delta V_{DSP}}{\Delta I_{DP}} \downarrow$ $R_P \downarrow$ $C_{GDP} \uparrow$ $C_L \uparrow$ $t_{PLH} \downarrow$

③ $V_{DD} \uparrow$ $R_N \downarrow$ $R_P \downarrow$ Power $\uparrow$ $t_{PLH} \downarrow$ $t_{PHL} \downarrow$

$I_{DS} \propto (V_{DD})^2$ in sat.

$$R_N = \frac{1}{2K_N \ln 2} \frac{1}{V_{DD} - V_{TN}} \left(\frac{2V_{TN}}{V_{DD} - V_{TN}} + \ln \frac{3V_{DD} - 4V_{TN}}{V_{DD}} \right)$$

$$R_P = \frac{1}{2K_P \ln 2} \frac{1}{V_{DD} + V_{TP}} \left(\frac{-2V_{TP}}{V_{DD} + V_{TP}} + \ln \frac{3V_{DD} + 4V_{TP}}{V_{DD}} \right)$$

$V_{TN} > 0$
$V_{TP} < 0$

$$K_N = \frac{1}{2} \mu_n C_{ox} \frac{W_N}{L_N}$$

$$K_P = \frac{1}{2} \mu_P C_{ox} \frac{W_P}{L_P}$$

$t_{PHL} = \ln 2 \, R_N C_L$ only depend on NMOS parameters

$t_{PLH} = \ln 2 \, R_P C_P$ only depend on PMOS parameters

Ex / $R_N = \frac{30k\Omega}{(W/L)_N}$ and $R_P = \frac{80k\Omega}{(W/L)_P}$ are given.

If $C_L = 6\,fF$, and $t_{PHL} < 40ps$ and

$t_{PLH} < 40ps$

desired, determine the minimum $\left(\frac{W}{L}\right)$ ratios.

$$t_{PHL} = 0{,}69 \left(\frac{30k}{(W/L)_N} \right) \cdot 6\,10^{-15} = 40\,10^{-12}$$

$$\left(\frac{W}{L}\right)_N = 3{,}1 \rightarrow \underline{4}$$

$$t_{PLH} = 0{,}69 \left(\frac{80k}{(W/L)_P} \right) \cdot 6\,10^{-15} = 40\,10^{-12} \Rightarrow$$

$$\left(\frac{W}{L}\right)_P = 8{,}28 \rightarrow \underline{9}$$

$$t_{PHL} = \frac{C_L L_N}{\mu_n C_{ox} W_N} M_N \qquad t_{PLH} = \frac{C_L L_P}{\mu_P C_{ox} W_P} M_P$$

$$M_N = f(V_{DD}, V_{TN}) \qquad M_P = f(V_{DD}, V_{TP})$$

independent of W and L

$$t_{PHL} = \frac{C_L}{C_N} \tau_N \quad (\text{eq.}) \qquad C_N = C_{ox} W_N L_N$$

$$t_{PLH} = \frac{C_L}{C_P} \tau_P \qquad C_P = C_{ox} W_P L_P$$

$C_N + C_P \cong C_{in}$ of an inverter

$$\tau_N = M_N \frac{L_N^2}{\mu_n} \qquad \tau_P = M_P \frac{L_P^2}{\mu_P}$$

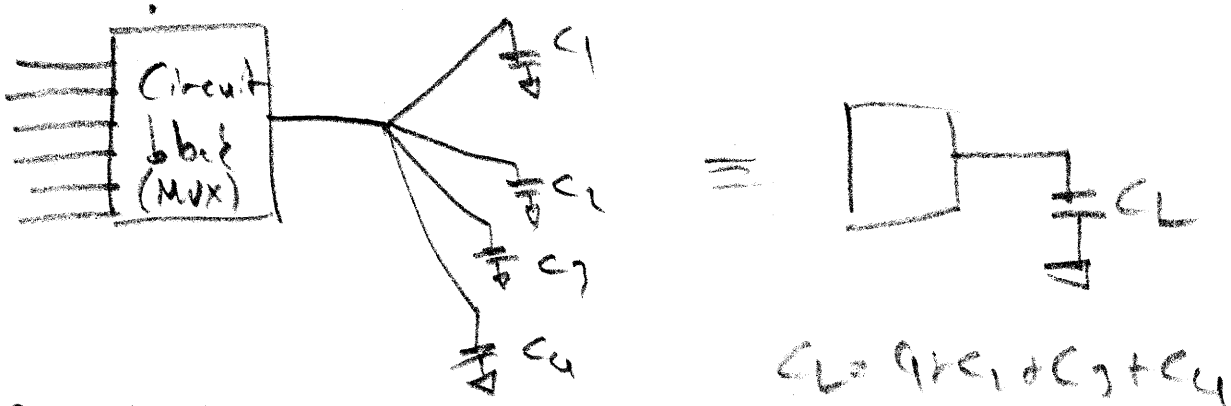
constant for a certain technology

$(L_{min} = L_N = L_P)$

Chain Inverters

Purpose: to drive large capacitors

- Consider a circuit block (MUX) supposed to drive a large load capacitor.



Fan-in (6)

Fan-out (4)

Fan-out ↑ C_L ↑ Delay ↑

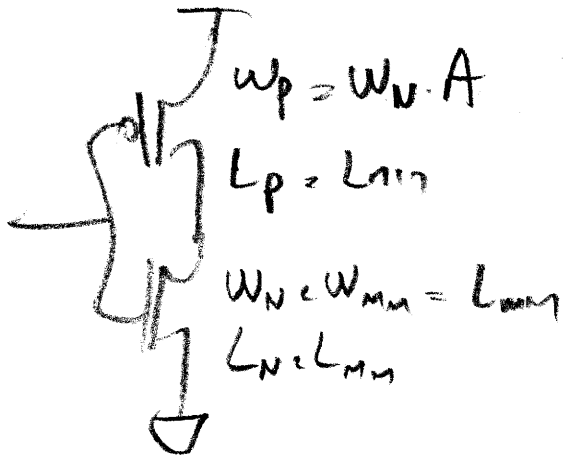
- Supposed that the block has equivalent resistors

$$R_{N\text{-}eq} = R_{P\text{-}eq} = R_{N\text{-}inv\ (min\ size)} = R_{P\text{-}inv\ (min\ size)}$$

$$\Downarrow$$

$$C_{N\text{-}eq} = C_{P\text{-}inv} \qquad C_{P\text{-}eq} = C_{P\text{-}inv}$$

MM size inverter ($R_N = R_P$)



$$A = \frac{\tau_P}{\tau_N}$$

$$t_{PHL} = \frac{C_L}{C_N}\tau_N \,, \quad C_N = W_N L C_{ox}$$

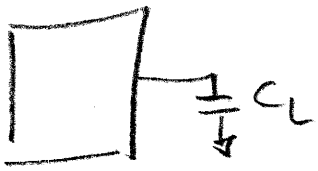
$$t_{PLH} = \frac{C_L}{C_P}\tau_P \,, \quad C_P = A W_N L C_{ox}$$

$$\Rightarrow \boxed{C_P = A \cdot C_N}$$

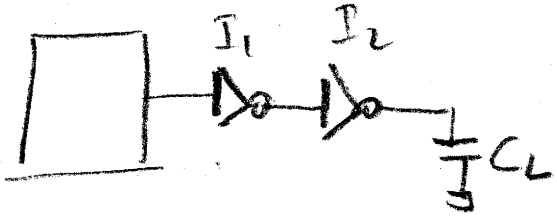
$$t_{PHL} = t_{PLH}$$

Ex $C_L = 30\,fF$ $\quad C_{N-eq} = 1\,fF$ $\quad \tau_N = 1\,ns$

$A = 2$ $\quad C_{P-eq} = 2\,fF$ $\quad \tau_P = 2\,ns$

a) 

find t_{PHL} and t_{PLH}

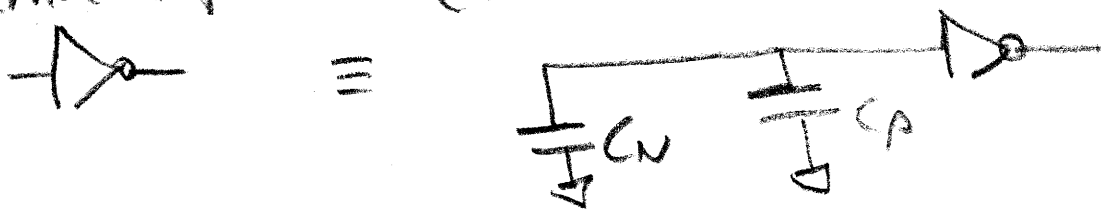
b) 

find t_{PHL} and t_{PLH}

$W_{N1} = L_{min}$ $\quad W_{N2} = 3W_{N1}$

$W_{P1} = A \cdot L_{min}$ $\quad W_{P2} = 3A\,W_{N1}$

- Suppose that inverters have only input internal capacitors (no output internal capacitor)



$C_N = W_N L C_{ox}$ $C_P = W_P L C_{ox}$

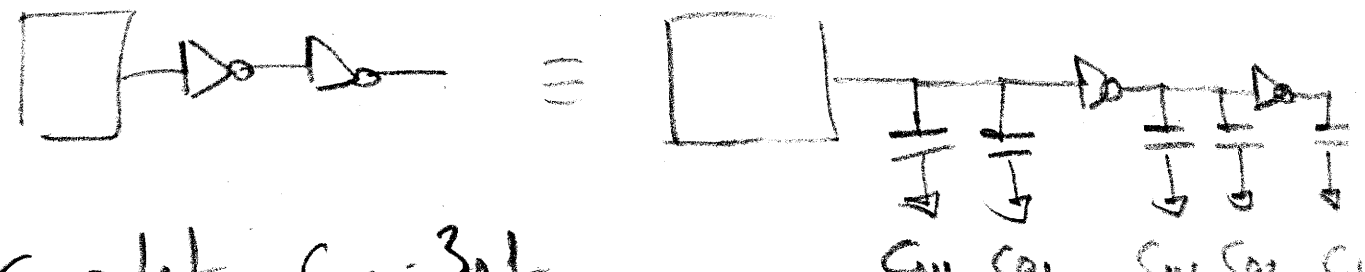
- Suppose that the block has no output internal capacitors

a) $t_{PHL} = \frac{C_L}{C_N} \tau_N = \frac{30}{1} 1_n = 30 n s$

$t_{PLH} = \frac{C_L}{C_P} \tau_P = \frac{30}{2} 2_n = 30 n s$

b) $t_{PHL} = t_{PHL-2} + t_{PLH-1} + t_{PHL-Block}$

$t_{PLH} = t'_{PLH-2} + t_{PHL-1} + t_{PLH-Block}$



$C_{N1} = 1nf$ $C_{N2} = 3nf$

$C_{P1} = 2nf$ $C_{P2} = 6nf$

$$t_{PHL-2} = \frac{C_L}{C_{N-2}} \tau_N = \frac{30}{3} 1_n = 10_n$$

$$t_{PLH-1} = \frac{C_{N2} + C_{P2}}{C_{P1}} \tau_P = \frac{9}{2} 2_n = 9_n$$

$$t_{PLH-Block2} = \frac{C_{N1} + C_{P1}}{C_{N-eq}} \tau_N = \frac{3}{1} \cdot 1_n = 3_n$$

$$t_{PHL} = 22_{ns}$$

$$t_{PLH-2} = \frac{30}{6} \cdot 2 = 10_n$$

$$t_{PHL-1} = \frac{9}{1} 1 = 9_n$$

$$t_{PLH-Block2} = \frac{3}{2} \cdot 2 = 3_n$$

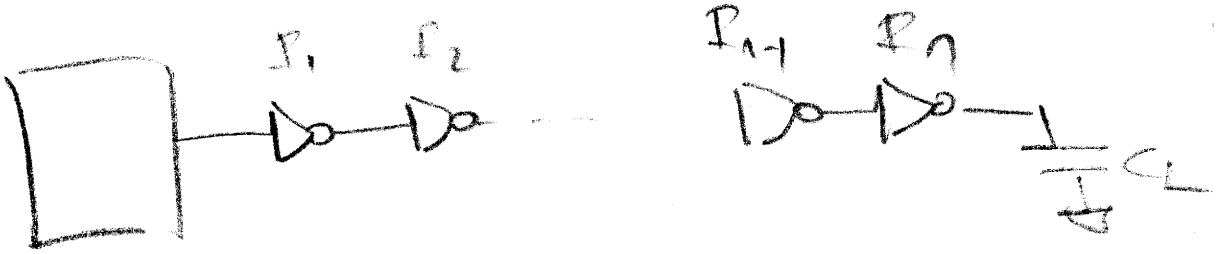
$$t_{PLH} = 22_{ns}$$

Adding two inverters make the delay 22ns from 30ns

8ns (≈30%) improvement

How to select the sizes and the number of inverters?

How to optimize $t_p = \frac{t_{pHL} + t_{pLH}}{2}$

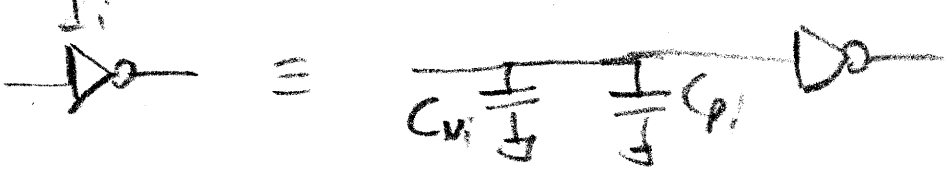


$$A = \frac{W_{P,i}}{W_{N,i}} = \frac{\tau_p}{C_N} \qquad 1 \leq i \leq n$$

$$\beta = \frac{W_{P,i+1}}{W_{P,i}} = \frac{W_{N,i+1}}{W_{N,i}}$$

$W_{N1} = L_{min} = L_{N1}$ $\quad W_{N2} = \beta L_{min}$ $\quad \dots$ $\quad W_{Nn} = \beta^{(n-1)} L_{min}$

$W_{P1} = A \cdot L_{min}$ $\quad W_{P2} = A \beta L_{min}$ $\quad W_{Pn} = A \cdot \beta^{(n-1)} L_{min}$



no internal output capacitors

block equivalent caps

$$C_{N-eq} = C_{N1}$$

$$C_{p-eq} = C_{p1}$$

$$C_{p1} = A \cdot C_{N1} \qquad C_{p2} = A \cdot B C_{N1} \qquad \dots \qquad C_{pn} = A B^{(n-1)} C_{N1}$$

$$C_{N1} \qquad C_{N2} = B \cdot C_{N1} \qquad \dots \qquad C_{Nn} = B^{(n-1)} C_{N1}$$

$$C_L = C_{pnH} + C_{NnH} = (A+1) B^n C_{N1} \Rightarrow B = \sqrt[n]{\frac{C_L}{C_{IN}}} \rightarrow C_{p1} + C_{N1}$$

$$t_{pHL} = t_{pLH} = t_{pBlock} + t_{p1} + t_{p2} + \dots + t_{pn}$$

$$t_p = t_{pHL} = t_{pLH} = \frac{C_L}{C_N} \tau_N = \frac{C_L}{C_p} \tau_p$$

$$t_{pBlock} = \frac{C_{N1} + C_{p1}}{C_{N-eq}} \tau_N = (A+1) \tau_N$$

$$t_{p1} = \frac{C_{N2} + C_{p2}}{C_{N1}} \tau_N = (A+1) B \tau_N$$

$$t_{p2} = \frac{C_{N3} + C_{p3}}{C_{N2}} \tau_N = (A+1) B \tau_N$$

$$t_{p(n-1)} = \qquad = (A+1) B \tau_N$$

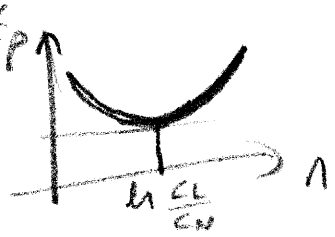
$$t_{pn} = \frac{C_L}{C_{Nn}} \tau_N = (A+1) B \tau_N$$

$$t_p = (A+1)\tau_N + (A+1)\cdot B\tau_N \cdot N$$

$$t_p = (A+1)\tau_N + (A+1)\left(\frac{C_L}{C_{IN}}\right)^{1/N} \cdot N$$

$$\frac{dt_p}{dN} = \left(\frac{C_L}{C_{IN}}\right)^{1/N} + \left(\frac{C_L}{C_{IN}}\right)^{1/N} \ln\left(\frac{C_L}{C_{IN}}\right)\frac{-1}{N^2}\cdot N$$

$$\frac{dt_p}{dN} = 0 \Rightarrow 1 - \ln\left(\frac{C_L}{C_{IN}}\right)/N = 0$$



$$\Rightarrow N = \ln\left(\frac{C_L}{C_{IN}}\right)$$

$$\Rightarrow B = \left(\frac{C_L}{C_{IN}}\right)^{\left(\frac{1}{\ln\left(\frac{C_L}{C_{IN}}\right)}\right)}$$

Reminder

$$\frac{d}{dx}(a^v) = a^v(\ln a)\left(\frac{dv}{dx}\right)$$

How to design an inverter chain?

Step by Step

1) Determine $\underline{\underline{A}}$ to make $t_{PHL} = t_{PLH}$ for each block, gate, or inverter

2) Determine $N = \ln\left(\frac{C_L}{C_{IN}}\right)$ — round to the nearest odd number if inverter is intended; round to the nearest odd number if buffer is needed

3) Determine $B = \left(\frac{C_L}{C_{IN}}\right)^{1/N(\text{rounded})}$

(or buffer)

Ex Design an inverter chain to invert the block's output.

$t_{PHL} = t_{PLH}$ for inverters. Determine W values of all inverters.

$C_L = 100\,pF$ $\quad C_{IN} = 3\,pF$

$L_{MIN} = 1\mu$ $\quad \mu_n = 2\mu_p$

$W_{min} = 1\mu$ $\quad M_p = 1.5\,M_N$

Remind

$\tau_N = M_N \frac{L_N^2}{\mu_n}$

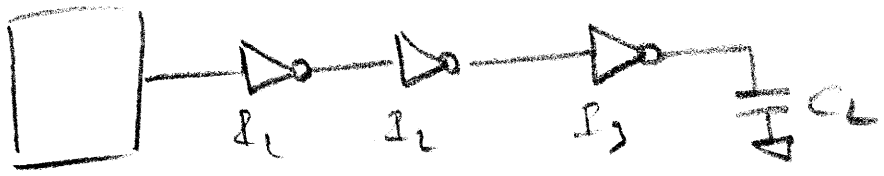
$\tau_p = M_p \frac{L_p^2}{\mu_p}$

In exam, I might want you to calculate τ_N, τ_p

$$A = \frac{\tau_p}{\tau_N} = \frac{M_p}{M_N}\,\frac{\mu_n}{\mu_p} = 1.5 \cdot 2 = 3$$

$$n = \ln(100/3) = 3.5 \xrightarrow{\text{Inverter}} 3$$

$$B = \left(\frac{100}{3}\right)^{1/3} \simeq 3.2$$



$$A = \frac{W_{Pi}}{W_{Ni}} \qquad B = \frac{W_{Ni+1}}{W_{Ni}} = \frac{W_{Pi+1}}{W_{Pi}}$$

$\Rightarrow$ $W_{N1} = L_{MIN} = 1\mu$ $\quad W_{N2} = W_{N1} \cdot B = 3.2\mu$

$W_{P1} = A\,W_{N1} = 3\mu$ $\quad W_{P2} = A\,W_{N2} = 9.6\mu$

$\Rightarrow$ $W_{N3} = W_{N2}\,B = 10.2\mu$

$W_{P3} = A\,W_{N3} = 30.7\mu$