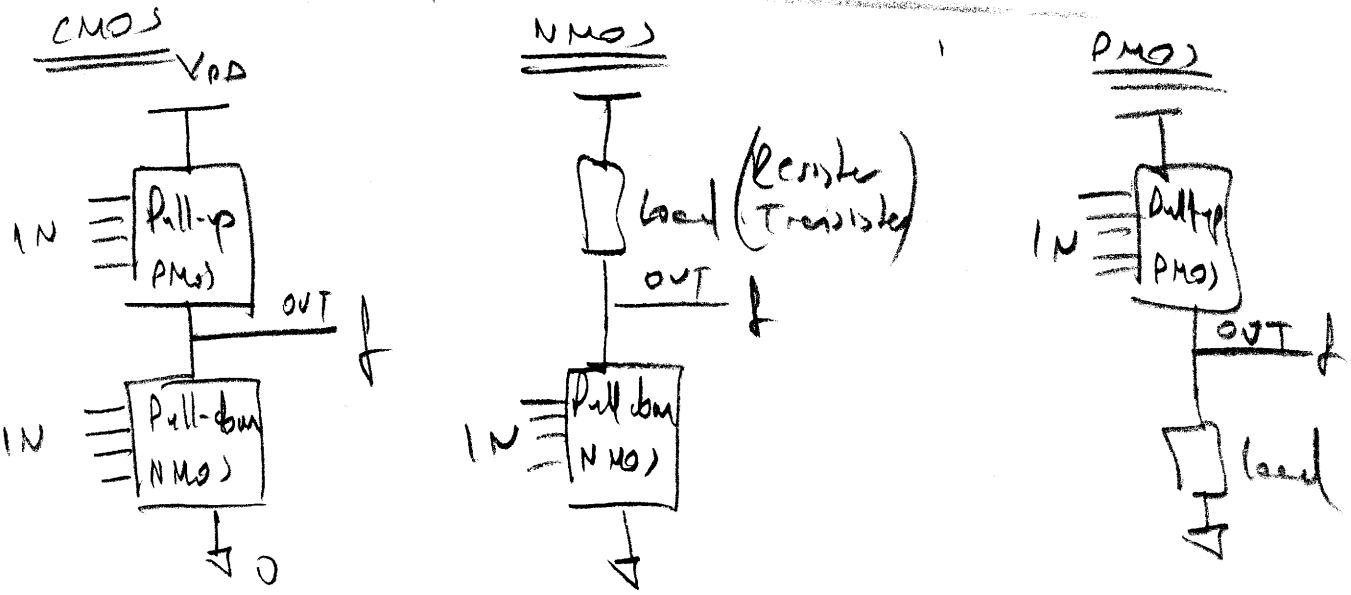
09/03/2015-W6

EHB 322E: Digital Electronic Circuits
Spring 2015

Implementing any Boolean function with NMOS, PMOS, and CMOS circuits

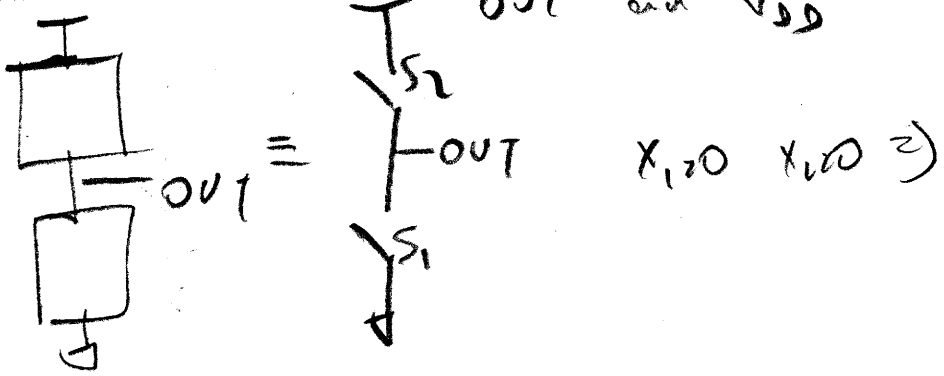


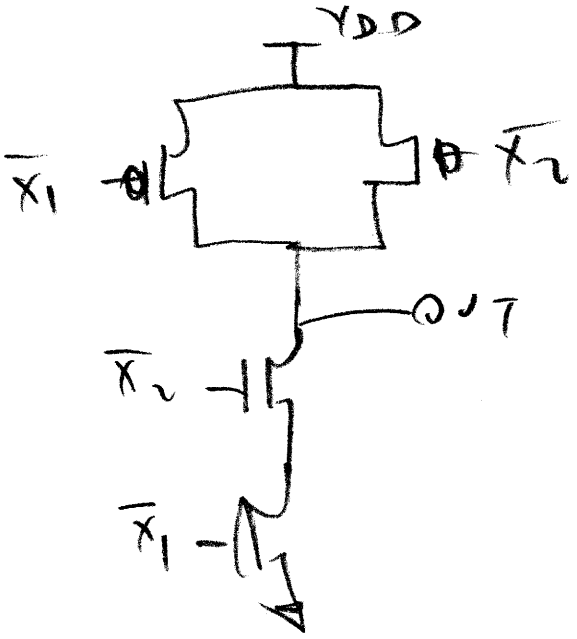
Ex: Implement $f = x_1 + x_2$ with a CMOS circuit

x_1	x_2	f
0	0	0
0	1	1
1	0	1
1	1	1

S_1 is ON S_2 is OFF
→ Pull down is active - closed path between OUT and GND

S_1 is OFF S_2 is ON
→ Pull up is active closed path between OUT and V_{DD}

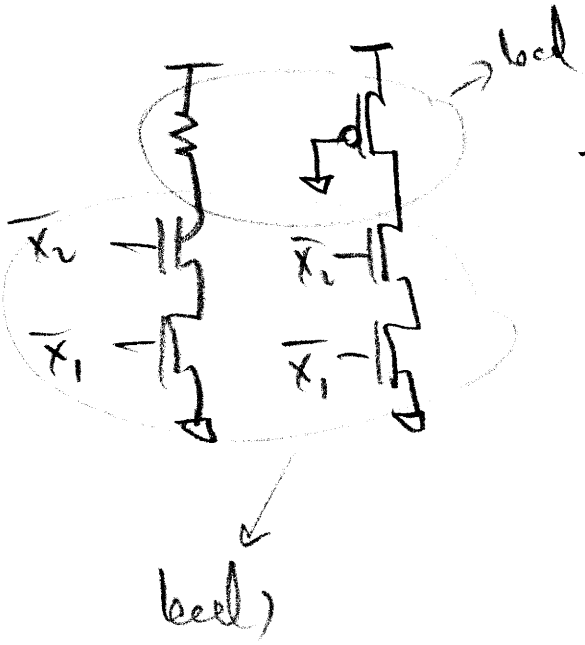




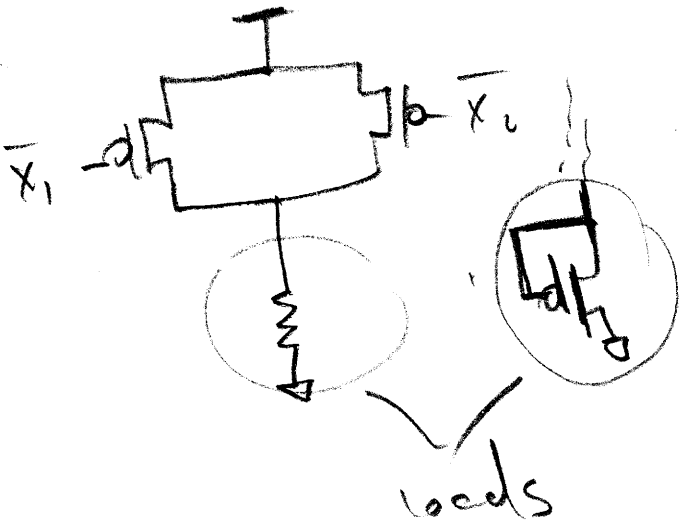
- Use dual circuits for NMOS and PMOS parts
- Use negated inputs
- Use same inputs for NMOS and PMOS parts

Ex: Implement $f = X_1 + X_2$ with NMOS and PMOS transistors

- NMOS



PMOS

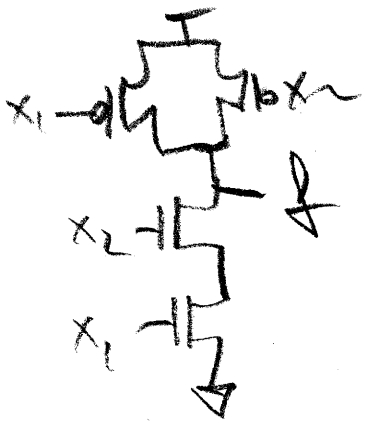


(Universal)

Implementing NAND and NOR gates with CMOS circuits

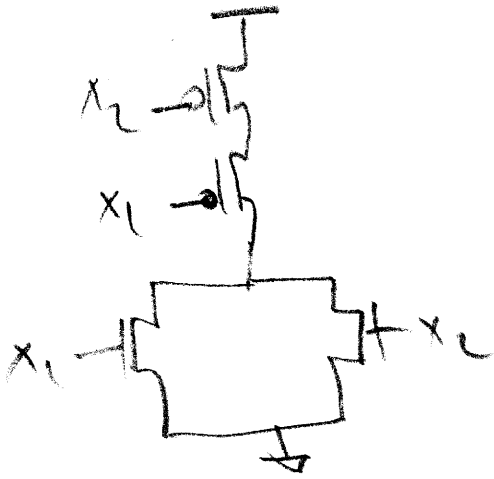
NAND

$f = \overline{x_1 \cdot x_2}$



NOR

$f = \overline{x_1 + x_2}$



Implementing complex gates for any Boolean function with CMOS circuits

Given a Boolean function f

1) Express f in minimal factored form such that the expression has minimal number of literals (literal count)
   - # of literals = # of NMOS transistors
   - = # of PMOS transistors

COST FUNCTION

2) Assign negated form of each literal to an NMOS (PMOS) transistor such that AND operations in the expression correspond to parallel NMOS and (series PMOS)

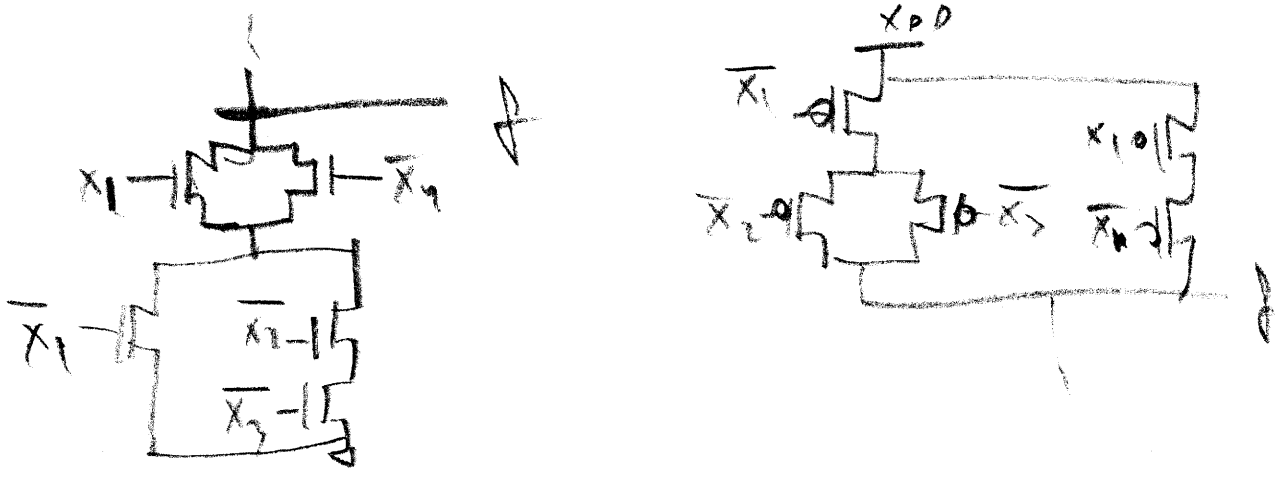
OR operations in the expression correspond to series NMOS transistors (parallel PMOS).

Ex Implement $f = x_1 x_2 + x_1 x_3 + \bar{x}_1 x_4$ a CMOS gate.

1) $f = x_1 (x_2 + x_3) + \bar{x}_1 x_4$ 5 literals

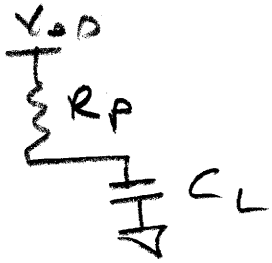
5 NMOS transistors 5 PMOS transistors

2)



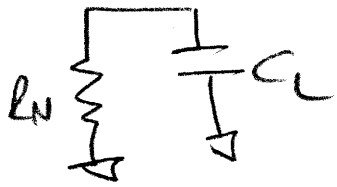
Propagation delay for static CMOS circuits or gates

t_{PLH}



$t_{PLH} = 0{,}69 R_P C_L$

t_{PHL}



$t_{PHL} = 0{,}66 R_N C_L$

- How to obtain R C values?

1.) Model each closed NMOS (PMOS) transistor with its equivalent resistor
   - NMOS is closed if gate voltage is V_{DD}
   - PMOS is closed if gate voltage is 0

2.) Model each open NMOS (PMOS) transistor as an open switch.

3.) For each node calculate the equivalent capacitor

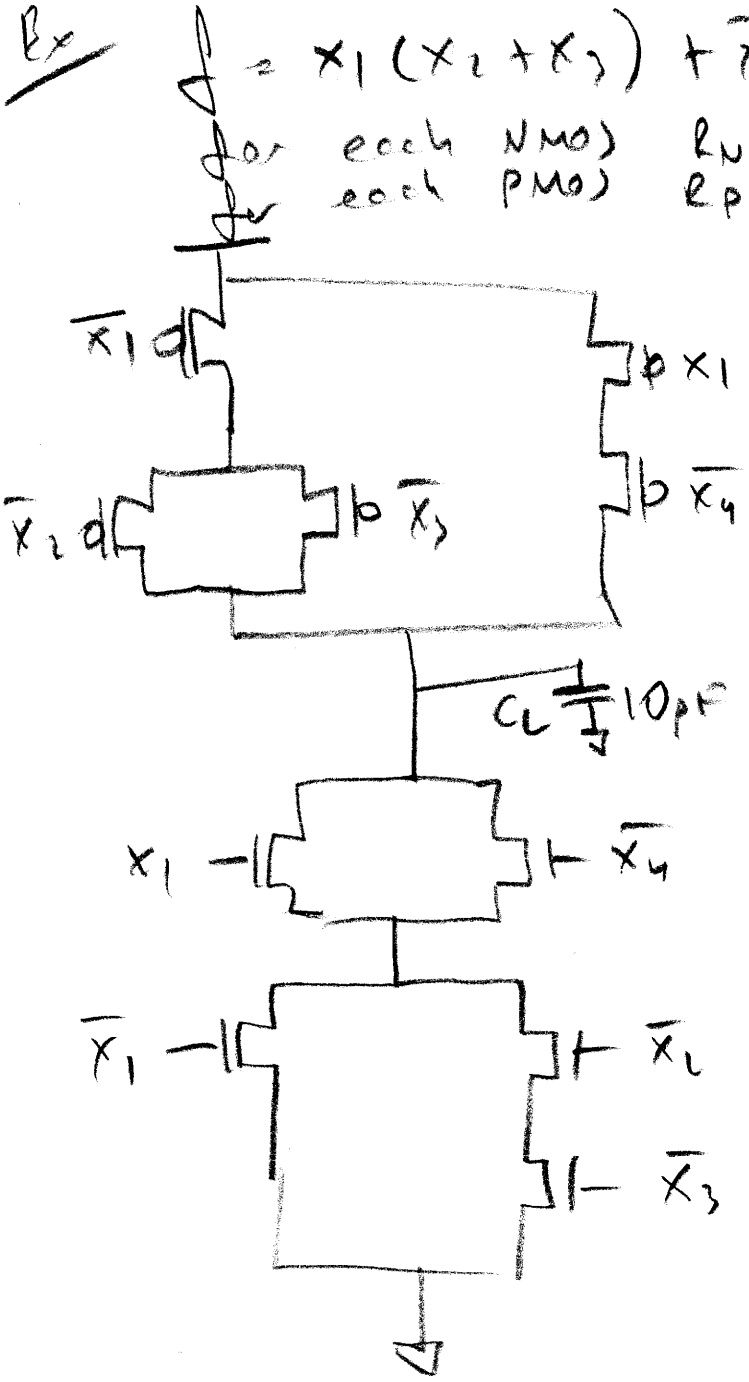
(1) Neglecting internal capacitors (only consider the o-tp-t capacitor)

How to calculate W.C. & B.C delays?

Ex $f = x_1(x_2 + x_3) + \bar{x}_1 x_4$

for each NMOS $R_N = 10k\Omega$
each PMOS $R_P = 20k\Omega$

$C_L = 10pF$



Calculate the delays

a) $x_1 = 0$ ●
$x_2 = 0$ ●
$x_3 = 0$ ●
$x_4 = 0 \to 1$ ↑

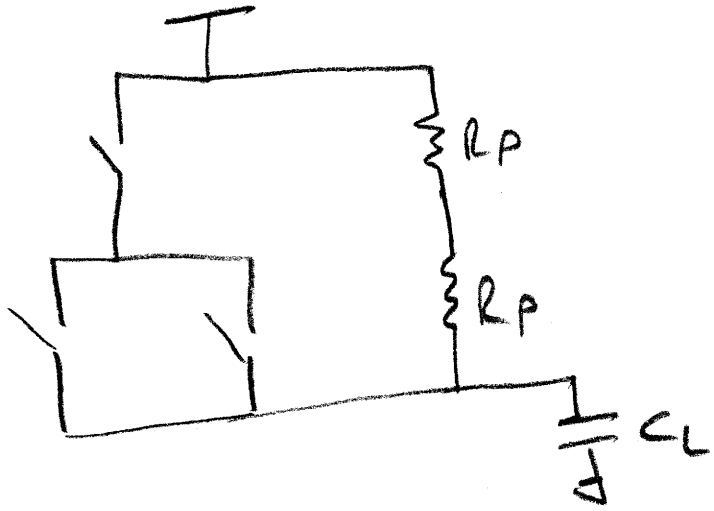
b) $x_1 = 1$ ●
$x_2 = 0 \to 1$ ↑
$x_3 = 0 \to 1$ ↑
$x_4 = 1$ ●

c) $x_1 = 1 \to 0$ ↓
$x_2 = 1 \to 0$ ↓
$x_3 = 1 \to 0$ ↓
$x_4 = 1 \to 0$ ↓

d) W.C t_{PLH} t_{PHL}

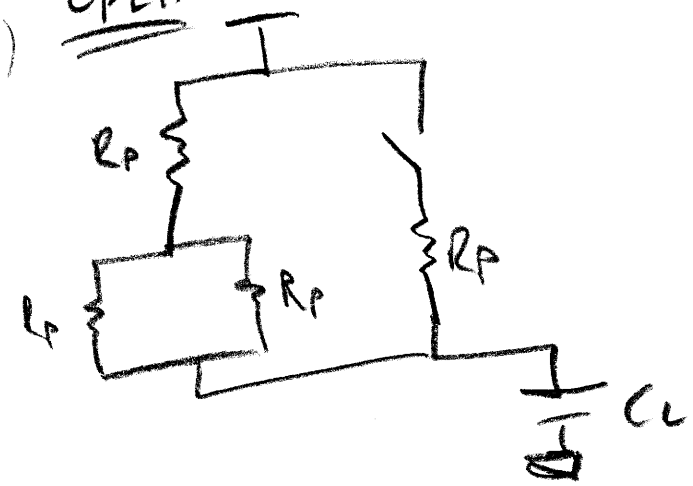
e) B.C t_{PLH} t_{PHL}

c) t_{PLH}



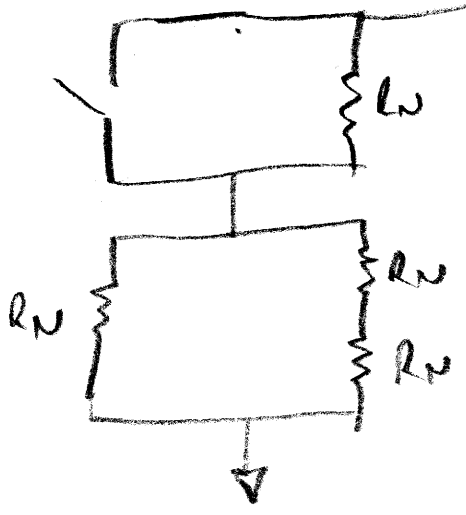
$$t_{PLH} = 0{,}69(2R_P)C_L$$
$$= 276\,ns$$

b) t_{PLH}



$$t_{PLH} = 0{,}69\left(\frac{3}{2}R_P\right)C_L$$
$$= 207\,ns$$

c) t_{PHL}



$$t_{PHL} = 0{,}69\left(\frac{5}{3}R_N\right)C_L$$
$$= 115\,ns$$

d) W.C t_{PLH}

$0,69(2R_P)C_L = 276ns$

$(x_1=0 \quad x_4=1, x_2=x_3=)$ do not care

W.C t_{PHL}

$0,69\ (2,5R_N)C_L = 172,5ns$

$(x_1=1 \quad x_2=0 \quad x_3=0 \quad x_4=0)$

e) B.C t_{PLH}

$0,69\ (1,5R_P)C_L = 207ns$

$(x_1=1 \quad x_2=1 \quad x_3=1 \quad x_4=$) do not care

B.C t_{PHL}

$0,69\left(\frac{5}{3}R_N\right)C_L = 115ns$

$(x_1=0 \quad x_2=0 \quad x_3=0 \quad x_4=0)$

$207ns \leq t_{PLH} \leq 276ns$

$115ns \leq t_{PHL} \leq 172,5ns$

Not $R \propto \frac{1}{W}$