Student Name: **Instructor: Mustafa Altun**

Student ID:

Date: 9/04/2018

EHB322E Digital Electronic Circuits
Quiz 2

Duration: 30 Minutes; *Grading: 1) 40%, 2) 60%,*
Quiz is in closed-notes and closed-books format; calculators are allowed
For your answers please use the space provided in the exam sheet
GOOD LUCK!

- Suppose that all NMOS transistors are identical and all PMOS transistors are identical.
  Equivalent resistor for an NMOS transistor: $\boldsymbol{R_N}$**= (12kΩ) / (W/L)$_N$**
  Equivalent resistor for a PMOS transistor: $\boldsymbol{R_P}$**= (24kΩ) / (W/L)$_P$**
- Suppose that each of the output circuit nodes has a capacitance value of **10pF**. Neglect other internal node capacitor.

1) Consider a Boolean function $f = x_1\overline{x_3} + \overline{x_1}\,\overline{x_2}x_3 + x_2\overline{x_3}$ to be implemented. Find the minimum value of (**(W/L)$_P$** + **(W/L)$_N$**) if $\boldsymbol{f}$ is implemented with "NMOS and PMOS (CMOS) Pass Transistor Logic" and worst case propagation delays **t_{PLH} = t_{PHL} = 82,8ns (120 × 0,69 = 82,8)** should be achieved.

2) Consider an approximate adder shown below. Derive Boolean expressions for outputs ***Sum*** and ***Cout*** in terms of inputs **A**, **B**, and ***Cin***. Calculate worst case propagation delays $\mathbf{t_{PLH}}$ and $\mathbf{t_{PHL}}$ if $\mathbf{(W/L)_P = (W/L)_N}$=1 for all transistors.