EHB 335E HW#4

Due: 22 November 2017 @9:00 am – No late homework will be accepted.

1) Determine the polarity of the feedback for the amplifier in Fig 1a. Clearly explain your reasoning.

2) Suppose the amplifier in Fig. 1b is described by

$$H(s) = \frac{A_0}{\left(1+\frac{s}{\omega_{p1}}\right)\left(1+\frac{s}{\omega_{p2}}\right)},$$

where $\omega_{p2} >> \omega_{p1}$. Compute the phase margin if the circuit is employed in a feedback system with K = 0.5. Assume that $\lambda > 0$.

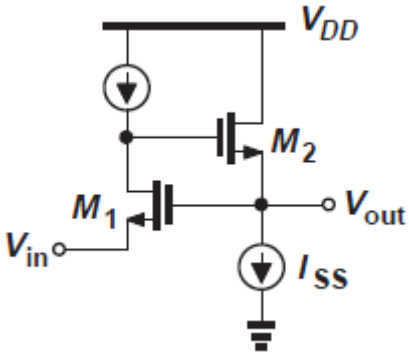

Fig 1a. Figure of Question 1

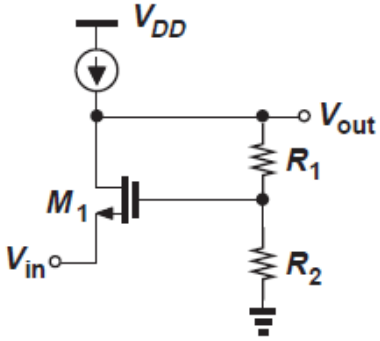

Fig 1b. Figure of Question 2

3) Assuming $V_A = \infty$, determine the closed-loop gain and I/O impedances of the amplifier in Fig 2a.

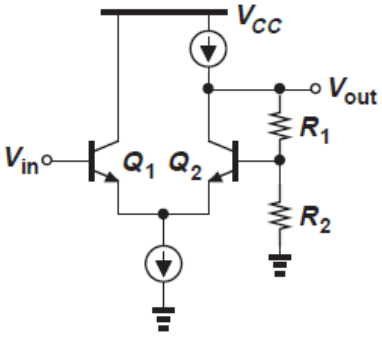

Fig 2a. Figure of Question 3

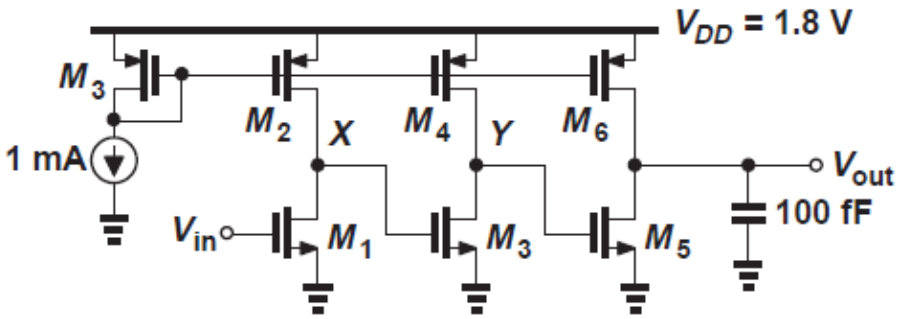

Fig 2b. Figure of Question 4

4) In the three-stage amplifier of Fig 2b., all transistors except M_1 and M_5 have W/L = 20 µm / 0.18 µm. For M_1 use W/L = 42 µm / 0.18 µm and for M_5 use W/L = 10 µm / 0.18 µm. Employ the transistor models provided in the last homework for Spice simulations. Assume a DC input level of 0.55 V.
   a. Determine the phase margin.
   b. Place a capacitor between nodes X and Y so as to obtain a phase margin of 60 degrees. What is the unity-gain bandwidth under this condition?
   c. Repeat (b) if the compensation capacitor is tied between X and ground and compare the results.