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**Student ID:**

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# EHB322E Digital Electronic Circuits
# QUIZ I

*Duration: 60 Minutes*

*Grading: 1) 50%, 2) 50%*

*For your answers please use the space provided in the exam sheet*

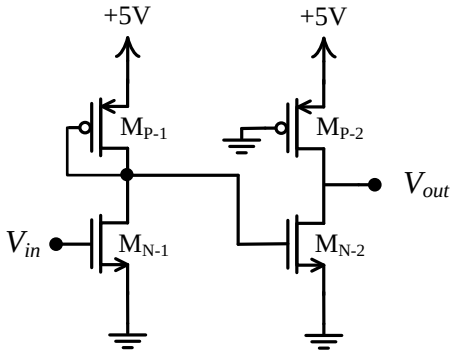
*GOOD LUCK!*

**1)** Consider a buffer shown below. Use the following equations for your calculations.

Saturation region current-voltage equation: $I_D = \frac{1}{2} k'_{p,n} \frac{W}{L} (V_{GS} - V_{T0\,p,n})^2$

Linear region current-voltage equation: $I_D = \frac{1}{2} k'_{p,n} \frac{W}{L} \left[ 2(V_{GS} - V_{T0\,p,n}) V_{DS} - V_{DS}^2 \right]$

*Transistor parameters:* $k_p' = \mu_p c_{ox} = 35\text{uA/V}^2$, $k_n' = \mu_n c_{ox} = 98\text{uA/V}^2$, $V_{TN}=1\text{V}$, $V_{TP}=-0.5\text{V}$, $W_{N-1}=5\text{u}$, $W_{N-2}=5\text{u}$, $L_P=L_N=1\text{u}$.

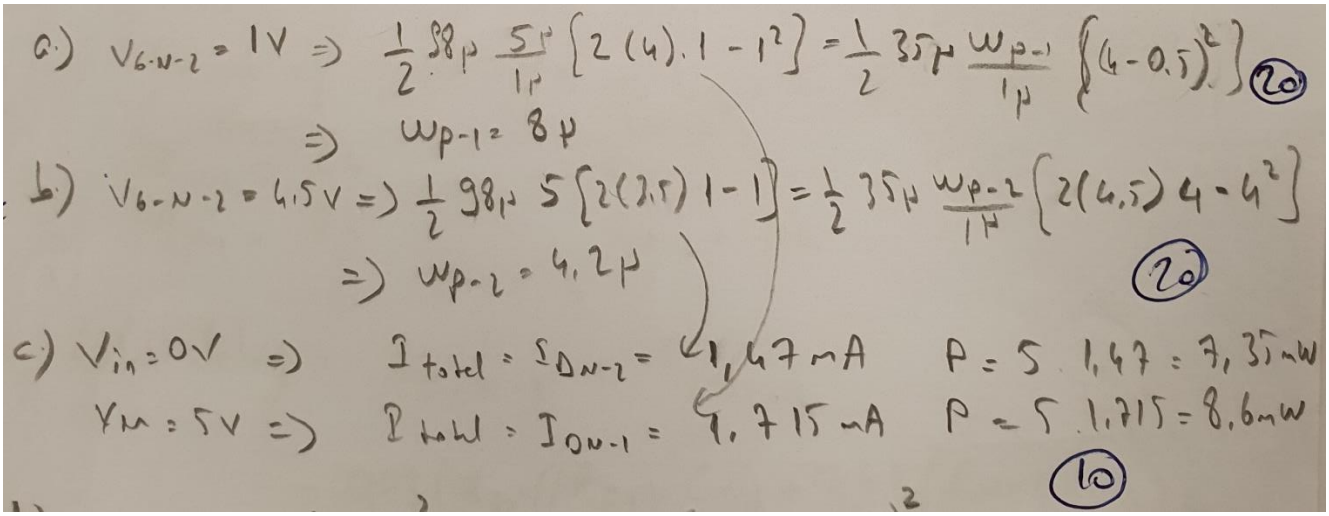



*Buffer*

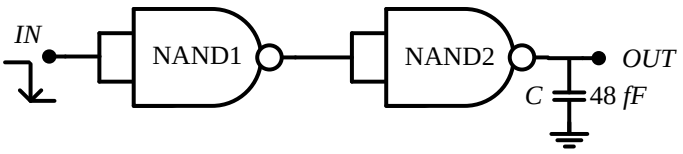
**a)** Find the maximum value of $\mathbf{W_{P-1}}$ satisfying that $\boldsymbol{V_{in}}$**=5V** results in $\boldsymbol{V_{out}}$**= 5V**.

**b)** Find the value of $\mathbf{W_{P-2}}$ if $\boldsymbol{V_{in}}$**=0V** results in $\boldsymbol{V_{out}}$**= 1V**.

**c)** Find the buffer's static power consumption values when $\boldsymbol{V_{in}}$**=0V** and $\boldsymbol{V_{in}}$**=5V.**



**2)** Consider a buffer circuit consisting of two CMOS NAND gates, shown below. An external capacitor of 48*fF* is connected to the output. A signal switching from high to low is applied to the input.
*Equivalent resistor for an NMOS transistor:* $\boldsymbol{R_N}$**= (12kΩ) / (W/L)$_N$**
*Equivalent resistor for a PMOS transistor:* $\boldsymbol{R_P}$**= (24kΩ) / (W/L)$_P$**
*Gate capacitors* $\boldsymbol{C_{GS\text{-}N}}$= $c_{ox}W_NL_N$ and $\boldsymbol{C_{GS\text{-}P}}$= $c_{ox}W_PL_P$; neglect $\boldsymbol{C_{GD}}$ capacitors.
*Transistor parameters:* $c_{ox}$=1 fF/um2, $L_N$=$L_P$=1u, $W_{N1}$=2u, $W_{P1}$=3u, $W_{N2}$=4u, $W_{P2}$=6u.




*Digital circuit with two CMOS NAND gates*

**a)** Implement a NAND gate with a Boolean function $f = \overline{x_1 x_2}$ using CMOS transistors. If inputs of a NAND gate are shorted, as we use in our circuit, then find its Boolean function. Draw the CMOS implementation of the above circuit.

**b)** Find the **total propagation delay value** (delay of NAND1 + delay of NAND2) between the input and the output.

- You should consider $C_{GS}$ capacitors as well as the external *C*=48*fF* capacitor
- Do not consider capacitors at nodes other than the node of gate inputs/outputs.