Quiz 4 Designing Adder, Substracter ve Comparator Circuits with Block Structure ile Tasarımı

A circuit that will be designed which is used to compare two n-bit positive integers, $A=(a_{n-1}a_{n-2}\ldots a_1a_0)_2$ and $B=(b_{n-1}b_{n-2}\ldots b_1b_0)_2$. The circuit has three 1-bit outputs, x,y,z. The definitions and the Boole functions of the outputs are given below.

$$A > B \Rightarrow (1, 0, 0) = (x, y, z)$$
$$A = B \Rightarrow (0, 1, 0) = (x, y, z)$$
$$A < B \Rightarrow (0, 0, 1) = (x, y, z)$$

$$a_i > b_i \Rightarrow (1, 0, 0) = (u_i, t_i, v_i)$$
$$a_i = b_i \Rightarrow (0, 1, 0) = (u_i, t_i, v_i)$$
$$a_i < b_i \Rightarrow (0, 0, 1) = (u_i, t_i, v_i)$$

$x = u_{n-1}+t_{n-1}u_{n-2}+t_{n-1}t_{n-2}u_{n-3}+\ldots+t_{n-1}t_{n-2}\ldots t_2u_1+t_{n-1}t_{n-2}\ldots t_2t_1u_0$
$y = t_{n-1}t_{n-2}\ldots t_1t_0$
$z = v_{n-1}+t_{n-1}v_{n-2}+t_{n-1}t_{n-2}v_{n-3}+\ldots+t_{n-1}t_{n-2}\ldots t_2v_1+t_{n-1}t_{n-2}\ldots t_2t_1v_0$

The schematic of the basic block that will be used to design the circuit is shown in Fig. 1.

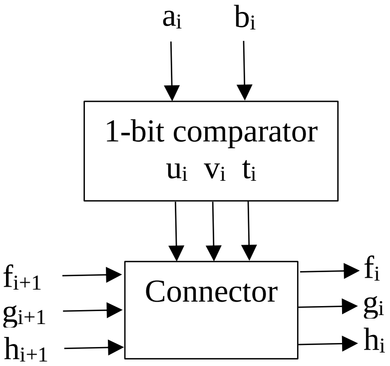

Figure 1

If the relation between the numbers represented by the bits from (n-1) to i is $(a_{n-1}a_{n-2}\ldots a_{i-1}a_i)_2 > (b_{n-1}b_{n-2}\ldots b_{i-1}b_i)_2$ then $f_i=1$
If the relation between the numbers represented by the bits from (n-1) to i is $(a_{n-1}a_{n-2}\ldots a_{i-1}a_i)_2 < (b_{n-1}b_{n-2}\ldots b_{i-1}b_i)_2$ then $g_i=1$
If the relation between the numbers represented by the bits from (n-1) to i is $(a_{n-1}a_{n-2}\ldots a_{i-1}a_i)_2 = (b_{n-1}b_{n-2}\ldots b_{i-1}b_i)_2$ then $h_i=1$

1) Draw the schematic of the 1-bit comparator circuit using the logic gates.
2) Draw the schematic of the connector circuit using the logic gates.
3) Draw the schematic of the comparator circuit for two 3-bit positive numbers, $A=(a_2a_1a_0)_2$ and $B=(b_2b_1b_0)_2$, by using the circuit shown in Fig. 1 as the basic building block.