EHB 335E // TERM PROJECT // SERDEN SAIT ERANIL // 040170025

In this project, Ltspice is used to simulate a two-stage CMOS operational amplifier whose schematic is shown below.

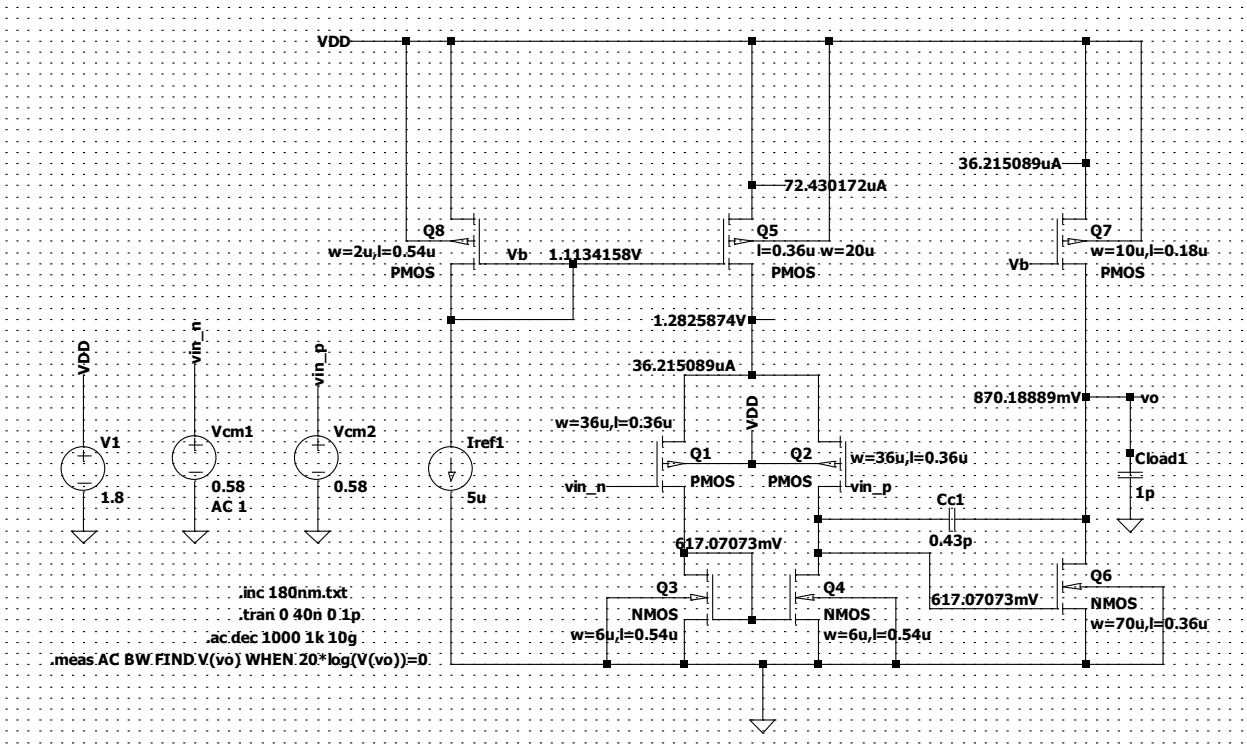

Figure 1: Two-stage CMOS operational amplifier

In this circuit configuration we have two stages, one is active loaded PMOS differential amplifier and the other one is a basic common-source amplifier. Low frequency gain of the active-loaded differential amplifier is given as $Av_1 = -gm_2(ro_2 \,//\, ro_4)$ and the low frequency gain of common-source stage is given as $Av_2 = -gm_6(ro_6 \,//\, ro_7)$ and the overall gain can be calculated as $Av = Av_1 \, x \, Av_2$ since Cc acts like an open-circuit at low frequencies. Also, the bulk terminals of each NMOS are tied to ground, and the bulk terminals of each PMOS is tied to VDD to ensure the reverse biasing.

I started to design by selecting overdrive voltages for the transistors. Since the drain currents of Q1, Q2, Q3 and Q4 are all equal and they are equal to half of the drain current of Q5, I tried to select respectively low overdrive voltage value to be able to get highest capability of playing with transistor's aspect ratios. I decided to make all overdrive voltages to be between 0.2V and 0.3V. Therefore, I needed to determine the value of the source of Q5 to be able to give an input that produces these overdrive voltages. Since VDD = 1.8V, I determined the value of the source of Q5 to be approximately 1.2V, allocating the each MOSFET a Vds value of 0.6V. After the selection of Vs = 1.2V, we know that Vov = Vsg – |Vthp| = Vs – Vg -|Vthp|. Therefore, Vg = Vcm = Vs-|Vthp|-Vov. We can calculate the common-mode value of the differential pair since we know that Vthp=-0.42V from the transistor's file. From these calculations, we get a common-mode value of 0.58V.

We selected the Vcm, now we have to decide for suitable aspect ratios to produce desired specifications. Since we have 3 options for the length of the transistors which are 180nm, 360nm and 540nm, and since Av_1 is highly dependent on the output impedance of the transistors, I selected 360nm and 540nm for the

differential pair. The higher the length of the transistors the higher the output impedance value; thereby, increasing the gain.

Since the differential pair and the common-source amplifiers are biased with a current mirror which duplicates the current Iref, any value of drain current can be chosen by selecting an appropriate aspect ratio between the transistors. Therefore, I chose Iref = 5uA because power is an important design metrics that we would want to optimize.

Then for Q8, I decided to minimize its aspect ratio so that I can use mirroring more effectively. And I used the values in Figure 1 to create biasing currents of transistors.

Unity-gain bandwidth is approximately equal to $fu \approx \frac{\mathrm{gm1}}{2\pi Cc}$ and slew-rate is approximately equal to $\frac{Id1}{Cc}$. Slew rate is about the settling time of the transistor, Therefore, for both phase margin and for the settling time I chose Cc to be 0.43pF. I deduced this value by experimentally and did not change it so much.

Since by Miller effect Cc produces two poles one at the output of the common-source stage and another at the output of the differential pair. The output pole affects phase margin thoroughly which governed by the miller approximation. In order to get a phase margin of 60 degree or more, we shouldn't increase the gain of the second stage so much because $Cout = Cc(1 - \frac{1}{Av})$ starts to decrease. Therefore, I tried to maintain a balance between the phase margin and the bandwidth.

Input of the second stage is the output of the differential amplifier and since I selected Vov voltage of 0.2V the input of the second stage should be around 0.6V. Also, since the current on the second stage is a fixed value which is determined by the ratio of the current mirror's aspect ratio, I adjusted the W/L values of the second stage so that to obtain both minimum gain and maximum voltage headroom.

In order to obtain maximum voltage headroom, I decided to make Vo to be always 0.9V. Therefore, to sustain this voltage, I adjusted W/L of the Q6 every time I changed another parameter.

After my first implications are completed, I run .op command to see if anything is wrong and I get the results as shown:

--- Operating Point ---

V(vdd):	1.8	voltage
V(vb):	1.11342	voltage
V(n001):	1.28259	voltage
V(vo):	0.870189	voltage
V(vin_n):	0.58	voltage
V(n003):	0.617071	voltage
V(vin_p):	0.58	voltage
V(n002):	0.617071	voltage
Id(Q6):	0.000462848	device_current
Ig(Q6):	0	device_current
Ib(Q6):	-8.80189e-013	device_current
Is(Q6):	-0.000462848	device_current
Id(Q4):	3.62151e-005	device_current
Ig(Q4):	0	device_current
Ib(Q4):	-6.27071e-013	device_current
Is(Q4):	-3.62151e-005	device_current
Id(Q3):	3.62151e-005	device_current
Ig(Q3):	0	device_current
Ib(Q3):	-6.27071e-013	device_current
Is(Q3):	-3.62151e-005	device_current
Id(Q2):	3.62151e-005	device_current
Ig(Q2):	-0	device_current
Ig(Q2):	-0	device_current
Ib(Q2):	1.72034e-012	device_current
Is(Q2):	-3.62151e-005	device_current
Id(Q1):	3.62151e-005	device_current
Ig(Q1):	-0	device_current
Ib(Q1):	1.72034e-012	device_current
Is(Q1):	-3.62151e-005	device_current
Id(Q7):	0.000462848	device_current
Ig(Q7):	-0	device_current
Ib(Q7):	9.39811e-013	device_current
Is(Q7):	-0.000462848	device_current
Id(Q5):	7.24302e-005	device_current
Ig(Q5):	-0	device_current
Ib(Q5):	5.27413e-013	device_current
Is(Q5):	-7.24302e-005	device_current
Id(Q8):	5e-006	device_current
Ig(Q8):	-0	device_current
Ib(Q8):	6.96584e-013	device_current
Is(Q8):	-5e-006	device_current
I(Cload1):	8.70189e-025	device_current
I(Cc1):	1.08841e-025	device_current
I(Iref1):	5e-006	device_current
I(V1):	-0.000540279	device_current
I(Vcm2):	0	device_current
I(Vcm1):	0	device_current

Figure 2: Operating points

After I make DC analysis and ensure that all transistors are in saturation and they have desirable currents I started to analyze this two-stage amplifier in terms of low-frequency gain, unity-gain bandwidth (the frequency at which the gain decreases to 1 or 0 dB), and phase margin to ensure the circuit is stable.

Since my main concern in this design is power, bandwidth and settling time, I did not look for high gain and high phase margin because high phase margin reduces the settling time and high gain reduces the bandwidth considerably.

My low-frequency gain results are shown as:

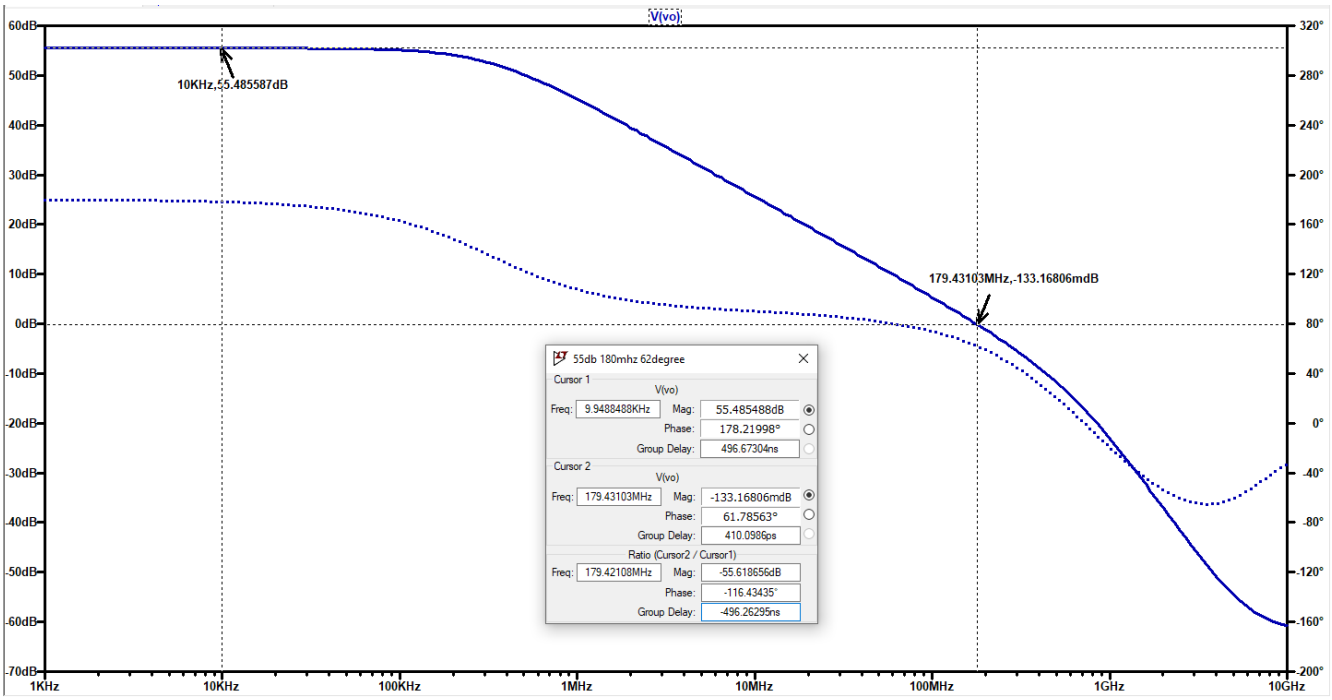

Figure 3: Gain, Bandwidth and phase margin

By bringing the cursor 1 and cursor 2 appropriate locations we can measure the low-frequency gain, unity-gain bandwidth and the phase margin. I can directly read the phase margin from the plot because I give the AC differential input to negative terminal of the operational amplifier which is the same as giving the AC voltage to positive terminal and subtracting 180 ° from the phase angle of the amplifier.

Curser-1 points to low-frequency gain and curser-2 points to the point where gain crossover occurs.

As it can be seen from the plot, we get

$$low-frequency\ gain\ Av_0 \approx 55.5\ dB$$

$$unity\ gain\ bandwidth\ f_u \approx 180\ Mhz$$

$$phase\ margin\ \theta_{phase} \approx 62\ °$$

Now, let us analyze the step response of the design.

By analyzing the transient response of the design, we can measure the settling time which is a very important because it is a key parameter for guaranteeing the performance of data acquisition systems. Output should settle before data acquisition.

Vinitial[V]:	0
Von[V]:	1
Tdelay[s]:	0
Trise[s]:	1p
Tfall[s]:	1p
Ton[s]:	40n
Tperiod[s]:	80n
Ncycles:	

I connected the negative input to the output and applying a pulse whose parameters are specified in the project description.

Then by using the command .tran 0 40n 0 1p, we can measure the settling time of the amplifier.

Figure 4: Pulse specifications

Transient simulation:

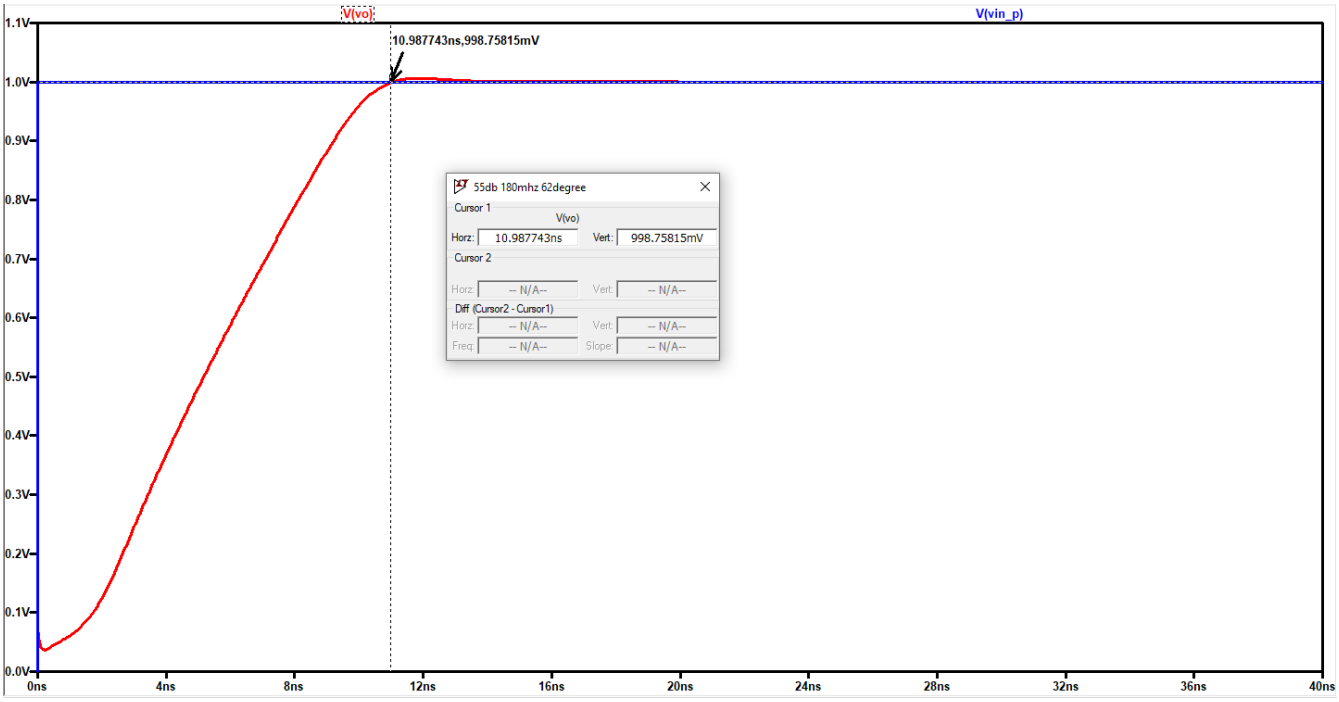

Figure 5:Transient simulation and settling time

As can be seen from the cursor, the output settles in approximately 11ns. Therefore,

$$Settling\ time\ T_s = 11\ ns$$

Now we need to calculate the power in order to calculate the figure of merit (FOM) value whose formula is given in the project description.

From the operating points (Figure 2), we can calculate the total current flowing into the transistors.

Since I selected Iref = 5 µA, $Id_{M8} = 5$ µA

Also, from the current mirrors and operating point analysis $Id_{M5} = 72.3$ µA , $Id_{M7} = 462.85$ µA

$$Id_{total} = 5\ \mu A + 72.3\ \mu A + 462.85\ \mu A = 540.15\ \mu A$$

$$Power\ P = Id_{total} * VDD = 540.15\ \mu A * 1.8\ V = 0.972\ mW$$

Now we can calculate the figure of merit (FOM) by using the formula

$$figure\ of\ merit\ (FOM) = \frac{gain(dB) * bandwidth(Hz)}{settling\ time(ns) * power(mW)}$$

$$figure\ of\ merit\ (FOM) = \frac{55.5\ dB * 180\ Mhz}{11\ ns * 0.972\ mW} = 934.34$$