Full Custom Layout and Standard Cell Approximation

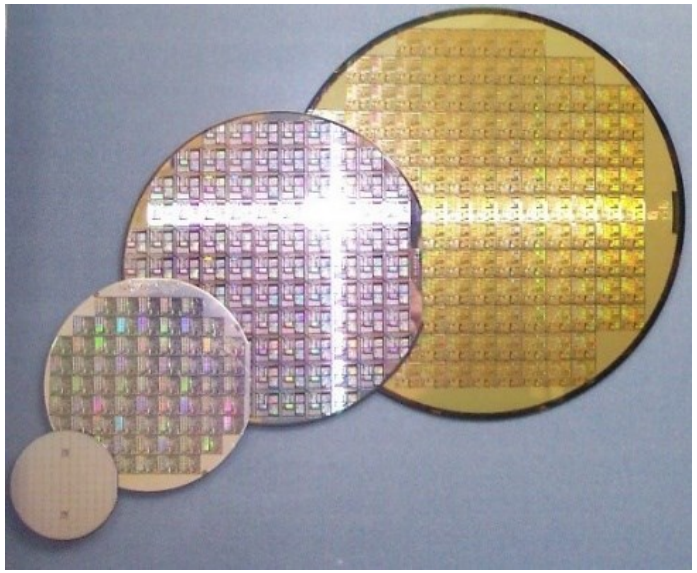
ALİ DOĞUŞ GÜNGÖRDÜ

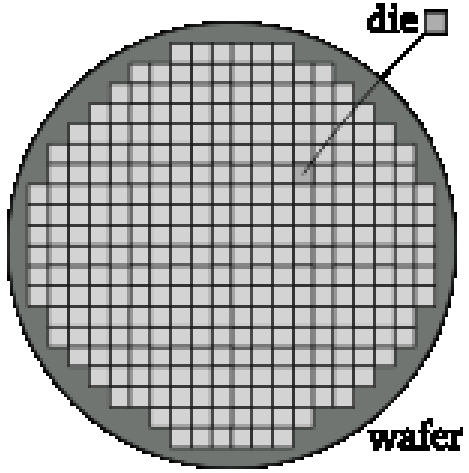
Outline

1. Introduction to the Integrated Circuits
2. Physical Layers for Layout
3. Standard Cells
4. DRC, LVS, PEX with Calibre
5. References

INTRODUCTION

How does an integrated circuit look like?





Wafer and die→ Almost pure silicon (%99)

INTRODUCTION

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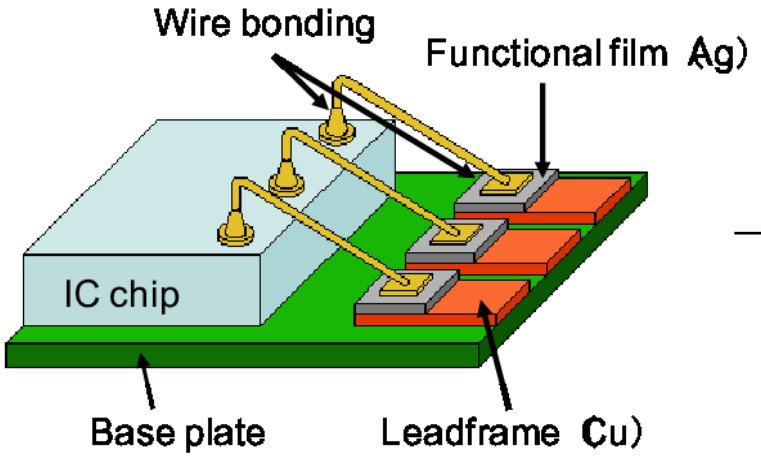
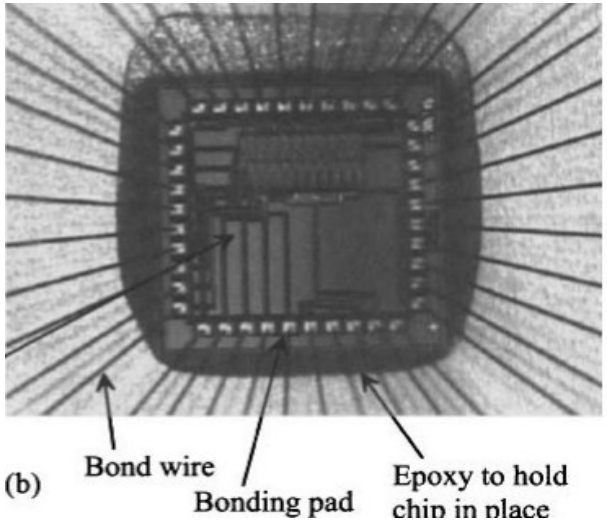
Inside a die

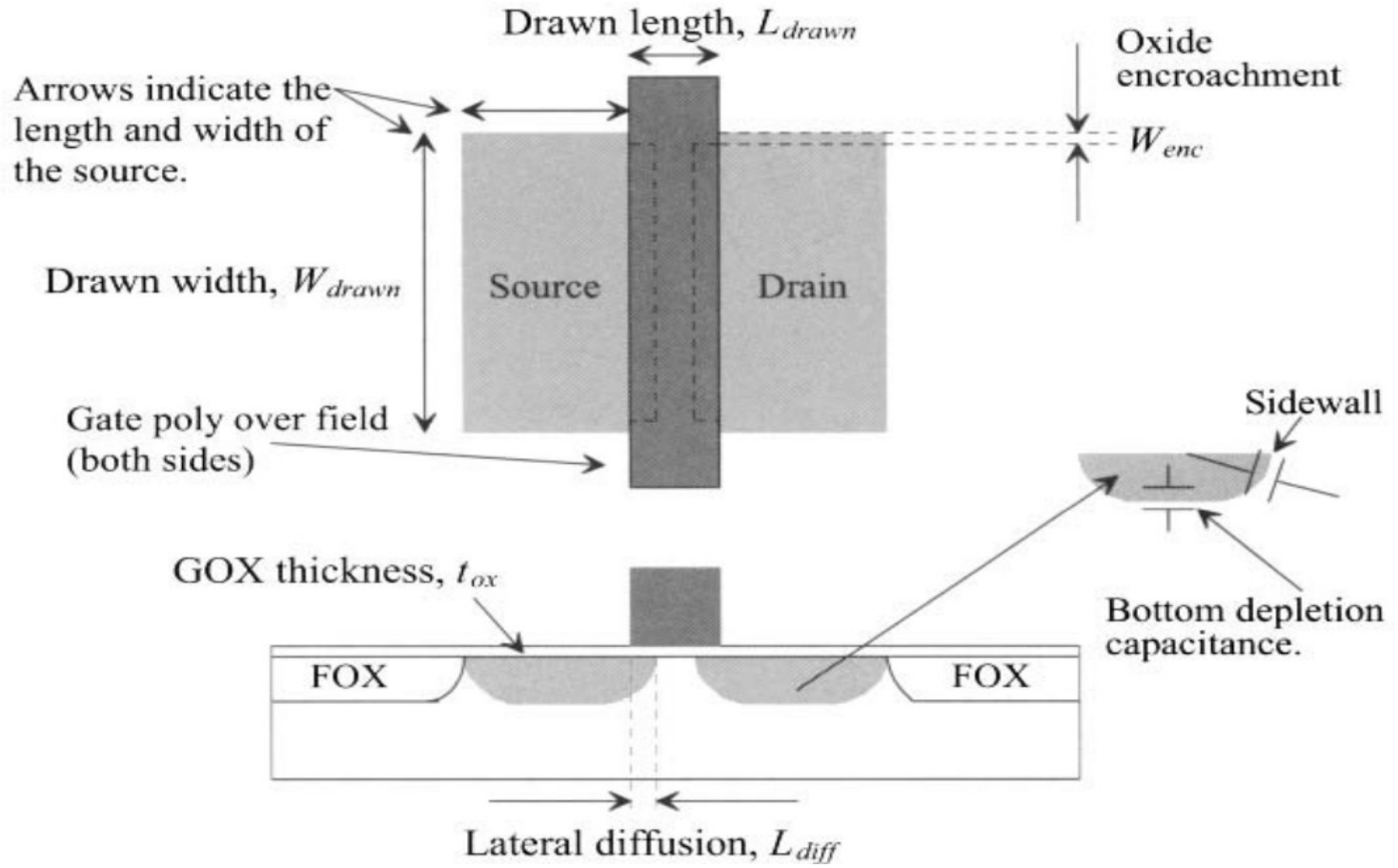




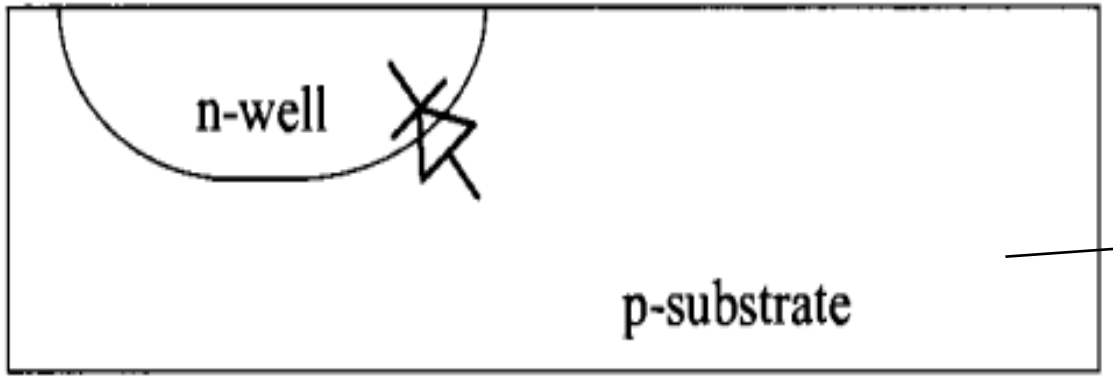
Die, bonding pads, bond wire and package & pins

Opening the chip (or die) to the real world to test or connect

HOW DOES A MOSFET LOOK LIKE?



PHYSICAL LAYERS IN THE LAYOUT (PSUB-NWELL)



→ Black screen in Cadence Layout

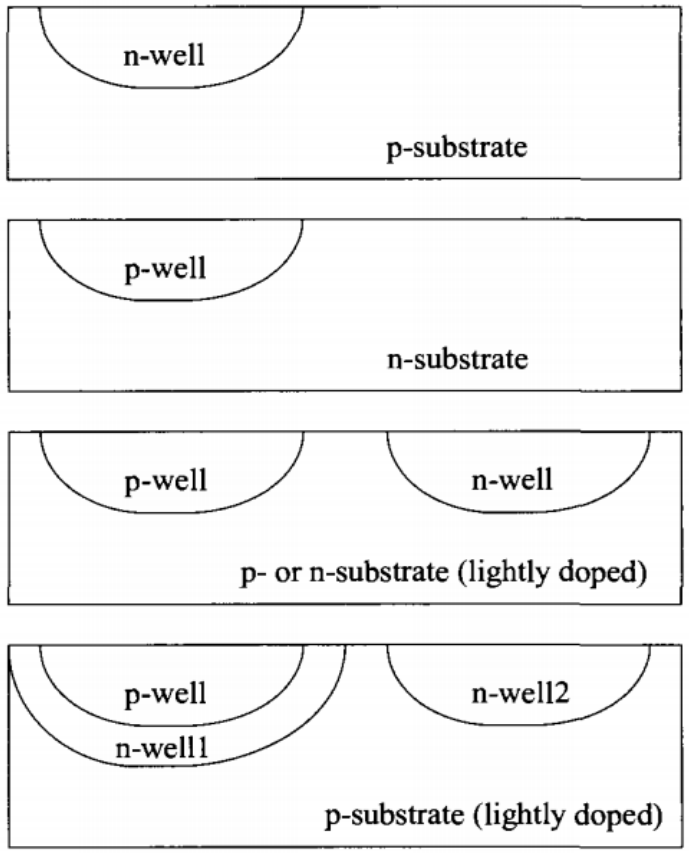
Watch out for parasitic diode between n-well and p-sub

P-sub → Ground (most negative supply)

N-well → VDD (most positive supply)

→ Reverse biasing the parasitic diode!

DIFFERENT CMOS PROCESSES



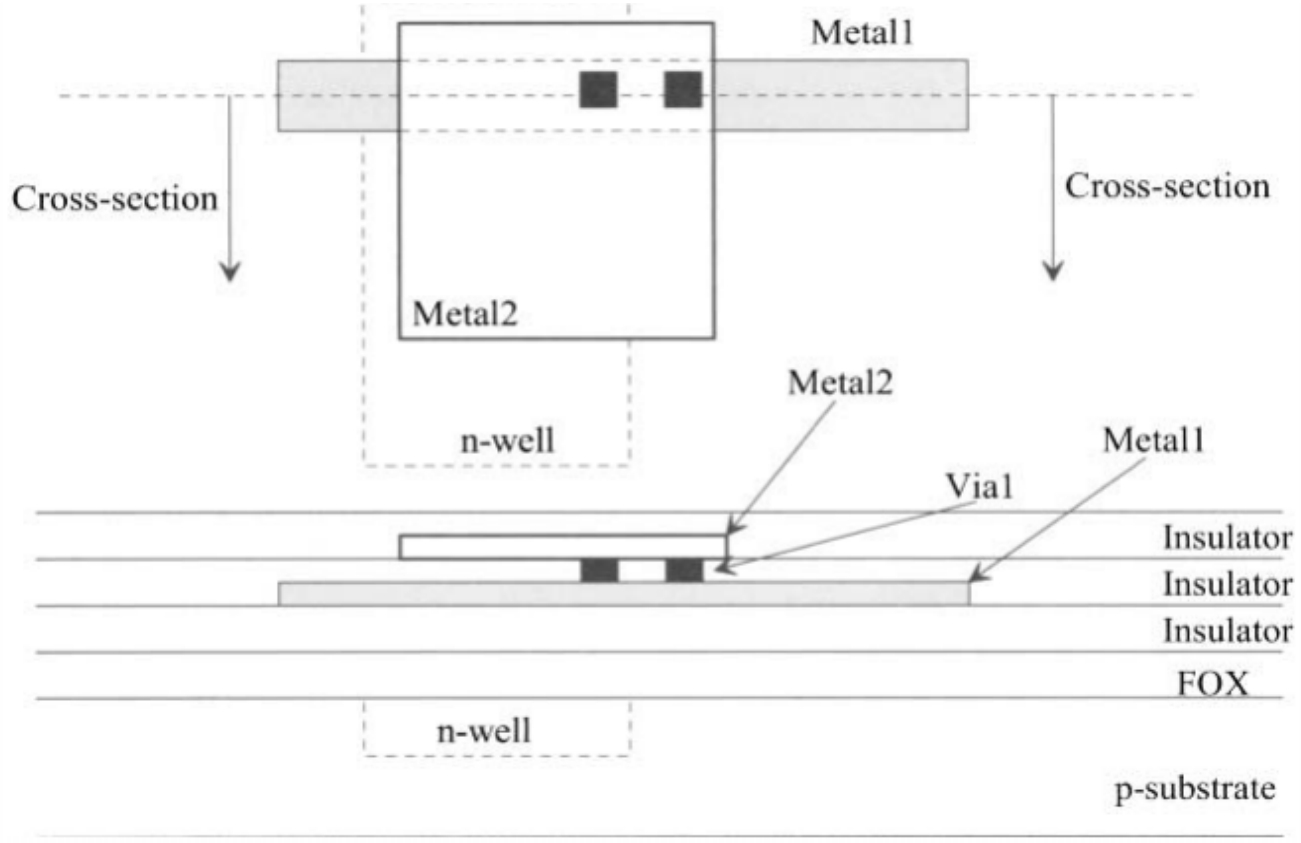
(a) n-well process ⟶ Okay for Fully Digital IC

(b) p-well process

(c) Twin-well process

(d) Triple-well process using p-substrate ⟶ Most common for Mixed-Signal and RF Purposes

METAL LAYERS



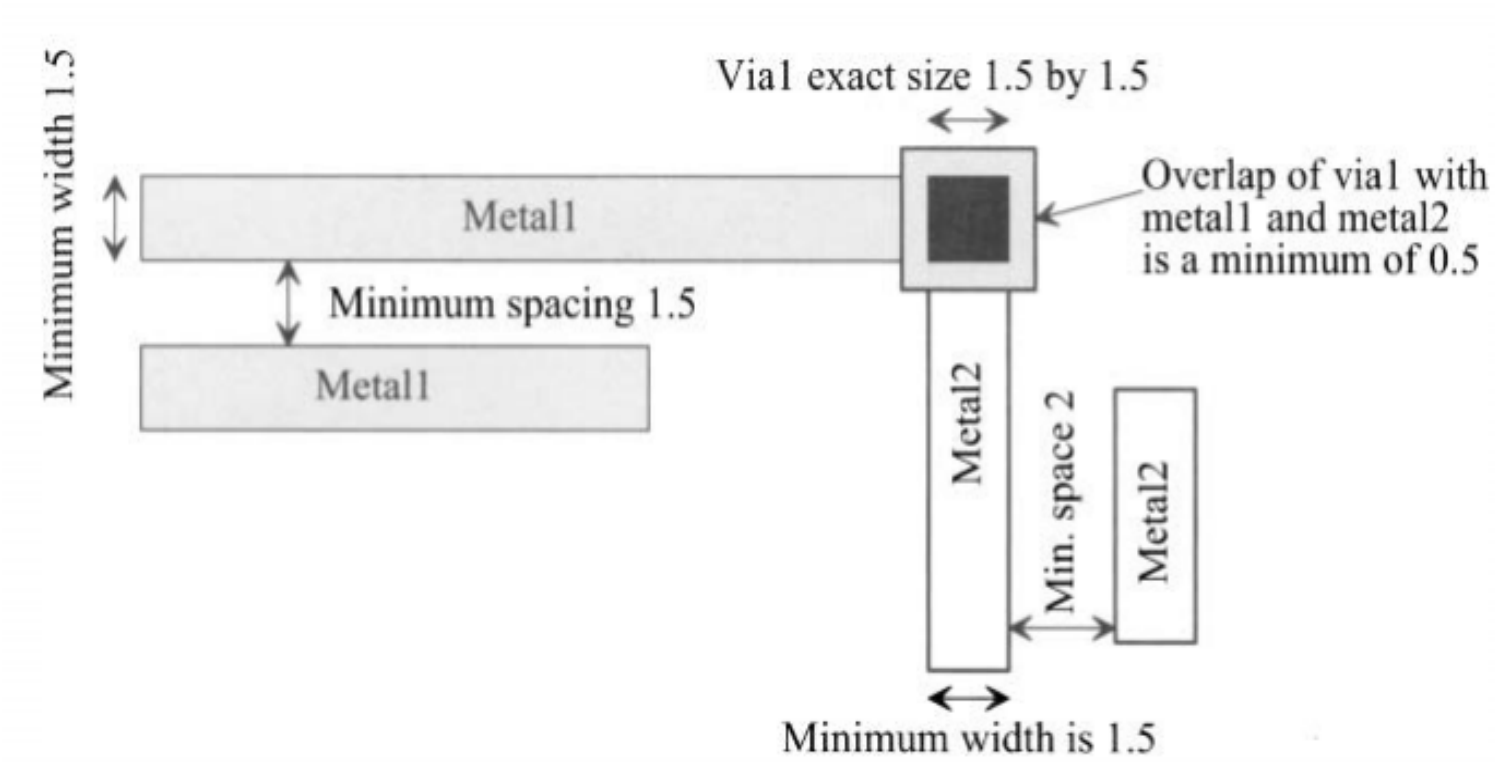
Metal-1 >> Via1 >> Metal-2

Metal-2 >> Via2 >> Metal-3

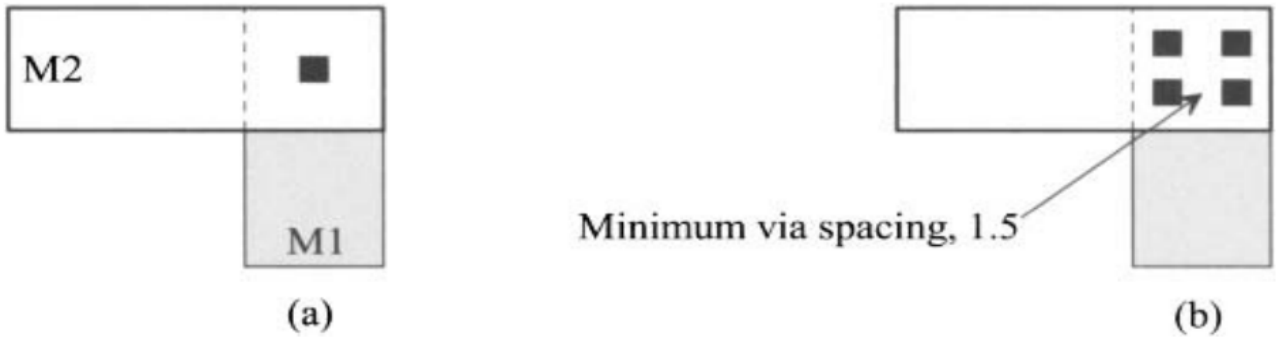
Metal-3 >> Via3 >> Metal-4

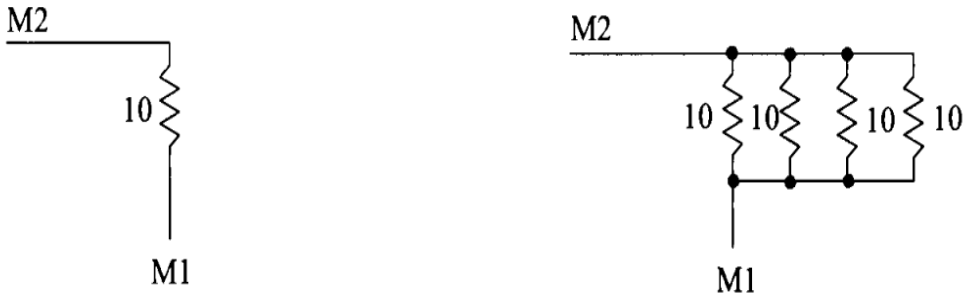
You cannot directly jump from M1 to M3 or M2 to M4 etc.

METAL DESIGN RULES

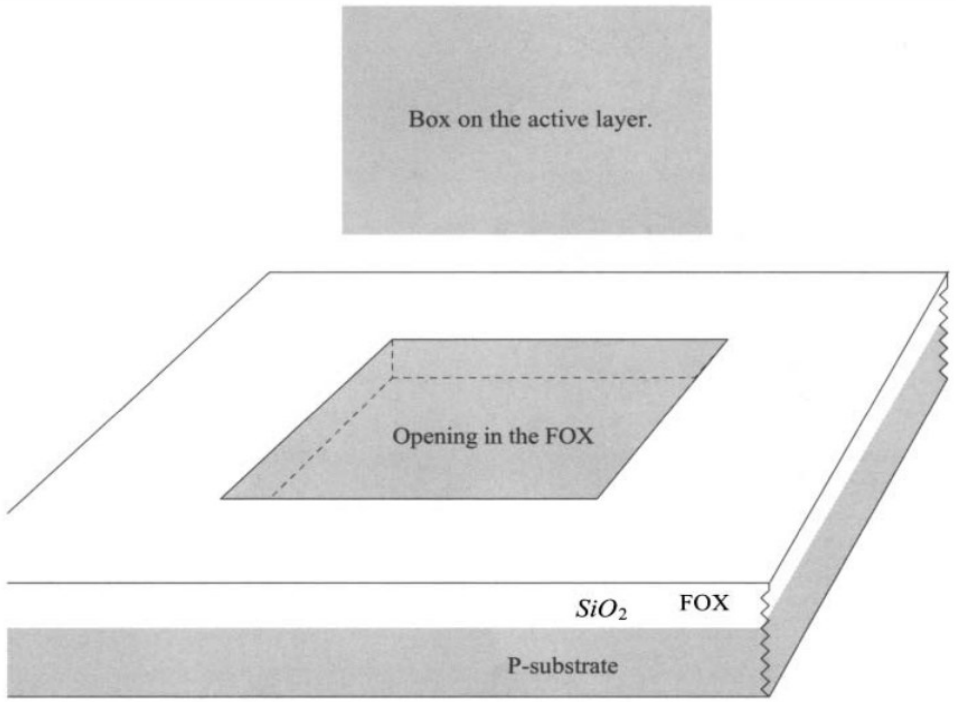


IMPORTANCE OF VIA



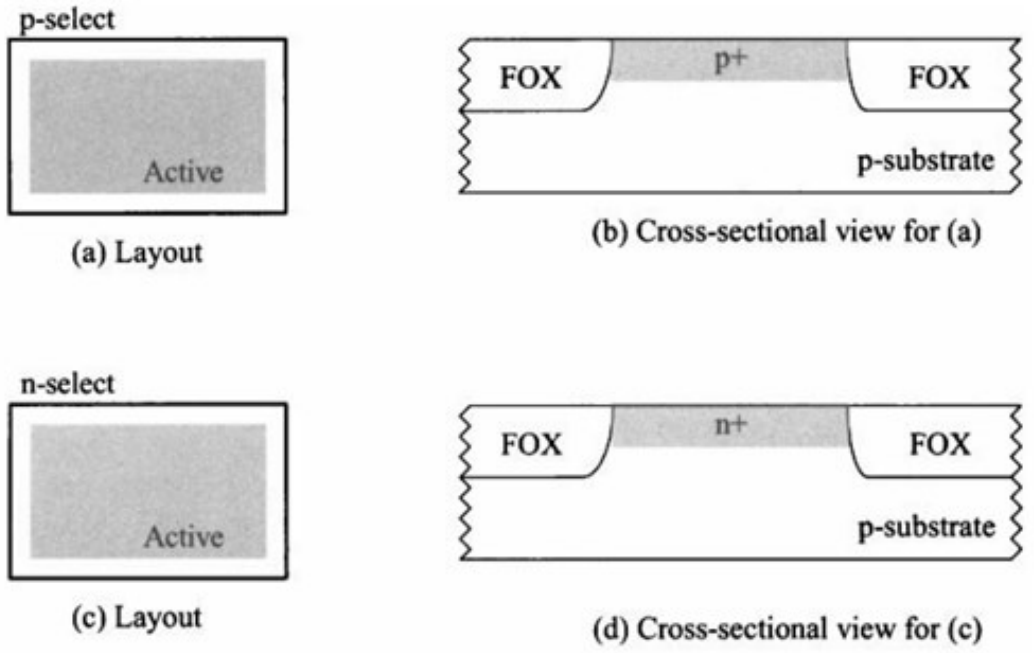


ACTIVE LAYER (DIFFUSION & DOPING)



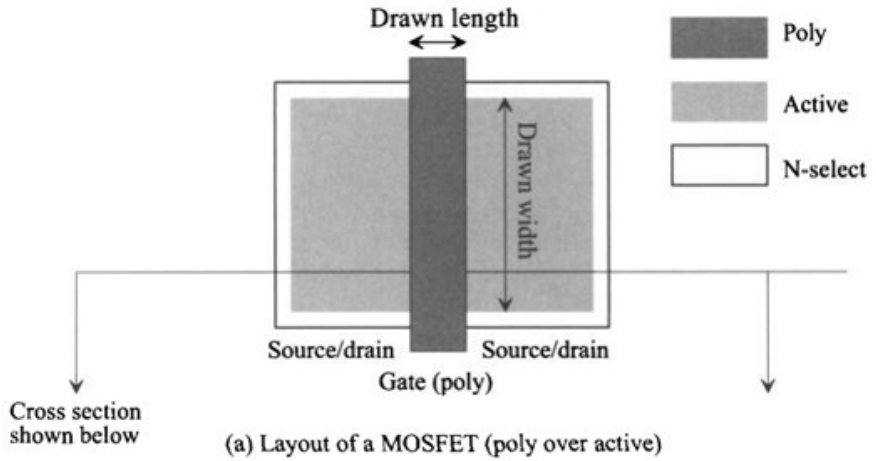
Opening in the field oxide to dope

ACTIVE LAYER (DIFFUSION & DOPING)

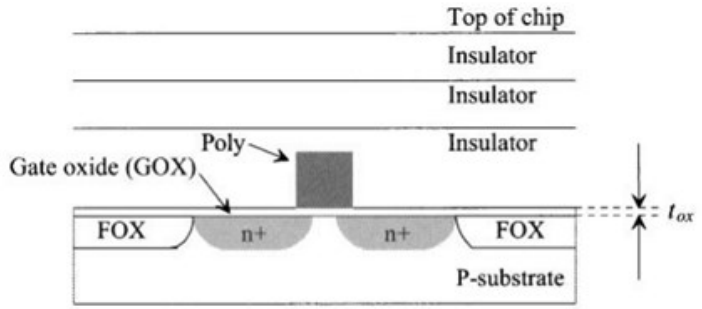


Correspondence of Diffusion Layer + Type of Doping in Cadence

POLY LAYER

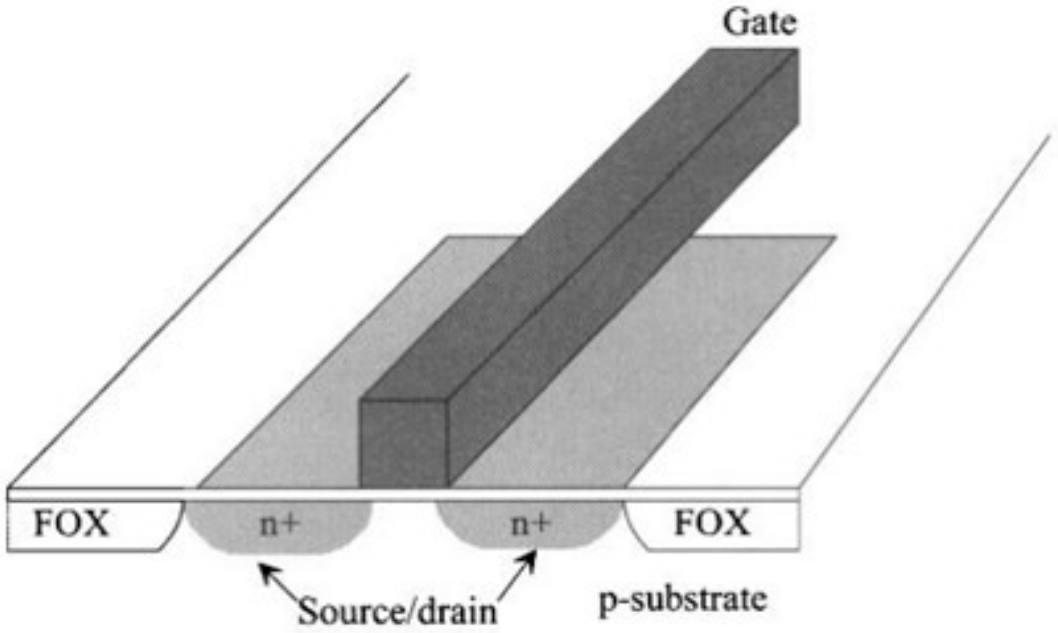


(a) Layout of a MOSFET (poly over active)

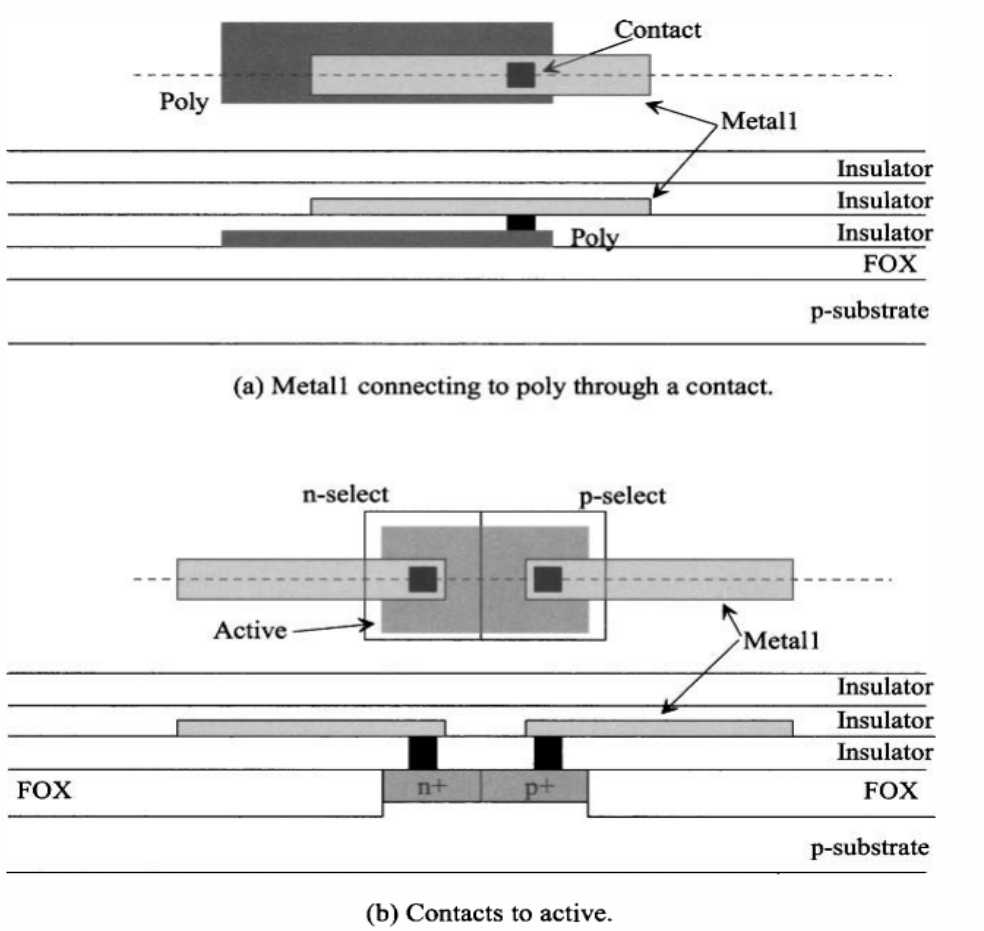


(b) Cross-sectional view of the layout in (a).

POLY LAYER



CONNECTING POLY-DIFF-MET LAYERS



You need a contact layer to reduce the resistance between semiconductor and metal interface

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CONTACT LAYER

POLY TO METAL OR DIFF TO METAL INTERFACE

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CREATING SCHEMATIC AND SYMBOL with CADENCE VIRTUOSO

XFAB 0.18 PROCESS → Create a Library with your name (i.e. AliDogus)→ Create a new cell

Name the Cell (i.e. NAND_Custom

Select “ne” and “pe” from PRIMLIB as nmos and pmos, respectively

Do not forget the bulk connections (nwell to DVDD and psub to gnd)

DVDD-> as power supply naming
DGND-> as ground naming
IN1→INPUT1
IN2→INPUT2
OUT->OUTPUT

→

Follow this naming to work together without any problem

Create symbol for hierarchical simulation from schematic editor

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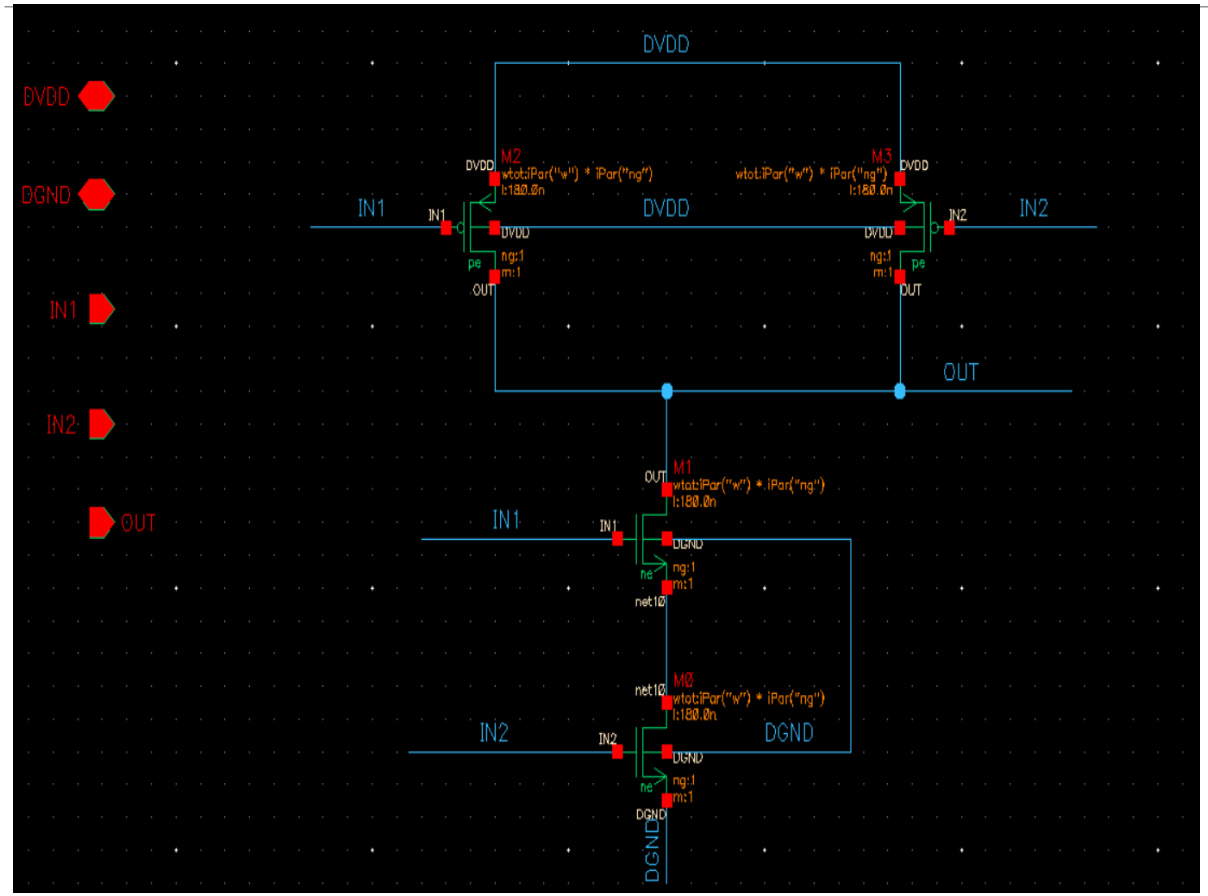
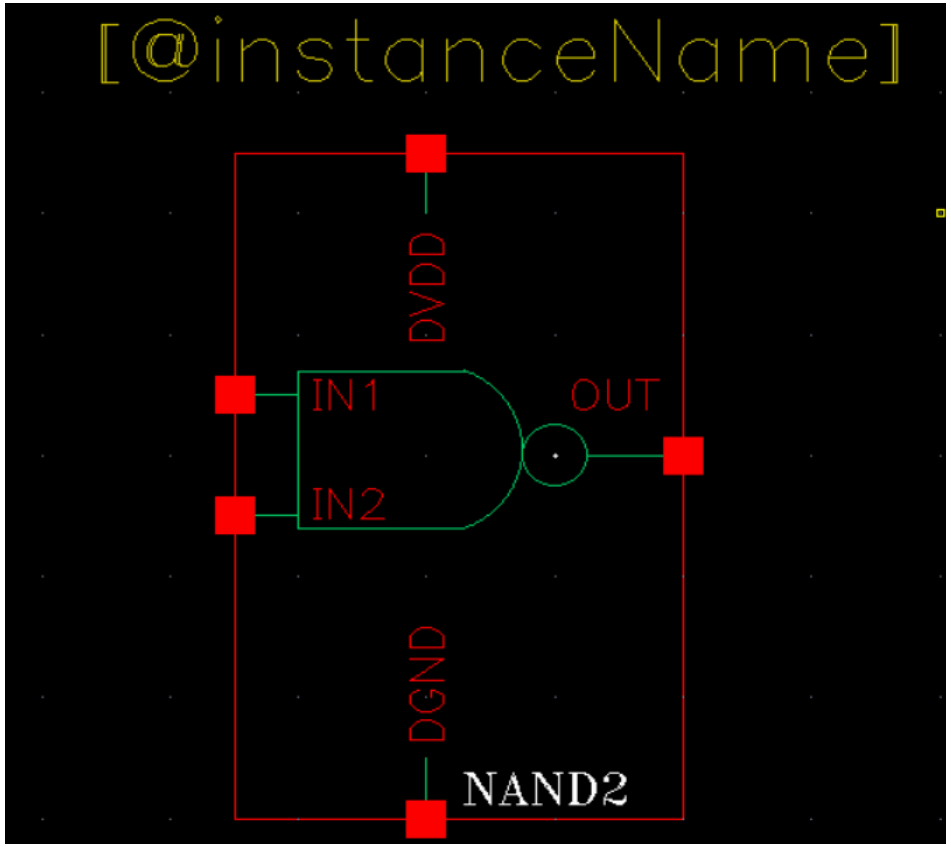
CREATING SCHEMATIC AND SYMBOL with CADENCE VIRTUOSO





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POST SCHEMATIC SIMULATION USING ADEL

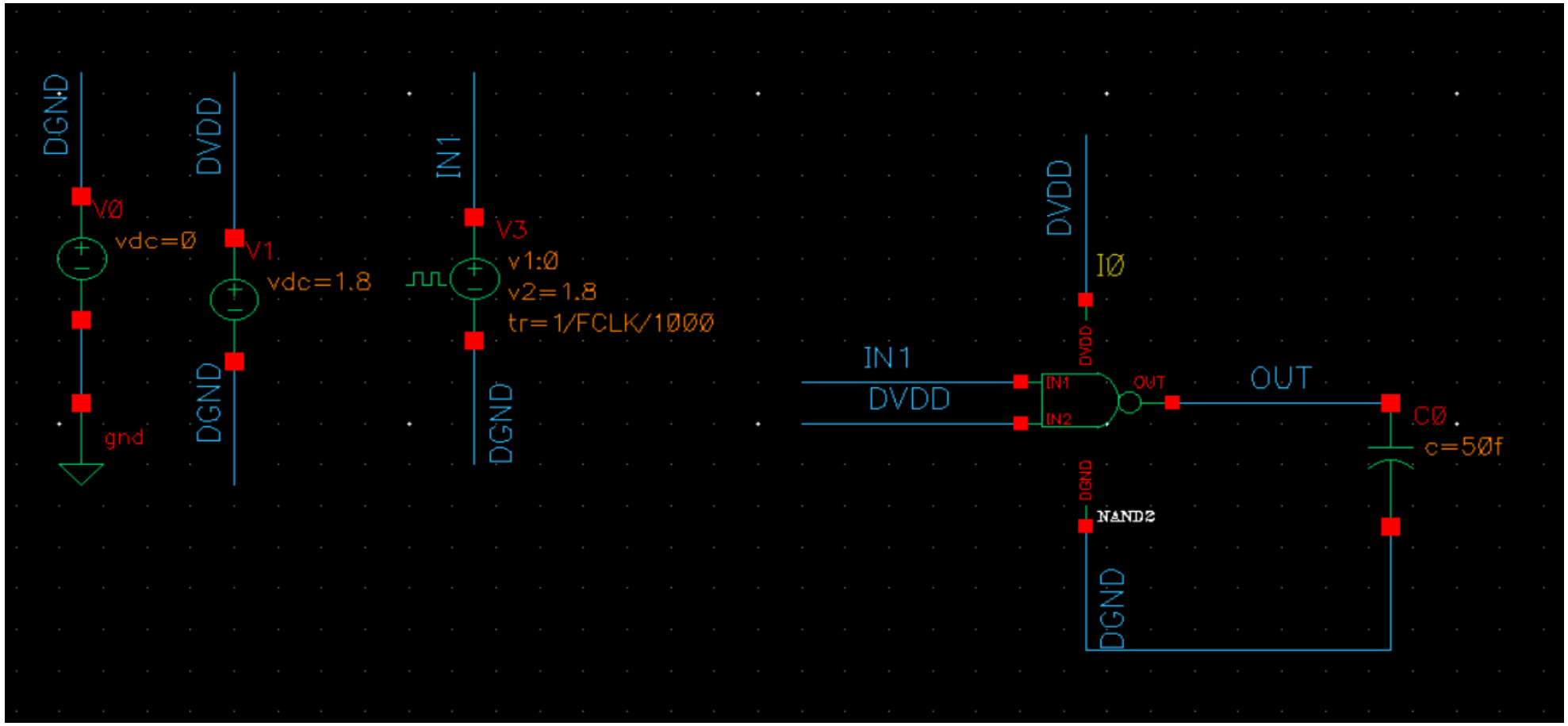
Create a new cell-view for simulation (i.e. NAND_custom_sim)

Call the cell that you designed from your library

Apply stimulation to characterize the gate

DVDD=1.8V, only use a one global GND

POST SCHEMATIC SIMULATION USING ADE-L



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