13/04/15 - W11

BHD 3226 Digital Electronic Circuits

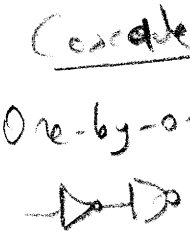
SPRING 2015

- In Dynamic CMOS logic INPUTS should be switched when CLK=0 (GND)
- How to satisfy this by considering delays

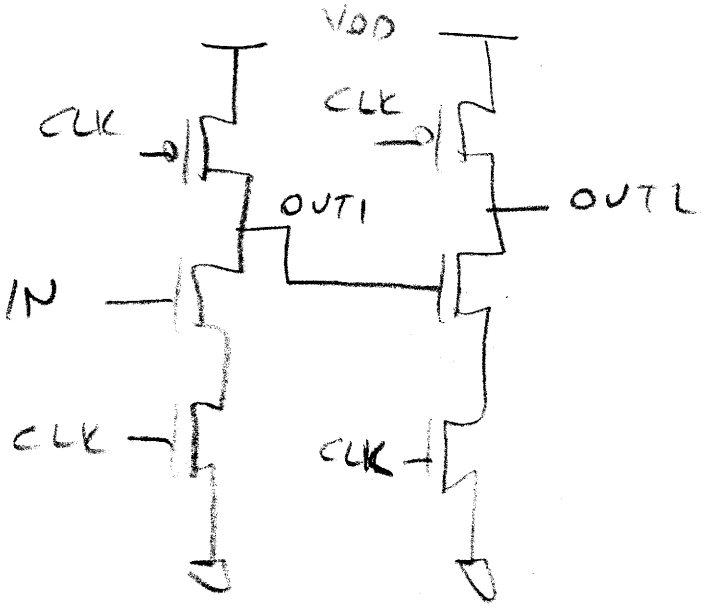
CASCADING PROBLEM

Reminder

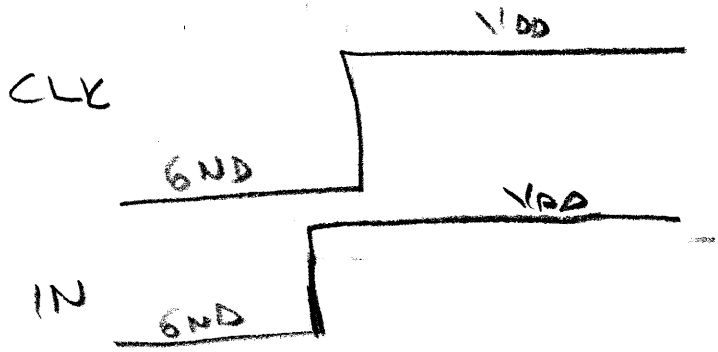
Cascade One-by-one

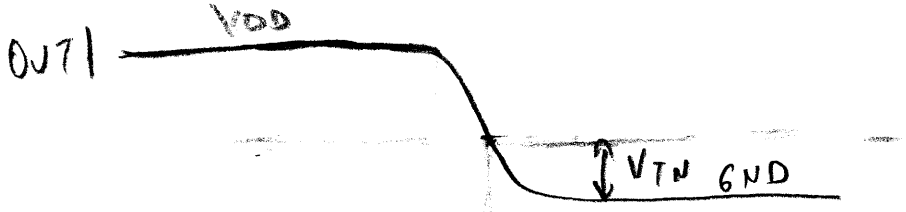


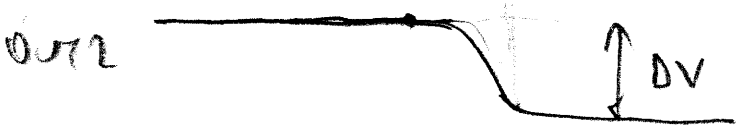
Cascade Series



Domino Logic Buffer





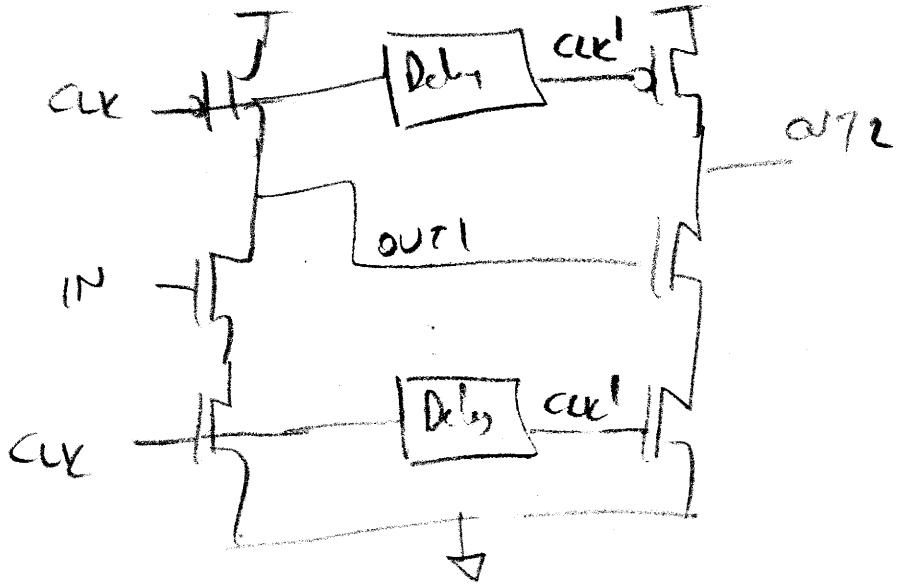


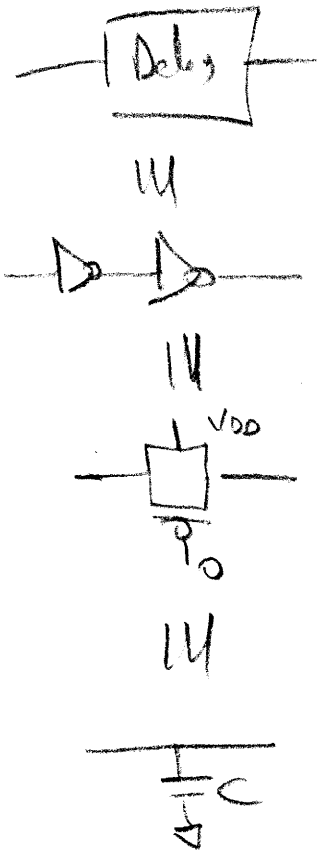
(Not because leakage or shorting)

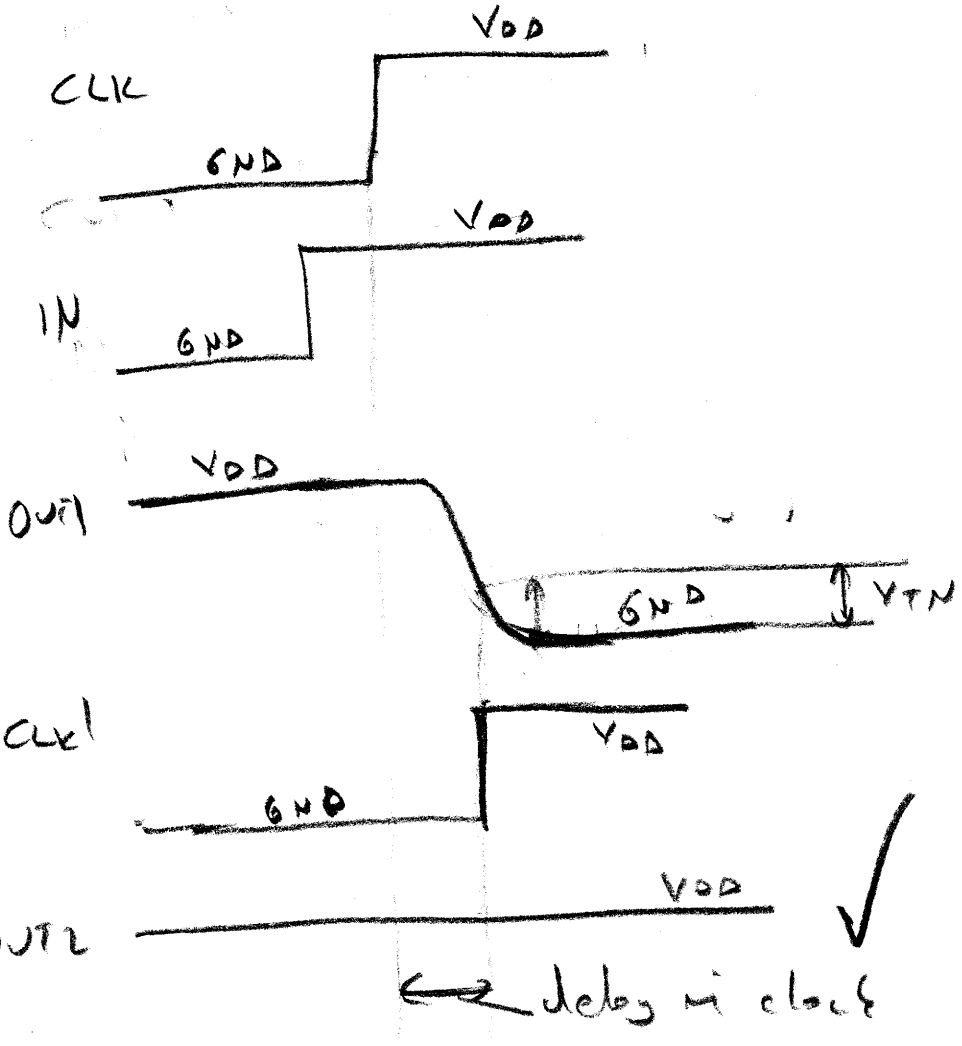
ONLY HAPPENS WHEN IN 1→0

SOLUTIONS

(1) Adding a delay to CLK







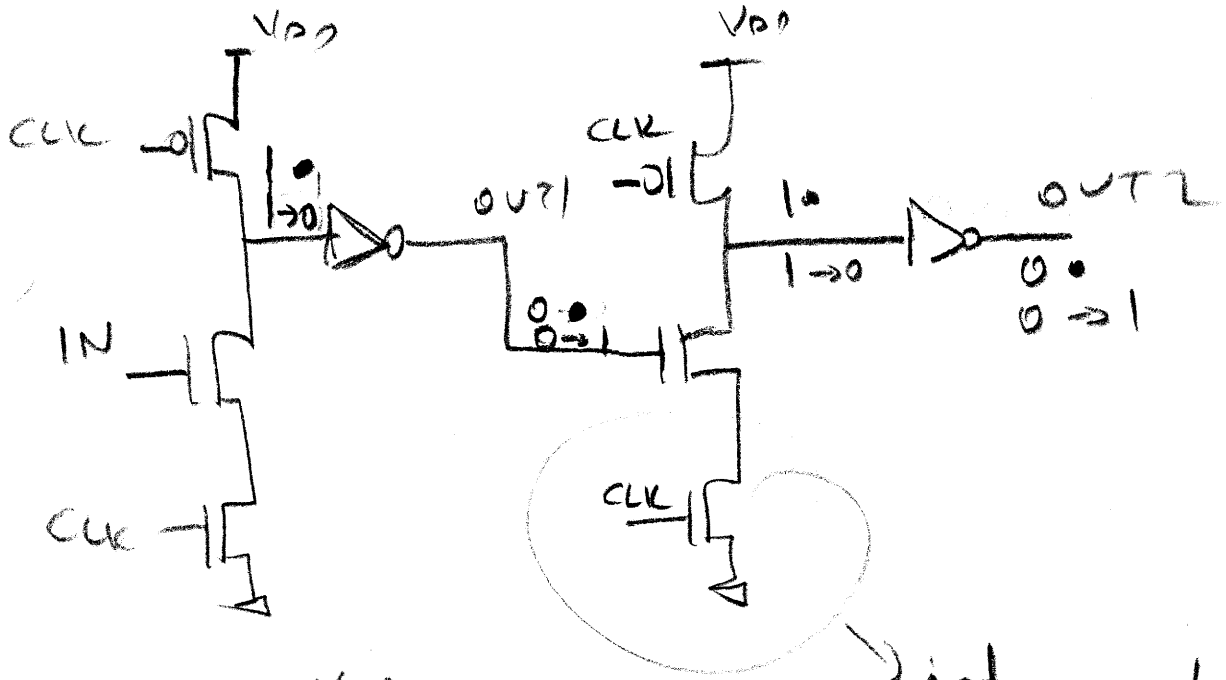
Problems

- Design is challenging

← delay in clock

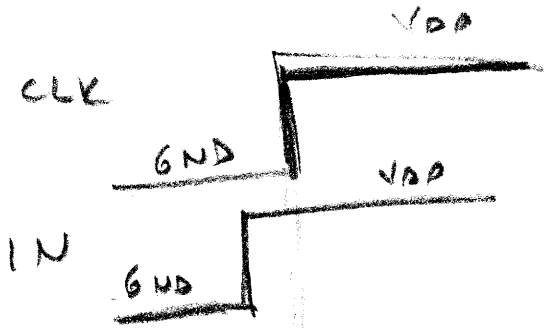
(2) Preventing 1→0 Inputs - DOMINO LOGIC

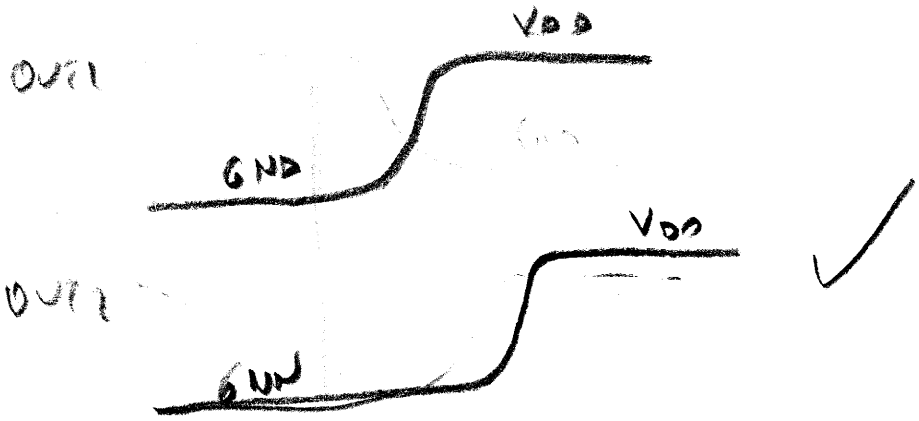
- Adding an Inverter to the outputs



not needed

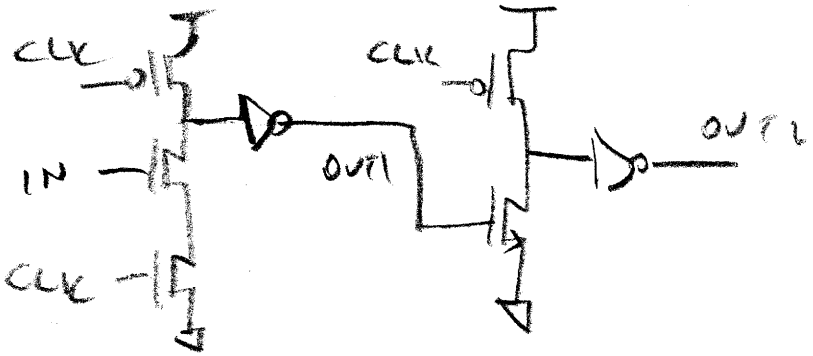
(Footless Domino)



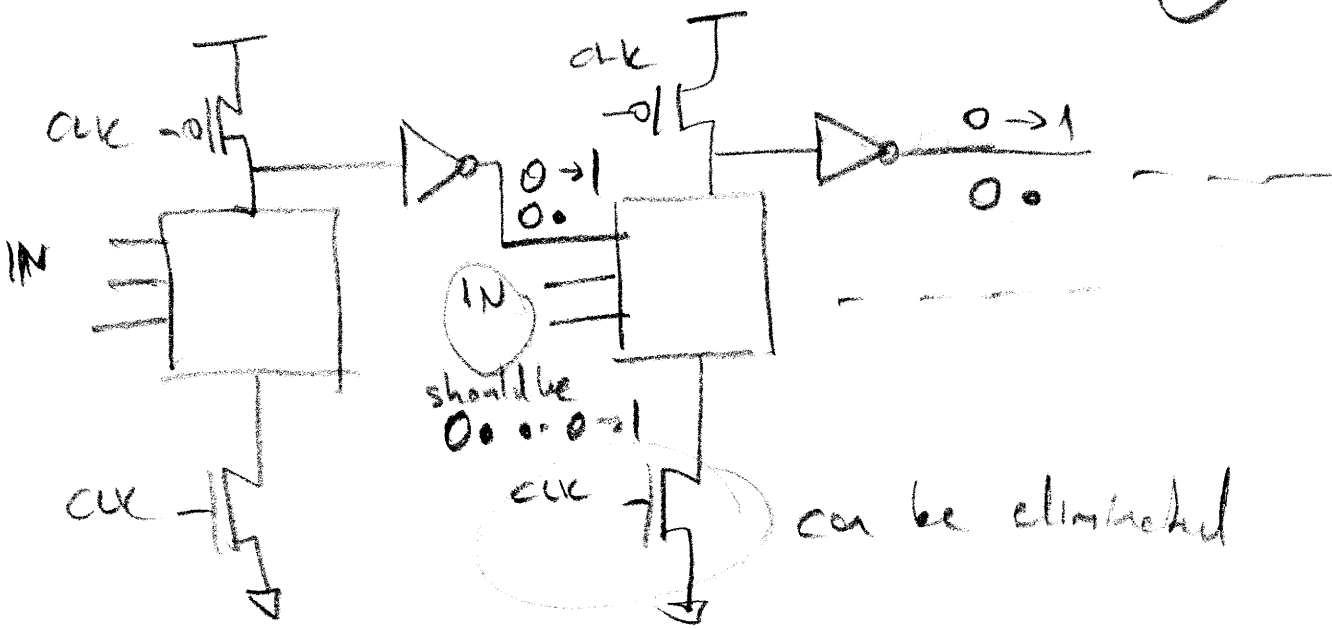


✓

FOOTLESS DOMINO

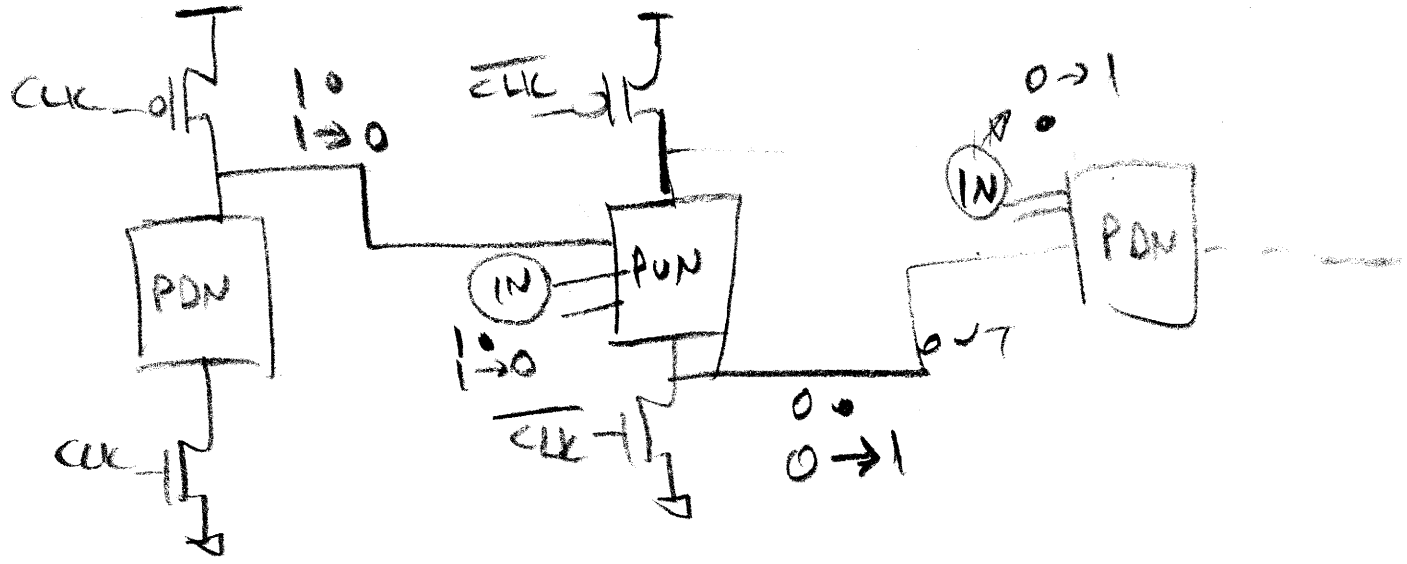


✓



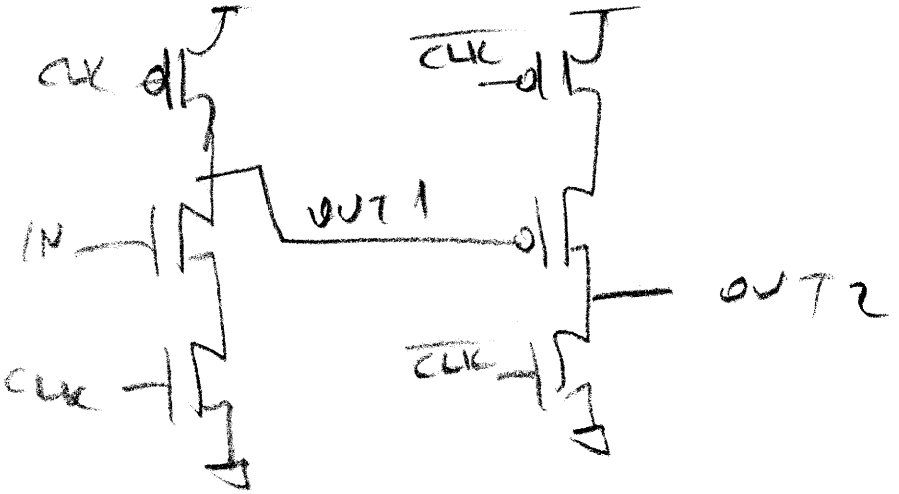
- If inputs are 0 during precharge then the bottom NMOS CLK driven transistor can be eliminated

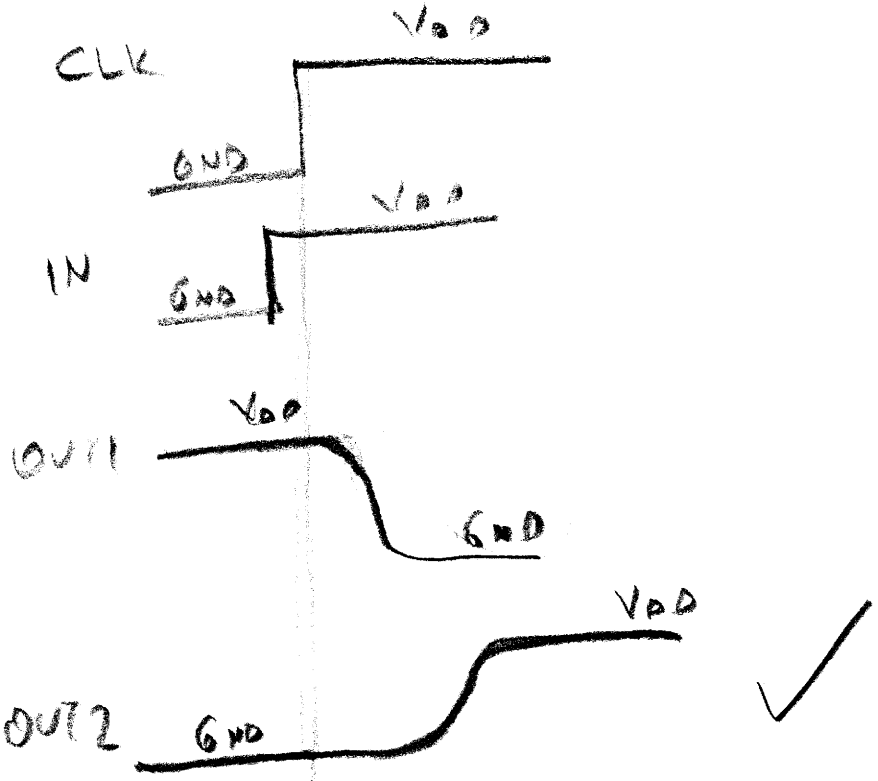
NORA LOGIC



One PDN One PUN

Fast, but very sensitive to noise
design is challenging





Problems in Domino

- Design is challenging
- With cascaded domino not all Boolean functions can be implemented

Inputs ↑ Outputs ↑ positive Boolean functions

Non-inverting logic