Homework-2 Solutions – EHB322E

a) • Complex Gate Circuit

$$f = x_1 x_2 \bar{x_4} + x_1 \bar{x_2} x_3 + x_2 x_3 \bar{x_4} \rightarrow \bar{\bar{f}} = f \rightarrow f = \overline{x_1 x_2 \bar{x_4} + x_1 \bar{x_2} x_3 + x_2 x_3 \bar{x_4}}$$

$$f = \overline{x_1 x_2 \bar{x_4}} \cdot \overline{x_1 \bar{x_2} x_3} \cdot \overline{x_2 x_3 \bar{x_4}} = (\bar{x_1} + \bar{x_2} + x_4) \cdot (\bar{x_1} + x_2 + \bar{x_3}) \cdot (\bar{x_2} + \bar{x_3} + x_4)$$

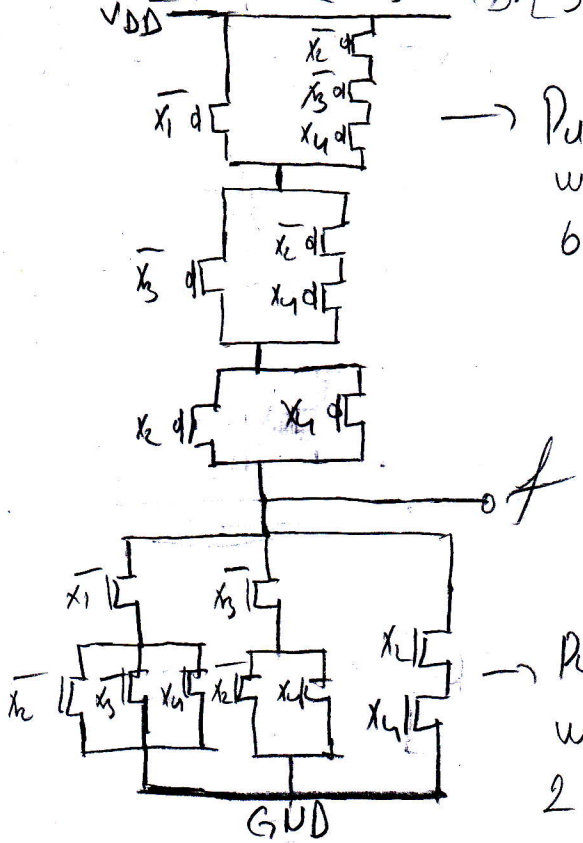
$$f = \overline{(\bar{x_1} + \bar{x_2} \bar{x_3} + x_2 x_4 + \bar{x_3} x_4) \cdot (\bar{x_2} + \bar{x_3} + x_4)}$$

$$f = \overline{\bar{x_1} \bar{x_2} + \bar{x_1} \bar{x_3} + \bar{x_1} x_4 + \bar{x_2} \bar{x_3} + x_2 x_4 + \bar{x_3} x_4} \rightarrow \text{for Pull-Down network}$$

$$= \bar{x_1}(\bar{x_2} + \bar{x_3} + x_4) + \bar{x_3}(\bar{x_2} + x_4) + x_2 x_4$$

⇒ Dual of this expression:

$$\left[\bar{x_1} + (\bar{x_2} \cdot \bar{x_3} \cdot x_4)\right] \cdot \left[\bar{x_3} + \bar{x_2} \cdot x_4\right] \cdot \left[x_2 + x_4\right]$$



→ Pull-up
worst case
6 transistors

→ Pull-down
worst case
2 transistors

b) $t_{PLH(wc)} = 0.69 \cdot 6.2,6.10^3 \cdot 10.10^{-12}$

$= 107,64$ ns

$t_{PHL(wc)} = 0,69 \cdot 2 \cdot 4,7 \cdot 10^3 \cdot 10.10^{-12}$

$= 64,86$ ns

NMOS PTL → $f = x_1 x_2 \bar{x_4} + x_1 \bar{x_2} x_3 + x_2 x_3 \bar{x_4}$

Shannon expansion $x_4 \rightarrow x_3 \rightarrow x_2 \rightarrow x_1$

$\Rightarrow x_1 x_2 \bar{x_4}(x_3 + \bar{x_3}) + x_1 \bar{x_2} x_3 (x_4 + \bar{x_4}) + x_2 x_3 \bar{x_4} (x_1 + \bar{x_1})$

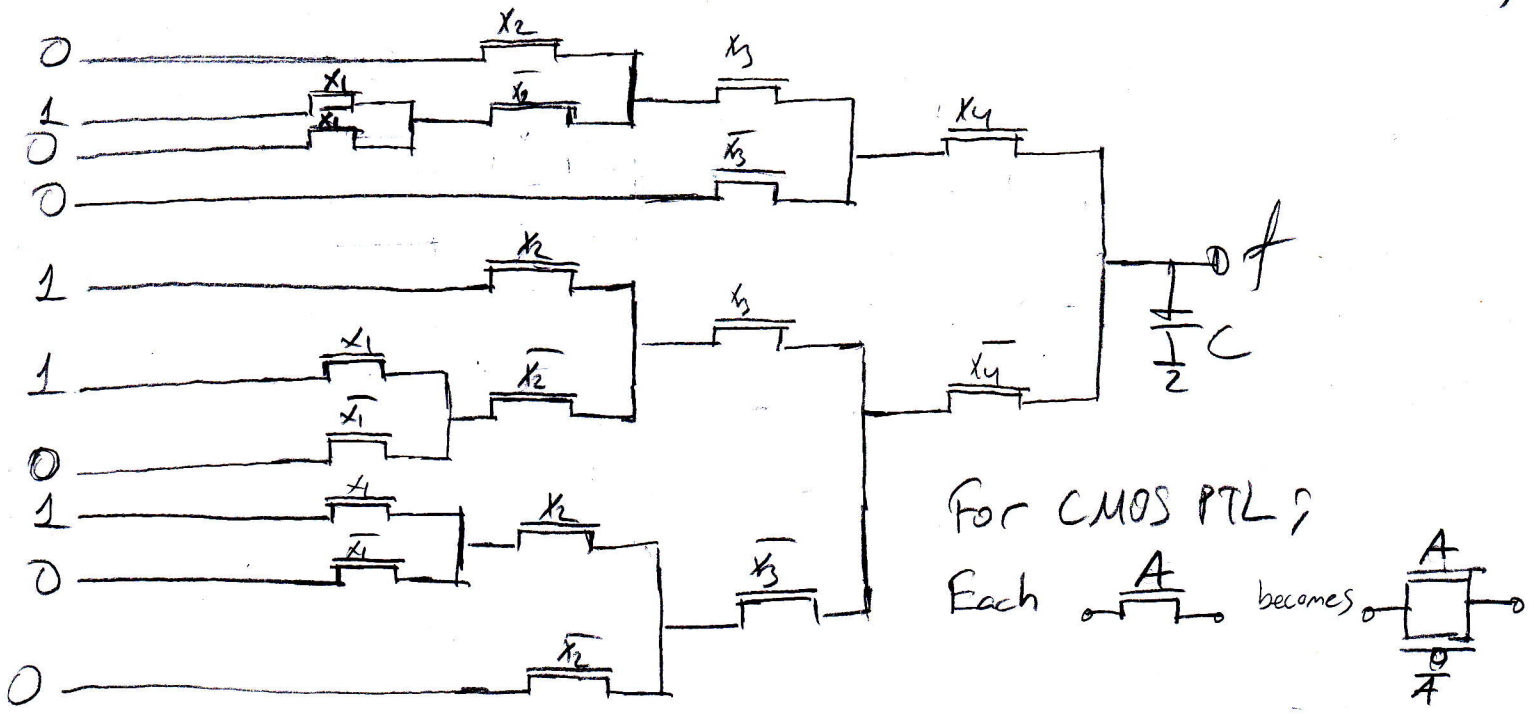
$\Rightarrow x_1 x_2 x_3 \bar{x_4} + x_1 x_2 \bar{x_3} \bar{x_4} + x_1 \bar{x_2} x_3 x_4 + x_1 \bar{x_2} x_3 \bar{x_4} + \cancel{x_1 x_2 x_3 x_4} + \bar{x_1} x_2 x_3 \bar{x_4}$

$\Rightarrow x_4 (x_1 \bar{x_2} x_3) + \bar{x_4} (x_1 x_2 x_3 + x_1 x_2 \bar{x_3} + x_1 \bar{x_2} x_3 + \bar{x_1} x_2 x_3)$

$x_4 (x_3 (x_1 \bar{x_2}) + \bar{x_3}(0)) + \bar{x_4} (x_3 (x_1 x_2 + x_1 \bar{x_2} + \bar{x_1} x_2) + \bar{x_3} (x_1 x_2))$

$x_4 (x_3 (x_2(0) + \bar{x_2}(x_1)) + \bar{x_3}(0)) + \bar{x_4} (x_3 (x_2 (x_1 + \bar{x_1}) + \bar{x_2}(x_1)) + \bar{x_3}(x_2(x_1) + \bar{x_2}(0)))$

$x_4 (x_3 (x_2(0) + \bar{x_2}(x_1(1) + \bar{x_1}(0))) + \bar{x_3}(0)) + \bar{x_4} (x_3 (x_2(1) + \bar{x_2}(x_1(1) + \bar{x_1}(0))) + \bar{x_3}(x_2(x_1(1) + \bar{x_1}(0)) + \bar{x_2}(0)))$



1.b) NMOS PTL → 4 transistors on H→L and L→H paths

$t_{PLH(WC)} = 0.69 \cdot 4 \cdot R_n \cdot C_{out} = 0.69 \cdot 4 \cdot 4.7 \cdot 10^3 \cdot 10 \cdot 10^{-12}$
$= 129.72\ ns$

$t_{PHL(WC)} = 0.69 \cdot 4 \cdot R_n \cdot C_{out} = 129.72\ ns$

b) CMOS PTL → 4 transmission gates on H→L and L→H paths

$t_{PLH(WC)} = 0.69 \cdot 4 \cdot (R_n \| R_p) \cdot C_{out} = 0.69 \cdot 4 \cdot (4.7 \cdot 10^3 \| 2.6 \cdot 10^3) \times 10 \cdot 10^{-12}$
$= 0.69 \cdot 4 \cdot 1677 \cdot 10 \cdot 10^{-12} = 46.28\ ns$

$t_{PHL(WC)} = 0.69 \cdot 4 \cdot (R_n \| R_p) \cdot C_{out} = 46.28\ ns$