Student Name: **Instructor: Mustafa Altun**

Student ID:

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EHB322E Digital Electronic Circuits
MIDTERM II

Duration: 120 Minutes

Grading: 1) 30%, 2) 30%, 3) 40%

Exam is in closed-notes and closed-books format; calculators are allowed

For your answers please use the space provided in the exam sheet

GOOD LUCK!

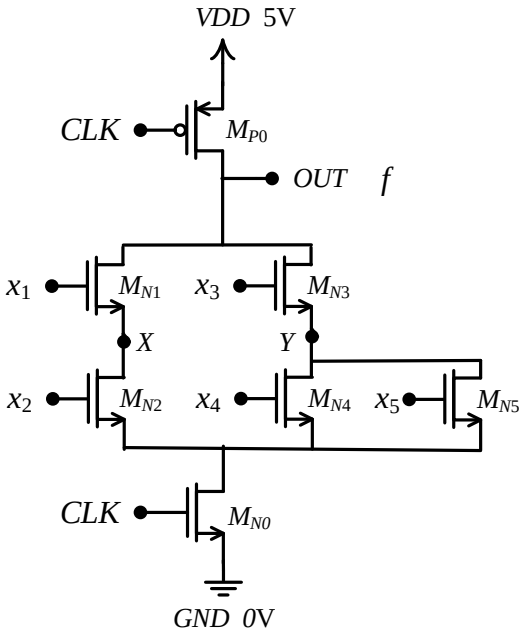
1) Consider a Boolean function $f = x_1x_2\overline{x_3} + x_1\overline{x_2}x_3 + \overline{x_1}x_2x_3 + \overline{x_1}\,\overline{x_2}\,\overline{x_3}$ to be implemented. Suppose that all NMOS transistors are identical and all PMOS transistors are identical.
Equivalent resistor for an NMOS transistor: $\boldsymbol{R_N = 8k\Omega}$
Equivalent resistor for a PMOS transistor: $\boldsymbol{R_P = 24k\Omega}$
Suppose that each circuit node (including outputs) has a capacitance value of **10pF**.

Implement ***f*** with "an NMOS and PMOS (CMOS) Pass Transistor Logic" using the ordering of $x_1 - x_2 - x_3$. Find the **minimum number** of transistors needed. Find the **worst case (largest)** and **the best case (smallest)** $\mathbf{t_{PHL}}$ and $\mathbf{t_{PLH}}$ values (total of 4 values).

- ***Hint:*** *in calculating delay values, use Elmore delay model.*

2) Consider a dynamic logic circuit shown below.

- Suppose that each transistor has an internal grounded gate capacitor C_G and drain capacitor C_D:
  C_G= c_{ox}W L; **C_D= (c_{ox}W L)**/2; c_{ox}=1 pF/um^2.
- Suppose that all NMOS transistors are identical and all PMOS transistors are identical.
- $W_{N0}=W_{N1}=W_{N2}=W_{N3}==W_{N4}=W_{N5}$=1u, W_{P0}=3u, L=1u, and $V_{TN}=|V_{TP}|$=1V.



Dynamic Logic Circuit

a) Derive a Boolean expression of $\boldsymbol{f}$ in terms of the inputs x_1 through x_5 in evaluation phase.

b) At the start of the evaluation phase suppose that $x_1 = 0 \longrightarrow 1$, $x_2 = 0$, $x_3 = 0 \longrightarrow 1$, $x_4 = 0$, $x_5 = 0$, and V_X = 0V, V_Y = 0V, V_{OUT} = 5V. Considering the charge share problem, find the final voltage value at the output.

c) To make the final voltage value at the output as 4.5V, determine the capacitor value of a load to drive.

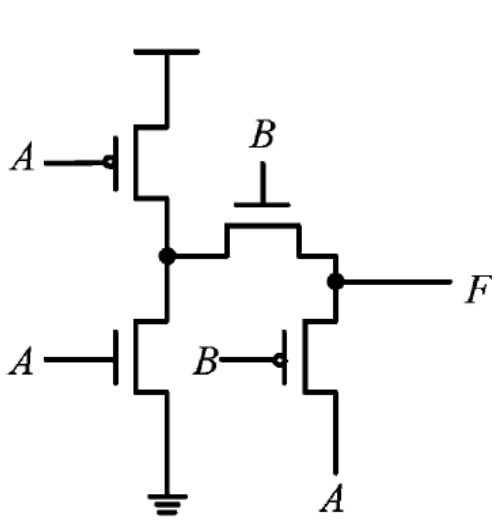
3) Consider the circuits in (a) and (b).

- Suppose that all NMOS transistors are identical and all PMOS transistors are identical.
  Equivalent resistor for an NMOS transistor: $\boldsymbol{R_N = 8k\Omega}$
  Equivalent resistor for a PMOS transistor: $\boldsymbol{R_P = 24k\Omega}$
- Suppose that each circuit node (including outputs) has a capacitance value of **10pF**.

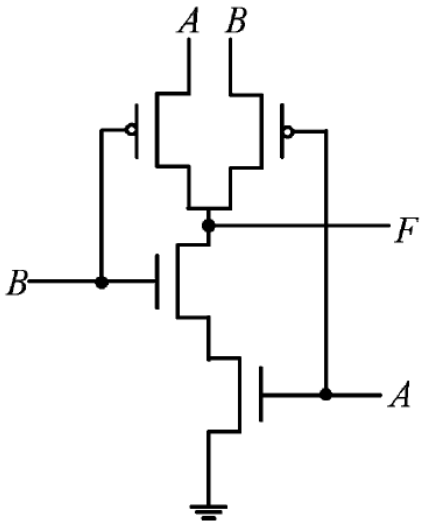
For both of the circuits,

a) Derive Boolean expressions for the output ***F*** in terms of inputs **A** and **B** (2 expressions).

b) Calculate the worst case and best case propagation delays, $\boldsymbol{t_{PLH}}$ and $\boldsymbol{t_{PHL}}$ values (total of 8 values).



(a)



(b)