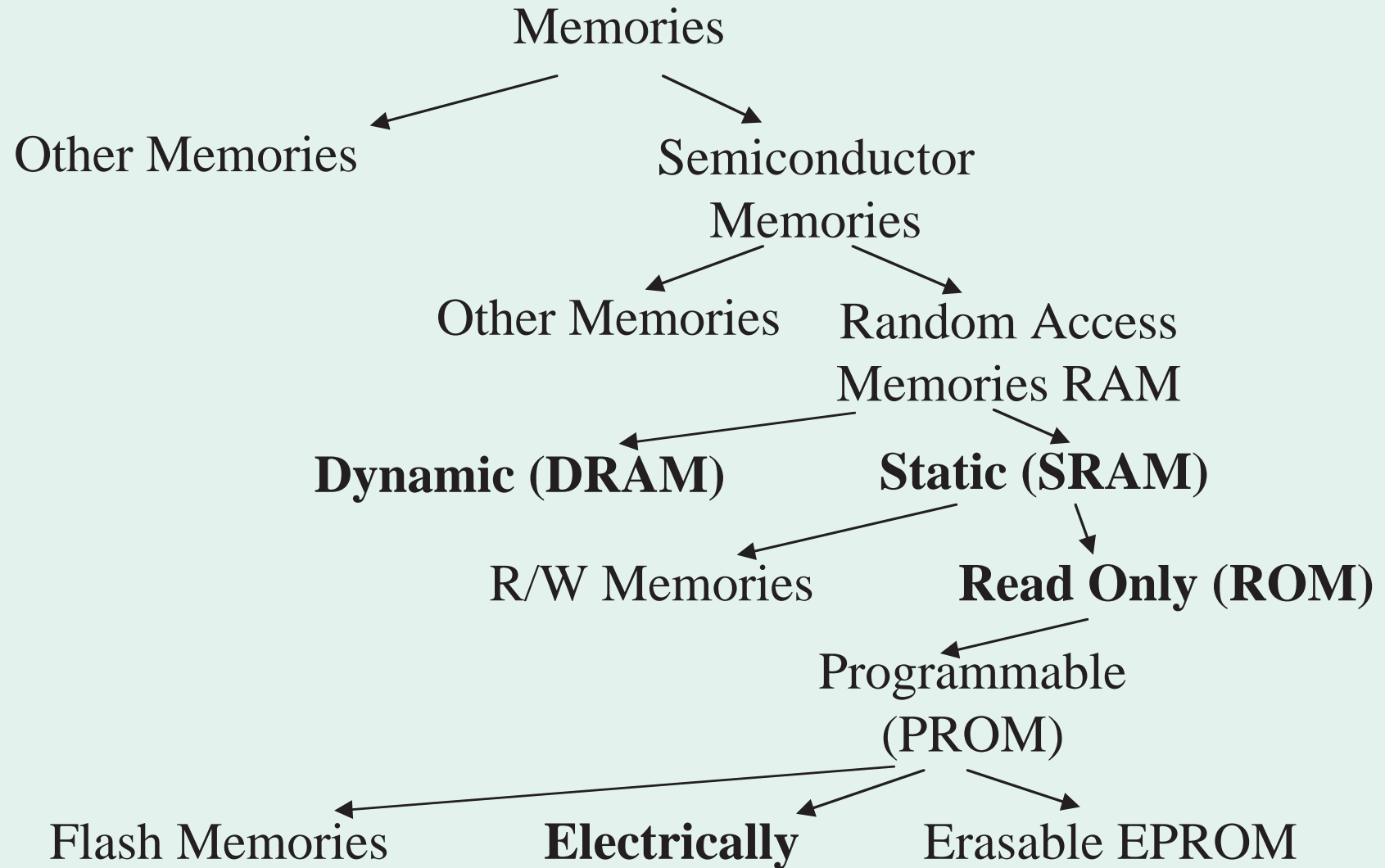


Static Random Access

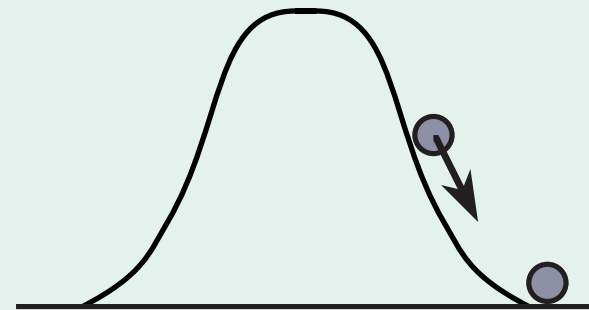
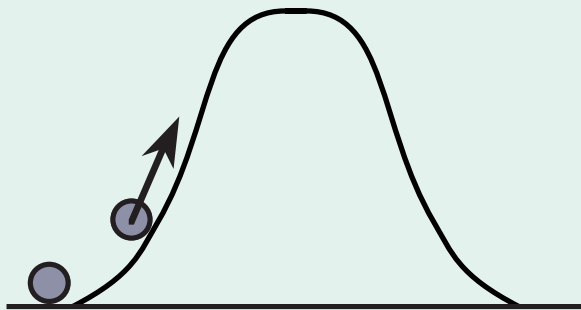
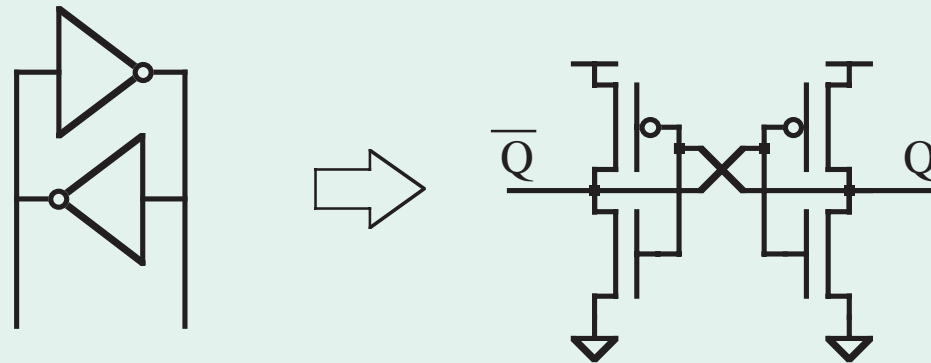
- **Memory Classification**
- **CMOS static memory**
 - Six transistor memory cell
 - Memory architecture
 - Decoders
 - Read/Write circuitry
- **RMOS static memory**
 - Four transistor memory cell
 - Technology
 - Memory cell layout

Memory Classification



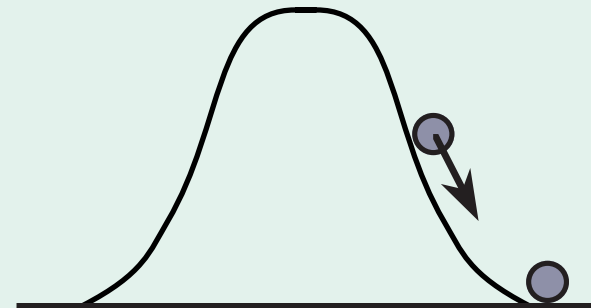
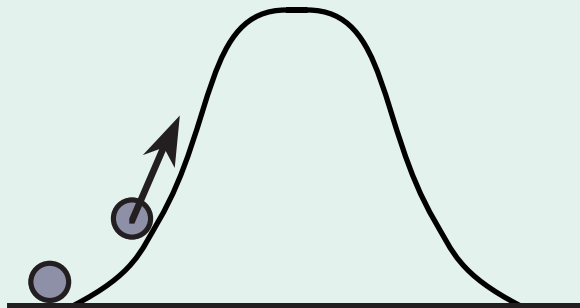
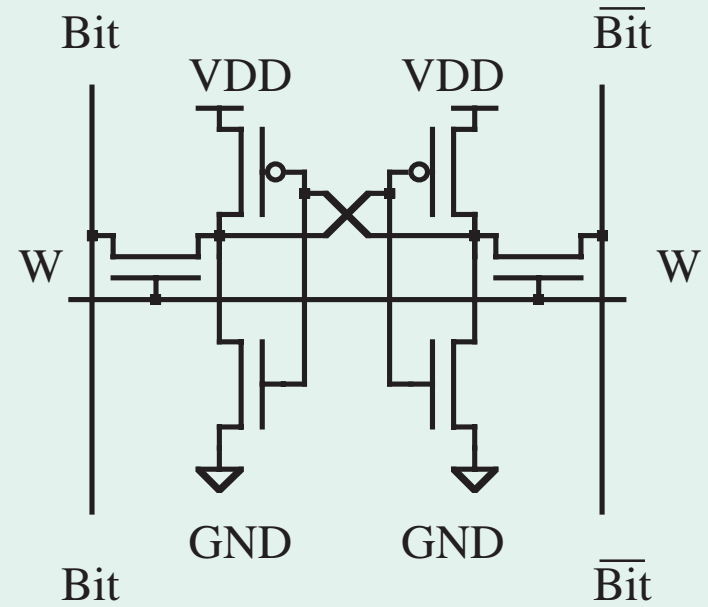
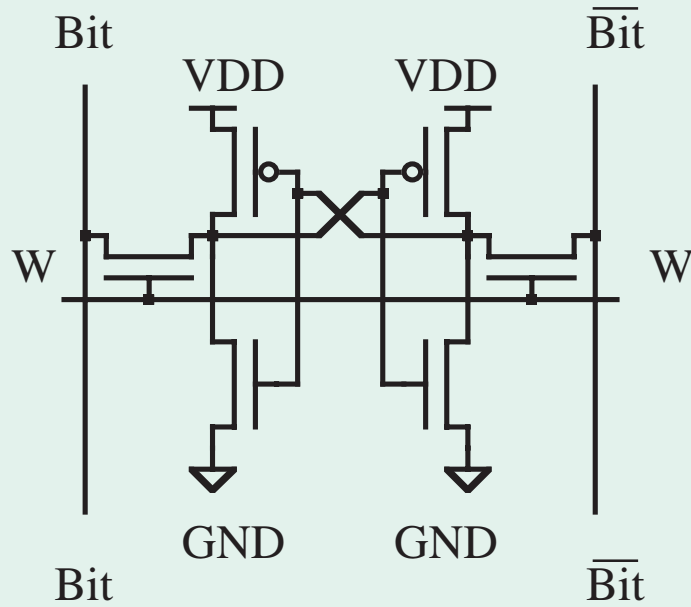
CMOS static memory

Six transistor memory cell



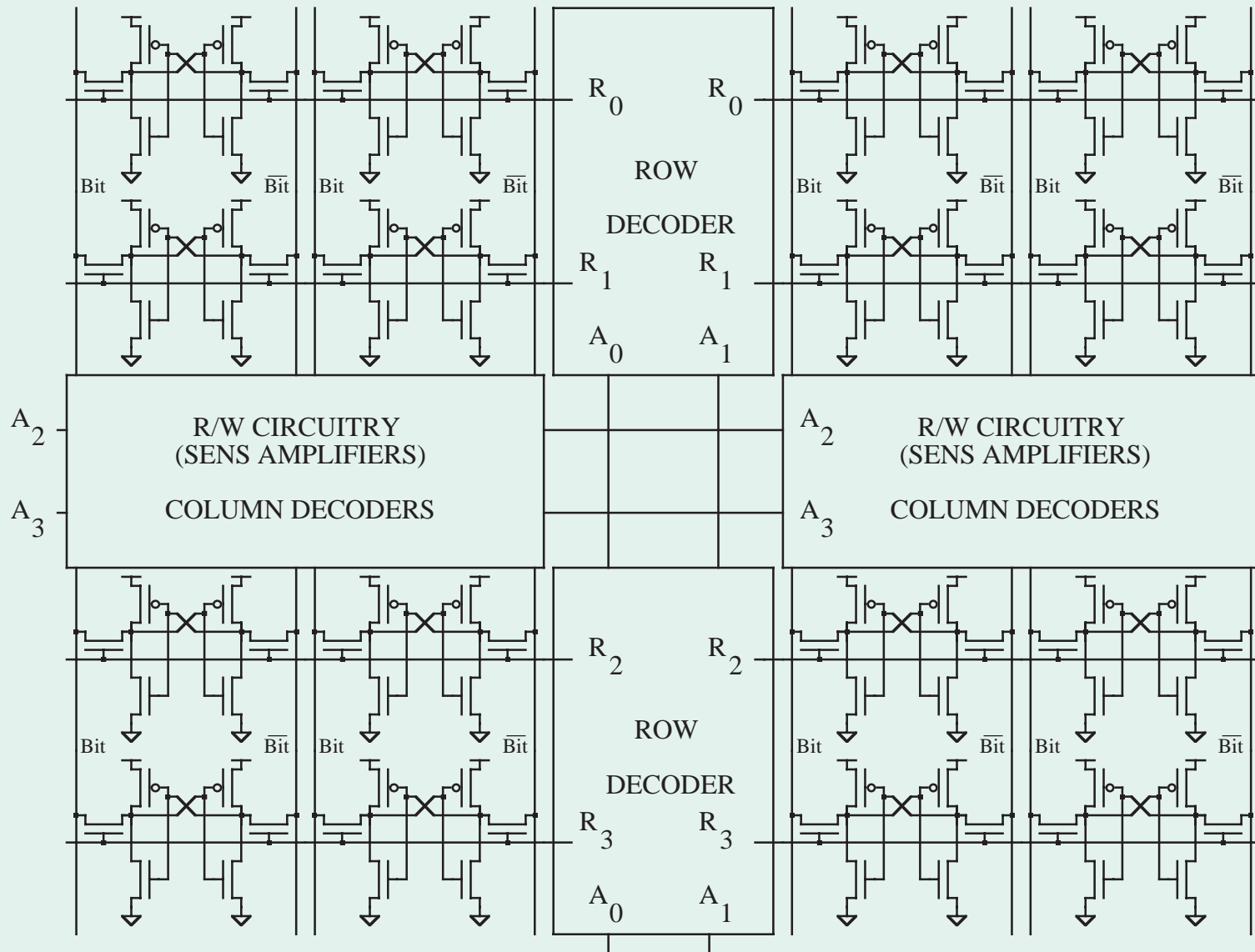
CMOS static memory

Six transistor memory cell



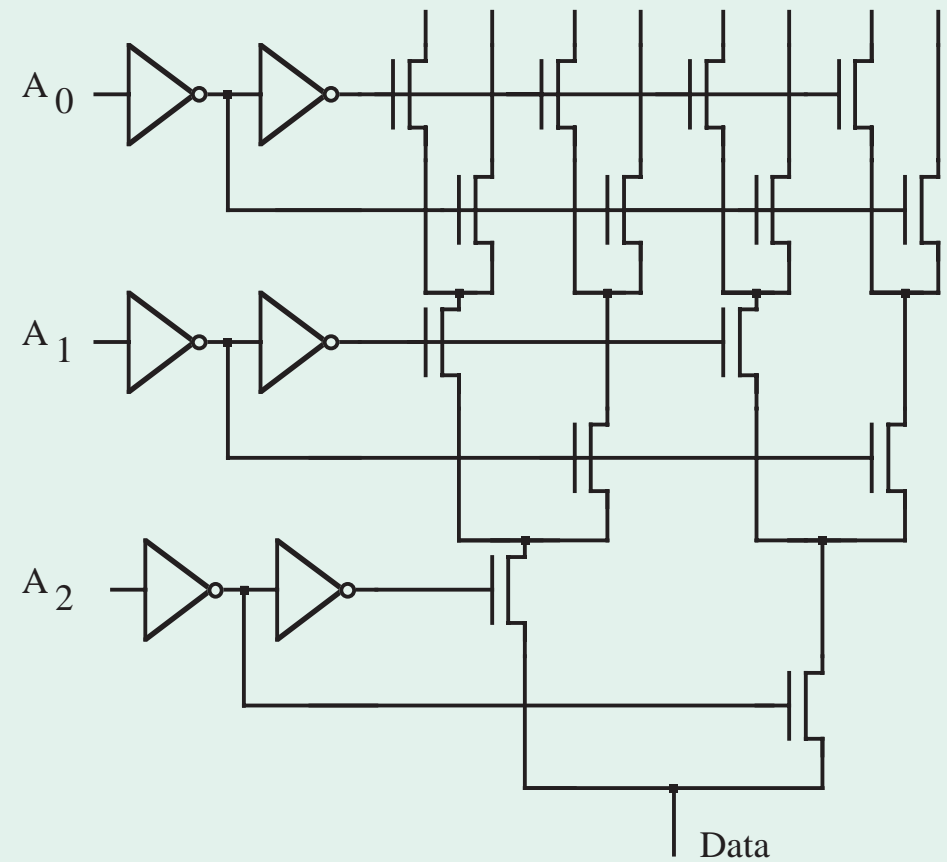
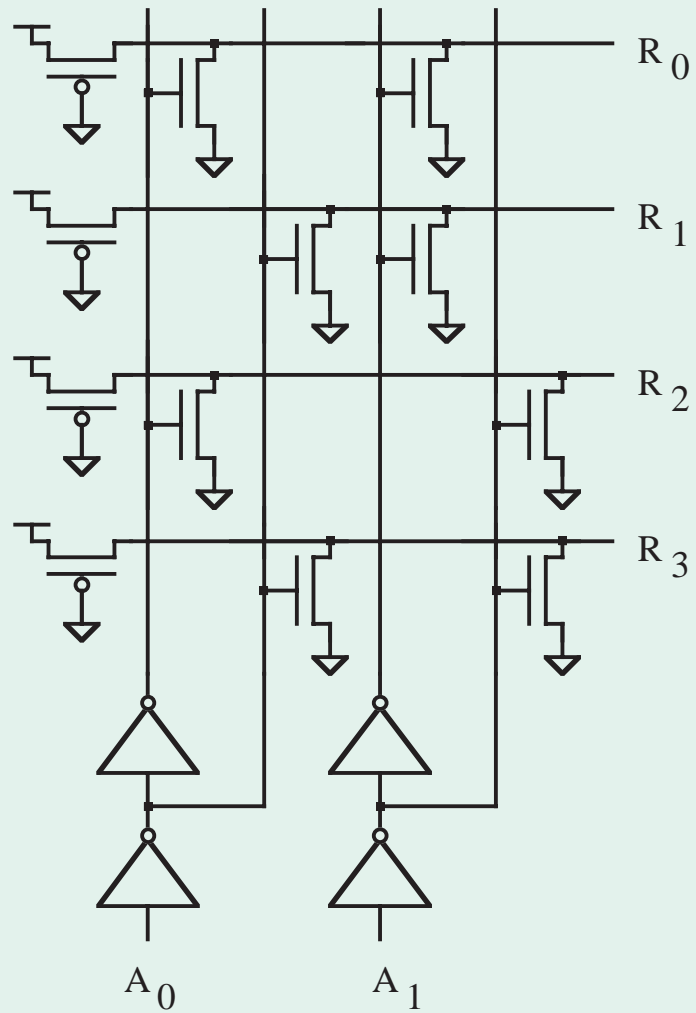
CMOS static memory

Memory architecture



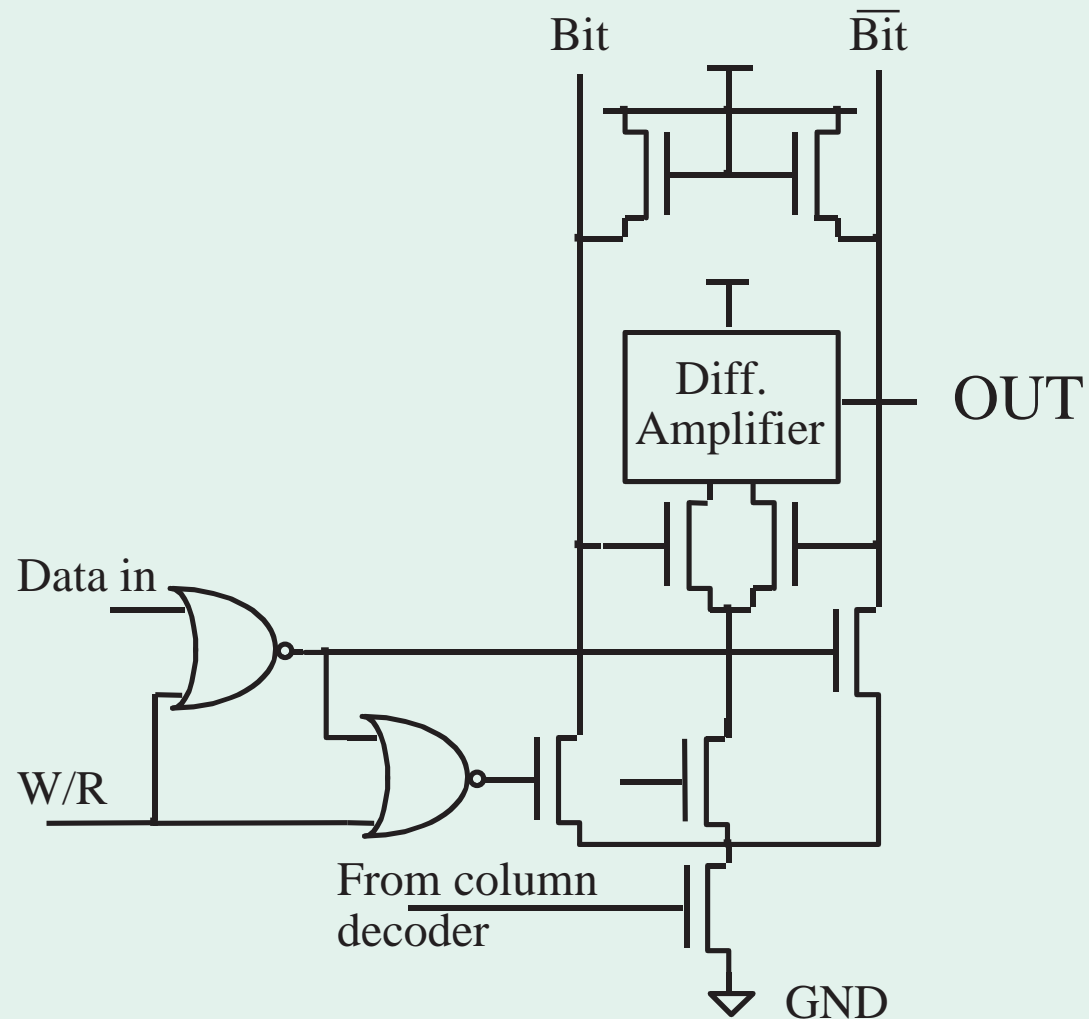
CMOS static memory

Decoders



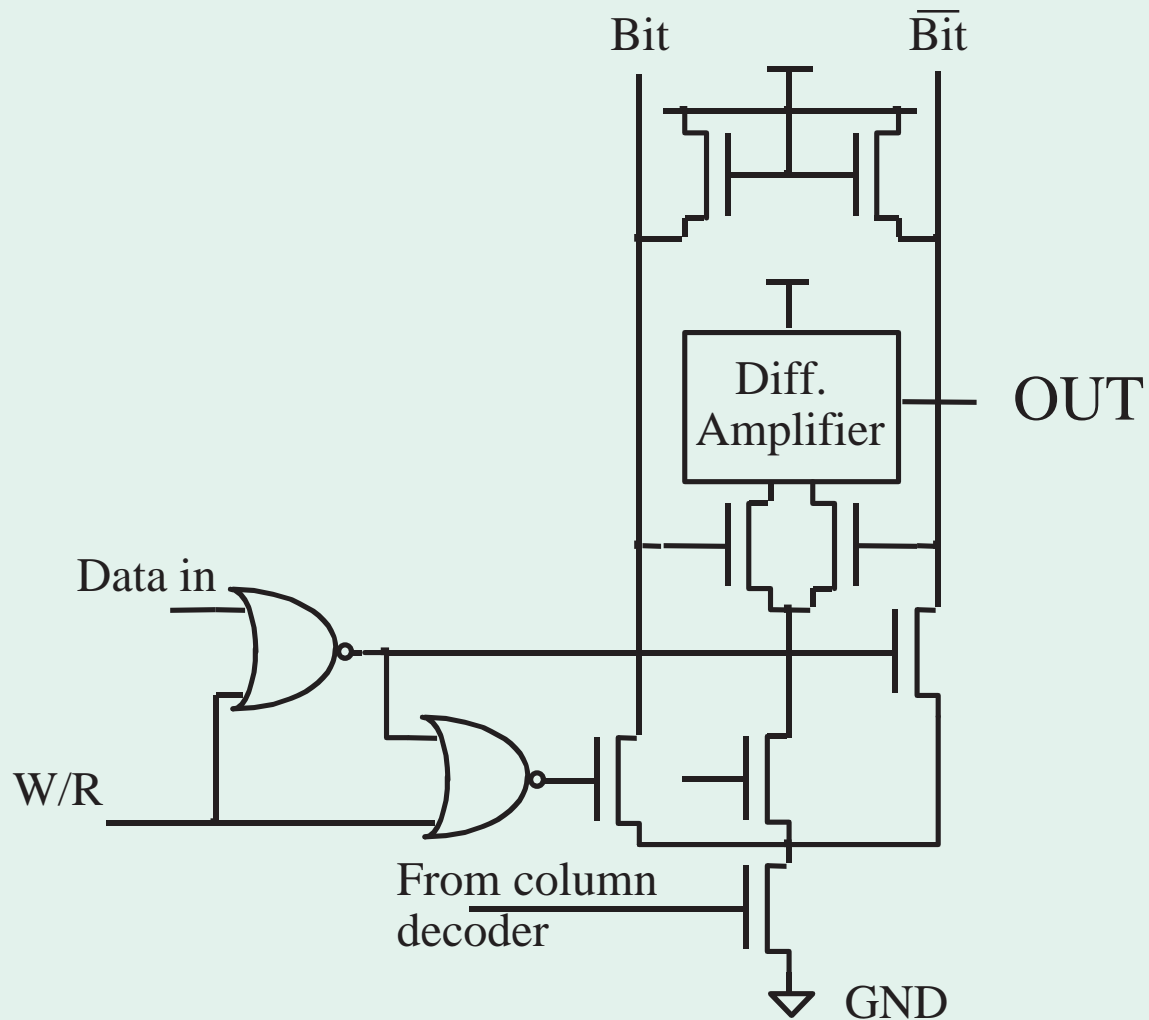
CMOS static memory

Read/Write circuitry



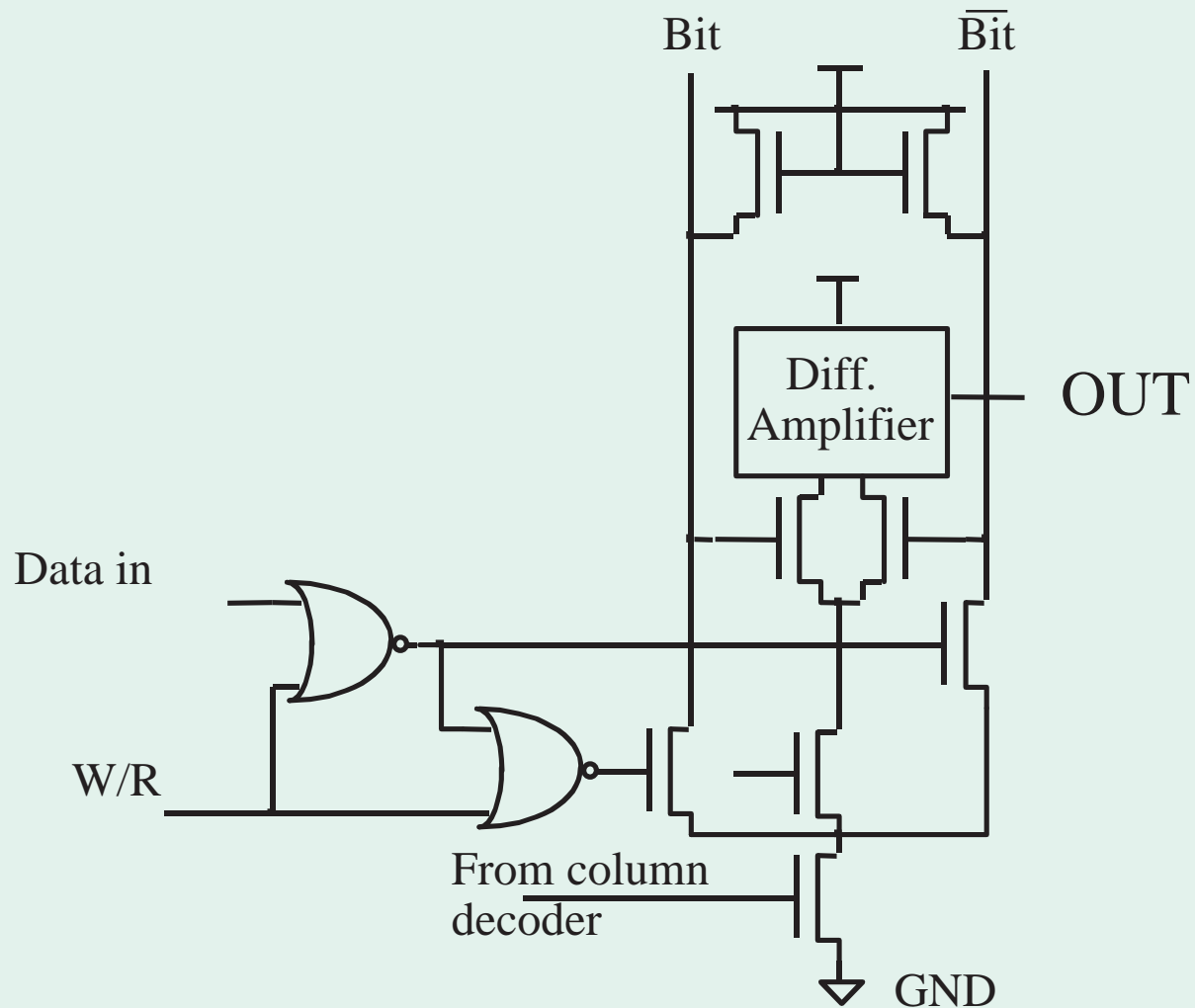
CMOS static memory

Read



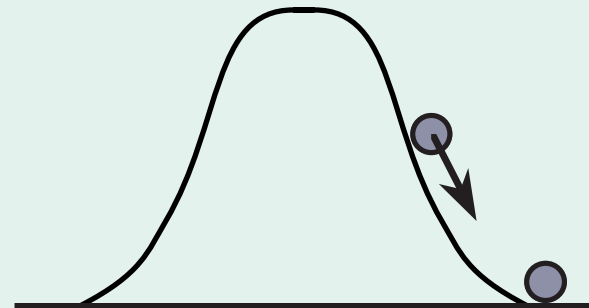
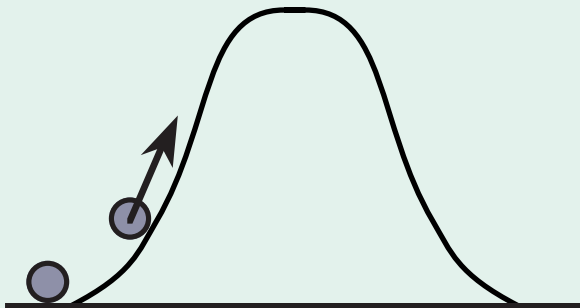
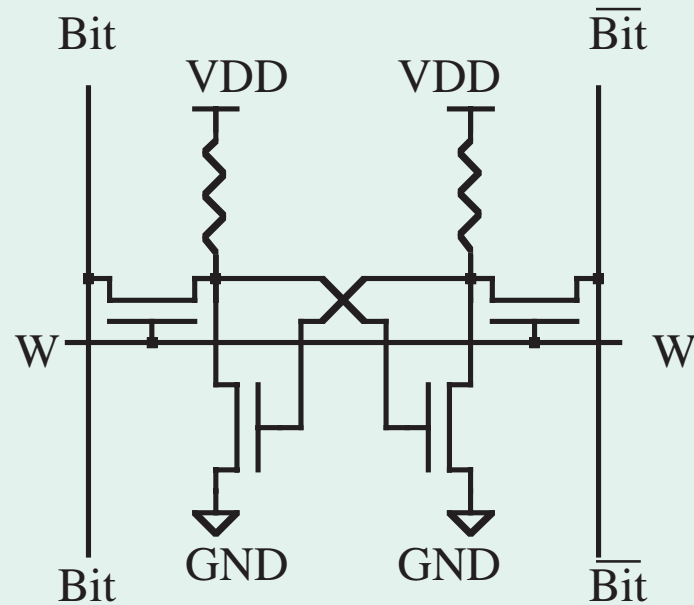
CMOS static memory

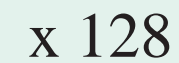
Write



RMOS static memory

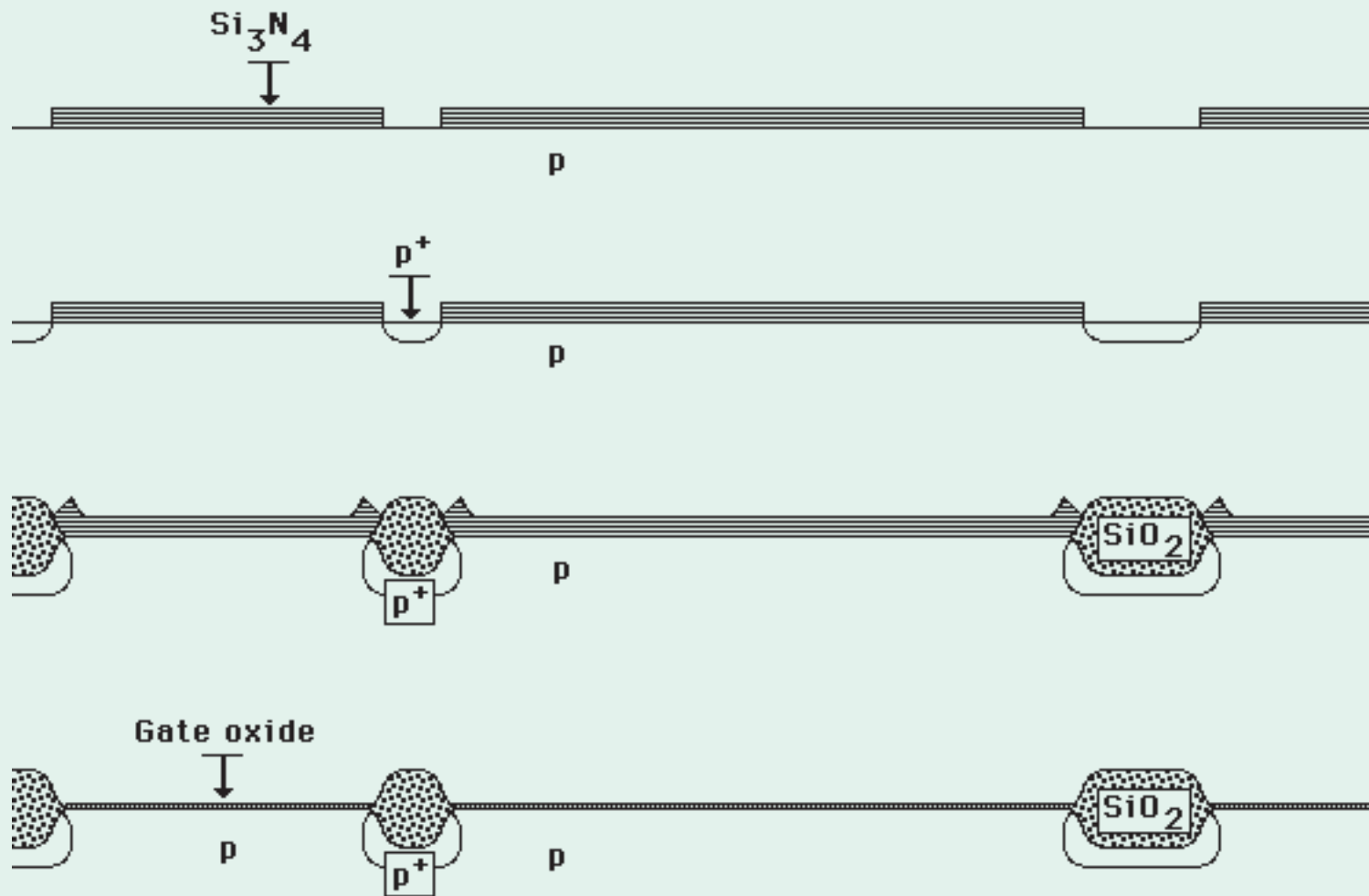
Four transistor memory cell





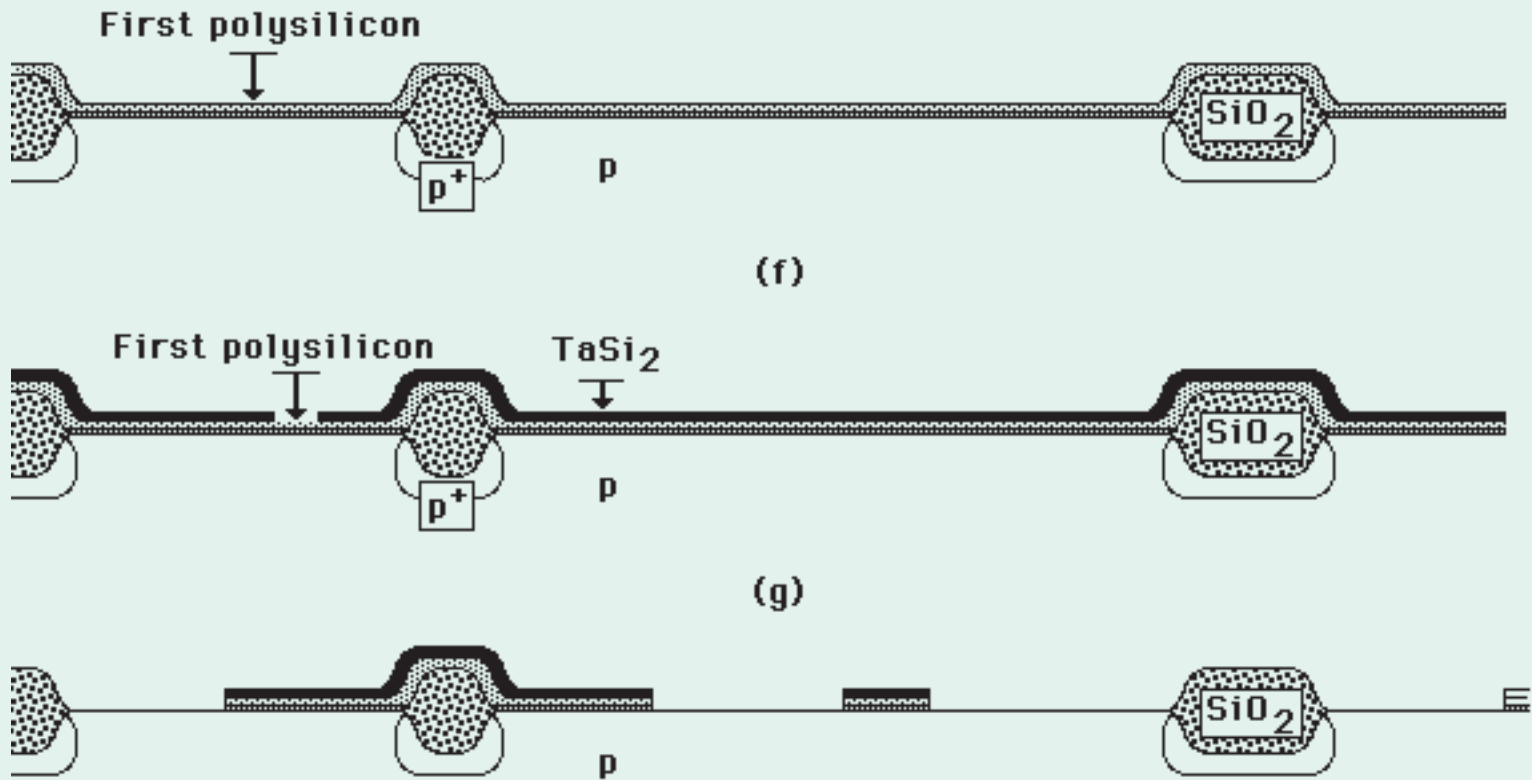
RMOS static memory

Technology



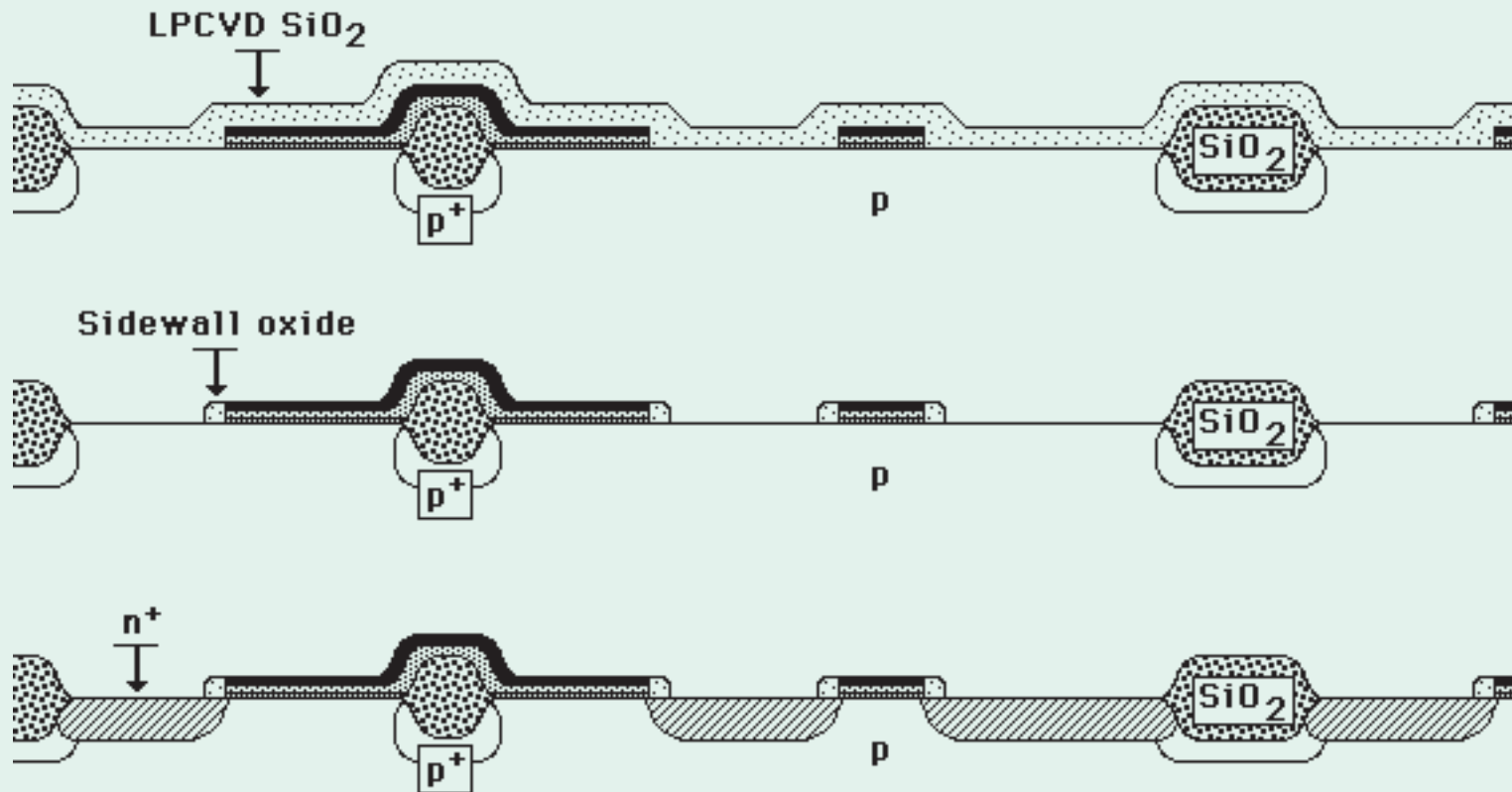
RMOS static memory

Technology



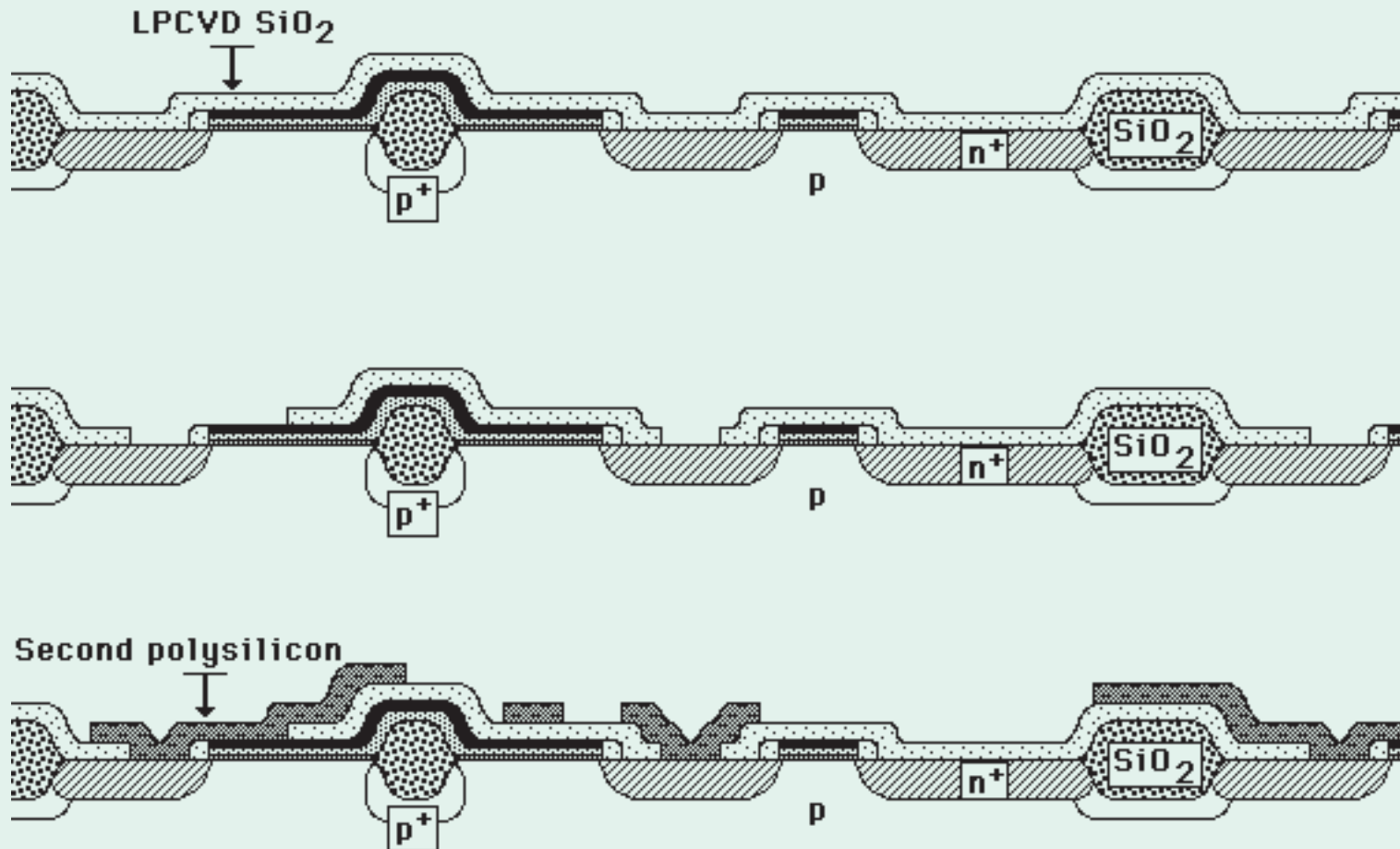
RMOS static memory

Technology



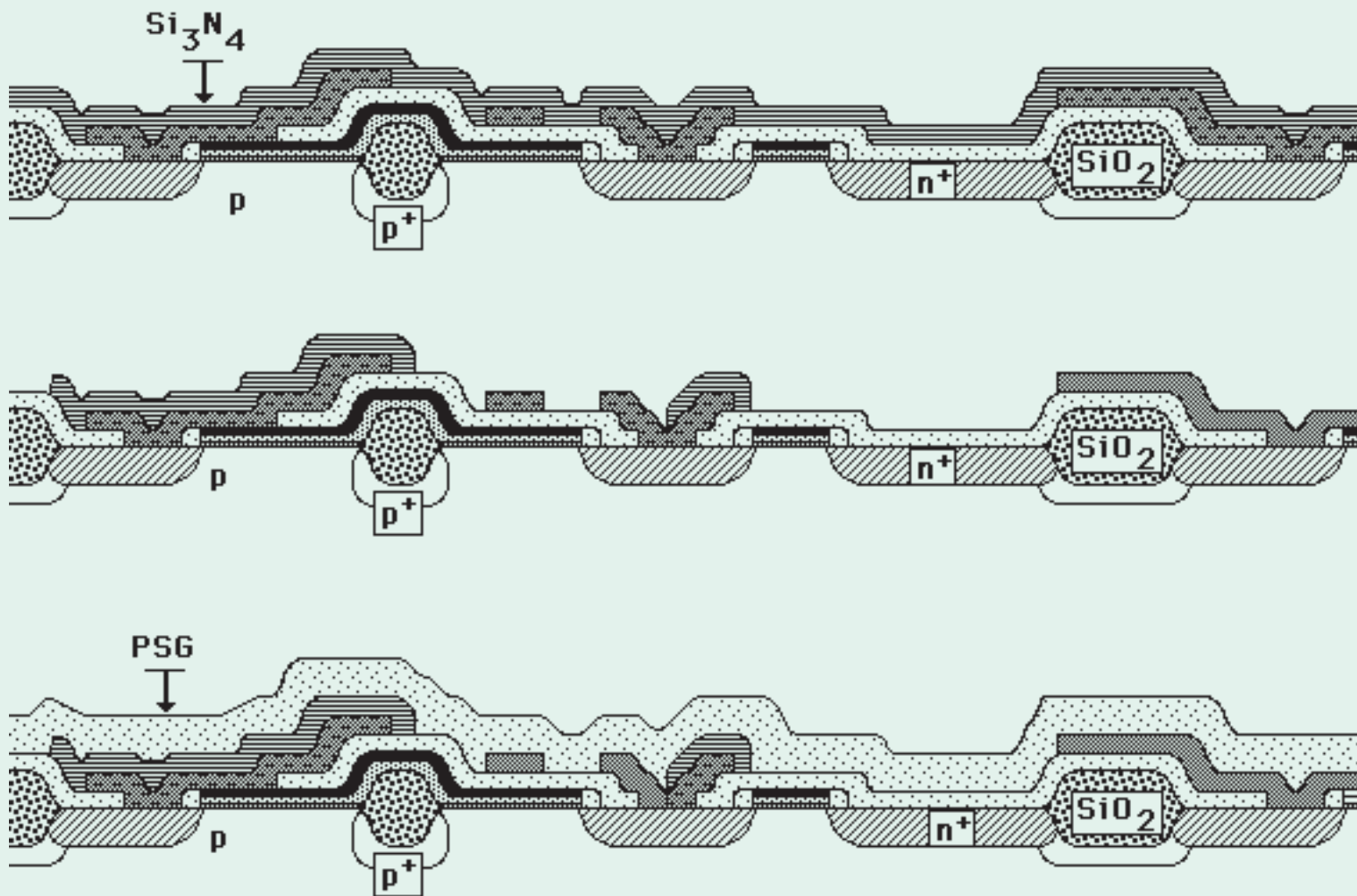
RMOS static memory

Technology



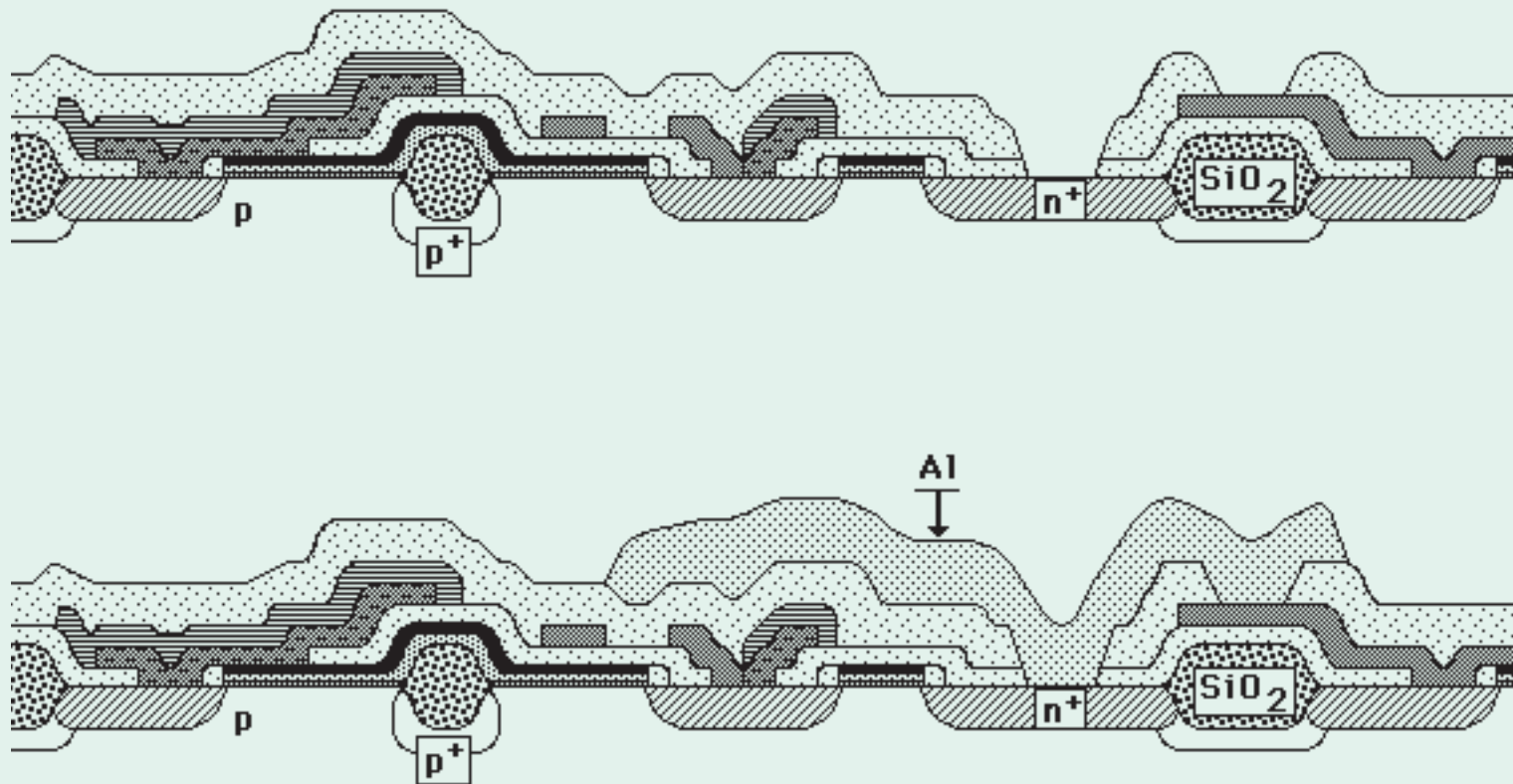
RMOS static memory

Technology

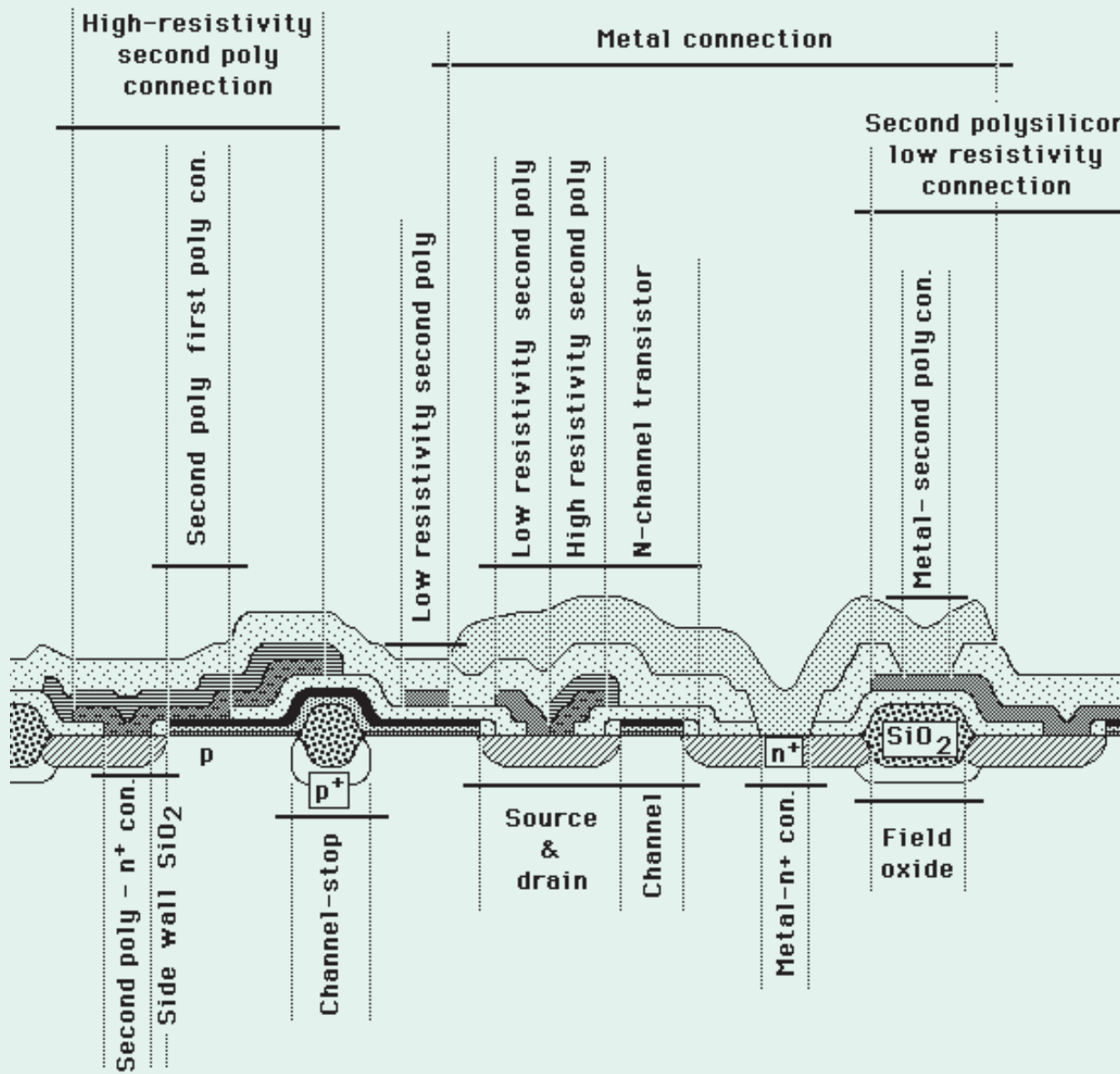


RMOS static memory

Technology

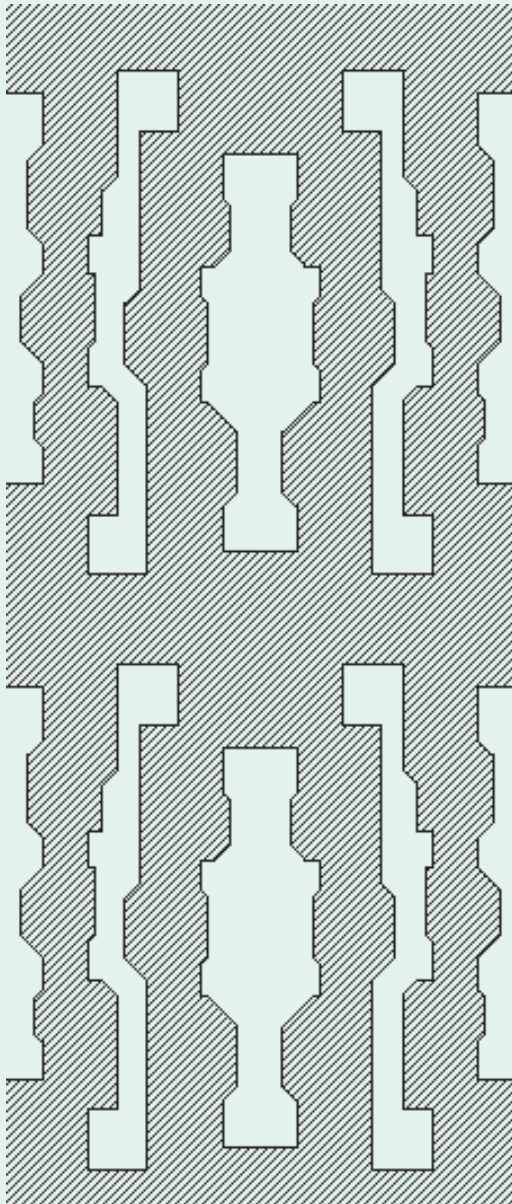


RMOS static memory Technology



RMOS static memory

Cell layout

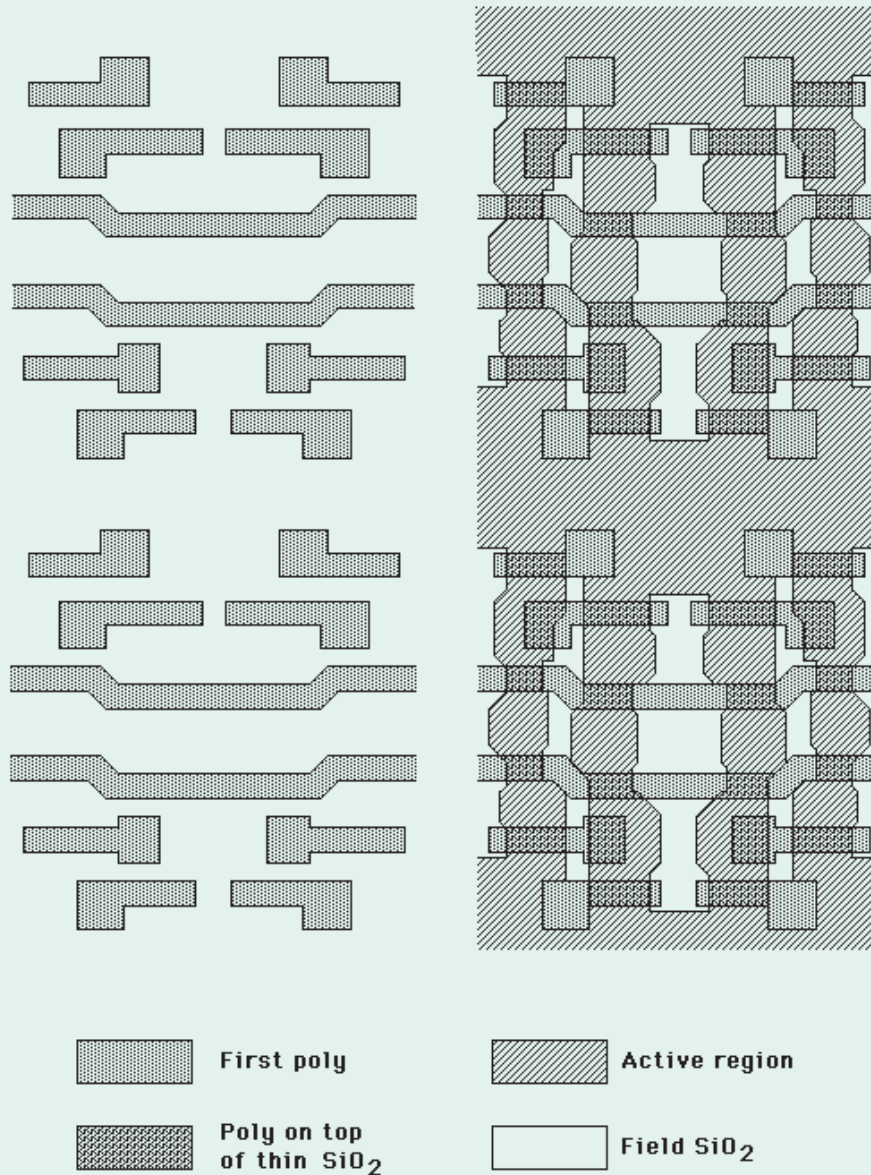


Active region

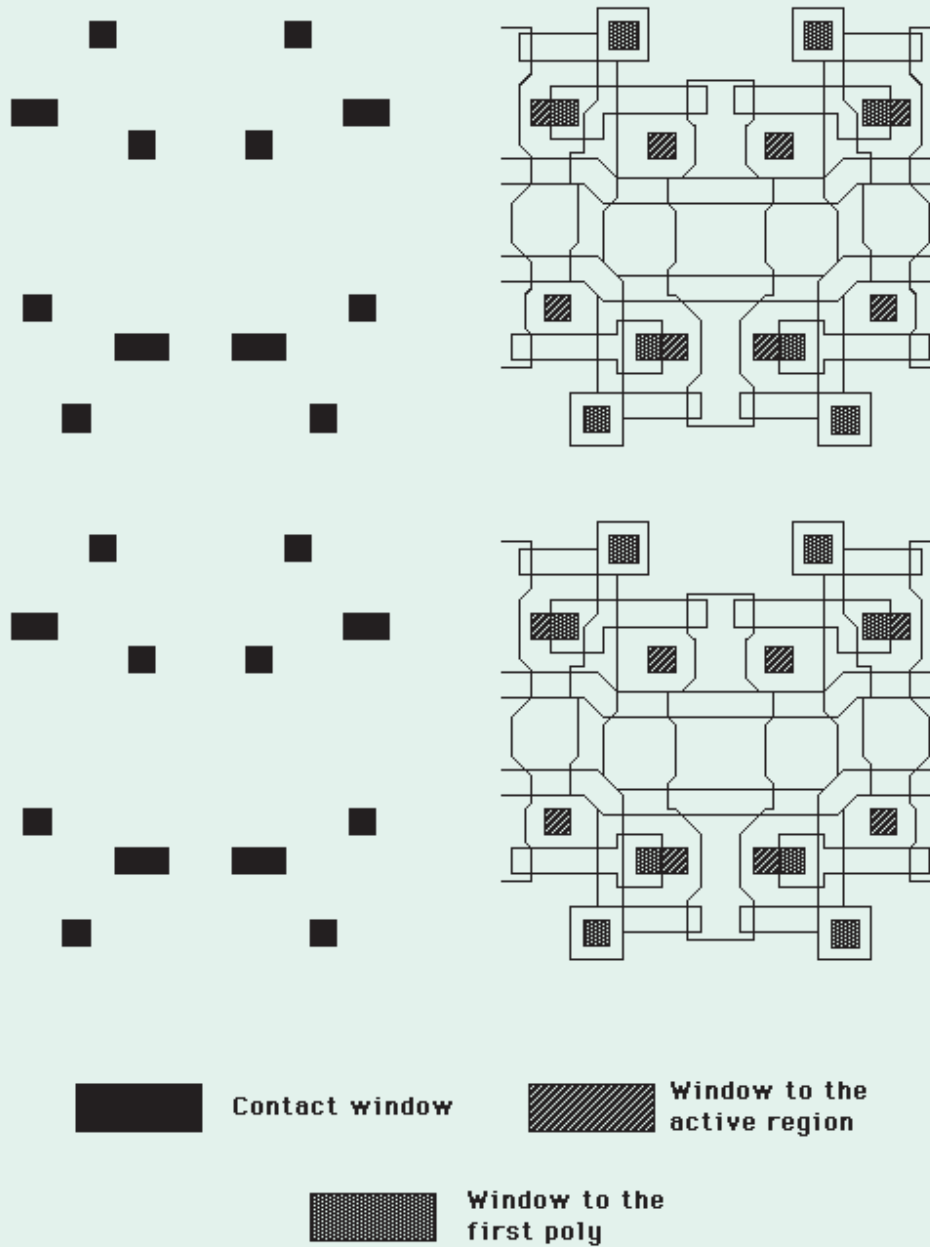


Field SiO₂

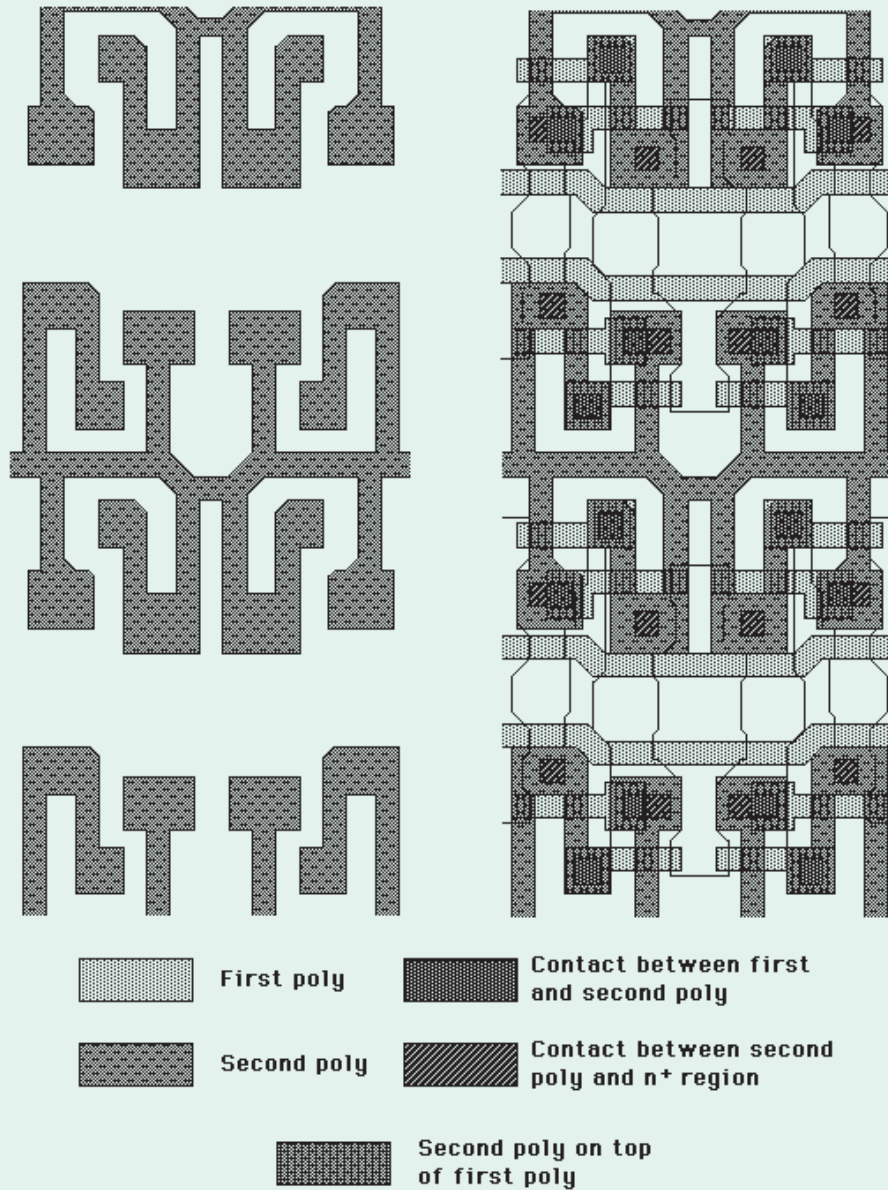
RMOS static memory Cell layout



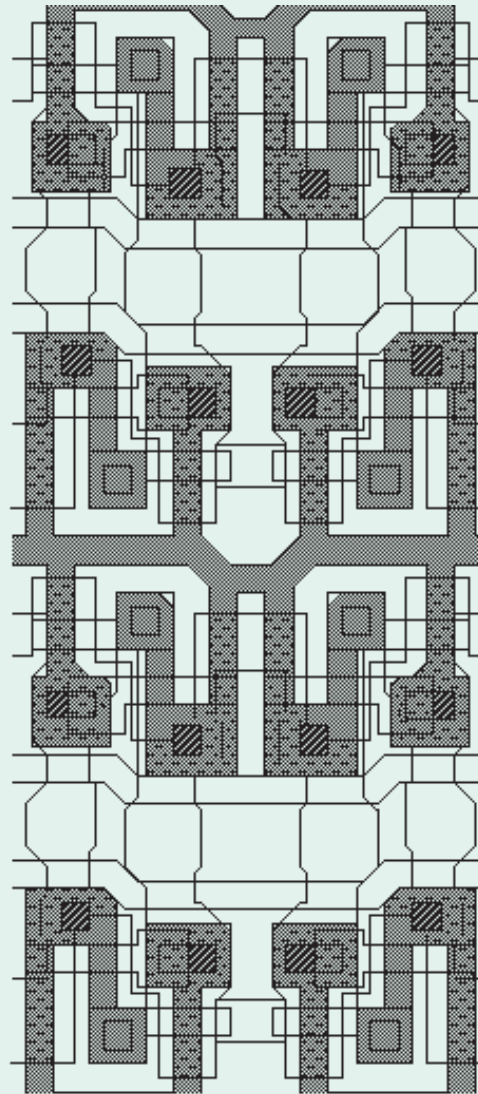
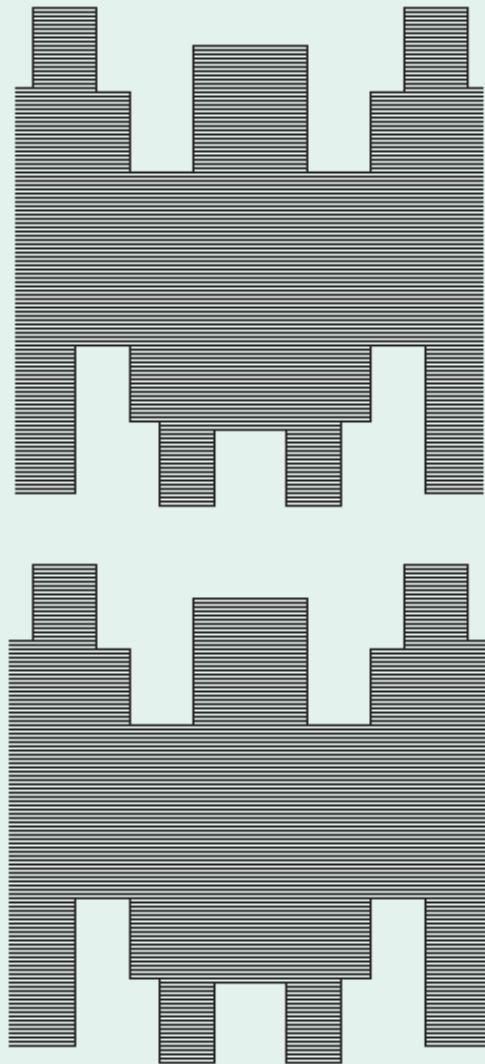
RMOS static memory Cell layout



RMOS static memory Cell layout



RMOS static memory Cell layout



Nitride



Second poly

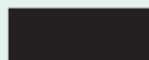
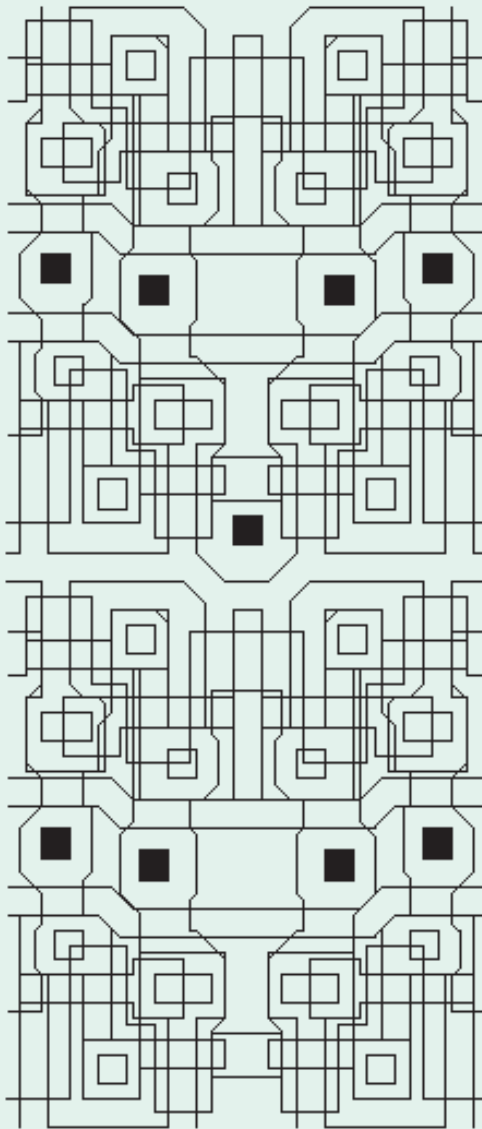
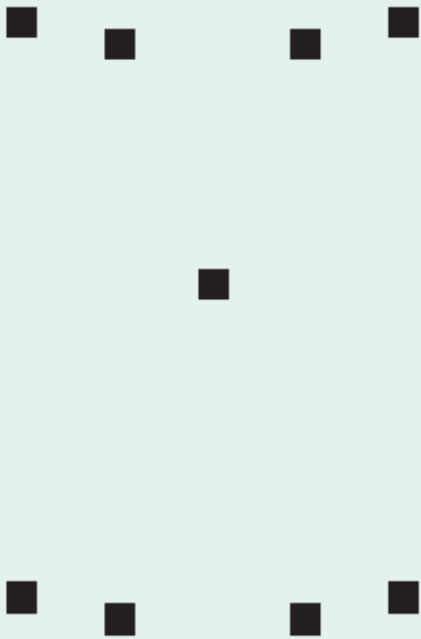


High resistivity
second poly



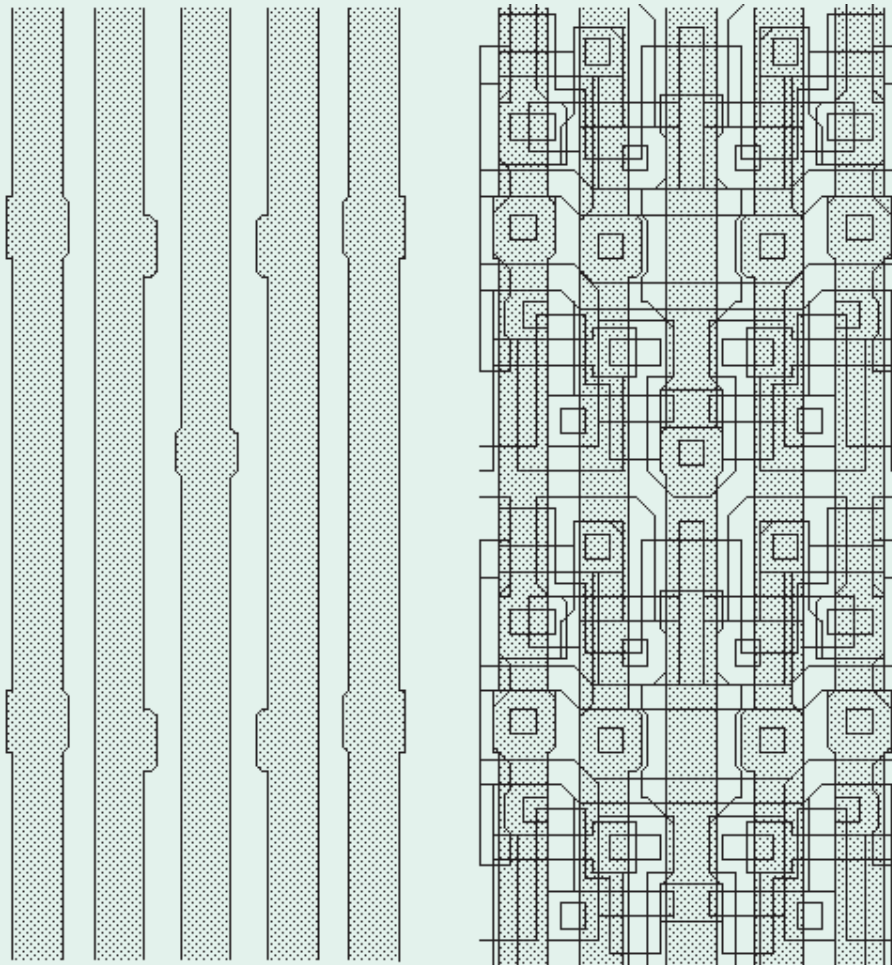
Contact between second
poly and n^+ region

RMOS static memory Cell layout



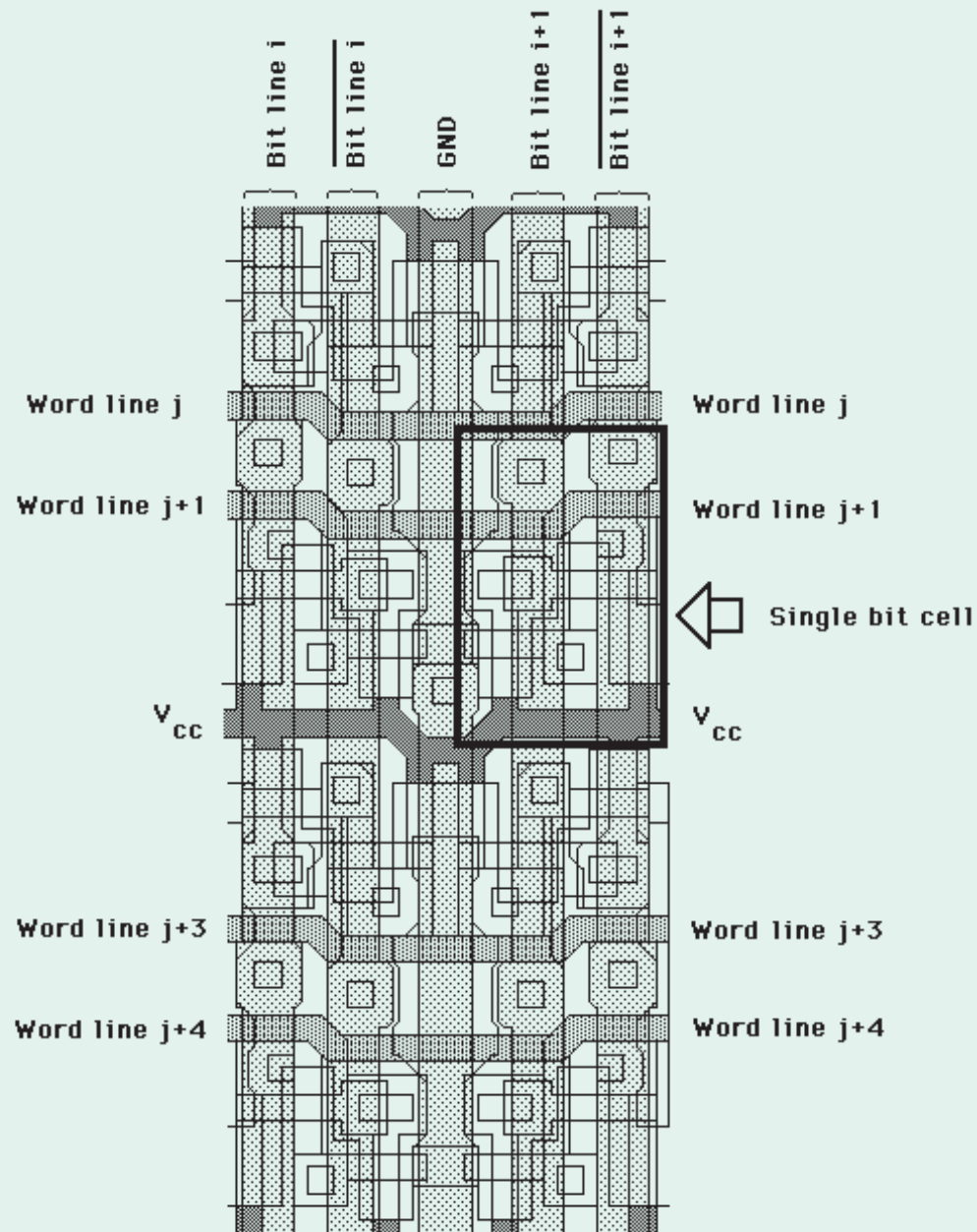
Windows in SiO₂

RMOS static memory Cell layout



Metal

RMOS static memory Cell layout



RMOS static memory

Cell layout

