EHB 335E HW#6

Due: 10 January 2021 @22 o'clock – **No late homework will be accepted.**

1) Assuming $\lambda \neq 0$ for M_2, but $\lambda = 0$ for M_1, determine the closed-loop gain and I/O impedances of the amplifier in Fig 1a. Assume that the output is the current through the "Device", which has a resistance of R_L.
2) An amplifier has a dc gain of 10^4 and poles at 10^5 Hz, 3.16×10^5 Hz, and 10^6 Hz. Find the value of β, and the corresponding closed-loop gain, for which a phase margin of 45° is obtained.

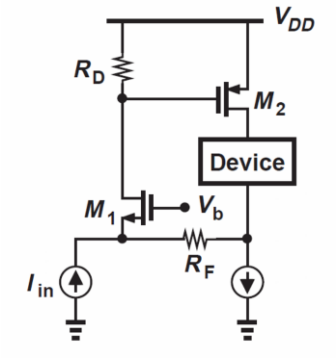

Fig 1. Figure of Question 1

3) Assuming $V_A = \infty$, determine the closed-loop gain and I/O impedances of the amplifier in Fig 2a. The output resistance is defined as the resistance looking into the collector of Q_3.

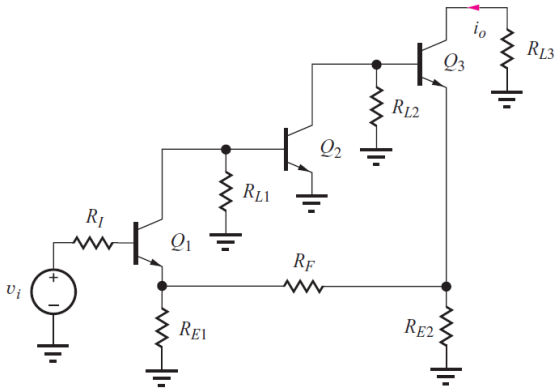

Fig 2a. Figure of Question 3

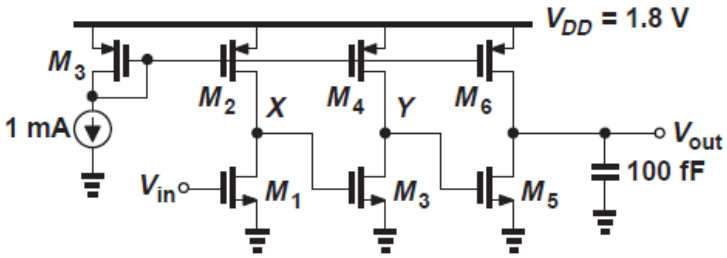

Fig 2b. Figure of Question 4

4) In the three-stage amplifier of Fig 2b., all transistors except M_1 and M_5 have W/L = 20 µm / 0.18 µm. For M_1 use W/L = 42 µm / 0.18 µm and for M_5 use W/L = 10 µm / 0.18 µm. Employ the transistor models provided in the last homework for Spice simulations. Assume a DC input level of 0.55 V.
   a. Determine the phase margin.
   b. Place a capacitor between nodes X and Y so as to obtain a phase margin of 55 degrees. What is the unity-gain bandwidth under this condition?
   c. Repeat (b) if the compensation capacitor is tied between X and ground and compare the results.