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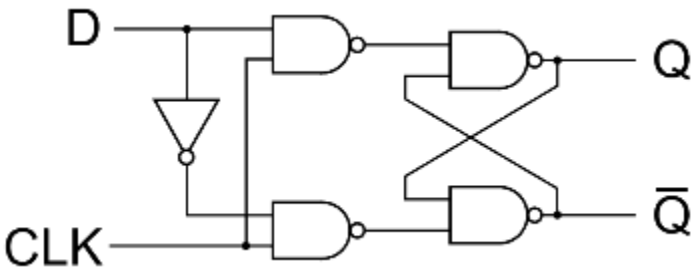
Student ID:

EHB322E Digital Electronic Circuits
Homework 3

Deadline: 21/05/2018 (before 13:30)
Submit your homeworks to Furkan Peker (Room: 3207 EEF)

Consider a CMOS D-flip-flop shown below.



A D-Flip-Flop

1) **CALCULATION:** Use the following parameter values.
   Equivalent resistor for an NMOS transistor: $\boldsymbol{R_N}$**= 1kΩ**
   Equivalent resistor for a PMOS transistor: $\boldsymbol{R_P}$**= 1,5kΩ**
   Suppose that each of the two output nodes has an internal capacitance of **10fF**. *Neglect the capacitors for the other nodes.*

   Problem: Find the **worst case propagation delay** values at the output (total of 2) when CLK=1 and the input is switching.

2) **SIMULATION:** Construct the flip-flop using SPICE. To satisfy the equivalent resistor values given in 1), determine $(W/L)_{NMOS}$ and $(W/L)_{PMOS}$ ratios by using an inverter and assuming that it has an output capacitor of 10fF. Select V_{DD}=5V (logic 1) and ground=0V (logic 0). Connect body terminals of NMOS and PMOS transistors to their source terminals. Use T15DN and T15DP spice models for NMOS and PMOS transistors, respectively (for details refer to Homework 1). Apply square pulse waves to required inputs.

   Problem: Find the **worst case propagation delay** values by performing transient analysis. Sketch input and output waveforms. Compare your result with that in **1)**; justify your answer.

Grading: 1) 50%, 2) 50%

Note: *Do not forget to attach SPICE* ***output file*** *prints to your homework!*