

EHB342E LOGIC DESIGN LABORATORY

Final Exam

- Students will solve the final exam version corresponding to their last digit of their ITU Student ID Number as explained below:
 - last digit of Student ID Number **0 or 1** → Final Exam Version **01**
 - last digit of Student ID Number **2 or 3** → Final Exam Version **23**
 - last digit of Student ID Number **4 or 5** → Final Exam Version **45**
 - last digit of Student ID Number **6 or 7** → Final Exam Version **67**
 - last digit of Student ID Number **8 or 9** → Final Exam Version **89**
- If a student submit solutions for a wrong final exam version based on the last digit of the Student ID Number, his/her final exam will be invalid.
- The exam is open-book and open-lecture notes. Exams are exclusive to students and they are expected to work on the solutions on their own.
- The students are expected to abide with the ITU Honor Code <http://www.sis.itu.edu.tr/yonetmelik/AkademikOnurSozuEsaslar.html>
- Solutions in PDF format are required to be uploaded to the Ninova system before the exam period ended. There will not be extra time for uploading the solutions.
- Each question should be solved on a different page, each page of the solution papers has to be numbered and should have name, last name and Student ID number on top right corner.
- The lecturer will open a Zoom session at the beginning of the exam for announcements and questions about the exam. The Zoom session will end at the end of exam period.
- By uploading the solutions, students here confirm that they have understood the instructions and will act accordingly.

FINAL EXAM 67

This final exam will be solved by only the students with a Student ID number ending with 6 or 7.

Experiment 2

A binary decoder decodes codewords from n-bit inputs into 2^n -bit output. Only one of the output bits can have a value of logic-1 and the input identifies which bit of the output is equal to logic-1. In case $n=3$,

- Obtain the truth table.
- Use Karnaugh diagram in order to find the optimum sum of product representation of the Boolean functions of the outputs that are defined by the truth table found in (a).
- Draw the circuit for the outputs using minimum number of logic gates.

Experiment 3

Draw the schematic diagram of the circuit which realizes the Boolean function $F = x'yz' + xz$ in sum of product (SOP) form by using **74138 IC** (3 input active-0 output DECODER) shown in Fig. 1 and necessary **AND**, **OR** and **NOT** gates (you don't need to draw the ICs for the logic gates, you can use the logic symbols of them).

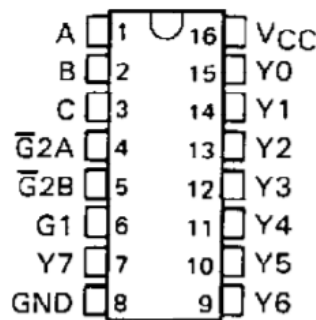


Figure 1

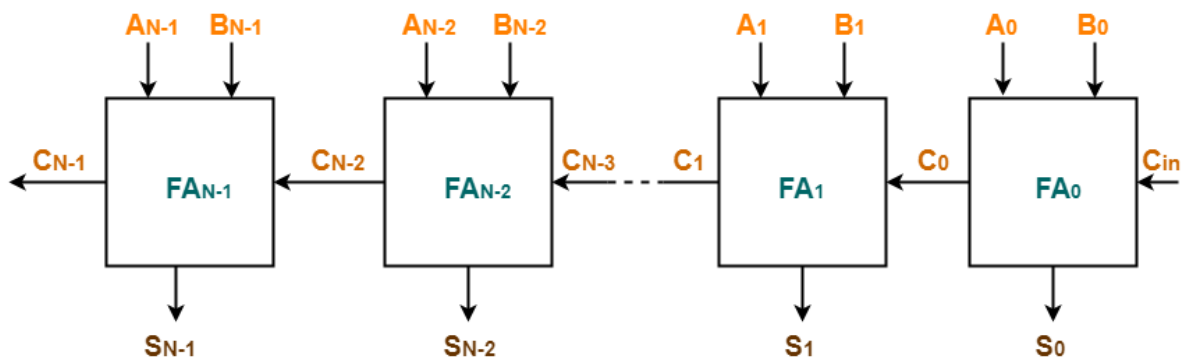
Experiment 4

- Find the optimum sum of product representation of the Boolean functions for the carry, C and sum, S outputs of a half adder (HA) which is used for adding 2 1-bit numbers and defined by the truth table shown in Fig. 2.
- Draw the HA circuit by using the optimal Boolean function that you found in (a).

A	B	C	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Figure 2

- Draw the circuit for a Full Adder (FA) which is used for adding 3 1-bit numbers by using the HA from (b) and necessary other logic gates.
- Consider you have an N-bit ripple carry adder structure. What modifications you should make on this structure in order to convert it to an adder/subtractor block? Briefly explain your reasoning.



N-bit Ripple Carry Adder

Figure 3

Experiment 5

A state transition table of a synchronous sequential circuit is shown in Fig. 4.

x	Q1	Q2	Q1+	Q2+	y
0	0	0	0	1	0
0	0	1	1	1	1
0	1	0	1	0	0
0	1	1	0	0	1
1	0	0	1	1	0
1	0	1	1	0	0
1	1	0	0	1	1
1	1	1	0	0	0

Figure 4

- Complete the timing diagrams for the initial state **Q1=0, Q2=0** using the given state transition table. If faulty outputs occur, show and name these faulty outputs.
- What type of state machine is the circuit? Explain why.

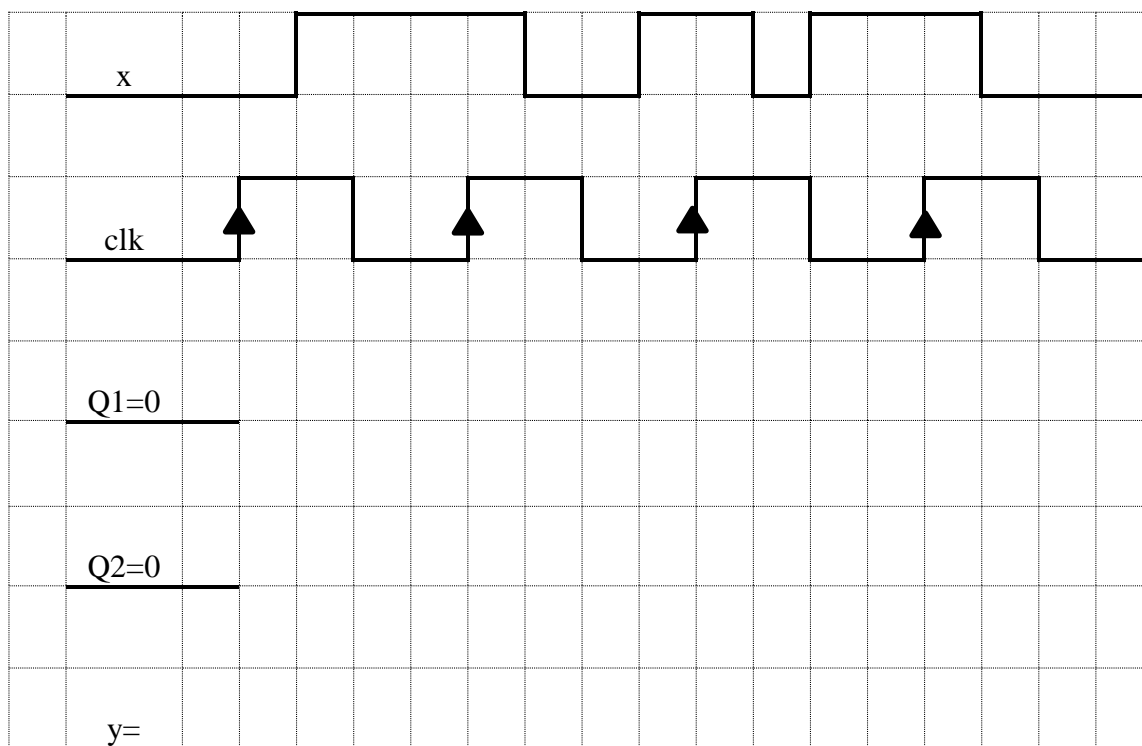


Figure 5

Experiment 6

We wish to design a synchronous sequential circuit whose state diagram is shown below. You will use JK-type flip-flops in your design.

- Encode the states
- Obtain the state transition table
- Draw the circuit

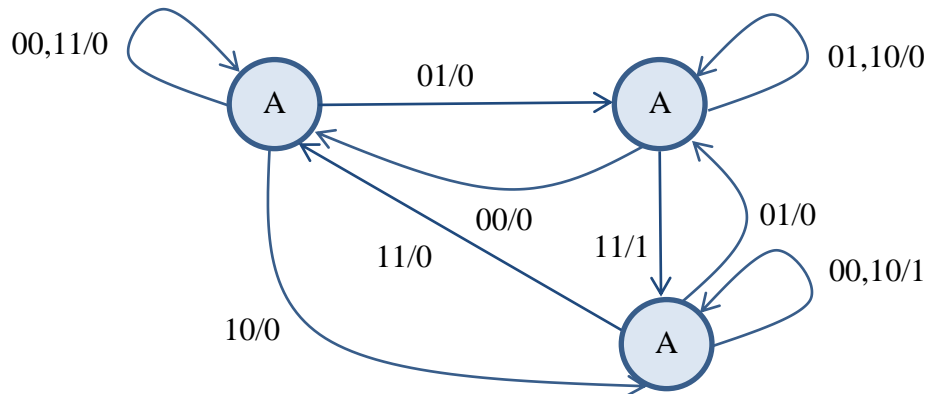


Figure 6

Experiment 7

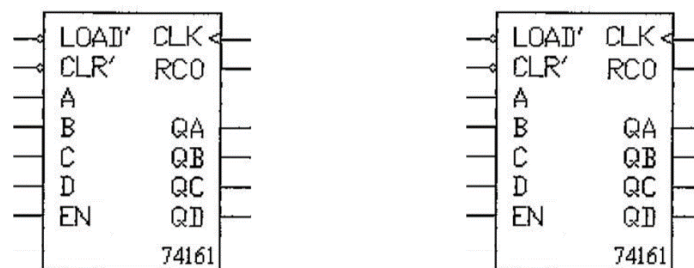


Figure 7

- Design a 6 to 66 counter by using two 74161 IC (synchronous counter) as shown in the figure. You are allowed to use all the logic gates.
- Explain the circuit operation briefly.