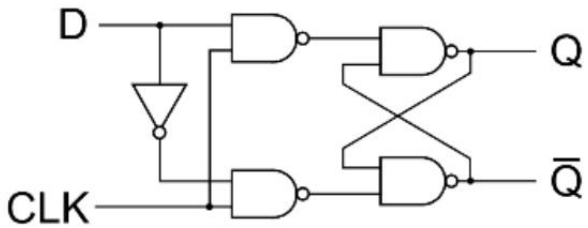
EHB322E - Homework 3 Solution – 2018 Spring

Consider a CMOS D-flip-flop shown below.



A D-Flip-Flop

1) **CALCULATION:** Use the following parameter values.
Equivalent resistor for an NMOS transistor: R_N**=1kΩ**
Equivalent resistor for a PMOS transistor: R_P**=1,5kΩ**
Suppose that each of the two output nodes has an internal capacitance of **10fF**. *Neglect the capacitors for the other nodes.*

Problem: Find the **worst case propagation delay** values at the output (total of 2) when CLK=1 and the input is switching.

Note that we only have 10 fF capacitances at outputs, Qand $\overline{Q}$. Therefore, any change in D would be directly (no delay on nodes) transferred to inputs of NAND gates which has Q and $\overline{Q}$ outputs.

When CLK = 1, input D can switch as 1 → 0 or 0 → 1 to change output states.

- For D = 1, Q = 1, $\overline{Q}$ = 0
  - When D = 1 → 0
    - Q doesn't change initially.
    - First $\overline{Q}$ switches 0 → 1,

$$t_{pLH(\bar{Q})} = 0.69\ x\ Rp\ x\ Cout = 0.69\ x\ 1.5\ x\ 10^3\ x\ 10\ x\ 10^{-15} = 10.35\ ps$$

    - Then, Q switches 1 → 0,

$$t_{pHL(Q)} = t_{pLH(\bar{Q})} + 0.69\ x\ 2\ x\ Rn\ x\ Cout = 10.35\ x\ 10^{-12} + 0.69\ x\ 2\ x\ 10^3\ x\ 10\ x\ 10^{-15} = 24.15\ ps$$

- For D = 0, Q = 0, $\overline{Q}$ = 1
  - When D = 0 → 1
    - $\overline{Q}$ doesn't change initially.
    - First Q changes 0 → 1,

$$t_{pLH(Q)} = 0.69\ x\ Rp\ x\ Cout = 0.69\ x\ 1.5\ x\ 10^3\ x\ 10\ x\ 10^{-15} = 10.35\ ps$$

    - Then, $\overline{Q}$ changes 1 → 0

$$t_{pHL(\bar{Q})} = t_{pLH(Q)} + 0.69\ x\ 2\ x\ Rn\ x\ Cout = 10.35\ x\ 10^{-12} + 0.69\ x\ 2\ x\ 10^3\ x\ 10\ x\ 10^{-15} = 24.15\ ps$$