



VLSI Circuit Design II– EHB 425E

HOMEWORK IV

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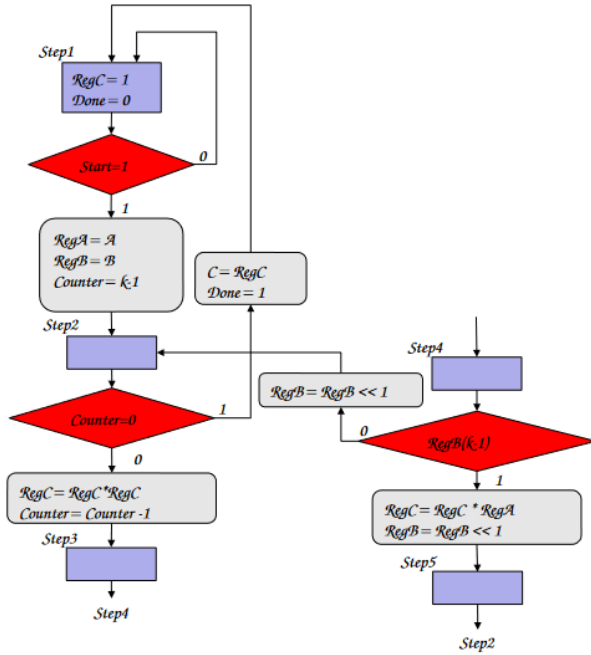
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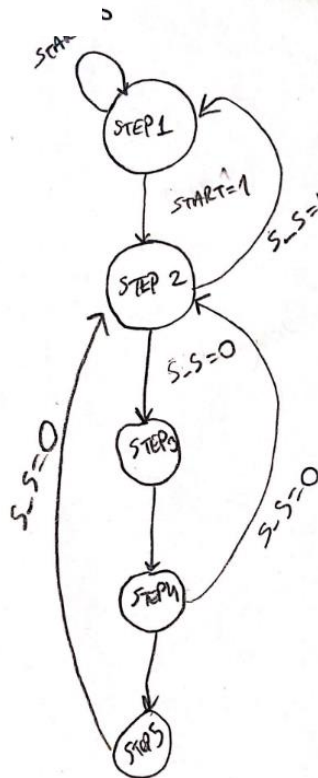
1- Controller

• State Diagram

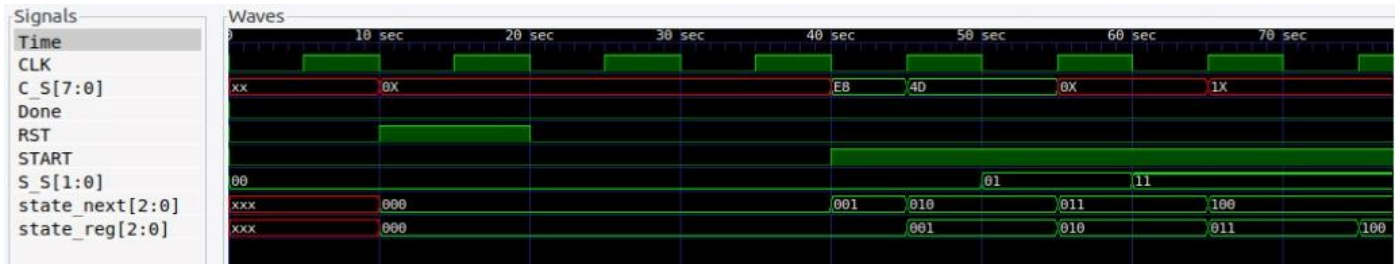
The state diagram of the figure whose ASM is given below is as shown in the figure. Controller is written according to the diagram in the figure.



		Status Signals		Control Signals						
State	Start	=	RegB (k-1)	Load A	Load Coun	Load B	Shift B	Load C	S Coun	S C
Step1	0	X	X	0	0	0	0	1	X	0
Step1	1	X	X	1	1	1	0	1	0	00
Step2	X	0	X	0	1	0	0	0	1	01
Step2	X	1	X	0	1	0	0	0	1	X
Step3	X	X	X	0	0	0	0	0	X	X
Step4	X	X	0	0	0	0	1	0	X	X
Step4	X	X	1	0	0	0	1	1	X	10
Step5	X	0	X	0	0	0	0	0	X	X



- **GTK Waveform**



As you can see, the code designed according to the state diagram works correctly. The simulation above shows this.

2- Datapath

As it was said in the assignment, the datapath was designed based on the k parameter and using the MUL block in HW3. The codes are zipped and put into the assignment file.

- **GTK Waveform**



3- Top Module

By combining Controller and Datapath, a top module is created.

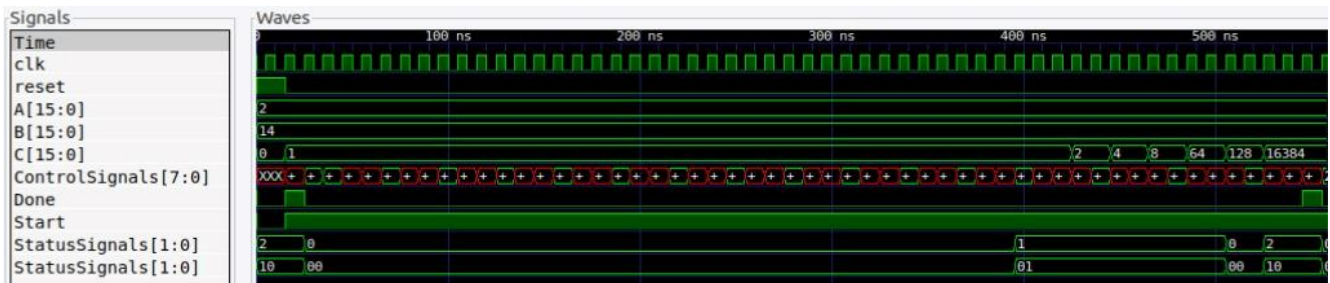
- **MATLAB**

Test vectors were obtained using the following MATLAB code.

```
Editor - C:\Users\yigit\Desktop\Okul\2023bahar\VLSI2\HW4\odev4\testvectors.m
testvectors.m
1 fid = fopen('test_vectors.txt', 'w'); % Open the file for writing
2 for A = 2:2^16
3     for B = 2:2^16
4         if (A^B > 2^16-1)
5             break;
6         end
7         AB_array(A-1,1) = uint16(A);
8         AB_array(A-1,2) = uint16(B-1);
9         AB_array(A-1,3) = uint16(A^(B-1));
10    end
11 end
12
13 % Print the output to the file
14 for i = 1:size(AB_array, 1)
15     fprintf(fid, '%d\t%d\t%d\n', AB_array(i,1), AB_array(i,2), AB_array(i,3));
16 end
17
18 fclose(fid); % Close the file
19 |
```

- **GTK Waveform**

where A is the value to be powered. B is the power of A. By looking at the power of 2 here, it can be understood whether the circuit is working correctly. The powers of 2 confirm that the circuit is working correctly. After 2^{14} is finally received, the done signal 1 appears to be lit. Indicates that the process is finished.



4- Openlane Section

```
ubuntu@ubuntu-VirtualBox: ~/Desktop/OpenLane
[INFO]: Running Magic Spice Export from LEF (log: designs/Top/runs/run001/logs/signoff/31-spice.log)...
[STEP 32]
[INFO]: Writing Powered Verilog (logs: designs/Top/runs/run001/logs/signoff/32-write_powered_def.log, designs/Top/runs/run001/logs/signoff/32-write_powered_verilog.log)...
[STEP 33]
[INFO]: Writing Verilog (log: designs/Top/runs/run001/logs/signoff/32-write_powered_verilog.log)...
[STEP 34]
[INFO]: Running LVS (log: designs/Top/runs/run001/logs/signoff/34-lvs.lef.log)...
[STEP 35]
[INFO]: Running Magic DRC (log: designs/Top/runs/run001/logs/signoff/35-drc.log)...
[INFO]: Converting Magic DRC database to various tool-readable formats...
[INFO]: No DRC violations after GDS streaming out.
[STEP 36]
[INFO]: Running OpenROAD Antenna Rule Checker (log: designs/Top/runs/run001/logs/signoff/36-antenna.log)...
[STEP 37]
[INFO]: Running Circuit Validity Checker ERC (log: designs/Top/runs/run001/logs/signoff/37-erc_screen.log)...
[INFO]: Saving current set of views in 'designs/Top/runs/run001/results/final'...
[INFO]: Saving runtime environment...
[INFO]: Generating final set of reports...
[INFO]: Created manufacturability report at 'designs/Top/runs/run001/reports/manufacturability.rpt'.
[INFO]: Created metrics report at 'designs/Top/runs/run001/reports/metrics.csv'.
[SUCCESS]: Flow complete.
OpenLane Container (f4c6f5f):/openlane$
```

```
=====
report_design_area
=====
Design area 12851 u^2 44% utilization.

=====
report_worst_slack -max (Setup)
=====
worst slack 2.68

=====
report_worst_slack -min (Hold)
=====
worst slack 0.21

6.98 data arrival time
```

As can be seen, no errors were encountered while synthesizing. The desired outputs are mentioned above. Max Frequency $\rightarrow 1/6.98 \times 10^{-9} = 143.266$ MHz

All verilog source codes and files with .dot extension are in the archive.