DIGITAL SYSTEM DESIGN APPLICATION – EHB 436E

Experiment V-Bonus Questions

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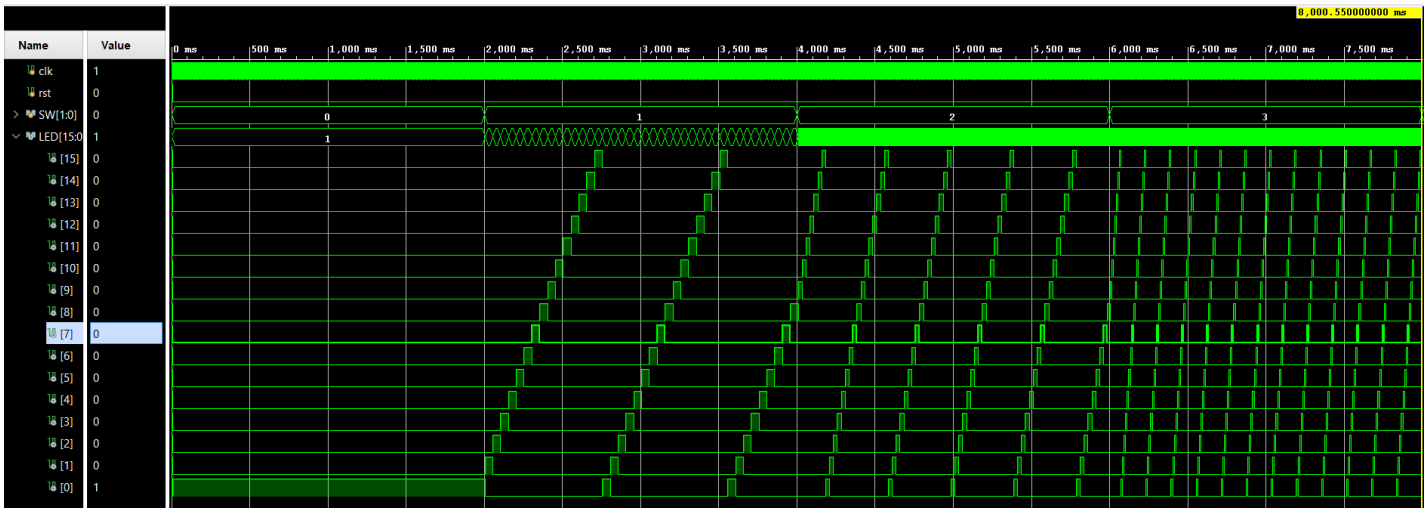
1. SLIDING LEDS

- Verilog Code

```
`timescale 1ns / 1ps

module sliding_leds#(
    parameter MAX_CNT_DEST = 500 // 100MHz / 10 = 10M
    )(
    input rst,clk,
    input [1:0]SW,
    output reg [15:0]LED
    );
    reg [$clog2(MAX_CNT_DEST-1)-1:0] divcounter = 0;
    reg divclk;
    always @(posedge clk or posedge rst)

        begin
        if(rst)
            LED<= 16'h0001;
        else
            begin
                case(SW)
                    //stop
                    2'b00:
                        LED <= LED;

                    //10Hz
                    2'b01:
                    begin
                        if(LED == 16'h8000)
                        begin
                            if (divcounter % (MAX_CNT_DEST-1) == 0 && divcounter !=0)
                                LED <= 16'h0001;
                        end

                        else
                        begin
                            if (divcounter % (MAX_CNT_DEST-1) == 0 && divcounter !=0)
                                LED <= LED<<1'b1;
                        end
                    end

                //20Hz
                2'b10:
                    begin
                        if(LED == 16'h8000)
                        begin
                            if (divcounter % ((MAX_CNT_DEST-1)/2) == 0 && divcounter !=0)
                                LED <= 16'h0001;

                        end

                        else
                        begin
                            if (divcounter % ((MAX_CNT_DEST-1)/2) == 0 && divcounter !=0)
                                LED <= LED<<1'b1;
                        end
                    end

                //50Hz
                2'b11:
                    begin
                        if(LED == 16'h8000)
                        begin
                            if (divcounter % ((MAX_CNT_DEST-1)/5) == 0 && divcounter !=0)
                                LED <= 16'h0001;
                        end

                        else
                        begin
                            if (divcounter % ((MAX_CNT_DEST-1)/5) == 0 && divcounter !=0)
                                LED <= LED<<1'b1;
                        end
                    end
                default : LED <= LED;
            endcase
        end
    end
```

```
    always @(posedge clk or posedge rst)
        begin
            if(rst)
                divcounter <=0;
            else
            begin
                if (divcounter == MAX_CNT_DEST)
                    divcounter <= 0;
                else
                    divcounter <= divcounter+1;
            end
        end
endmodule
```

- Behavioral Simulation
  - Our input named clk specifies the fpga clk. Our rst input initializes the system and lights the first led. Our SW inputs change the flashing speed of the leds (50Mhz, 20Mhz, 10Mhz), and in the 00 state, the leds keep their last state. As seen in the simulation, the frequencies of the LEDs increased and took up less space in the simulation. Frequency speeds can be controlled with switches.



- Realization
  - Frequency adjustment was made with the switch case structure. An rst definition was made before these cases started, the rst state is set to 1 before the program starts. In addition to this structure, there is always block where the frequency rate is set.

- Utilization report and critical path slack

  - Setup Time

Unconstrained Paths - NONE - NONE - Setup

Name	Slack	Levels	Routes	High Fanout	From	To	Total ...	Logic Delay	Net Delay	Requi...	Source Clock
Path 1	∞	12	9	29	divcounter_reg[4]/C	LED_reg[1]/CE	9.027	3.372	5.655	∞	
Path 2	∞	12	9	29	divcounter_reg[4]/C	LED_reg[2]/CE	9.027	3.372	5.655	∞	
Path 3	∞	12	9	29	divcounter_reg[4]/C	LED_reg[4]/CE	8.888	3.372	5.516	∞	
Path 4	∞	12	9	29	divcounter_reg[4]/C	LED_reg[0]/CE	8.881	3.372	5.509	∞	
Path 5	∞	12	9	29	divcounter_reg[4]/C	LED_reg[3]/CE	8.881	3.372	5.509	∞	
Path 6	∞	12	9	29	divcounter_reg[4]/C	LED_reg[3]_lopt_replica/CE	8.881	3.372	5.509	∞	
Path 7	∞	12	9	29	divcounter_reg[4]/C	LED_reg[4]_lopt_replica/CE	8.881	3.372	5.509	∞	
Path 8	∞	12	9	29	divcounter_reg[4]/C	LED_reg[5]/CE	8.850	3.372	5.478	∞	
Path 9	∞	12	9	29	divcounter_reg[4]/C	LED_reg[5]_lopt_replica/CE	8.850	3.372	5.478	∞	
Path 10	∞	12	9	29	divcounter_reg[4]/C	LED_reg[6]/CE	8.850	3.372	5.478	∞	

  - Hold Time

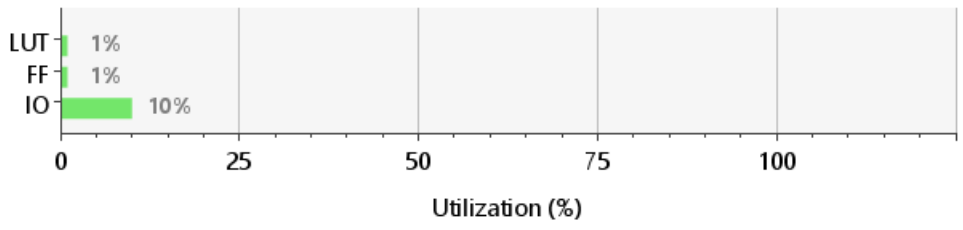
Unconstrained Paths - NONE - NONE - Hold

Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement
Path 11	∞	1	1	3	LED_reg[3]/C	LED_reg[4]_lopt_replica/D	0.262	0.128	0.134	-∞
Path 12	∞	1	1	3	LED_reg[14]/C	LED_reg[15]/D	0.268	0.141	0.127	-∞
Path 13	∞	1	1	3	LED_reg[8]/C	LED_reg[9]/D	0.274	0.141	0.133	-∞
Path 14	∞	1	1	3	LED_reg[5]/C	LED_reg[6]/D	0.275	0.141	0.134	-∞
Path 15	∞	1	1	3	LED_reg[8]/C	LED_reg[9]_lopt_replica/D	0.277	0.141	0.136	-∞
Path 16	∞	1	1	3	LED_reg[5]/C	LED_reg[6]_lopt_replica/D	0.277	0.141	0.136	-∞
Path 17	∞	1	1	3	LED_reg[10]/C	LED_reg[11]/D	0.278	0.141	0.137	-∞
Path 18	∞	2	1	3	LED_reg[3]/C	LED_reg[0]/D	0.303	0.227	0.076	-∞
Path 19	∞	1	1	3	LED_reg[3]/C	LED_reg[4]/D	0.322	0.128	0.194	-∞
Path 20	∞	1	1	3	LED_reg[11]/C	LED_reg[12]_lopt_replica/D	0.325	0.141	0.184	-∞

  - Utilization Summary

Summary

Resource	Utilization	Available	Utilization %
LUT	50	32600	0.15
FF	38	65200	0.06
IO	20	210	9.52



  - There are 50LUT , 38FF(flip-flop) and 20IO (input-out) in usage in our device.