Lecture 3

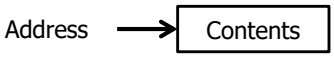
Memory Organization

Topics

- Memory Organization
- Memory Map

Memory Addressing

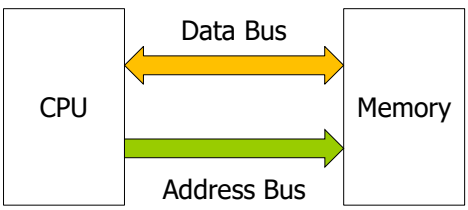
- Memory consists of a sequence of directly addressable locations.
- A memory location is referred to as an information unit.
- An information unit has two components:
  - Address
  - Contents



3

Memory Addressing

- Each location in memory has an address.
- CPU first identifies the location's address and then passes the address on address bus.
- Data are transferred between memory and CPU along data bus.



- Number of bits that can be transferred on data bus at once is called the **data bus width** of processor.
- Examples:
  - 8-Bit CPU means that the Data Bus is 8 bit.
  - 32-Bit CPU means Data Bus is 32 bit.

4

Dimensions of a Memory Chip

- Memory chip capacity is measured by two dimensions.
  - **Length :** Total number of locations (rows).
  - **Width :** Number of bits in each location (columns).

- Length is a function of address lines.

  Length = $2^{(\text{Number of address lines})}$

- **Example:** A memory chip with 10 address lines would have
  2^{10} = 1024 locations (1K)

- **Example:** A memory chip with 4K locations would need
  $\log_2 4096 = 12$ address lines

5

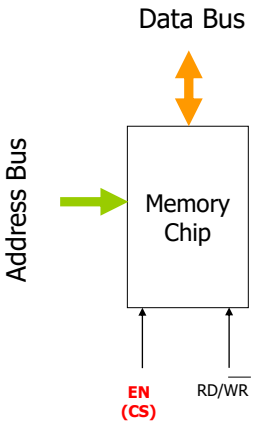
Memory Units

Unit (Bytes)	Name	Synonym	Exact Value (Base 2)	Approximate Value (Base 10)
1 KB	Kilo	Thousand	2^{10} = 1024	10^3 = 1000
1 MB	Mega	Million	2^{20}	10^6
1 GB	Giga	Billion	2^{30}	10^9
1 TB	Tera	Trillion	2^{40}	10^{12}

6

Memory Chip Selection

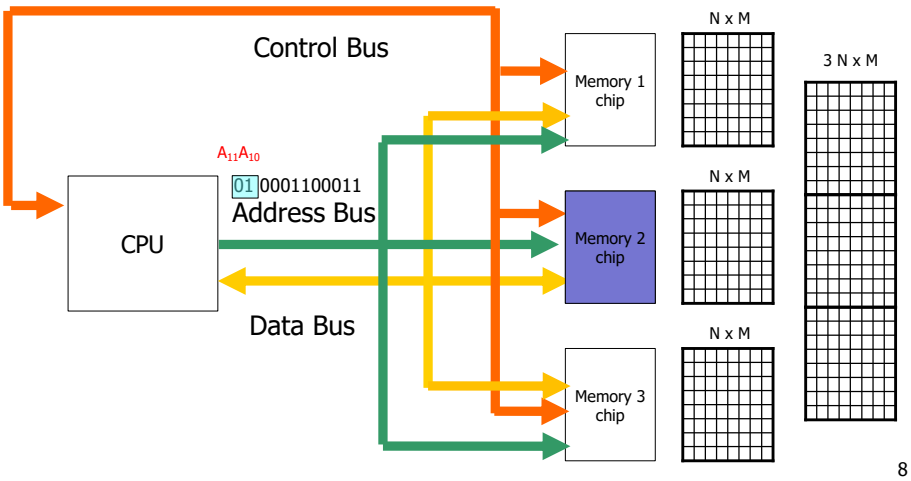
- Each memory chip has a **Chip Select (CS) input** (Enable).
- The chip will only work if an active signal is applied on CS.
- To allow use of **multiple memory chips**, we need to use some of address lines for the purpose of **chip selection**.
- Address decoders are used for chip selection.



7

Memory Access (Memory chip selection)

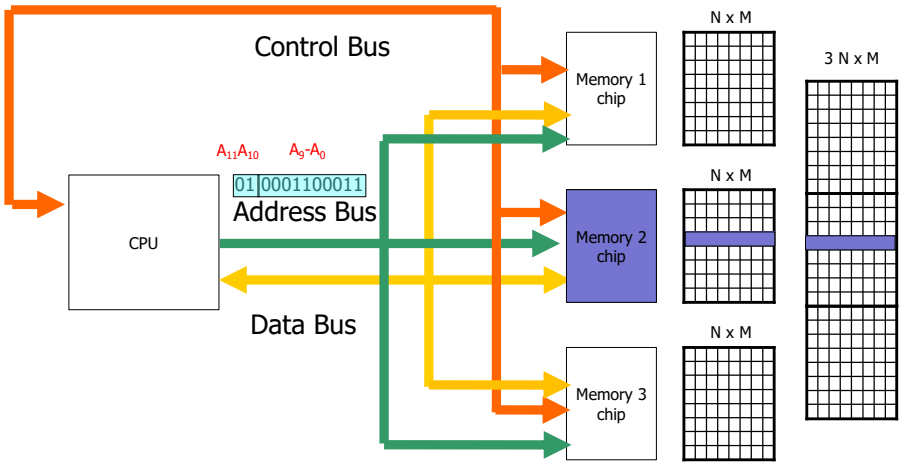
- Three memory chips have consecutive memory addresses.
- **A11** and **A10** address lines are used for **chip selection** (using 2-to-4 decoder).



8

Memory Access (Location selection within a chip)

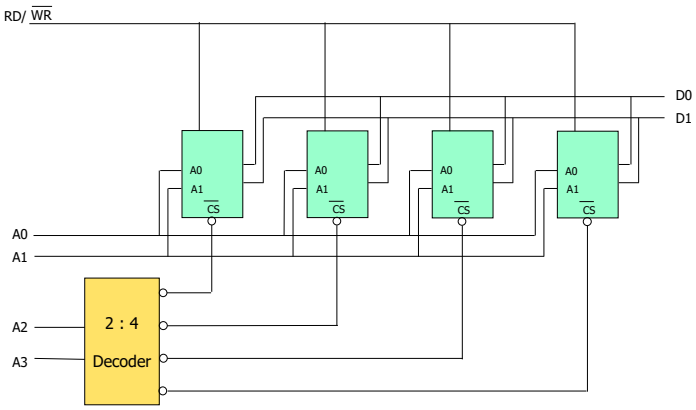
- **A9-A0** lines are used for **location selection** within a chip.



9

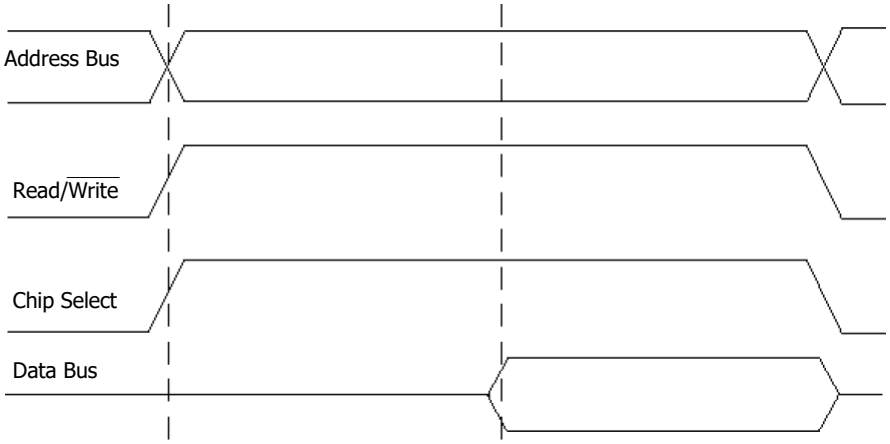
Using Decoder for Chip Selection

- The following is a simple memory system made up of 4 memory chips.
- Each memory chip has 4x2 bits.
- An **Address Decoder** (2 to 4) is used for chip selections.
- The Decoder outputs are connected to chip selects (CS) of memory chips.



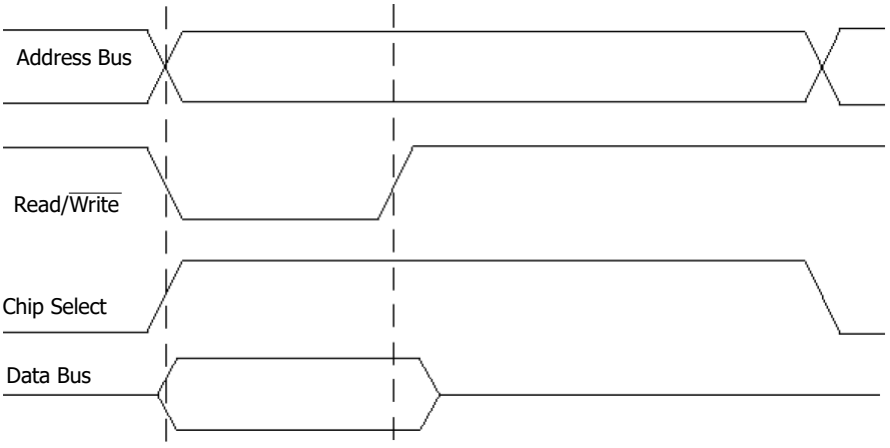
10

Timing Diagram of READ Operation from Memory



11

Timing Diagram of WRITE Operation to Memory



12

Educational CPU and Memory

- Educational CPU (**Mikbil**) has following features.
  - Address Bus has 16 address lines.
  - Data Bus has 8 data lines.
- It can address **2^{16} = 64 K** total memory locations.
- Each memory location is 8 bits (1 byte).
- There are many alternative chip configurations to organize 64 KB total memory, by using different chips.

13

Example : Using one 64KB memory chip

- Only one memory chip that has 64 K locations can be used.
- 64 K locations require **16** address lines.
  ($2^{16} = 2^6 . 2^{10} = 64 . 1K = 64K$)
- All lines (16 lines) of the Address Bus are used for location selection within the memory chip.
- There is no need for an Address Decoder, because only one memory chip is used.

14

Example : Using four 16KB chips

- 4 memory chips, each chip having 16 K locations, can be used.
- 16K locations require **14** address lines (2^{14} = 16 K)
- These 14 lines are used for location selection within a memory chip.
- Because there are 4 memory chips, we have to use an Address Decoder (2:4 type) for memory chip selections.
- The decoder should use **2** address lines as its inputs.
- Total number of required address lines is = 14 + 2 = **16** lines

15

Table for Alternative Memory Configurations

Capacity of each memory chip	Chip capacity as 2^X	Number of address lines used for location selection within a chip	Number of memory chips	Number of address lines used for memory chip selections (As Decoder inputs)	Type of Address Decoder	Total Memory
64 KB	2^{16}	16	1	0	None	64 KB
32 KB	2^{15}	15	2	1	1:2	64 KB
16 KB	2^{14}	14	4	2	2:4	64 KB
8 KB	2^{13}	13	8	3	3:8	64 KB
4 KB	2^{12}	12	16	4	4:16	64 KB
2 KB	2^{11}	11	32	5	5:32	64 KB
1 KB	2^{10}	10	64	6	6:64	64 KB

16

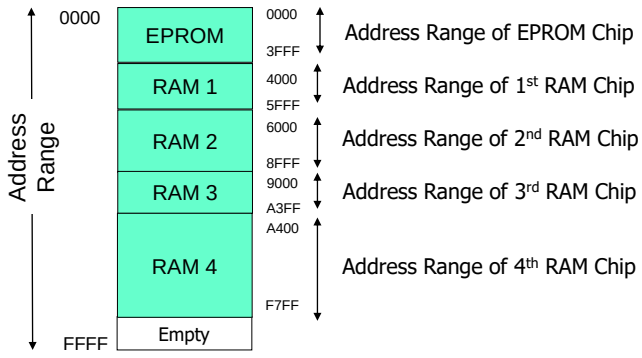
Topics

- Memory Organization
- Memory Map

17

Memory Map

- Memory map shows the address space for each memory chip.
- Address ranges for chips define the memory map.



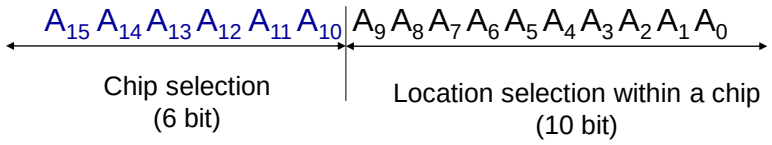
18

Example : 64Kx8 Bit Total Memory

- An CPU with **16 address bits** can address a total of **64K memory locations**. (2^{16} = 65536 = 64 x 1024 = 64 K)
  - If we use memory chips with **1K** locations each, then we will need **64 memory chips**.
  - 1K memory chip needs 10 address lines to uniquely identify the 1K locations. ($\log_2 1024 = 10$)
  - That leaves **6 address lines**, which is the exact number needed for selecting between the 64 different chips ($\log_2 64 = 6$).
    - These 6 lines are used as inputs of a decoder (6:64).
    - The 64 output lines of the decoder are used for chip selections.

Parts of Memory Address

- 16 bit address lines can be separated into two parts.
  - Depending on the combination of lines A_{15}-A_{10} , only one chip is selected.
  - Other address lines (A_9-A_0) determines location addresses within a chip.
- Whole address line determines address range of each memory chip.



For 64 memory chips

Each memory chip is 1KB

Address Range of First Memory Chip (1Kx8 Bit)

- The FIRST chip uses the bit combination **[A_{15}-A_{10}]= 000000** as its chip selection value (fixed).
- **[A_9-A_0]** address lines are used for locations within the chip.
  - There are 1024 locations in a chip. (2^{10} = 1024 bytes = 1KB)
- Minimum address in chip is **$0000,** maximum address is **$03FF**.
  - To obtain hexadecimal value of a binary address, the bits are grouped as 4-bits from right-to-left.
- Followings are the minimum and maximum addresses in the FIRST chip.

Grouping of 4-bits are shown for easy hexadecimal conversion

	A_{15} A_{14} A_{13} A_{12}	A_{11} A_{10} A_9 A_8	A_7 A_6 A_5 A_4	A_3 A_2 A_1 A_0	
Min →	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	→ $0000
Max →	0 0 0 0	0 0 1 1	1 1 1 1	1 1 1 1	→ $03FF

Chip selection lines

Location selection lines within chip

Table for Memory Chip Capacities and Maximum Addresses

Number of address lines (N)	Address lines for location selection	Memory chip capacity (Kilo Byte)	Capacity as 2^N	Capacity as hexadecimal	Maximum address (Hexa decimal)
10	**A_9 - A_0**	**1 K**	**2^{10}**	**0400**	**03FF**
11	A_{10} - A_0	2 K	2^{11}	0800	07FF
12	A_{11} - A_0	4 K	2^{12}	1000	0FFF
13	A_{12} - A_0	8 K	2^{13}	2000	1FFF
14	A_{13} - A_0	16 K	2^{14}	4000	3FFF
15	A_{14} - A_0	32 K	2^{15}	8000	7FFF
16	**A_{15} - A_0**	**64 K**	**2^{16}**	**1 0000**	**FFFF**
17	A_{16} - A_0	128 K	2^{17}	2 0000	1 FFFF
18	A_{17} - A_0	256 K	2^{18}	4 0000	3 FFFF
19	A_{18} - A_0	512 K	2^{19}	8 0000	7 FFFF
20	**A_{19} - A_0**	**1024 K (1MB)**	**2^{20}**	**10 0000**	**F FFFF**

Example1 : Memory Organization

- A CPU has **8-bit** Data Bus and **16-bit** Address Bus.
- Build the memory that spans between **$0000** and **$1FFF**.
- Use several **2Kx8** memory chips.

- Notation :
  - 2K means each chip has 2048 locations
  - x8 means each location has 8 bits

- QUESTIONS:
  - What is the total memory space (KB) ?
  - How many of the 2Kx8 chips are needed?

23

Solution

- Minimum address is $0000, maximum address is $1FFF.

- $(1FFF)_{16} = (8191)_{10}$
  - For address $0000, 1 should be added to 8191.

- Total memory space = **8192** locations (bytes).

- KB calculation for total memory = 8192 / 1024 = **8 KB**
  - 1 KB = 1024 bytes

- 8 KB / 2 KB = 4 chips are required.
  - Each chip has 2 KB.

24

Memory Map

- **A0-A10:** Used for locations within a memory chip.
- **A11-A12:** Used for memory chip selections.
  (Chip select is done with address bits that are not used within the memory chip.)
- **A13-A15:** Used for decoder enable.

Chips	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}..... A_0
Memory 1	0	0	0	0	0	Used to address locations within a memory chip. (**2K** locations each)
Memory 2	0	0	0	0	1	
Memory 3	0	0	0	1	0	
Memory 4	0	0	0	1	1	

For enabling the decoder (optional) — For chip selections — For location selection within a chip

25

Memory Map

- 2 K locations within a chip requires 11 address bits.
- $\log_2 2048 = 11$ **(A_0 thru A_{10})**

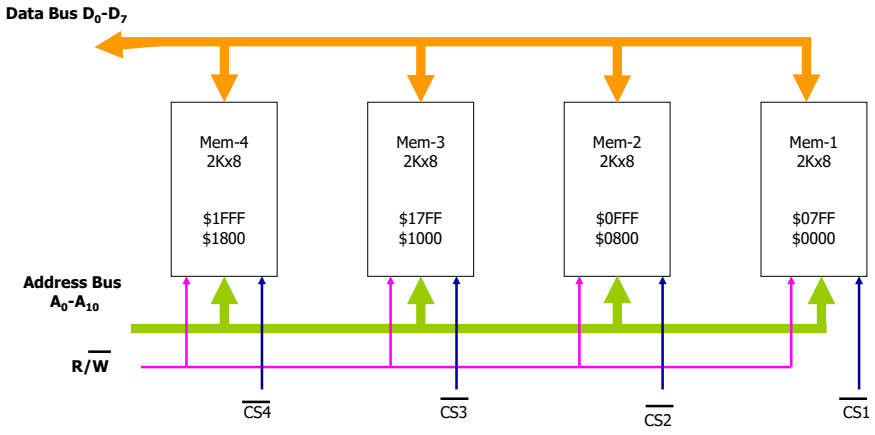
$A_{15}A_{14}A_{13}A_{12}$	$A_{11}A_{10}A_9A_8$	$A_7A_6A_5A_4$	$A_3A_2A_1A_0$		
0000	0000	0000	0000	$0000	**CHIP1**
0000	0111	1111	1111	$07FF	
0000	1000	0000	0000	$0800	**CHIP2**
0000	1111	1111	1111	$0FFF	
0001	0000	0000	0000	$1000	**CHIP3**
0001	0111	1111	1111	$17FF	
0001	1000	0000	0000	$1800	**CHIP4**
0001	1111	1111	1111	$1FFF	

Decoder Enable — Chip selection — Location selection within a chip

26

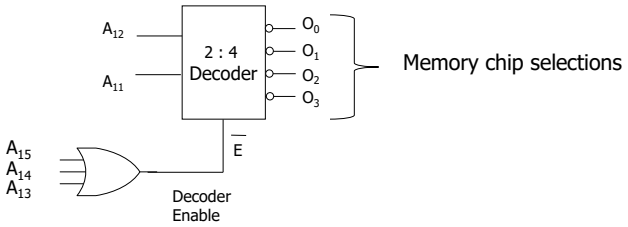
Memory Organization

- Connect the DATA BUS, ADDRESS BUS, R/W' signals together.
- The CS's will be determined by using A12 and A11 thru a decoder.



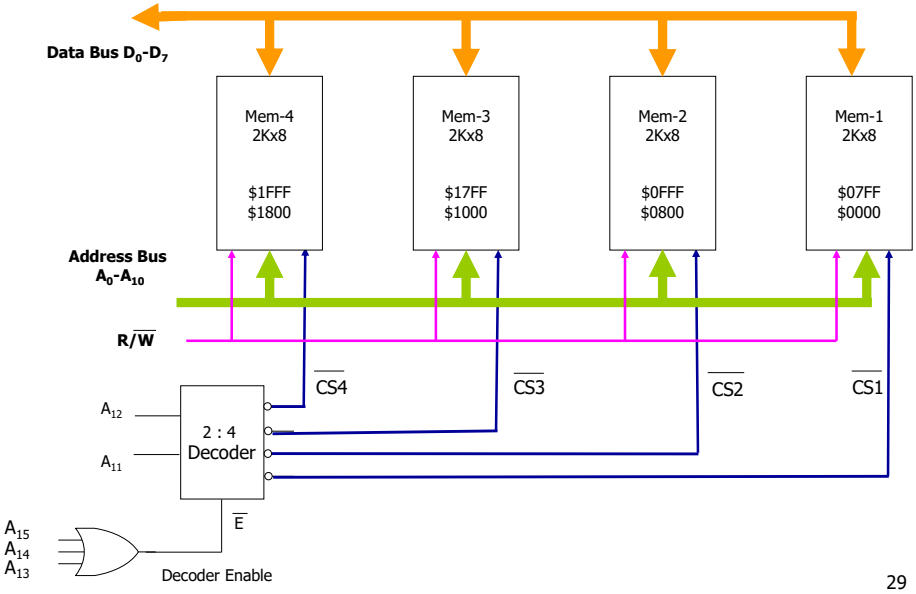
Decoder Design

- A_{15}, A_{14}, A_{13} address lines remain at low at all times.
  - When all of them are 0, the decoder will be activated.
  - They are used to form the decoder selection (**Decoder Enable**) signal.
- A_{12} and A_{11} can be used to select memory chips with 2-to-4 decoder.



Memory Organization

(Complete with the decoder shown)



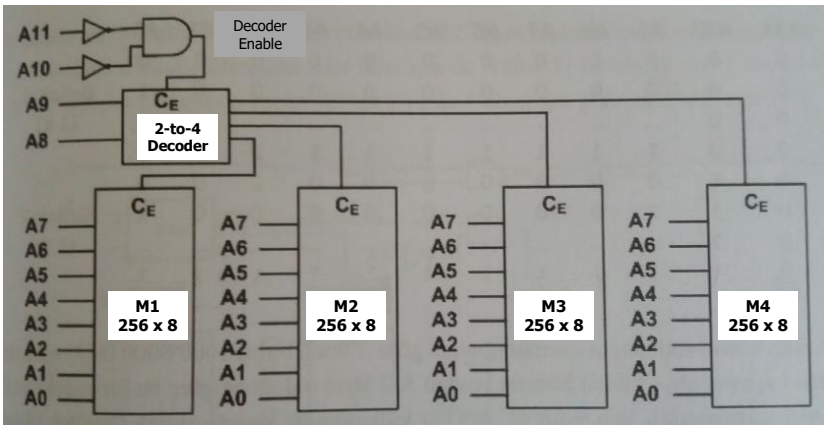
Example2 : Memory Design

- Suppose a memory subsystem will be designed for a microprocessor with the following features.
  - **Data Bus** = 8 bits
  - **Address Bus** = 12 bits
  - Each memory chip is **256 x 8** bits.
  - Total addressable capacity will be **1 KB**.

- **QUESTIONS:**
  - How many memory chips are required?
  - Determine the address lines for location selection within a chip, and also the address lines for the decoder inputs.
  - Draw the block diagram of memory design.
  - Write the address ranges (smallest and biggest addresses) for each memory chip.

Solution

- Address bus is **12 lines**, data bus is **8 lines**.
- **4** memory chips will be used with **256x8** bits each. (Total is 1024x8)
- **A_0 - A_7** are used for location selection within a chip (2^8 = 256 locations)
- **Address Decoder** is used for chip selections (CE : Chip Enable) (**A_8 and A_9** are inputs of the decoder.)
- **A_{10} and A_{11}** are used to select the decoder itself (Decoder Enable).
- Data Bus and R/W ' lines have been omitted in this block diagram.



Summary of Memory Address Map (Binary)

MEMORY CHIP	DECODER ENABLE		MEMORY CHIP SELECT		LOCATION SELECTION WITHIN A CHIP (X means bit can be either 0 or 1)							
	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
MEMORY1	0	0	0	0	X	X	X	X	X	X	X	X
MEMORY2	0	0	0	1	X	X	X	X	X	X	X	X
MEMORY3	0	0	1	0	X	X	X	X	X	X	X	X
MEMORY4	0	0	1	1	X	X	X	X	X	X	X	X

Details of Memory Address Map (Binary)

MEMORY CHIP	DECODER ENABLE		MEMORY CHIP SELECT		LOCATION SELECTION WITHIN A CHIP							
	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
MEMORY1	0	0	0	0	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	0	0	0	0	1
	0	0	0	0	. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .
	0	0	0	0	1	1	1	1	1	1	1	1
MEMORY2	0	0	0	1	0	0	0	0	0	0	0	0
	0	0	0	1	0	0	0	0	0	0	0	1
	0	0	0	1	. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .
	0	0	0	1	1	1	1	1	1	1	1	1
MEMORY3	0	0	1	0	0	0	0	0	0	0	0	0
	0	0	1	0	0	0	0	0	0	0	0	1
	0	0	1	0	. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .
	0	0	1	0	1	1	1	1	1	1	1	1
MEMORY4	0	0	1	1	0	0	0	0	0	0	0	0
	0	0	1	1	0	0	0	0	0	0	0	1
	0	0	1	1	. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .
	0	0	1	1	1	1	1	1	1	1	1	1

33

Memory Address Map (Hexadecimal)

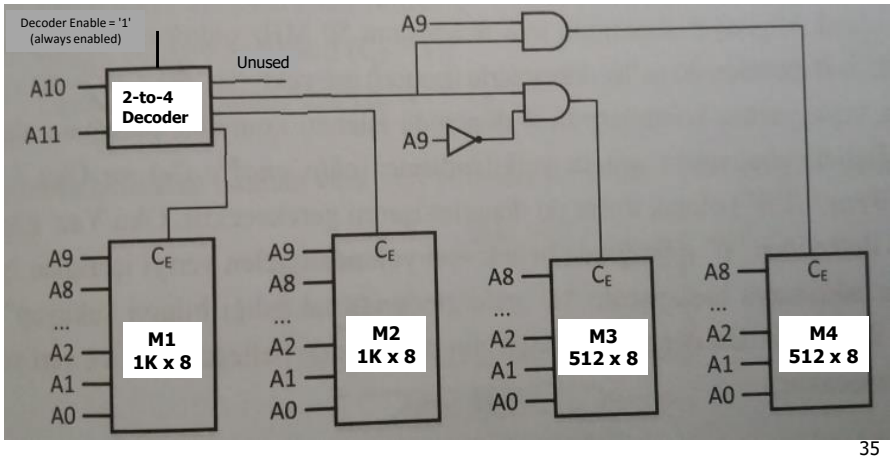
CHIP	SMALLEST ADDRESS ($A_{11} - A_0$)	BIGGEST ADDRESS ($A_{11} - A_0$)	CAPACITY
M1	0 0 0	0 F F	256 B
M2	1 0 0	1 F F	256 B
M3	2 0 0	2 F F	256 B
M4	3 0 0	3 F F	256 B
EMPTY	4 0 0	F F F	3 KB

- Total capacity is $2^{12} = 2^2 . 2^{10} =$ **4 KB**
- Addressable capacity = 4 x 256 B = 1024 B = **1 KB** (used)
- Empty = 4 KB – 1 KB = 3 KB

34

Example3 : Memory Design with Different Chip Types

- Total addressable memory capacity is = (1 KB * 2) + (512 B * 2) = 3 KB
- A9 address line is used to distinguish between M3 and M4 memory chips.
  - If A9 is 0, then M3 is selected.
  - If A9 is 1, then M4 is selected.



Memory Address Map (Binary)

CHIP	SMALLEST ADDRESS												BIGGEST ADDRESS											
	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
M1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
M2	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1
M3	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	1	1	1	1	1	1	1
M4	1	0	1	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	1	1	1	1

Chip select — M3/M4 distinguished

Chip select — M3/M4 distinguished

Memory Address Map (Hexadecimal)

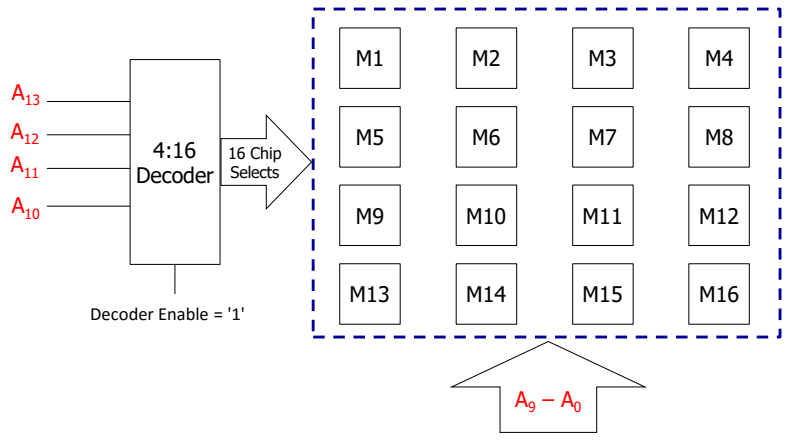
CHIP	SMALLEST ADDRESS ($A_{11} - A_0$)	BIGGEST ADDRESS ($A_{11} - A_0$)	CAPACITY
M1	0 0 0	3 F F	1 KB
M2	4 0 0	7 F F	1 KB
M3	8 0 0	9 F F	512 B
M4	A 0 0	B F F	512 B
EMPTY	C 0 0	F F F	1 KB

- Total capacity is $2^{12} = 2^2 . 2^{10}$ = **4 KB**
- Addressable capacity = 1KB + 1KB + 512B + 512B = **3 KB** (used)
- Empty = 4 KB – 3 KB = 1 KB

37

Example4 : 16 Memory Chips (Each 1KBx8 Bit)

- There are 16 identical memory chips.
- Each memory chip is 1 KB (1024 bytes = 2^{10}). Therefore 10 addres lines (A_9-A_0) are used for location selection within a memory chip.
- 4:16 decoder is used for memory chip selections. 4 address lines (A_{13}-A_{10}) are used as inputs. 16 outputs of decoder are used for memory chip selections.
- Total number of address lines = **10 + 4 = 14 lines**



38

Memory Address Map (Hexadecimal)

CHIP	SMALLEST ADDRESS ($A_{13} - A_0$)	BIGGEST ADDRESS ($A_{13} - A_0$)	CAPACITY
M1	0 0 0 0	0 3 F F	1 KB
M2	0 4 0 0	0 7 F F	1 KB
M3	0 8 0 0	0 B F F	1 KB
M4	0 C 0 0	0 F F F	1 KB
M5	1 0 0 0	1 3 F F	1 KB
M6	1 4 0 0	1 7 F F	1 KB
M7	1 8 0 0	1 B F F	1 KB
M8	1 C 0 0	1 F F F	1 KB
M9	2 0 0 0	2 3 F F	1 KB
M10	2 4 0 0	2 7 F F	1 KB
M11	2 8 0 0	2 B F F	1 KB
M12	2 C 0 0	2 F F F	1 KB
M13	3 0 0 0	3 3 F F	1 KB
M14	3 4 0 0	3 7 F F	1 KB
M15	3 8 0 0	3 B F F	1 KB
M16	3 C 0 0	3 F F F	1 KB

- Total capacity is $2^{14} = 2^4 . 2^{10}$ = **16 KB**
- Addressable capacity = 16 chips x 1KB = **16 KB**

39