Homework 2

Notes:

1) *For questions related to the usage of the tool, please refer to the last lecture recording.*
2) *This is not a group work. Each student will design their assigned gate(s) separately.*

In this homework, each student will design the gate that are assigned to them at CMOS level. Each student should design their own given gate(s) INDIVIDUALLY. Refer to the list at the end of the document for assignments.

1) Create new schematic(s) and symbols for your gates within your workplace, using the naming scheme below.

- For cells: <gatename>_<yourname> **(Ex: NAND2_firatkula)**
- For simulations: <gatename>_<yourname>_sim

a) Use L=150 nm. Explain your designing process. Add screenshots of the final circuit schematics to your report. While naming circuit pins, use the naming scheme below.
   - For inputs: IN1, IN2, IN3…
   - For outputs: OUT
   - Power supply: DVDD, DGND

b) Create new simulation environments for your designs. Using Ngspice, simulate your circuit for all possible input combinations. Input sets should change at each 100 ns. Use 100 fF capacitive load. Show your output waveform. Explain your results.

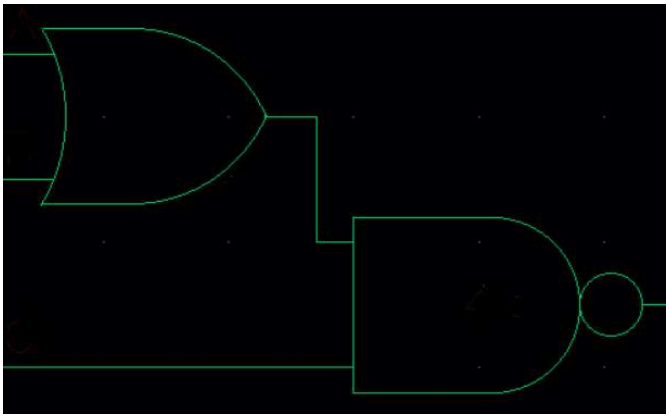
c) Do layouts for your circuits using Magic, following the sizing ruleset below. Add screenshots of your final layouts. Show that your layout is DRC and LVS clean.

   - DVDD and DGND heights: 1 µm each
   - Core height: 8 µm (Netting 10µm total height)

d) Do parasitic extraction after the layout process. Compare your results with schematic results.

Muhammet Alçın	3-input OR gate (OR3)
Mahmud Emin Ertürk	ORNAND gate(*)
Oğuzhan Vatansever	ANDNOR gate(**)
Murat Faruk Aydın	2-input NAND gate (NAND2), 3-input NOR gate (NOR3)
Muhammed Erkmen	2-input NOR gate (NOR2), 3-input NAND gate (NAND3)
Azmi Enes Şentürk	2-input AND gate (AND2), NOT gate
Behiç Erdem	2-input OR gate (OR2), NOT gate
Ömer Faruk Sert	3-input AND gate (AND3)
Burak Can Doğan	3-input OR gate (OR3)
Hüseyin Cahit Erbil	ORNAND gate(*)
Yiğit Bektaş Gürsoy	ANDNOR gate(**)
Yiğit Arda Özen	2-input NAND gate (NAND2), 3-input NOR gate (NOR3)
Telat Işık	2-input NOR gate (NOR2), 3-input NAND gate (NAND3)
İbrahim Sevinç	2-input AND gate (AND2), NOT gate
Cemalettin Cem Belentepe	2-input OR gate (OR2), NOT gate
Ekin Türkü Erdoğan	3-input AND gate (AND3)
Rana Tilki	3-input OR gate (OR3)
Deniz Bashgoren	ORNAND gate(*)
Mustafa Emre Yılmaz	ANDNOR gate(**)
Bora İnan	2-input NAND gate (NAND2), 3-input NOR gate (NOR3)
Mehmet Eymen Ünay	2-input NOR gate (NOR2), 3-input NAND gate (NAND3)
Mert Olpak	2-input AND gate (AND2), NOT gate
Fatih Enes Doğan	2-input OR gate (OR2), NOT gate
Fatih Bebe	3-input AND gate (AND3)
Armin Asgharifard	3-input OR gate (OR3)
Alp Eren Kıyak	ORNAND gate(*)

(*)OR-NAND



(**)AND-NOR