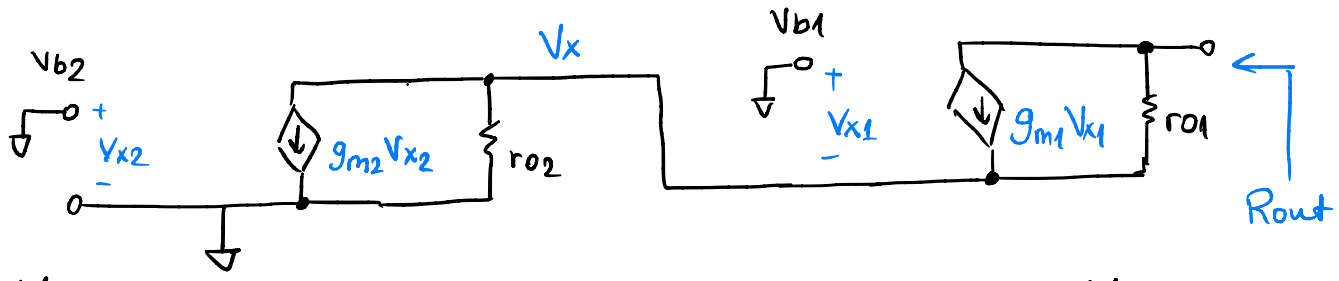
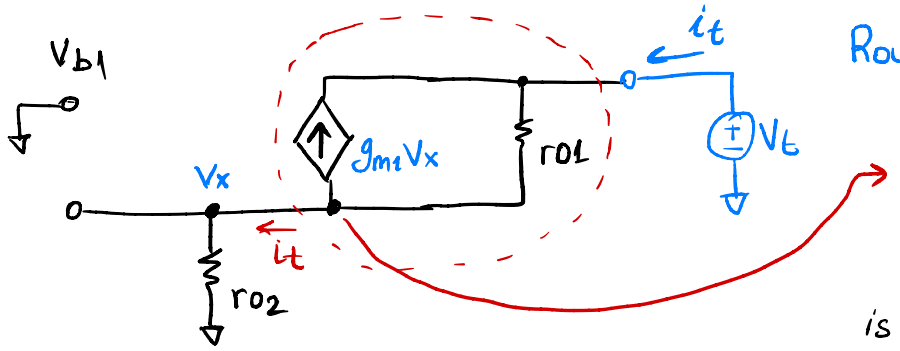
EHB 262E - Electronics II

Homework-2 Solutions

(50p) a) First, let's draw the small signal model. Remember, DC sources will be zero. $V_{b1,2}$ and V_{DD} are the DC voltage sources.



$V_{x2} = 0 \longrightarrow g_m V_{x2} = 0 \longrightarrow$ open circuit, so let's simplify the circuit:



$R_{out} = \frac{V_t}{i_t}$

Notice $V_{x1} = V_{b1} - V_x = 0 - V_x = -V_x$

So, current source direction is changed.

Node equation:

$$i_t + \frac{V_x - V_t}{r_{o1}} + g_{m1} V_x = 0 \quad (\text{Notice } V_x = i_t r_{o2})$$

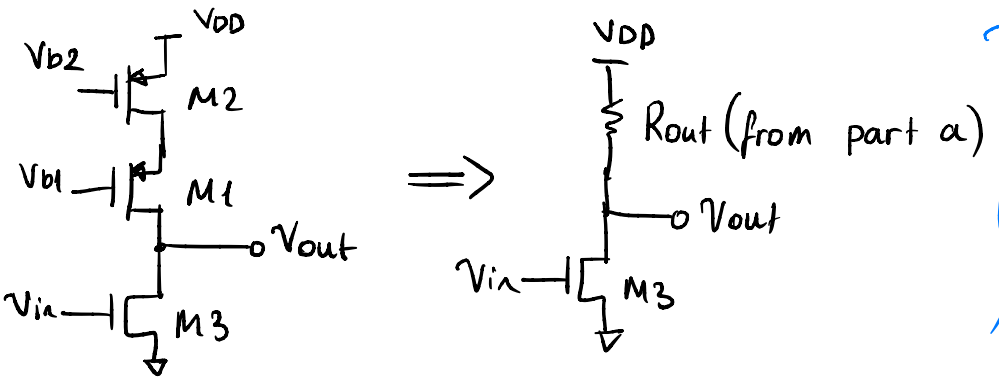
$$\Downarrow$$

$$i_t + \frac{i_t r_{o2} - V_t}{r_{o1}} + g_{m1} i_t r_{o2} = 0 \Rightarrow i_t \left(1 + \frac{r_{o2}}{r_{o1}} + g_{m1} r_{o2}\right) = \frac{V_t}{r_{o1}}$$

$$\Rightarrow i_t \left(r_{o1} + r_{o2} + g_{m1} r_{o2} r_{o1}\right) = V_t \Rightarrow R_{out} = r_{o1} + r_{o2} + g_{m1} r_{o1} r_{o2}$$

Sometimes we use $R_{out} \cong (g_{m1} r_{o1}) r_{o2}$. Therefore, cascode topology boosts the output resistor by an intrinsic gain $(g_{m1} r_{o1})$ factor. If we use only M2, output resistance will be r_{o2}. In this topology, trade-off is the headroom. In order to keep both M1 and M2 into saturation, we need at least $2 \times (V_{GS} - V_{TH})$ voltage drop on the transistors.

(50p) b)



$K_v = \frac{V_{out}}{V_{in}} = -g_{m3} R_{out}$

Note: In reality, $K_v = -g_{m3}(r_{o3} \,//\, R_{out})$ and generally $r_{o3} < R_{out}$ so $K_v \cong -g_{m3} r_{o3}$. Because of that we need to use cascode for NMOS part as well. But I wanted you to ignore this.

$$g_{m3} = \sqrt{2 I_{D3} \mu_n C_{ox} \left(\frac{W}{L}\right)_3} = 1.73\,mS$$

$$g_{m2} = \sqrt{2 I_{D2} \mu_p C_{ox} \left(\frac{W}{L}\right)_2} = 1.41\,mS$$

$$r_{o1} = r_{o2} = \frac{1}{\gamma_p I_{D1,2}} \cong 13.3\,k\Omega$$

$$R_{out} = r_{o1} + r_{o2} + g_{m2} r_{o2} r_{o1} \cong 276\,k\Omega \Rightarrow K_v \cong -477\,\frac{V}{V}$$