VLSI-2 HOMEWORK-8

1. **Pipelineing the processor:**
   Convert your single cycle processor to a 5-stage pipelined RISC-V processor by using the structure shown on page 18 of lecture slides **"ITU_VLSI_II_Computer_Organization_Pipeline.pdf"** as basis. Note that your design might be different from this example. You will first design your processor without any hazard handling.
   a. Explain your pipeline design and all other work that you have done for implementing the 5-stage pipelined structure.
   b. Draw a detailed structure of your entire design. You may use horizontal page layout.
   c. Write machine code for the algorithm shown in Fig. 1.
   d. Attempt to run the code you've prepared at **Homework 7-Part 5c** on your pipelined processor on a behavioral simulation. Because you do not have any hazard handling in your design, the simulation result may not be correct. Explain your findings and try to solve the problem (if there is any) by introducing NOP operations where you think that will be useful.

2. **Structural Hazards:**
   a. Considering your current 5-stage pipeline, describe one scenario that could cause a structural hazard in your processor.
   b. Change your Register file design in order to avoid the hazard that you described in 2.a (Hint: Separate write and read ports, half cycle operation). If you've already designed your Register file in a way it would not cause any structural hazard, you may skip to step 1d.
   c. Show the added and edited parts in your corresponding Verilog code.
   d. Perform behavioral simulation for processor in order to show that your design works as expected by applying a small sequence of instructions that would only cause this structural hazard. Explain your results by showing your waveform outputs and verify that hazard is handled.

3. **Data Hazards - Read-After-Write (RAW) Hazards:**
   a. Consider all scenarios that cause RAW hazards (including memory-to-memory copies). Choose one of the hardware solutions shown in lecture slides **"ITU_VLSI_II_Computer_Organization_Pipeline_2.pdf"** to integrate within the appropriate places in your pipeline.
   b. Apply stalling and/or forwarding circuitry in your design, depending on your selection.
   c. Show the added/edited parts in your corresponding Verilog code.
   d. Perform behavioral simulation for your processor in order to show that your design works as expected by applying a small sequence of instructions. Individually simulate each case and show that the hazards are properly handled. Clearly show and explain your results on waveform outputs.
   e. Explain your results by showing your waveform outputs and verify that hazard is handled.

   Note: CPI=1 is expected for getting a full grade in this question.

4. **Data Hazards - Load-Use Hazards:**
   a. Consider the case where load-use hazard will occur. Apply the hardware solution shown in lecture slides **"ITU_VLSI_II_Computer_Organization_Pipeline_2.pdf"** within the appropriate places in your pipeline.
   b. Add extra stalling and forwarding circuitry to appropriate places, if needed.
   c. Show the added/edited parts in your corresponding Verilog code.

d. Perform behavioral simulation for your processor in order to show that your design works as expected by applying a small sequence of instructions. Individually simulate each case and show that the hazards are properly handled. Clearly show and explain your results on waveform outputs.

Note: CPI=2 is expected for full grade in this question.

5. **Control Hazards - Jumps:**
   a. It is shown that the instruction that is fetched right after a jump instruction must be terminated to prevent it from wrongly altering the data within registers and memory. This operation is called **"flushing"**. Add flushing circuitry for jumps to your processor structure.
   b. Show the added/edited parts in your corresponding Verilog code.
   c. Perform behavioral simulation for your processor in order to show that your design works as expected by applying the sequence of instructions given below. Show that the hazards are properly handled. Clearly show and explain your results on waveform outputs.

```
<arbitrary arithmetic instruction>
JAL …
<arbitrary arithmetic instruction >
<arbitrary arithmetic instruction >
(JAL destination) <arbitrary arithmetic instruction >
<arbitrary arithmetic instruction >
```

6. **Control Hazards - Branches:**
   a. Resolve branch hazards in your pipeline by applying one of the hardware solutions shown in lecture slides **"ITU_VLSI_II_Computer_Organization_Pipeline_2.pdf".** You do not need to consider branch decisions at IF stage.
   b. Apply the required circuitry in your design.
   c. Show the added/edited parts in your corresponding Verilog code.
   d. Perform behavioral simulation for your processor by in order to show that your design works as expected by applying a small sequence of instructions. Individually simulate each case and show that the hazards are properly handled. Clearly show and explain your results on waveform outputs.

Note: CPI=2 is expected for full grade in this question (You are NOT expected to handle the branch decision in IF stage).

7. **Running an Example Program:**
   An example bubble sort algorithm is provided within Homework files, under and archive named "bubble_sort.zip". Note that all files within this archive can be opened by a text editor. Contents of this archive are as follows:
   - ***bubble_sort.c:*** Original algorithm written in C.
   - ***bubble_sort.s:*** Compiled and disassembled version of "bubble_sort.c", done for RV32I set.
   - ***bubble_sort.instr:*** Instruction memory initialization file, containing machine code level instructions from "bubble_sort.s", through its <.text> section.
   - ***bubble_sort.data:*** Data memory initialization file, containing read only data from "bubble_sort.s", through its <.rodata> section.

   a. Create a testbench that contains an instance of your pipelined processor, one instance of instruction memory and one instance of data memory from Homework 5. Each memory should

have 128 words, with their word length set to 32-bits. Connect memories to the processor within the testbench.

b. Initialize the instruction memory with **"bubble_sort.instr"**, and data memory with **"bubble_sort.data"** files; using **$readmemh** function.
c. The program you've loaded in your instruction memory takes the unsorted integer array `arr[] = {195,14,176,128}` from data memory from data memory addresses **0x10C through 0x118,** and writes its sorted version to the data memory addresses **0x1D4 through 0x1E0**. Perform a behavioral simulation and run the program **until PC value becomes 0x108**. Show that your processor can run this program successfully.

8. OpenLane Flow:

a. Apply full OpenLane flow to the final version of your processor. Max fanout, capacitance and slew warnings can be ignored.
b. After successfully completing the flow, navigate through OpenLane reports to obtain approximate maximum clock frequency, total die area, total cell count and approximate power consumption of your design. Add the report folder associated with your run to your design submission archive folder.
c. By using OpenRoad GUI interface, add post place and route layout schematic of your design to the report.

Note: Consider using ROUTING_CORES and KLAYOUT_XOR_THREADS configuration variables in your config.json file. These variables set the number of cores to participate on certain time-consuming sections of OpenLane flow, thereby decreasing the runtime. Refer to link below:

https://openlane.readthedocs.io/en/latest/reference/configuration.html

Please write your reports as a group homework. Do not forget to add cover page and page numbers. Try to write the report regularly and well organized! You may use tables, explanations, figures, drawings, etc.