



VLSI Circuit Design II– EHB 425E

HOMEWORK II

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Class Lecturer: Sıddıka Berna Örs Yalçın

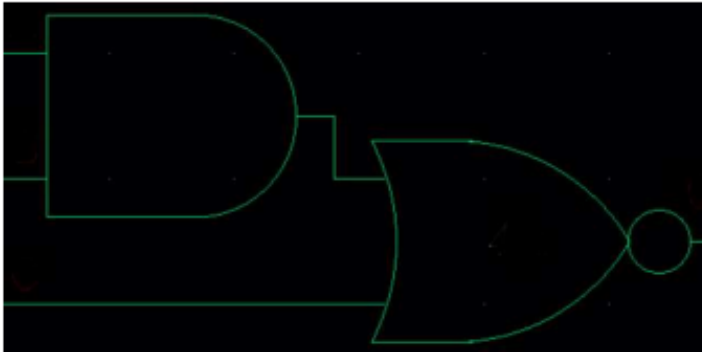
**Class Assistant:
Yasin Fırat Kula**

1- Circuit in Homework

As stated in the assignment 2 file, my circuit consists of 1 AND and 1 NOR gate.


Yiğit Bektaş Gürsoy

ANDNOR gate(**)




The individual truth tables for these gates are shown below.

AND



INPUT		OUTPUT
A	B	
0	0	0
1	0	0
0	1	0
1	1	1

NOR



INPUT		OUTPUT
A	B	
0	0	1
1	0	0
0	1	0
1	1	0

In order to create a truth table of the circuit shown, x, y and z inputs are given respectively as a representation. The value coming out of the AND gate is "xy" and the inputs entering the NOR gate are xy and z. The value to be output at the NOR gate is $(x'+y')z'=x' + y'z'$. The truth table resulting from this boolean equation is also given below.

X,Y (AND) XY

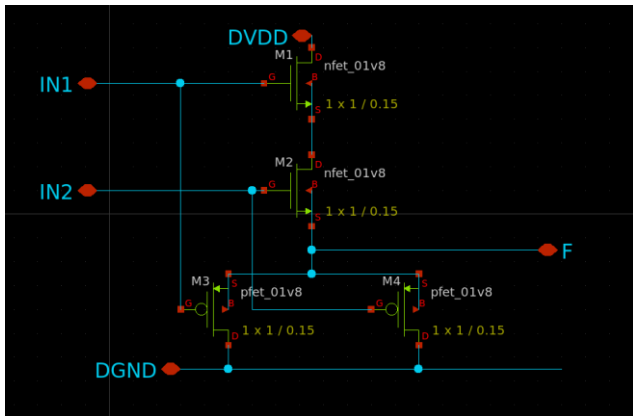
XY,Z (NOR) $(XY+Z)'=(X'+Y')Z'=X'Z'+Y'Z'$

Truth Table

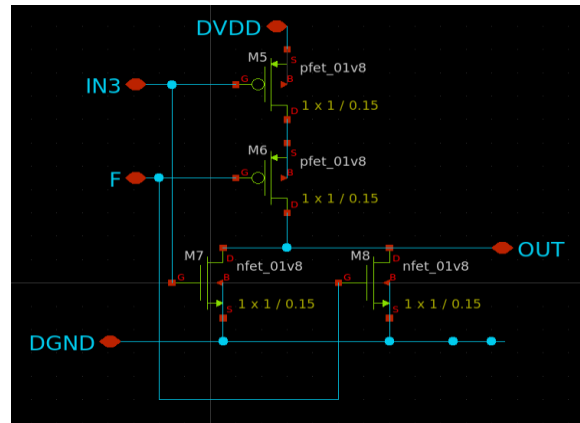
	A	B	C	Y
0	0	0	0	1
1	0	0	1	0
2	0	1	0	1
3	0	1	1	0
4	1	0	0	1
5	1	0	1	0
6	1	1	0	0
7	1	1	1	0

2- Designing Process

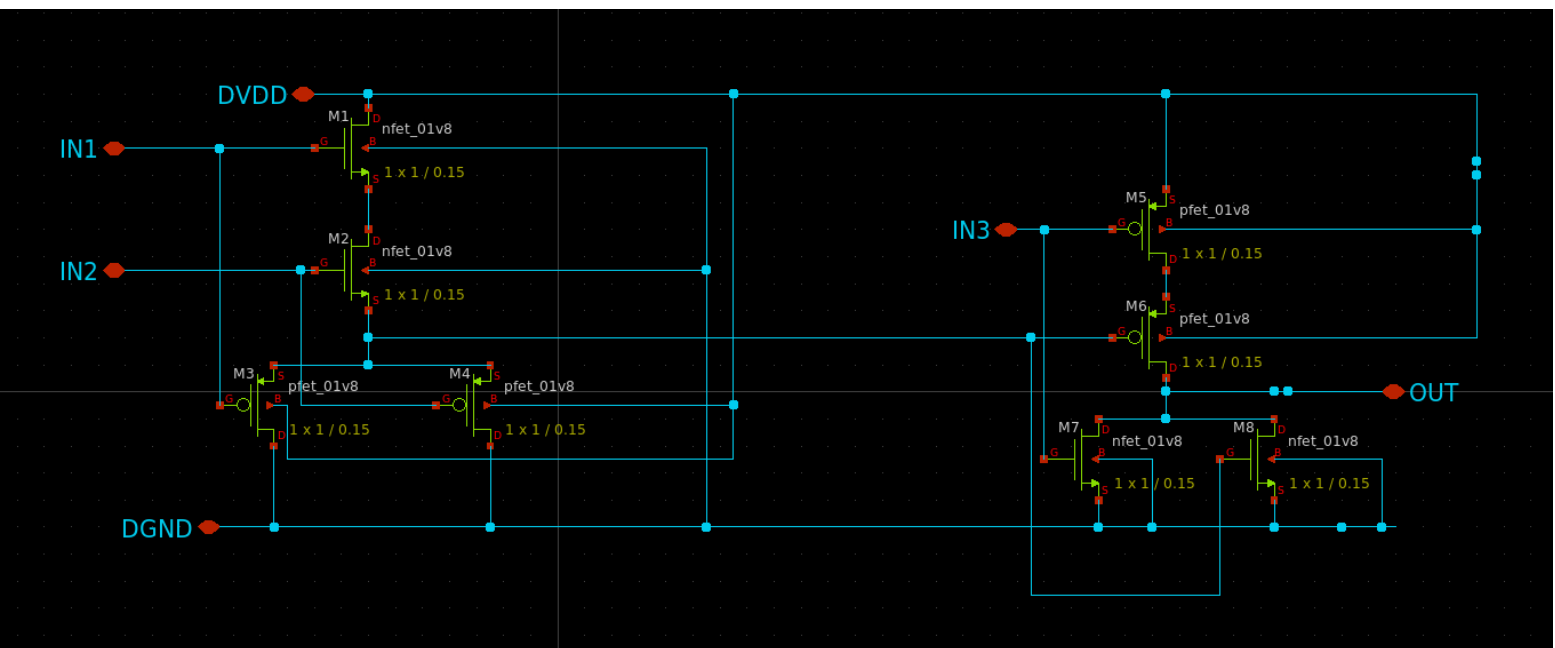
Using pmos and nmos symbols in xschem program, AND and NOR gates were implemented as follows. The inputs are listed as IN1, IN2 and IN3. DVDD is specified as the power source and DGND is specified as the ground. "F", which is the output from the AND gate, is determined as an input of the other gate.



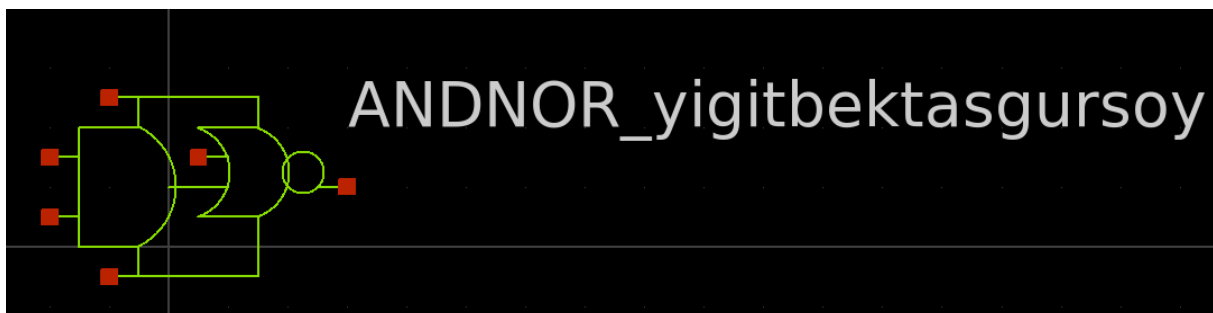
AND GATE



NOR GATE

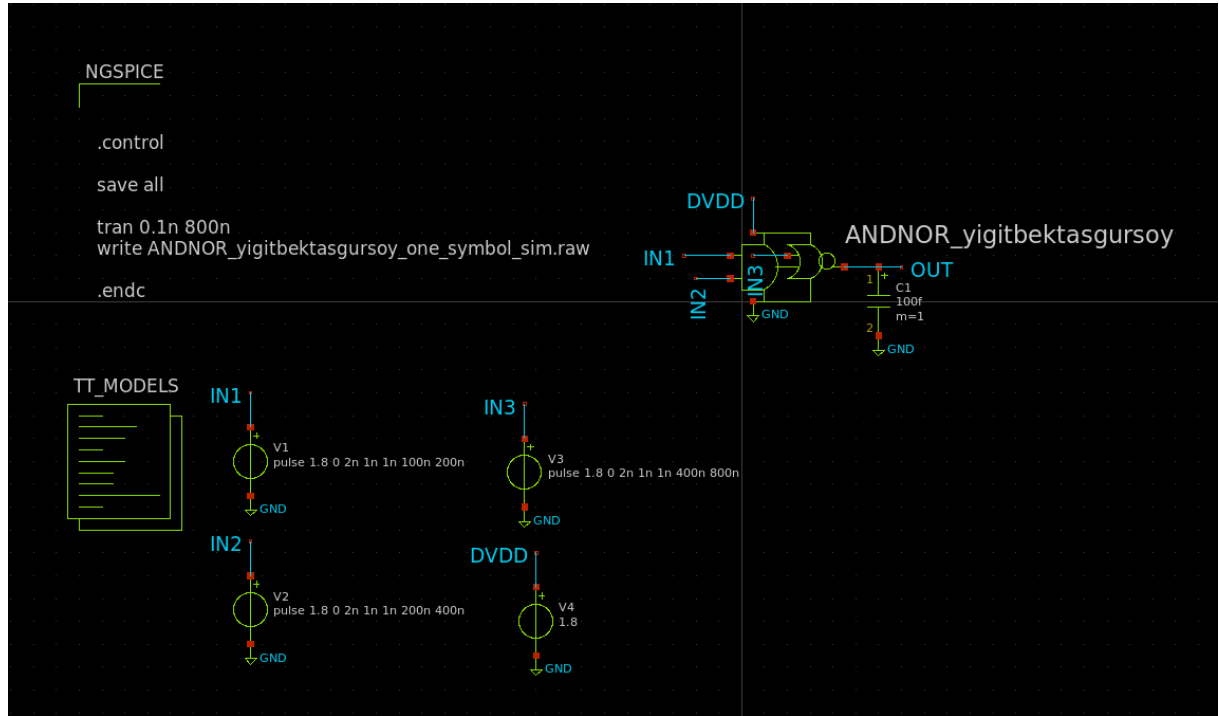


ANDNOR GATE



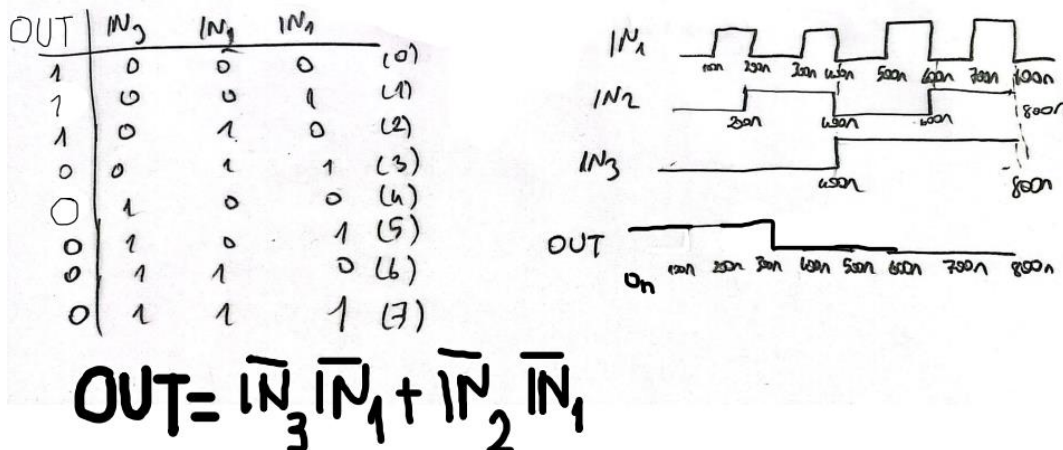
ANDNOR GATE SYMBOL

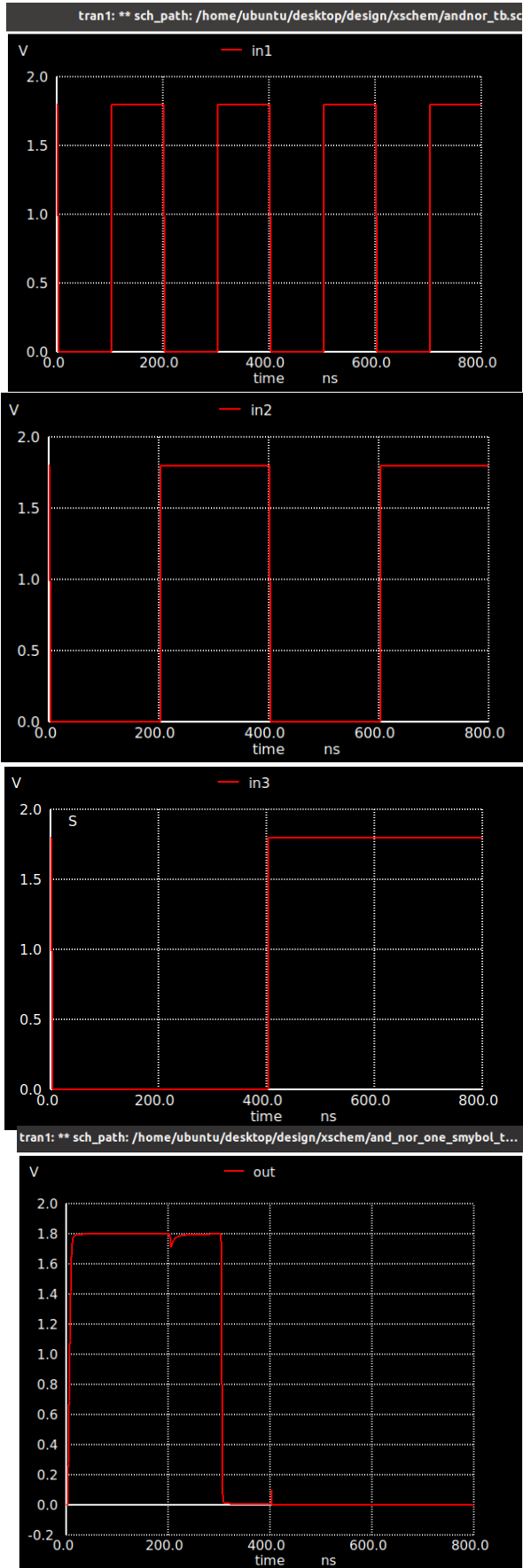
Above, representative symbols for properly connecting the gates to each other have been drawn and put into a single schematic. Then, source and ground are connected to the relevant places to simulate the circuit. After entering the appropriate values for ngspice, the simulation was performed by clicking the "Netlist" button and then the "Simulation" button. The relevant schematic and related results are given below.



3- Simulation Process

In order to match the hand results with the simulation results, the boolean function of the circuit was extracted and the logic signals were drawn. The simulation results then need to be compared with ngspice simulations to validate.





```
andnor_TB.spice" -a || sh

** The U. C. Berkeley CAD Group
** Copyright 1985-1994, Regents of the University of California,
** Copyright 2001-2020, The ngspice team.
** Please get your ngspice manual from http://ngspice.sourceforge.net/docs.html
** Please file your bug-reports at http://ngspice.sourceforge.net/bugrep.html
** Creation Date: Fri Mar  4 13:38:42 UTC 2022
*****

Compatibility modes selected: hs a

Warning: m=xx on .subckt line will override multiplier m hierarchy!

Circuit: ** sch_path: /home/ubuntu/desktop/design/xschem/andnor_tb.sch
option SCALE: Scale is set to 1e-06 for instance and model parameters
Doing analysis at TEMP = 27.000000 and TNOM = 27.000000

Warning: v3: no DC value, transient time 0 value used
Warning: v2: no DC value, transient time 0 value used
Warning: v1: no DC value, transient time 0 value used

Initial Transient Solution

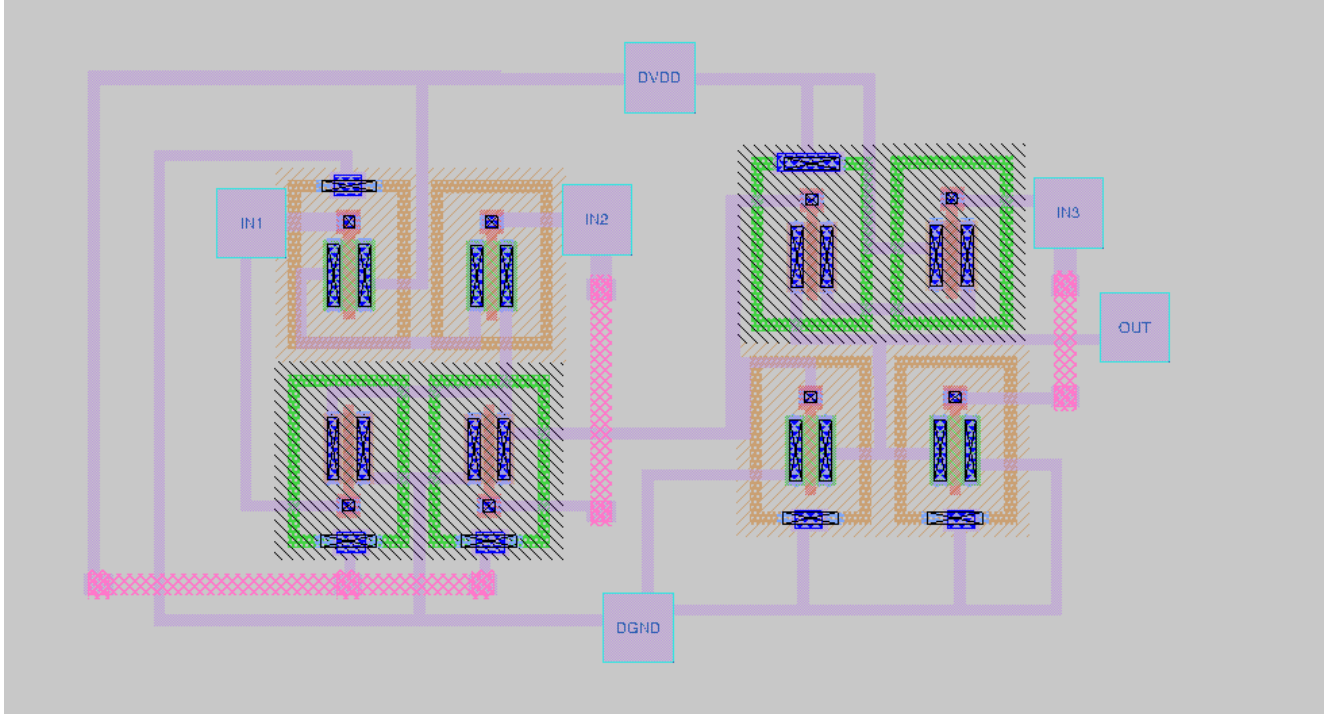
-----
Node                Voltage
-----
dvdv                1.8
in1                 1.8
x1.net1             1.59123
in2                 1.8
x2                 1.56561
x2.net1             1.75749
out                 9.08841e-08
in3                 1.8
v4#branch           -2.54168e-10
v3#branch           0
v2#branch           0
v1#branch           0

Reference value : 0.00000e+00
No. of Data Rows : 8065
Binary raw file "ANDNOR_yigitbektasgursoy.sim.raw"
Doing analysis at TEMP = 27.000000 and TNOM = 27.000000

Warning: v3: no DC value, transient time 0 value used
Warning: v2: no DC value, transient time 0 value used
Warning: v1: no DC value, transient time 0 value used
ngspice 1 -> plot in1
ngspice 2 -> plot in2
ngspice 3 -> plot in3
ngspice 4 -> plot out
```

First, as shown in the image above, IN1, IN2, IN3 and OUT signals were plotted, respectively. All possible situations are given at 100ns intervals and 100fF capacite load is added to the circuit. Then it was put on the same scale and compared with the previously found results. The simulation results were matched with the above mentioned truth table and the drawn waveform. The circuit is working correctly.

The layout of the given circuit was created by taking help from the TUTEL pdf files in the class files in Ninova and using the magic program. The layout is as follows.



The necessary commands were written to confirm the correctness of the extracted layout, and a file was created for testing on netgen. Then it was tested. No errors were found in the tests, the layout and the circuit match each other exactly. The relevant results are given below. (DRC and LVS are clean)

```
tkcon 2.3 Main
File Console Edit Interp Prefs History Help
Writing 'and_nor_one_symbol'
% extract all
Extracting skyl130_fd_pr_nfet_01v8_5WU4M2 into /home/ubuntu/Desktop/design/mag/skyl130_fd_pr_nfet_01v8_5WU4M2.ext:
Extracting skyl130_fd_pr_nfet_01v8_4WUEFQ into /home/ubuntu/Desktop/design/mag/skyl130_fd_pr_nfet_01v8_4WUEFQ.ext:
Extracting skyl130_fd_pr_pfet_01v8_AQMKDE into /home/ubuntu/Desktop/design/mag/skyl130_fd_pr_pfet_01v8_AQMKDE.ext:
Extracting skyl130_fd_pr_pfet_01v8_NKK3FE into /home/ubuntu/Desktop/design/mag/skyl130_fd_pr_pfet_01v8_NKK3FE.ext:
Extracting skyl130_fd_pr_pfet_01v8_QKK3FL into /home/ubuntu/Desktop/design/mag/skyl130_fd_pr_pfet_01v8_QKK3FL.ext:
Extracting skyl130_fd_pr_nfet_01v8_BXYDM4 into /home/ubuntu/Desktop/design/mag/skyl130_fd_pr_nfet_01v8_BXYDM4.ext:
Extracting and_nor_one_symbol into /home/ubuntu/Desktop/design/mag/and_nor_one_symbol.ext:
% ext2spice lvs
% ext2spice
ext2spice finished.
Unknown macro or short command: 'Control_XK_Pointer_Button4'
% drc why
No errors found.
```

```
tkcon 2.3 Main
File Console Edit Interp Prefs History Help
No property ad found for device skyl30_fd_pr_pfet_01v8
No property ps found for device skyl30_fd_pr_pfet_01v8
No property pd found for device skyl30_fd_pr_pfet_01v8
No property mult found for device skyl30_fd_pr_pfet_01v8
No property sa found for device skyl30_fd_pr_pfet_01v8
No property sb found for device skyl30_fd_pr_pfet_01v8
No property sd found for device skyl30_fd_pr_pfet_01v8
No property nf found for device skyl30_fd_pr_pfet_01v8
No property nrd found for device skyl30_fd_pr_pfet_01v8
No property nrs found for device skyl30_fd_pr_pfet_01v8
No property area found for device skyl30_fd_pr_pfet_01v8
No property perim found for device skyl30_fd_pr_pfet_01v8
No property topography found for device skyl30_fd_pr_pfet_01v8
Comparison output logged to file comp.out
Logging to file "comp.out" enabled
Circuit skyl30_fd_pr_nfet_01v8 contains no devices.
Circuit skyl30_fd_pr_pfet_01v8 contains no devices.

Contents of circuit 1: Circuit: 'and_nor_one_symbol'
Circuit and_nor_one_symbol contains 8 device instances.
  Class: skyl30_fd_pr_nfet_01v8 instances: 4
  Class: skyl30_fd_pr_pfet_01v8 instances: 4
Circuit contains 9 nets.
Contents of circuit 2: Circuit: 'and_nor_one_symbol'
Circuit and_nor_one_symbol contains 8 device instances.
  Class: skyl30_fd_pr_nfet_01v8 instances: 4
  Class: skyl30_fd_pr_pfet_01v8 instances: 4
Circuit contains 9 nets.

Circuit 1 contains 8 devices, Circuit 2 contains 8 devices.
Circuit 1 contains 9 nets, Circuit 2 contains 9 nets.

Netlists match uniquely.
Result: Circuits match uniquely.
Logging to file "comp.out" disabled
LVS Done.
(netgen) 6 % |
```

DVDD/DGND values are as shown below. It came out as given in the assignment.

```
microns: 1.000 x 1.000 ( 5.400, 9.000), ( 6.400, 10.000) 1.000
lambda: 100.00 x 100.00 ( 540.00, 900.00), ( 640.00, 1000.00) 10000.00
internal: 200 x 200 ( 1080, 1800 ), ( 1280, 2000 ) 40000
% |
```

The area occupied by the designed layout is as follows.

```
tkcon 2.3 Main
File Console Edit Interp Prefs History Help
Extracting and_nor_one_symbol into /home/ubuntu/Desktop/design/mag/and_nor_one_symbol.ext:
% ext2spice lvs
% ext2spice
ext2spice finished.
Unknown macro or short command: 'Control_XK_Pointer_Button4'
% drc why
No errors found.
Unknown macro or short command: 'Control_XK_Pointer_Button4'
select: Topmost cell in the window
Root cell box:
  width x height ( llx, lly ), ( urx, ury ) area (units^2)
microns: 15.650 x 8.930 (-2.400, 1.070), ( 13.250, 10.000) 139.754
lambda: 1565.00 x 893.00 (-240.00, 107.00), ( 1325.00, 1000.00) 1397545.00
internal: 3130 x 1786 ( -480, 214 ), ( 2650, 2000 ) 5590180
% |
```

4- Parasitic Extraction

After the layout operations, the steps in the TUTEL 5.pdf file placed in the class files were followed. The results (out) and the circuit are as follows. The results gave the same results as in the first simulation. The working logic of the circuit is still the same.

