Student Name: **Instructor: Mustafa Altun**

Student ID:

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EHB322E Digital Electronic Circuits
MIDTERM II

Duration: 120 Minutes
Grading: 1) 50%, 2) 50%
Exam is in closed-notes and closed-books format; calculators are allowed
For your answers please use the space provided in the exam sheet
GOOD LUCK!

1) Consider a Boolean function $f = x_1\,x_2\,x_3 + \overline{x_1}\,\overline{x_2} + \overline{x_1}\,\overline{x_3}$ to be implemented.
Suppose that all NMOS transistors are identical and all PMOS transistors are identical.
Equivalent resistor for an NMOS transistor: $\boldsymbol{R_N}$**= 12kΩ**
Equivalent resistor for a PMOS transistor: $\boldsymbol{R_P}$**= 24kΩ**
Suppose that each node in circuits has an internal capacitance of **0.5pF**.
Also an external load capacitor of **1pF** is connected to the outputs.

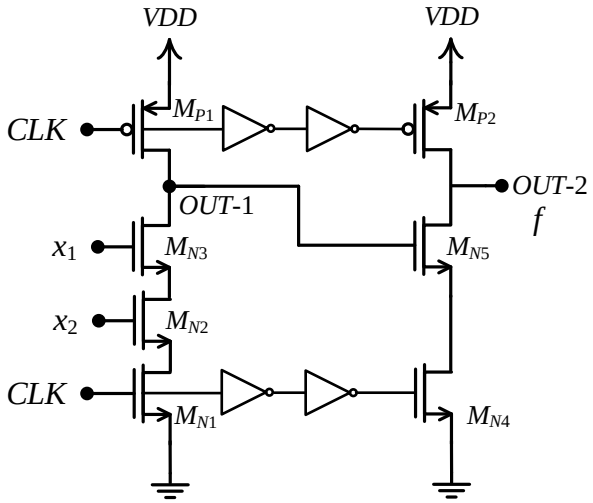
a) Implement $\boldsymbol{f}$ with "an NMOS and PMOS (CMOS) Pass Transistor Logic" using the ordering of $x_1 - x_2 - x_3$. Find the **minimum number** of transistors needed. Find the **worst case (largest) and best case (smallest)** $\boldsymbol{t_{PHL}}$ **and** $\boldsymbol{t_{PLH}}$ values (total of 4 values).

b) Implement $\boldsymbol{f}$ with "Dynamic (CMOS) Logic" using an NMOS pull-down network. Find the **minimum number** of transistors needed. Find the **worst case (largest) and best case (smallest)** $\boldsymbol{t_{PHL}}$ **and** $\boldsymbol{t_{PLH}}$ values (total of 4 values).

- ***Hint:*** *in calculating delay values, use Elmore delay model.*

2) Consider a dynamic domino logic circuit shown below.

- Suppose that each transistor has an internal gate capacitor C_G and drain capacitor C_D: **$C_G = c_{ox} W L$**; **$C_D = (c_{ox} W L)/2$**; c_{ox}=0.1 pF/um2.
- Equivalent resistor for an NMOS transistor: **$R_N = (12k\Omega) / (W/L)_N$**
  Equivalent resistor for a PMOS transistor: **$R_P = (24k\Omega) / (W/L)_P$**
- Suppose that all four CMOS inverters are identical with same **$W_{N\text{-}In}$** and **$W_{P\text{-}In}$** values.
- $W_{N1}=W_{N2}=W_{N3}=1u$, $W_{P1}=2u$, $W_{P\text{-}In}=2u$, $W_{N\text{-}In}=1u$, L=1u for all transistors, $V_{TN}=|V_{TP}|=1V$, $V_{DD}=5V$.



Cascaded Dynamic Circuits

a) Derive a Boolean expression of f in terms of x_1 and x_2 in evaluation phase.

b) Find the value of **W_{N5}** if $V_{OUT\text{-}1}$=4.5V as a result of charge sharing (problem).

c) Find the **worst case t_{PHL}** for OUT-1. Suppose that all input transitions happen in pre-charge phase and each circuit node has an initial voltage value of either 0V or 5V .

d) Find the values of **W_{P2}** and **W_{N4}** if the worst case t_{PHL} for OUT-1, calculated in **c)**, is same the clock delay (total delay of two cascaded inverters).