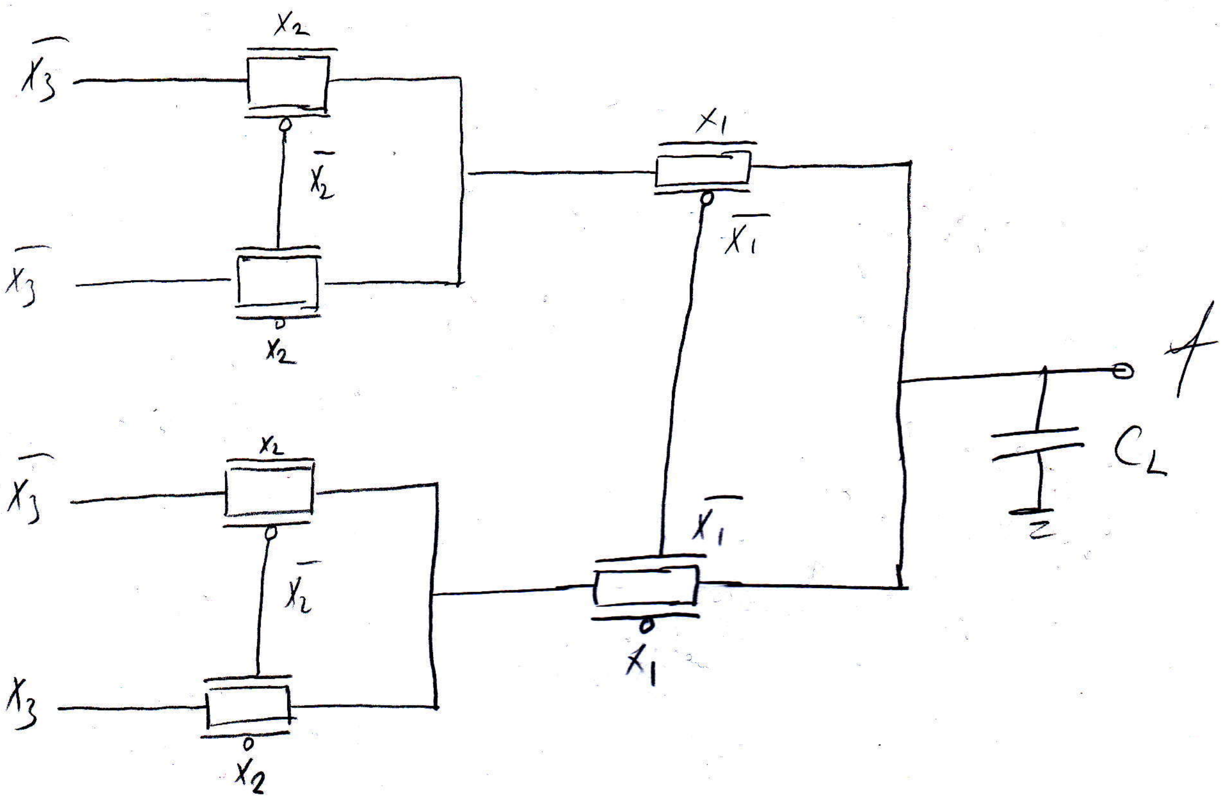
EHB 322E - Quiz 2

1) $f = x_1\overline{x_3} + \overline{x_1}\,\overline{x_2}\,x_3 + x_2\overline{x_3}$

$= x_1\overline{x_3}(x_2+\overline{x_2}) + \overline{x_1}\,\overline{x_2}\,x_3 + x_2\overline{x_3}(x_1+\overline{x_1})$ → missing variables added to complete shannon expression

$f = x_1(x_2(\overline{x_3}) + \overline{x_2}(\overline{x_3})) + \overline{x_1}(x_2(\overline{x_3}) + \overline{x_2}(x_3))$



worst case

2 pass transistors (4 total transistors) are used in worst case paths. In pass transistors, NMOS and PMOS are in parallel, therefore we can calculate equivalent resistance as $(R_p//R_n)$.

$t_{PLH}=t_{PHL}=0{,}69.2(R_n//R_p).(C_L) = 0{,}69.2(R_n//R_p).10.10^{-12} = 82{,}8.10^{-9}$

→ $(R_n//R_p) = 6.10^3 \Rightarrow \frac{1}{R_n}+\frac{1}{R_p} = \frac{1}{R_n//R_p} = \frac{1}{6.10^3} \Rightarrow \frac{1}{\frac{12.10^3}{(W/L)_n}} + \frac{1}{\frac{24.10^3}{(W/L)_p}}$

→ $2(W/L)_n + (W/L)_p = 4.$

$0 + 4 = 4$ highest possible sum

$2 \quad 0 = 2$ lowest possible sum

Considering minimum $(W/L) = 1$
$(W/L)_n = 1{,}5$
$(W/L)_p = 1$
$\Rightarrow \boxed{2{,}5}$

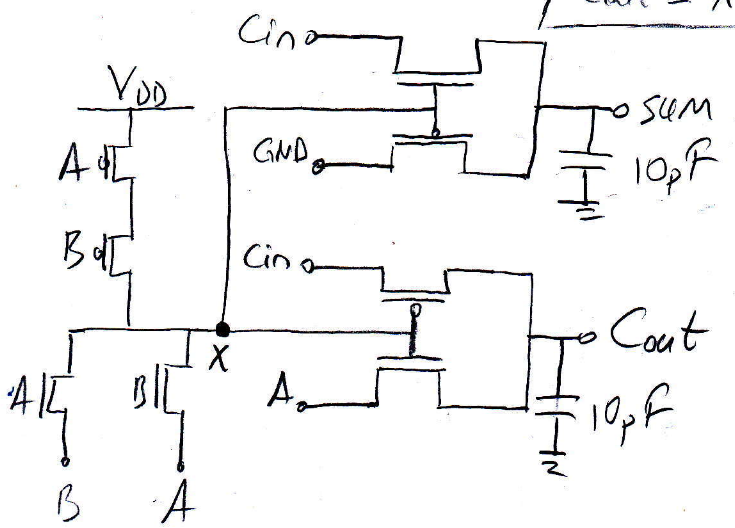
27)

A	B	X
0	0	1
0	1	0
1	0	0
1	1	1

X: Output of the first part on circuit.

$X = AB + \bar{A}\bar{B}$

$$\boxed{\begin{aligned} sum &= X.C_{in} + \bar{X}.0 = X.C_{in} \\ C_{out} &= \bar{X}.C_{in} + X.A \end{aligned}}$$



⇒ need to find worst-case t_{PLH} and t_{PHL} for 'sum' 'Cout' (total of 4 delay values).

$R_n = 12.10^3\ \Omega$, $R_p = 24.10^3\ \Omega$ since $(W/L)_N = (W/L)_p = 1$

for sum

low-to-high → only occurs when $C_{in} = 1$, $X: 0 \to 1$

$t_{PLH} = 0{,}69 . R_n . C_L = 0{,}69 . 12.10^3 . 10.10^{-12} = \boxed{82{,}8\ ns}$

high to-low → occurs when: $C_{in} = 0$, $X: 0 \to 1$

$C_{in} = 1$, $X: 1 \to 0$ → we use this case since $R_p > R_n$

$t_{PHL} = 0{,}69 . R_n . C_L = 0{,}69 . 24.10^3 . 10.10^{-12} = \boxed{165{,}6\ ns}$

for Cout

low-to-high → occurs when: $C_{in} = 1$, $A = 0$, $X: 1 \to 0$ → using PMOS $R_p > R_n$

$C_{in} = 0$, $A = 1$, $X = 0 \to 1$

$t_{PLH} = 0{,}69 . R_p . C_L = \boxed{165{,}6\ ns}$

high-to-low → occurs when: $C_{in} = 0$, $A = 1$, $X: 1 \to 0$ → using PMOS $R_p > R_n$

$C_{in} = 1$, $A = 0$, $X: 0 \to 1$

$t_{PHL} = 0{,}69 . R_p . C_L = \boxed{165{,}6\ ns}$