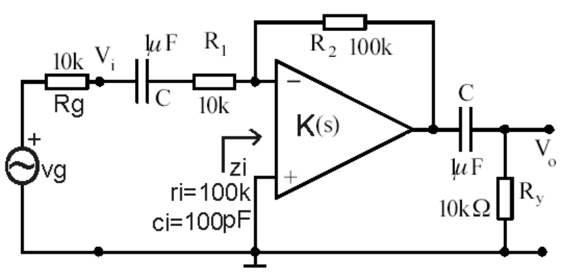
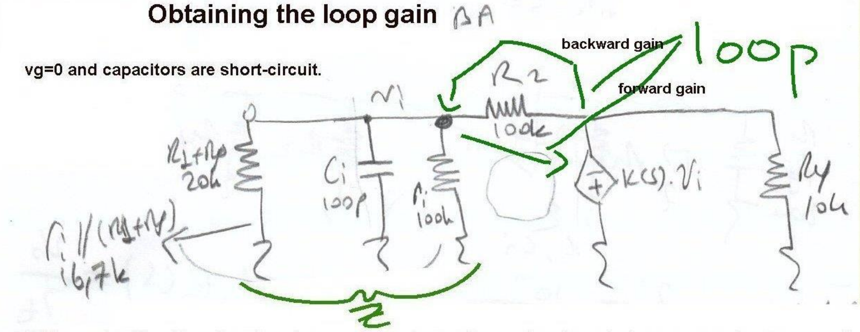
For the **amplifier** in the figure, for K(s)
$K_o=1000$, $\omega_2=10\omega_1$ and $\omega_1=28$Mrad/sn are given.
For the **amplifier**, ri=100k and ci=100pF'dır.
The output parasitic capacitance and the output resistance
Of the **amplifier** can be ignored.
Find the phase margin of the **circuit.**

$$K(s)=10^3\frac{\omega_1\omega_2}{(S+\omega_1)(S+\omega_2)}$$



Obtaining the loop gain βA

vg=0 and capacitors are short-circuit.



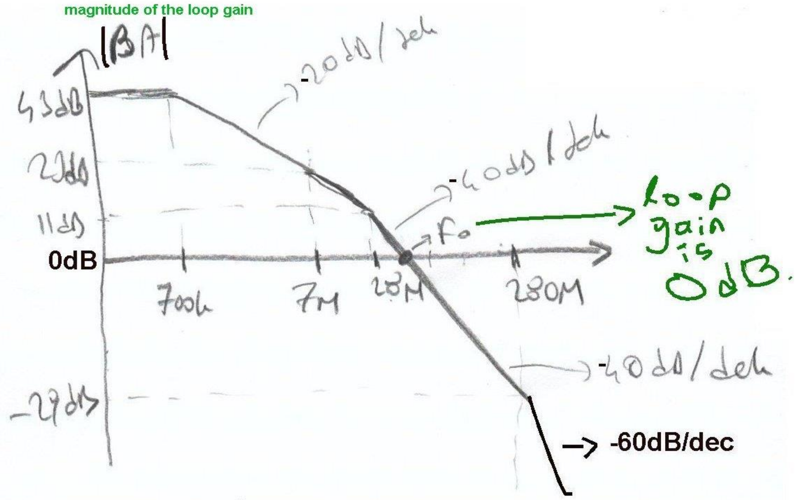
RY is not effective for the loop gain, since the output resistance can be ignored.

$$Z=(R_i+R_g)//r_i//\frac{1}{sC_i}=\frac{16{,}7k}{s\times16{,}7k\times100p+1}$$

$$\beta A=-\underbrace{\frac{Z}{R_2+Z}}_{\beta}\,\underbrace{K(s)}_{A}=\frac{100k}{s+700k}\cdot\frac{-1000\cdot28M\cdot280M}{(s+28M)(s+280M)}$$

$$\beta_oA_o\cong-143\rightarrow(\beta_oA_o)_{dB}\cong43\text{ dB}$$

magnitude of the loop gain



$$f_o\cong10^{11/40}\cdot28M\cong53MHz$$

$$\varphi|_{f_o}\cong\varphi_o-\text{Arctg}\left(\frac{f_o}{700k}\right)-\text{Arctg}\left(\frac{f_o}{28M}\right)-\text{Arctg}\left(\frac{f_o}{280M}\right)$$

Phase at fo — $\varphi_o = 180°$ — The loop phase at fo

$$\cong180-89-62-11=18°$$

The circuit is stable. Phase margin is 18°