Student Name: **Instructor: Mustafa Altun**

Student ID:

Date: 03/05/2021

EHB322E Digital Electronic Circuits
QUIZ II

Duration: 100 Minutes

Grading: 1) 50%, 2) 50%

For your answers please use the space provided in the exam sheet

GOOD LUCK!

1) Consider a Boolean function $f = g x_2 x_3 + \overline{x_1}\,\overline{x_2} + x_1\,\overline{x_3}$ where $g = x_4 + x_5$.
Suppose that all NMOS transistors are identical and all PMOS transistors are identical.
Equivalent resistor for an NMOS transistor: $\boldsymbol{R_N}$**= 12kΩ**
Equivalent resistor for a PMOS transistor: $\boldsymbol{R_P}$**= 24kΩ**
Suppose that the output circuit node has a capacitance value of **10pF**. Neglect other internal node capacitors.

Implement $\boldsymbol{f}$ with "NMOS Pass Transistor Logic – PTL - Network(s)" and "CMOS Inverters" with minimum number of transistors such that there is no threshold voltage drop at the output (output is VDD or GND all the time). For the PTL networks use the ordering of $x_1 - x_2 - x_3 - x_4 - x_5$. Also use only variables $x_1 - x_2 - x_3 - x_4 - x_5$ as inputs, not their negated forms. Find the **minimum number** of transistors needed. Find the **worst case (largest)** $\boldsymbol{t_{PHL}}$ **and** $\boldsymbol{t_{PLH}}$ values (total of 2 values).

2) Consider a Boolean function $f = gx_2\,x_3 + \overline{x_1}\,\overline{x_2} + x_1\,\overline{x_3}$ where $g = x_4 + x_5$. Implement f with "Dynamic Logic" using "Pull-Down NMOS Network(s)" using minimum number of transistors such that there is no charge sharing and cascading problems. Find the **minimum number** of transistors needed.