

A pattern detector which gives 1 at its 1-bit output when the last four values of its 1-bit input are 1011 will be designed. The detected streams will not overlap. JK type rising edge triggered flip-flops, AND (VE), OR (VEYA) and NOT (TÜMLEME) gates will be used for the implementation. ($Q = Jq' + K'q$)

- 1) Draw the Mealy type state diagram.
- 2) Draw the state transition table using binary encoding of the states (00, 01, 10, ...).