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EHB322E Digital Electronic Circuits
Quiz 2

Duration: 30 Minutes; *Grading: 1) 50%, 2) 50%,*
Quiz is in closed-notes and closed-books format; calculators are allowed
For your answers please use the space provided in the exam sheet
GOOD LUCK!

Consider a Boolean function $f = x_1\overline{x_2} + \overline{x_1}x_2 + x_3$ to be implemented.

- Suppose that all NMOS transistors are identical and all PMOS transistors are identical.
  Equivalent resistor for an NMOS transistor: R_N**= (12kΩ) / (W/L)$_N$**
  Equivalent resistor for a PMOS transistor: R_P**= (24kΩ) / (W/L)$_P$**
- Suppose that a load capacitor of **10pF** is connected to the outputs. Neglect all internal MOS capacitors.
- Worst case propagation delays $t_{PLH} = t_{PHL}$ **= 55,2ns (80** X **0,69 =55,2)** should be achieved.

1) Find the minimum values of **(W/L)$_P$** and **(W/L)$_N$** if f is implemented with "NMOS and PMOS (CMOS) Pass Transistor Logic".

2) Find the minimum values of **(W/L)$_P$** and **(W/L)$_N$** if f is implemented with "Dynamic (CMOS) Logic" using an NMOS pull-down network.