EHB 335E HW#5

Due: 13 December 2019 @17 o'clock – **No late homework will be accepted.**

HW assignments will be brought to the TA @ VLSI Laboratory (upstairs) – not to Prof. Yelten.

1) An amplifier has a dc gain of 3 x 10^4 and poles at 2 x 10^5 Hz, 3 × 10^5 Hz, and 2 x 10^6 Hz. Find the value of β, and the corresponding closed-loop gain, for which a phase margin of 45° is obtained.
2) An amplifier having a low-frequency gain of 10^4 and poles at 10^4 Hz and 10^5 Hz is operated in a closed negative-feedback loop with a frequency-independent *K*.
    a. For what value of *K* do the closed-loop poles become coincident? At what frequency?
    b. What is the low frequency, closed-loop gain corresponding to the situation in (a)? What is the value of the closed-loop gain at the frequency of the coincident poles?
3) Assuming $V_A = \infty$, determine the closed-loop gain and I/O impedances of the amplifier in Fig. 1a.

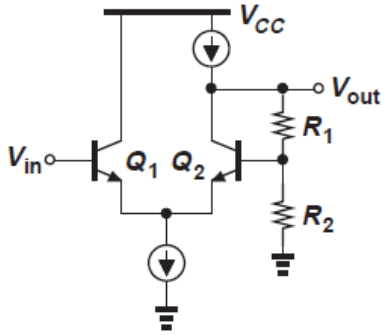

Fig. 1a Figure of Question 3

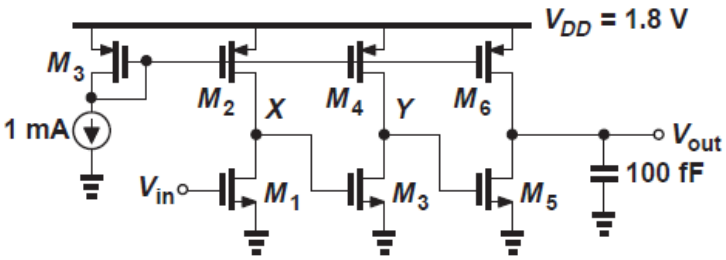

Fig. 1b Figure of Question 4

4) In the three-stage amplifier of Fig. 1b, all transistors except M_1 and M_5 have W/L = 20 µm / 0.18 µm. For M_1 use W/L = 42 µm / 0.18 µm and for M_5 use W/L = 10 µm / 0.18 µm. Employ the transistor models provided in the last homework for Spice simulations. Assume a DC input level of 0.55 V.
    a. Determine the phase margin.
    b. Place a capacitor between nodes X and Y so as to obtain a phase margin of 50 degrees. What is the unity-gain bandwidth under this condition?
    c. Repeat (b) if the compensation capacitor is tied between X and ground and compare the results.