02/03/15 - W5

EHB 322E Digital Electronic Circuits

Dynamic Power Consumption of an inverter

What is the source of power/energy? → power supply (battery, capacitor, inductor)

How is it consumed? → through heating flow of electrons (current)

$$\text{power} = \frac{\text{energy}}{\text{time}}$$

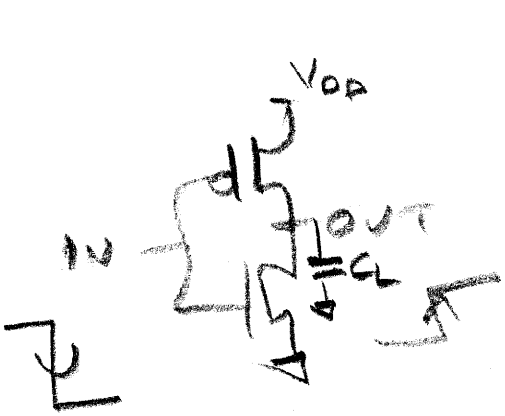
Total supplied energy ($E_{supp.}$)

Energy stored in the circuit ($E_{stor.}$) + Energy consumed by the circuit via heating (E_C)

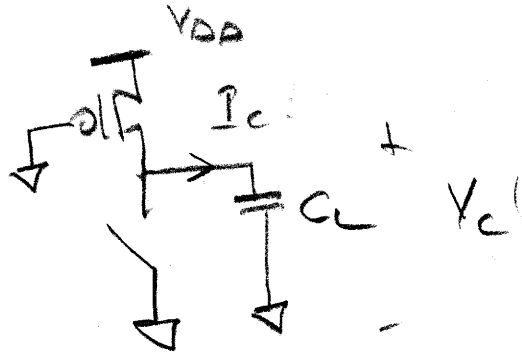
$$E_{supp} = E_{st} + E_C$$

- Energy supplied by power supplies
- Energy stored via capacitors and inductors
- Energy consumed by circuit elements.

① Energy consumed in charging



model ≡



$$E_{supp.} = \int_0^{\infty} I_1(t)\, V_{DD}\, dt \qquad \text{by } \underline{V_{DD}}$$

$$I_1(t) = C_L \frac{d V_c(t)}{dt}, \quad V_{out} = V_c$$

$$\Rightarrow E_{supp.} = C_L V_{DD} \int_0^{V_{DD}} dV_{out} = C_L V_{DD}^2 \Rightarrow \boxed{E_{supp.} = C_L V_{DD}^2}$$

$$E_{st} = \int_0^{\infty} I_c(t)\, V_c(t)\, dt \quad \text{(by capacitor)}, \quad I_c(t) = C_L \frac{d V_c(t)}{dt}, \quad V_{out} = V_c$$

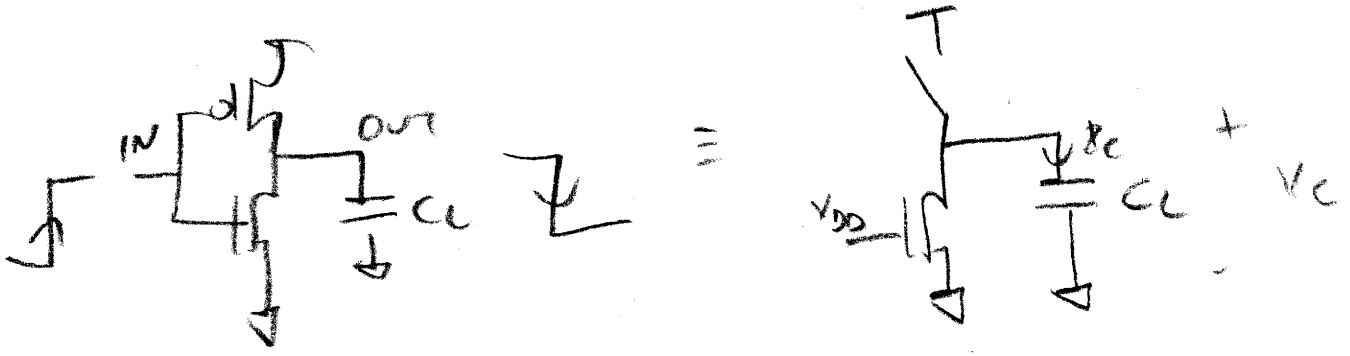
$$\Rightarrow E_{st} = C_L \int_0^{V_{DD}} V_{out}\, dV_{out}$$

$$\Rightarrow \boxed{E_{st} = C_L \frac{V_{DD}^2}{2}} \Rightarrow E_C = E_{p.s} - E_s$$

$$\boxed{E_C = \frac{C_L V_{DD}^2}{2}}$$

consumed energy through heating in the PMOS dren.

(2) Energy consumed in discharging



E_{supp} : Energy stored by capacitors during <u>charging</u>

$$E_{supp}: E_{st}\,(\text{charging}) = \frac{C_L V_{DD}^2}{2}$$

$$E_{st} = 0$$

$$\Rightarrow E_C = E_{supp} = \frac{C_L V_{DD}^2}{2}$$

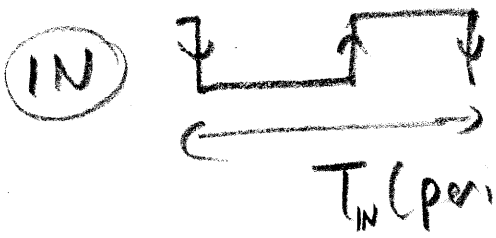
consumed energy through heating in the NMOS transi.

<u>Total energy</u> consumed in charging and discharging

$$E_{C\text{-total}} = \frac{C_L V_{DD}^2}{2} + \frac{C_L V_{DD}^2}{2} = C_L V_{DD}^2$$

Power is energy/time

Average power consumption in 1 period



$$P_{av} = \frac{E_{c\text{-}total}}{T_{IN}} = \frac{C_L V_{DD}^2}{T_{IN}} = C_L V_{DD}^2 f_{IN}$$

$$T_{IN} \geq T_{clk} \Rightarrow f_{IN} \leq f_{clk}$$

Ex Consider an Intel Core I5 microprocessor, 32nm with a clock frequency of 3 GHz. It has 1 billion transistors (0.5 NMOS, 0.5 PMOS) and $C_L = 1 fF$ for each transistor; $V_{DD} = 1V$.

Calculate the max power consumption?

for one NMOS PMOS pair $P_{av} \leq \frac{C_L V_{DD}^2}{f_{clk}}$

$\leq 10 \cdot 10^{-15} \cdot 3 \cdot 10^9$

$P_{av} \leq 30 \cdot 10^{-6} W$

for $0.5 \cdot 10^9$ pairs $P_{av} \leq 15 \mu W$ too high (should be $< 100 W$)

Why? not all trans. work in trans. are not work at the same time