Very Large Scale Integration II - VLSI II

Memory Structures

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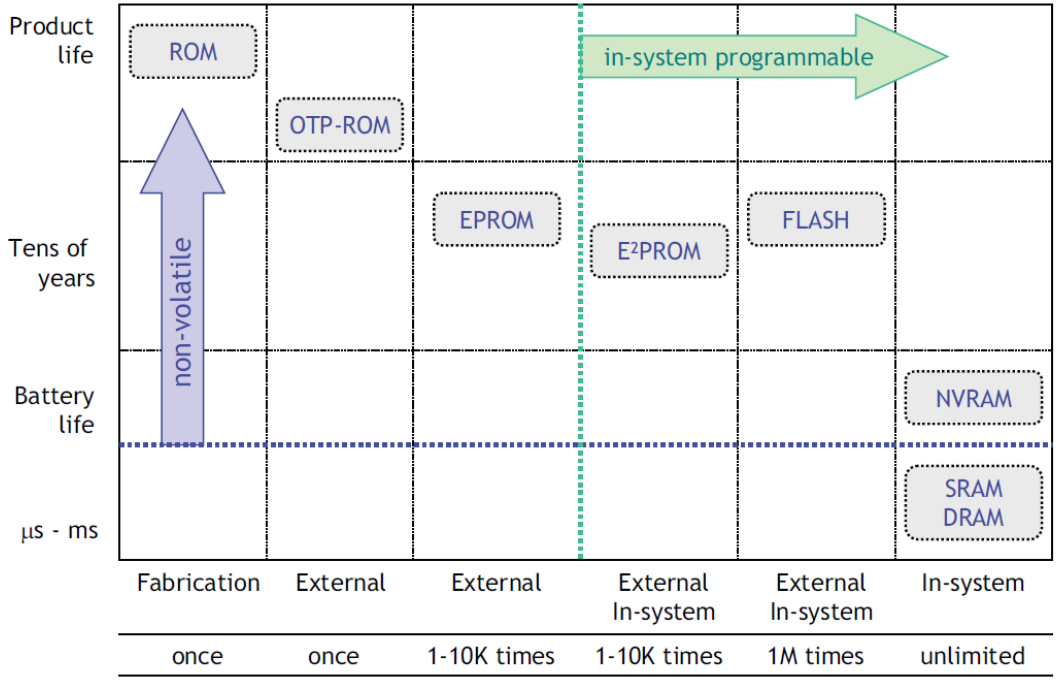
Memory Structures

- Traditional ROM/RAM distinctions:
  - ROM read only, data can be stored without power
  - RAM read and write, data can not be stored without power
- Traditional distinctions are blurred:
  - Advanced ROMs can be written e.g., EEPROM, FLASH
  - Advanced RAMs can hold bits without power e.g., NVRAM

Memory Structures

- There is trade-off between the **Write ability** and **storage permanence** (life)
- Write ability: Manner and speed a memory can be written.
- Storage permanence : Ability to hold stored bits once written

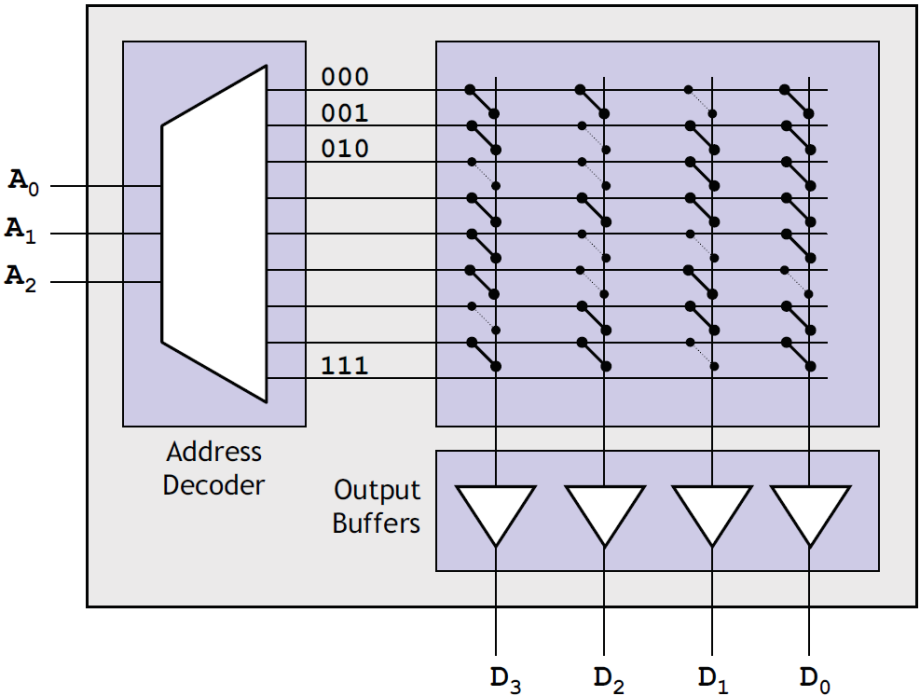


Memory Structures

- Ranges of write ability:
  - High end [RAM]
  - Middle range [EEPROM]
  - Lower range [EPROM, OTP ROM]
  - Low end [Mask-programmed ROM]
- Range of storage permanence
  - High end [mask-programmed ROM]
  - Middle range [NVRAM]
  - Lower range [SRAM]
  - Low end [DRAM]

Read-Only Memory (ROM)

- Read-Only Memories are nonvolatile
- Read-only memory is useful for storing software that is rarely changed.

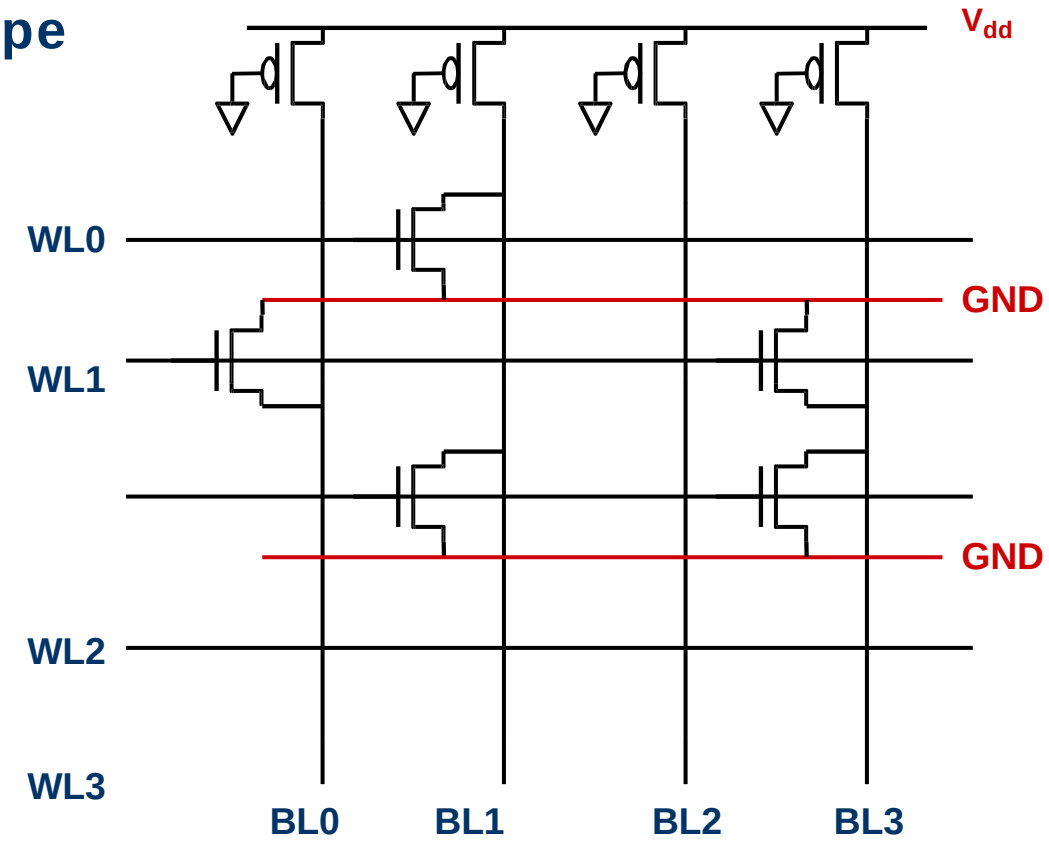


Mask-programmed ROM

- Mask-programmed ROM
  - Programmed only once by manufacturer at fabrication(mask) process.
  - Mask-programmed ROMs use one transistor per bit (Presence or absence determines 1 or 0).
  - Highest storage permanence (life of product).
  - Cheaper but design errors are costly.
  - Many microprocessors have Mask-ROM to store their microcode. Bootloaders and firmware can also be stored in Mask-ROMs.

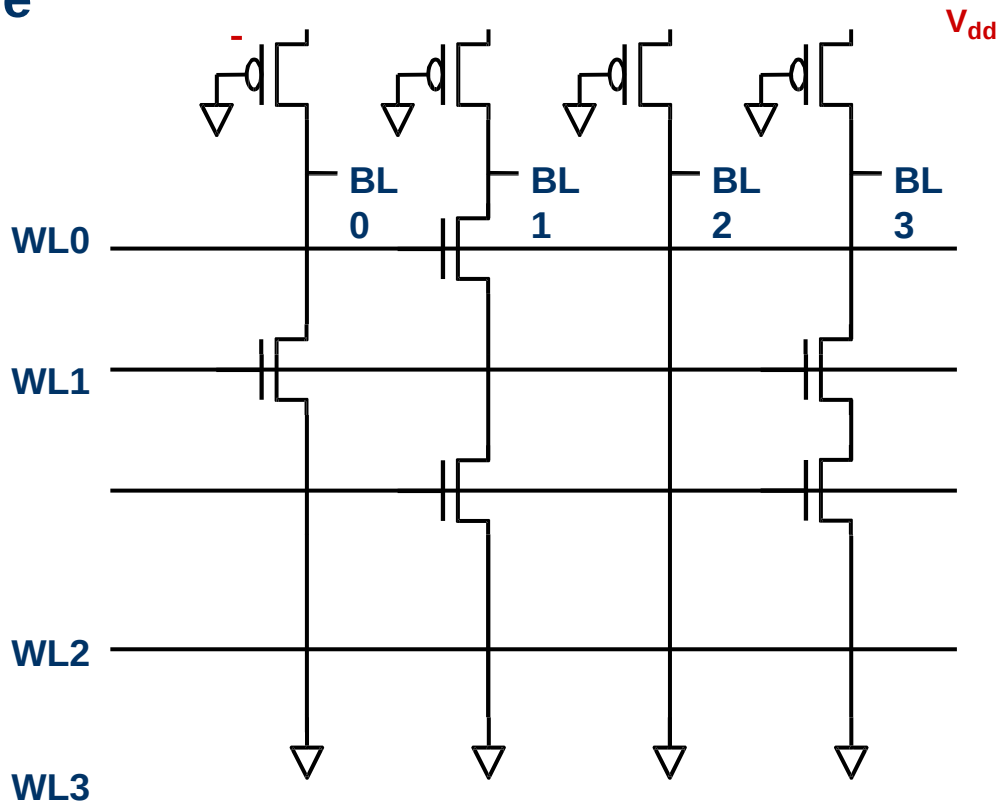
Mask-programmed ROM

4x4 NOR-type ROM



Mask-programmed ROM

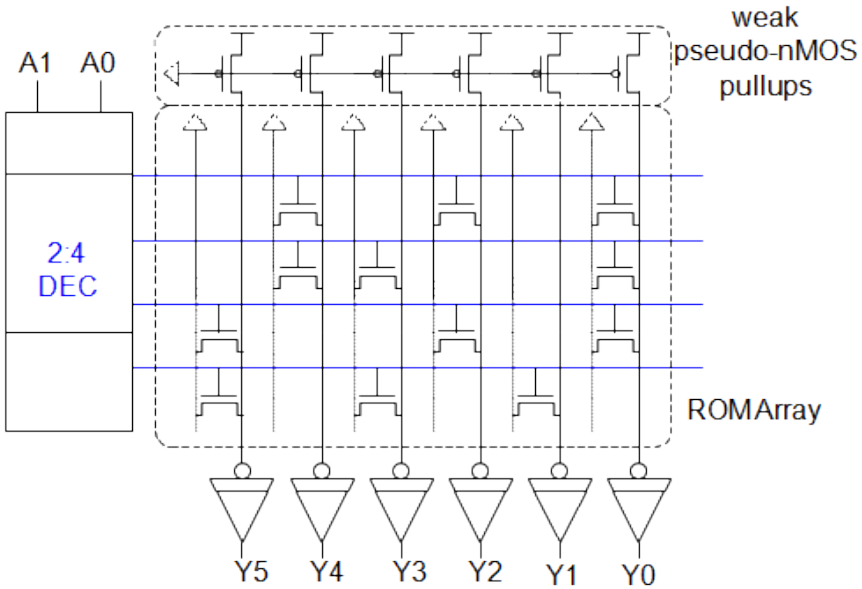
4x4 NAND-type ROM

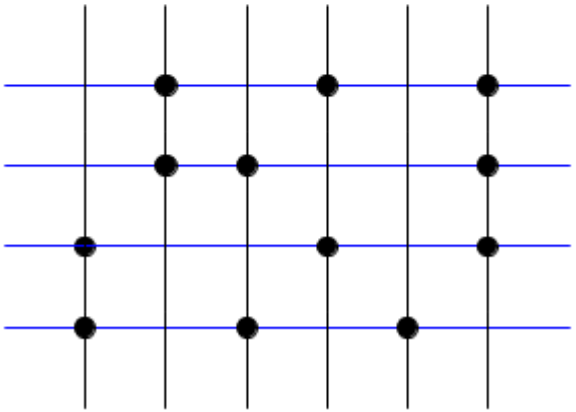


ROM Example

- 4-word x 6-bit ROM
- Represented with dot diagram
- Dots indicate 1's in ROM

```
Word 0: 010101
Word 1: 011001
Word 2: 100101
Word 3: 101010
```





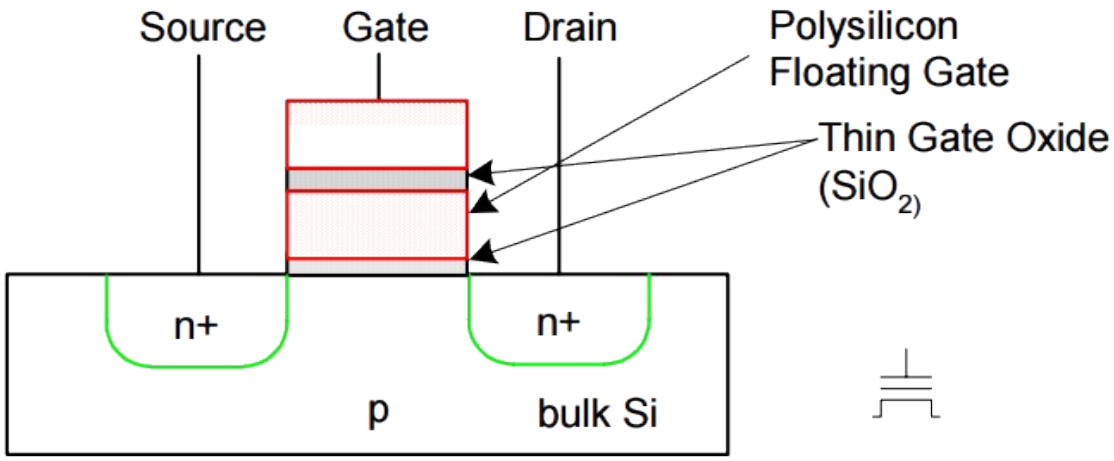
Looks like 6 4-input pseudo-nMOS NORs

Field Programmable ROMs

- Erasable programmable ROM (EPROM)
  - Programmable component is a MOS transistor, and transistor has “floating” gate.
  - Can be erased and reprogrammed thousands of times.
  - Reduced storage permanence, lasts about 10 years.
  - Not **in-system** programmable, historical.
- E2PROM
  - Programmed and erased electronically, **in-system** programmable.
  - Can be erased and programmed tens of thousands of times.
  - Storage permanence about 10 years.

FLASH

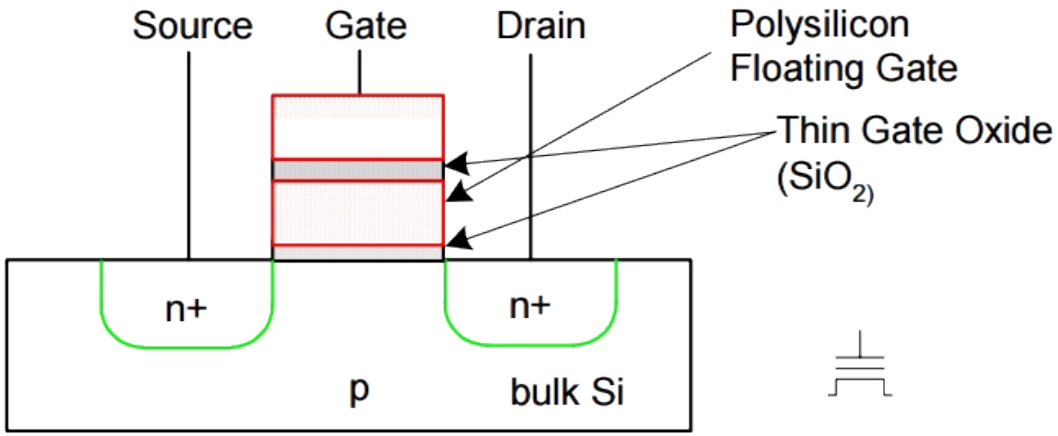
- Extension of EEPROM
  - Same floating gate principle.
  - Fast erase, better write ability.



FLASH

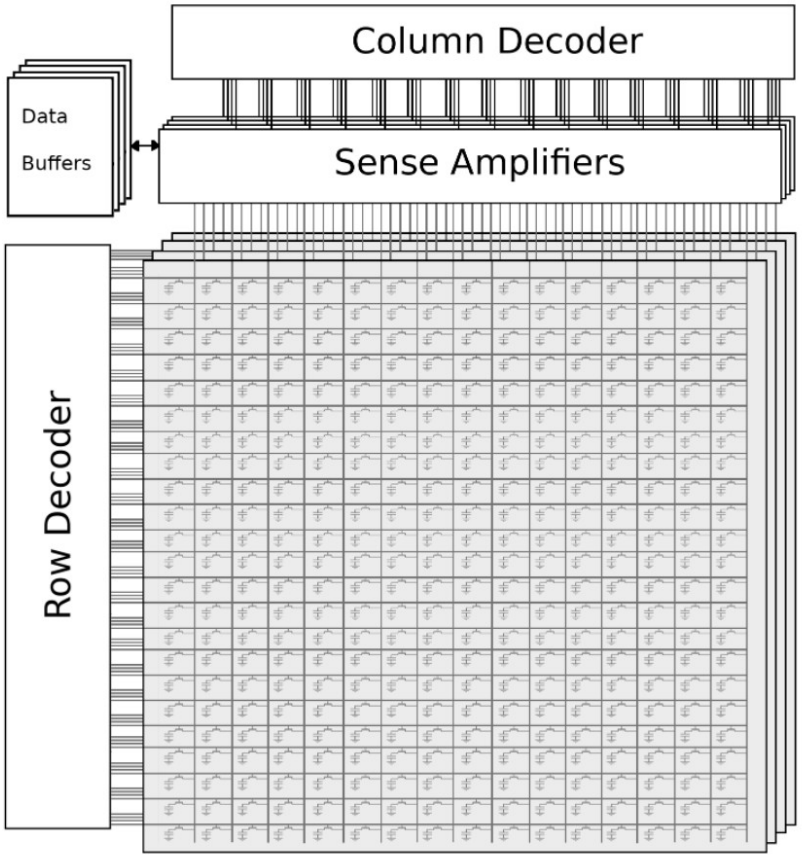
- The adding of a load of electrons at the isolated gate is "programming" of the transistor while electrons removal is "deleting".

- Has electron load V_T increases (open switch)
- Opposite case VT decreases (closed switch)



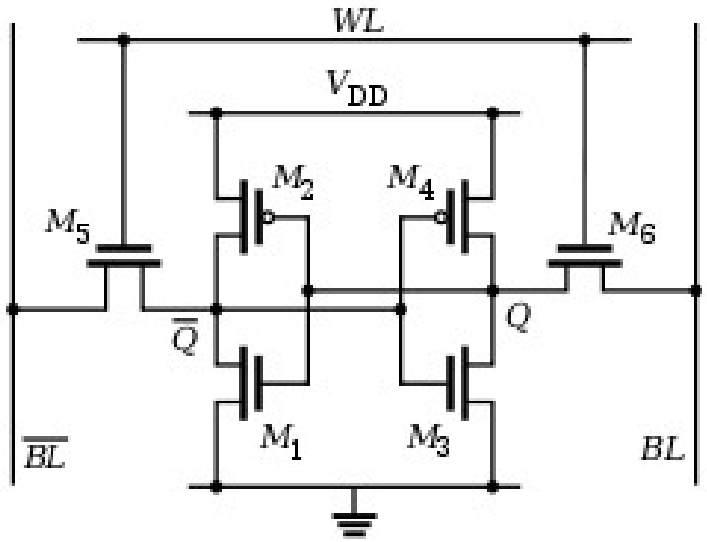
Random-Access Memory (RAM)

- Typically volatile memory
- Typically used to store working data and machine code.



Static-RAM (SRAM)

- Requires 6 transistors
- Holds data as long as power supplied



WL = 1 (Write or Read)

WL = 0 (Hold)

Use BL to write 1 or 0

BLbar = 1

BL = 1 when Read

(to speed up)

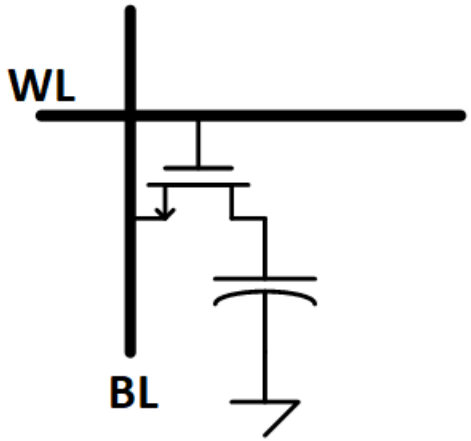
SRAM

- Not area efficient (at least 6 transistor for 1-bit data) ㅗㅏ
- Expensive due to area ineficiency ㅗㅏ
- No special semiconductor process (like in the FLASH) ㅅ
- Fast ㅅ
- Low power consumption ㅅ
- Easy to communicate ㅅ

- Used in
  - Embedded systems
  - CPU On-Chip Memory, Cache
  - FPGAs

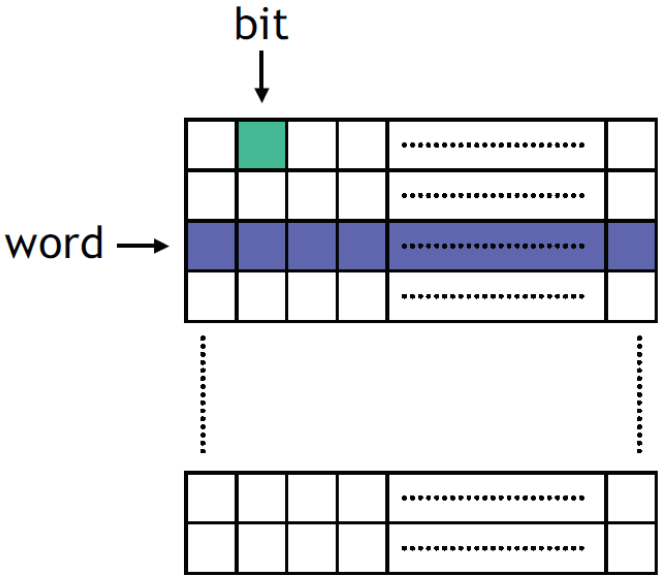
Dynamic RAM (DRAM)

- DRAM uses a MOS transistor and a capacitor to store a bit
- More compact than SRAM
- ”Refresh” required due to capacitor leak dynamic memory cells must be repeatedly read and restored.
- Slower than SRAM
- Cheaper



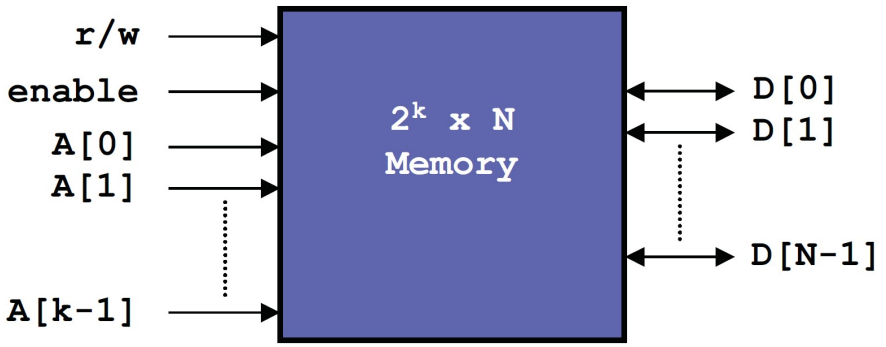
Basic Concepts

- Memories are organized in words (groups of bits 2^k)
- An M x N memory
  - $M=2^k$ words
  - N bits per word
- E.g.: 4096 x 8 memory:
  - 4,096 x 8 = 32,768 bits
  - $4,096 = 2^{12}$
  - 12 address input signals
  - 8 input/output data signals (buses)



Basic Concepts

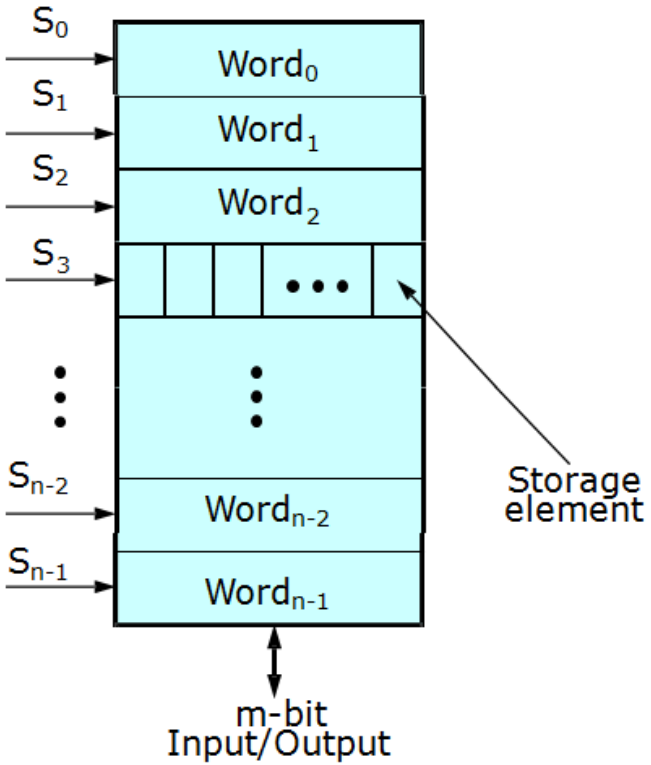
- Memory access signals
  - **r/w** Selects read or write
  - **enable** Read or write only when asserted
- Memory address/data
  - **A[0..k-1]** Address
  - **D[0..N-1]** Data



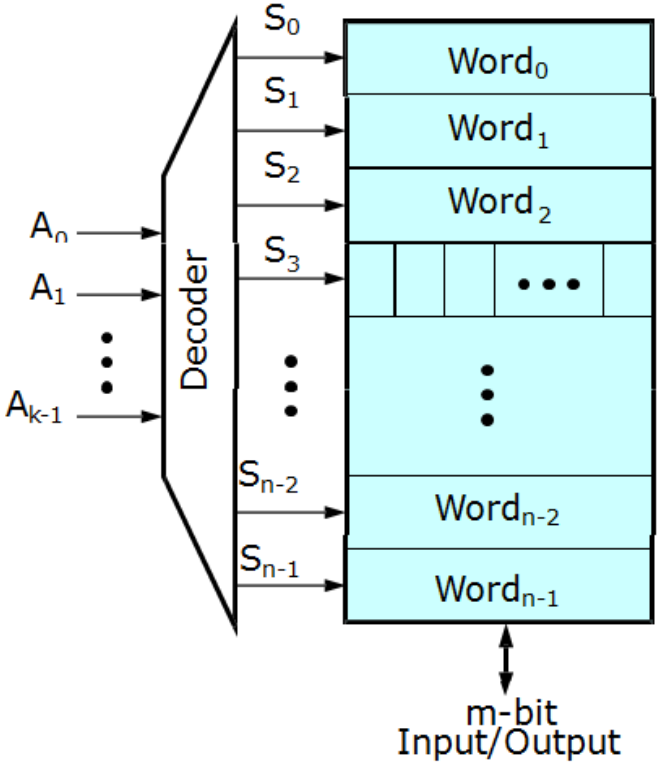
Memory Organization

- **Random Access:** Each memory location has a unique address, data can be accessed in any order.
- **Sequential Access:** Data can be accessed in a sequential order.
- **Content Addressable:** (Associative memory) compares the input with all the stored data

1-D Memory Architecture

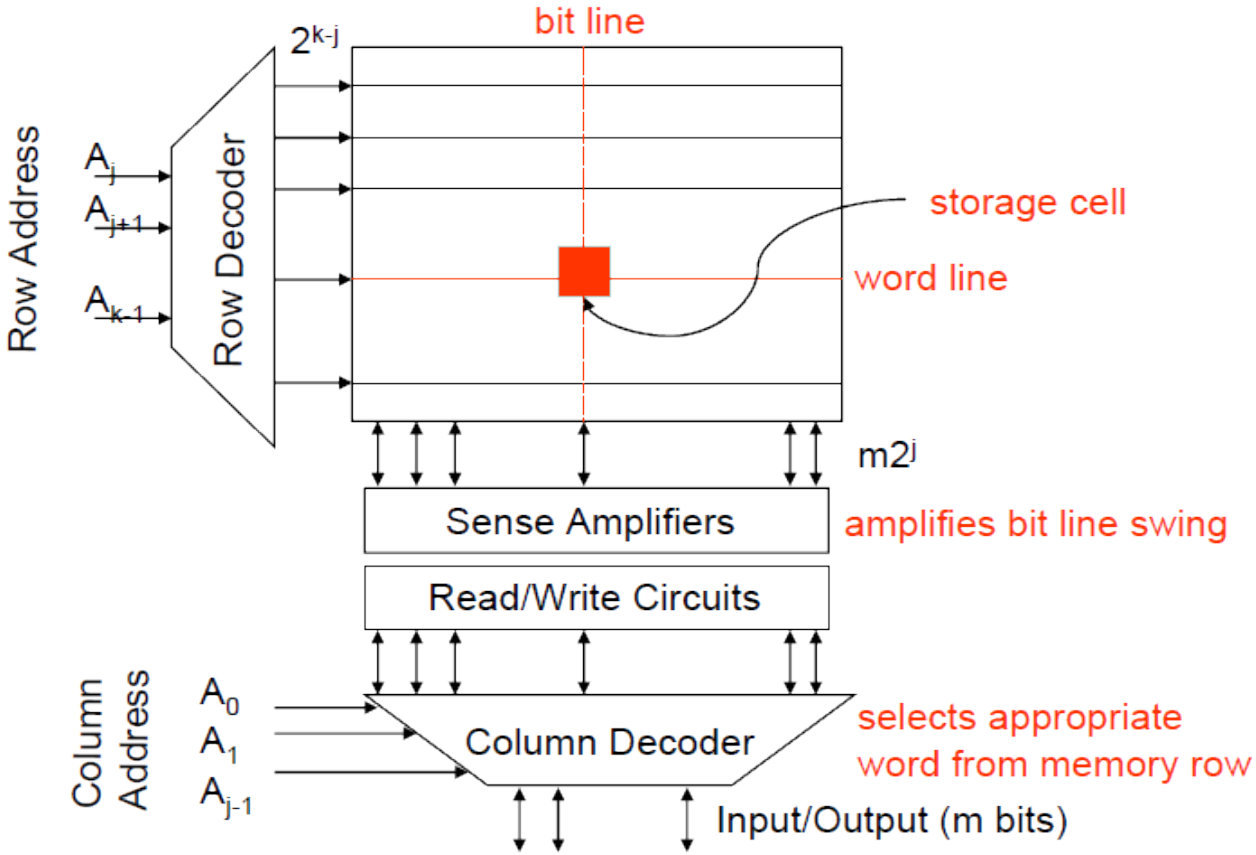


n select signals: S_0-S_{n-1}

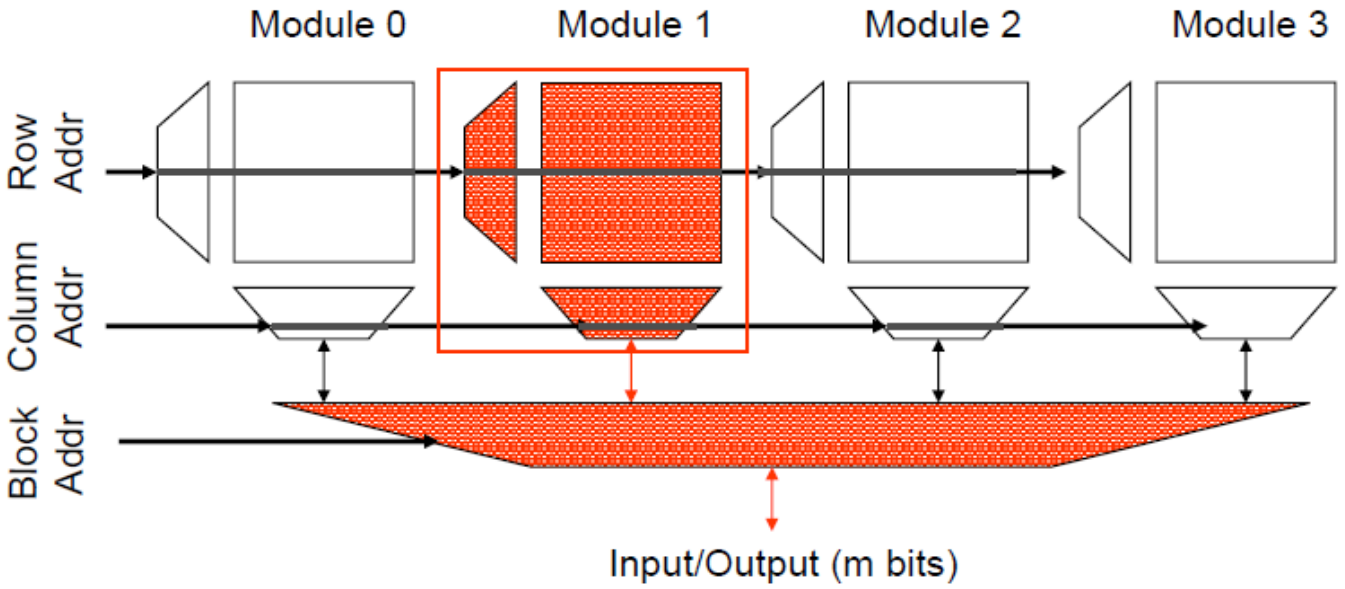


n select signals are reduced to k address signals: A_0-A_{k-1}

2-D Memory Architecture



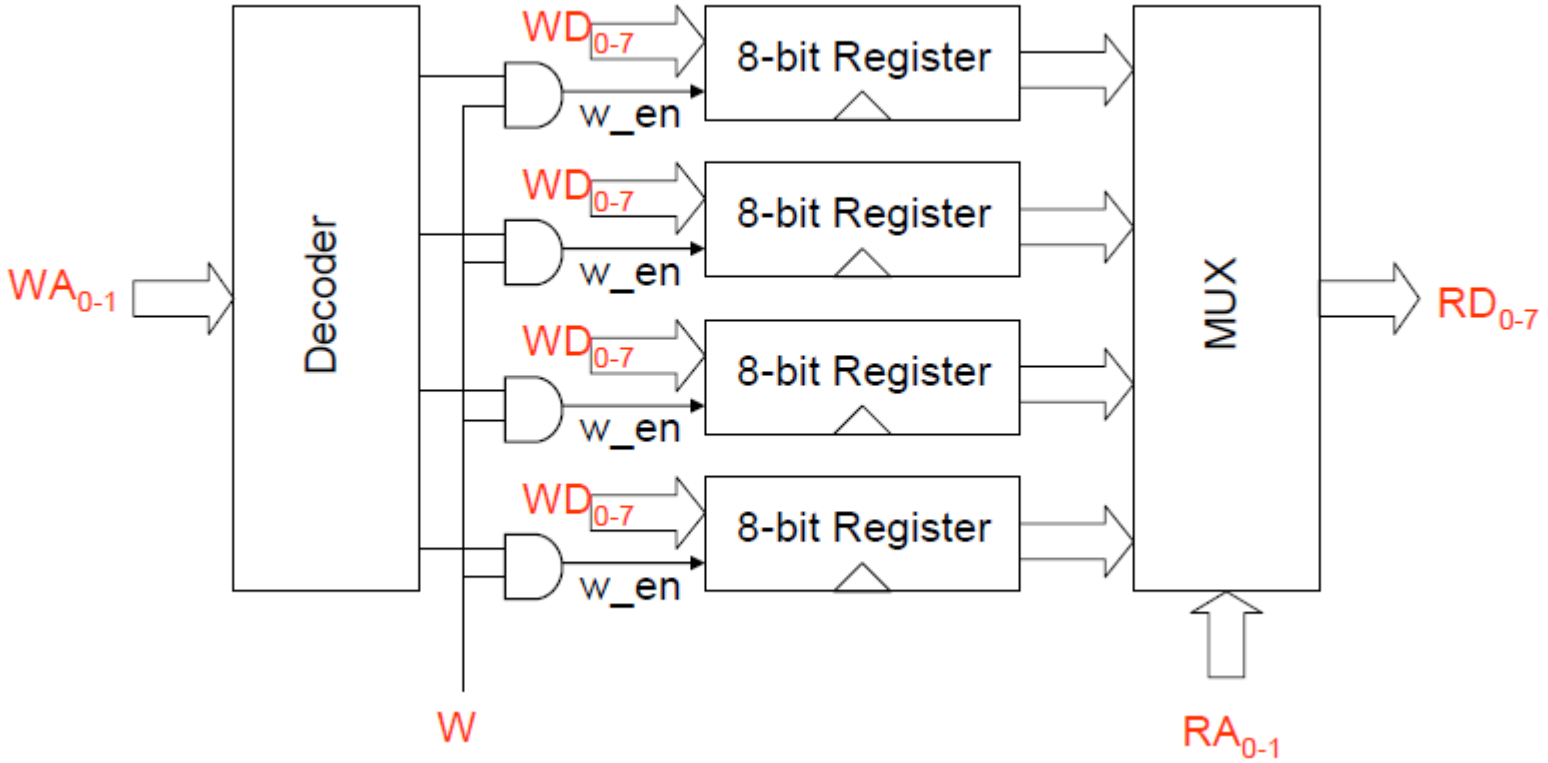
3-D Memory Architecture



Advantages:

1. Shorter word/bit lines **(reduced delay)**
2. Enable only one module at a time **(reduced power)**

FF Based Memories



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