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EHB205 Introduction to Logic Design
Homework 4

Part 1

1) Design a combinational circuit with three inputs, *x*, *y* and *z* , and three outputs, *A, B*, *C* . When the binary input is 0, 1, 2, or 3, the binary output is one greater than the input. When the binary input is 4, 5, 6, or 7, the binary output is two less than the input.
2) A majority circuit is a combinational circuit whose output is equal to 1 if the input variables have more 1's than 0's. The output is 0 otherwise. Design a 3-input majority circuit by finding the circuit's truth table, Boolean equation, and a logic diagram.
3) Design a BCD-to-decimal decoder using the unused combinations of the BCD code as don't-care conditions.
4) Construct a 5-to-32-line decoder with four 3-to-8-line decoders with enable and a 2-to-4-line decoder.
5) Using a decoder and external gates, design the combinational circuits defined by the following five Boolean functions:
   a) F1 = x'yz' + xz
   b) F2 = (y' + x)z
   c) F3 = xy'z' + x'y
   d) F4 = y'z' + x'y + yz'
   e) F5 = x'y'z' + xy

Part 2

1) Create a new project as explained in your first homework.

2) Design a circuit, COMP_1_bit, for comparing two 1-bit positive integers, a and b. The outputs are x, y, z as defined below:
   - a>b ⇒ x=1, y=0, z=0
   - a=b ⇒ x=0, y=1, z=0
   - a<b ⇒ x=0, y=0, z=1

   a) Write a VHDL code for COMP_1_bit. Save this file by giving name as "COMP_1_bit.vhd"
   b) Add your "COMP_1_bit.vhd" by "Add Sources", "Add or create design sources" to your project.
   c) Produce the RTL schematic of your design.
   d) Write a test bench file with name "COMP_1_bit_tb.vhd" to test your design.
   e) Add your "COMP_1_bit_tb.vhd" by "Add Sources", "Add or create simulation sources" to your project.
   f) Simulate your design.

3) Design a circuit, POZ_COMPARE, for comparing two 4-bit positive integers, A and B. The block diagram for comparing 4-bit numbers is shown in Fig. 1. The outputs are X, Y, Z as defined below:
   - A>B, then X=1, Y=0, Z=0
   - A=B, then X=0, Y=1, Z=0
   - A<B, then X=0, Y=0, Z=1

Figure 1 is the block diagram of the circuit which is used to calculate the following equations.

$$X = x_3 + y_3x_2 + y_3y_2x_1 + y_3y_2y_1x_0$$
$$Y = y_3y_2y_1y_0$$
$$Z = z_3 + y_3z_2 + y_3y_2z_1 + y_3y_2y_1z_0$$

   a) Write a VHDL code for CONNECT. Save this file by giving name as "CONNECT.vhd"
   b) Add your "CONNECT.vhd" by "Add Sources", "Add or create design sources" to your project.

c) Produce the RTL schematic of your design.
d) Write a VHDL code for a CON_COMP_1_bit by using COMP_1_bit and CONNECT as building blocks. Save this file by giving name as "CON_COMP_1_bit.vhd".
e) Add your "COMP_1_bit.vhd" by "Add Sources", "Add or create design sources" to your project.
f) Write a VHDL code for POZ_COMPARE by using COMP_1_bit and CON_COMP_1_bit as building blocks. Save this file by giving name as "POZ_COMPARE.vhd"
g) Add your "POZ_COMPARE.vhd" by "Add Sources", "Add or create design sources" to your project.
h) Produce the RTL schematic of your design.
i) Write a test bench file with name "POZ_COMPARE_tb.vhd" to test your design.
j) Add your "POZ_COMPARE_tb.vhd" by "Add Sources", "Add or create simulation sources" to your project.
k) Simulate your design.

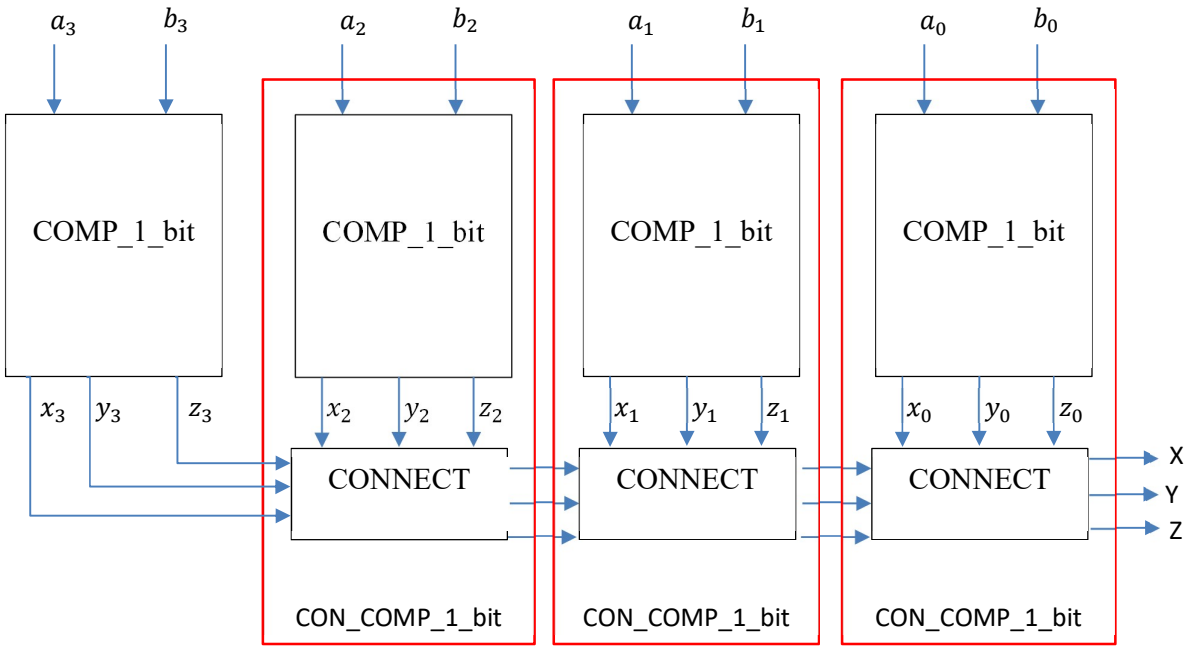

Figure 1

References

1) Frank Vahid, **Digital design, with RTL design, VHDL, and Verilog,** Hoboken, NJ : John Wiley, 2010.
2) Perry, Douglas L, **VHDL,** New York : McGraw-Hill, c1991
3) Botros, Nazeih, HDL with digital design : VHDL and Verilog, Dulles, Virginia : Mercury Learning and Information, [2015]
4) Vahid, Frank, VHDL for digital design, Hoboken, N.J. : Wiley, c2007
5) Short, Kenneth L, VHDL for engineers, Upper Saddle River, NJ : Pearson Prentice Hall, c2009
6) Coelho, David R., The VHDL Handbook, Boston, MA : Springer US, 1989
7) Lipsett, Roger., VHDL: Hardware Description and Design, Boston, MA : Springer US, 1989