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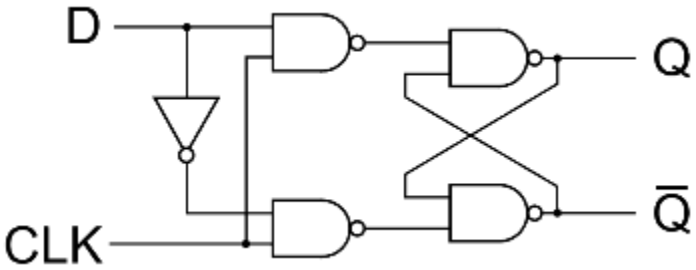
EHB322E Digital Electronic Circuits
QUIZ III

Duration: 100 Minutes
Grading: 1) 50%, 2) 50%
For your answers please use the space provided in the exam sheet
GOOD LUCK!

1) Consider a CMOS D-flip-flop shown below.



A D-Flip-Flop

Use the following parameter values.
Equivalent resistor for an NMOS transistor: $\boldsymbol{R_N}$**= 1kΩ**
Equivalent resistor for a PMOS transistor: $\boldsymbol{R_P}$**= 1,5kΩ**
Suppose that each node in the flip-flop has an internal capacitance of **1pF**.

When CLK=1 which condition (initial value of Q and change in D) gives the **worst case high-to-low propagation delay**. Find this delay value.

2) Implement $f = x_1\, x_2\, x_3 + \overline{x_1}\ \overline{x_2}\ \overline{x_3} + x_1\ \overline{x_3}$ with a pseudo NMOS NOR based PLA circuit. **Sketch the circuit**. For pseudo NMOS, use PMOS as a load.