DIGITAL SYSTEM DESIGN APPLICATION – EHB 436E

Experiment III

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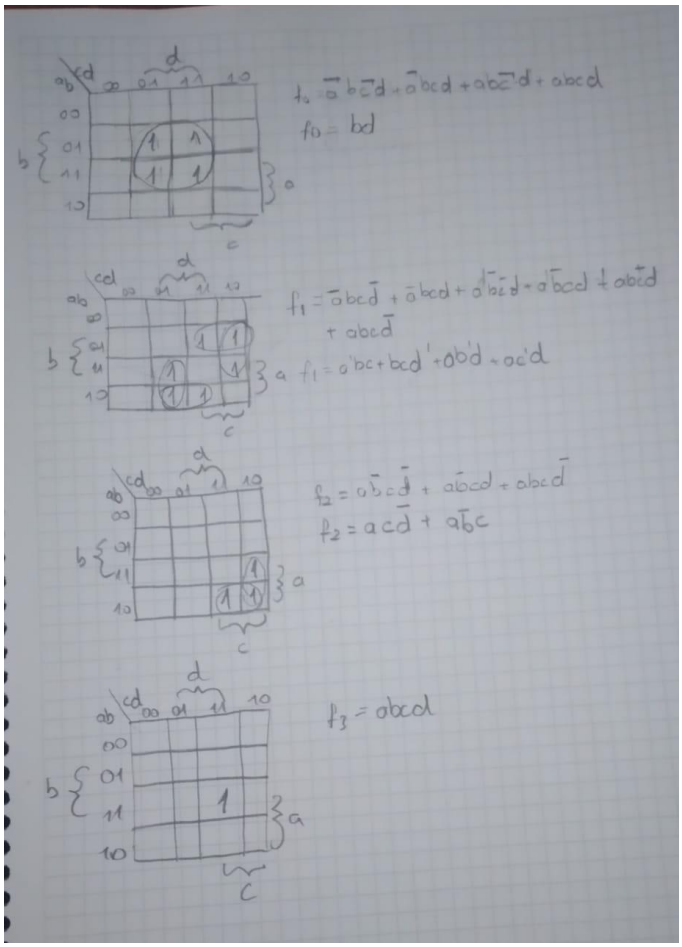
1. REALIZATION WITH SSI LIBRARY

- We have a truth table as indicated in the image below

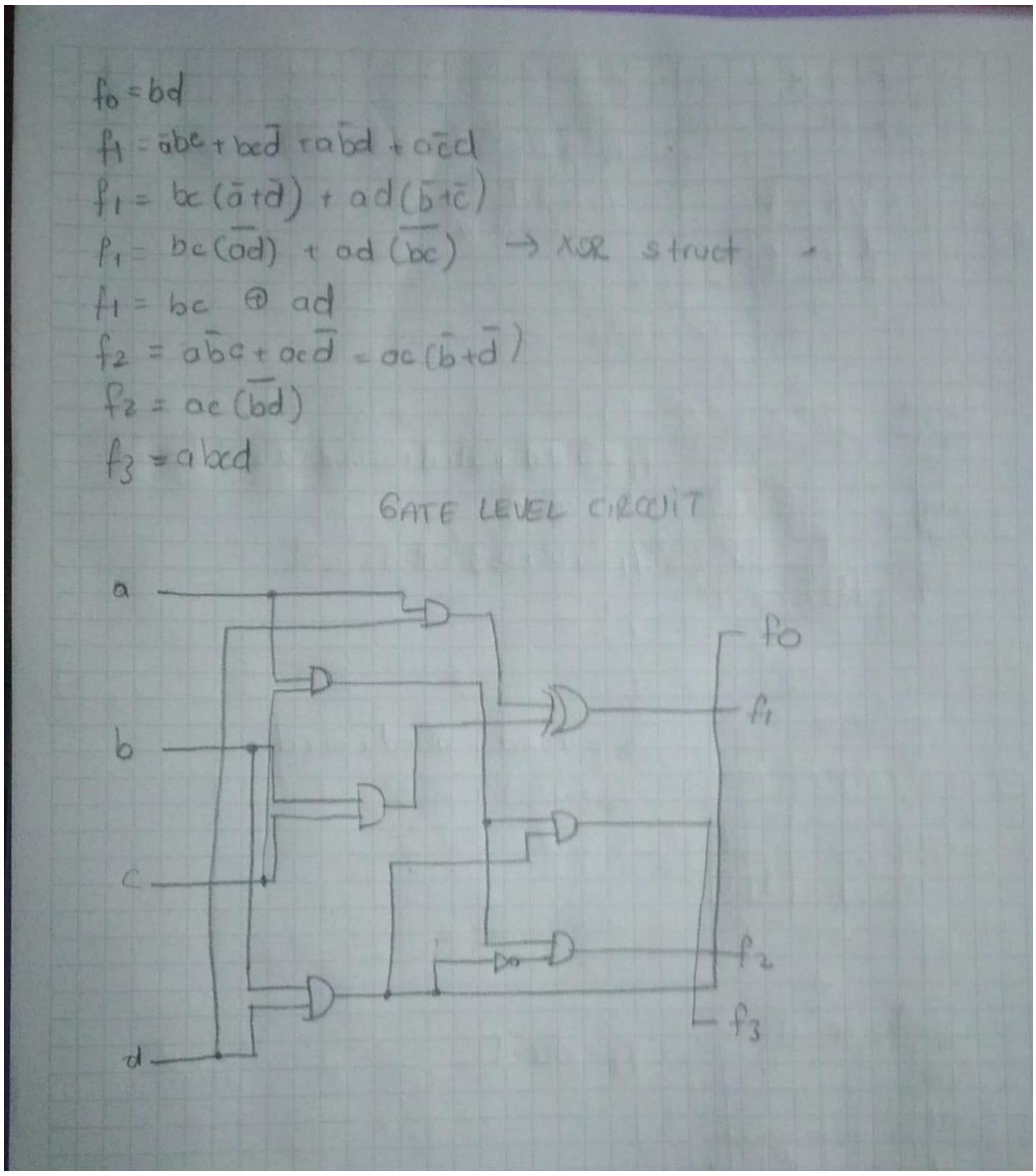
a	b	c	d	f_3	f_2	f_1	f_0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0
0	0	1	0	0	0	0	0
0	0	1	1	0	0	0	0
0	1	0	0	0	0	0	0
0	1	0	1	0	0	0	1
0	1	1	0	0	0	1	0
0	1	1	1	0	0	1	1
1	0	0	0	0	0	0	0
1	0	0	1	0	0	1	0
1	0	1	0	0	1	0	0
1	0	1	1	0	1	1	0
1	1	0	0	0	0	0	0
1	1	0	1	0	0	1	1
1	1	1	0	0	1	1	0
1	1	1	1	1	0	0	1

- We can write this function in its simplest form with the karnaugh map method we learned in logic circuits.

Reduction with Karnough MAP



Boolean expressions of the function and Gate Level Circuit



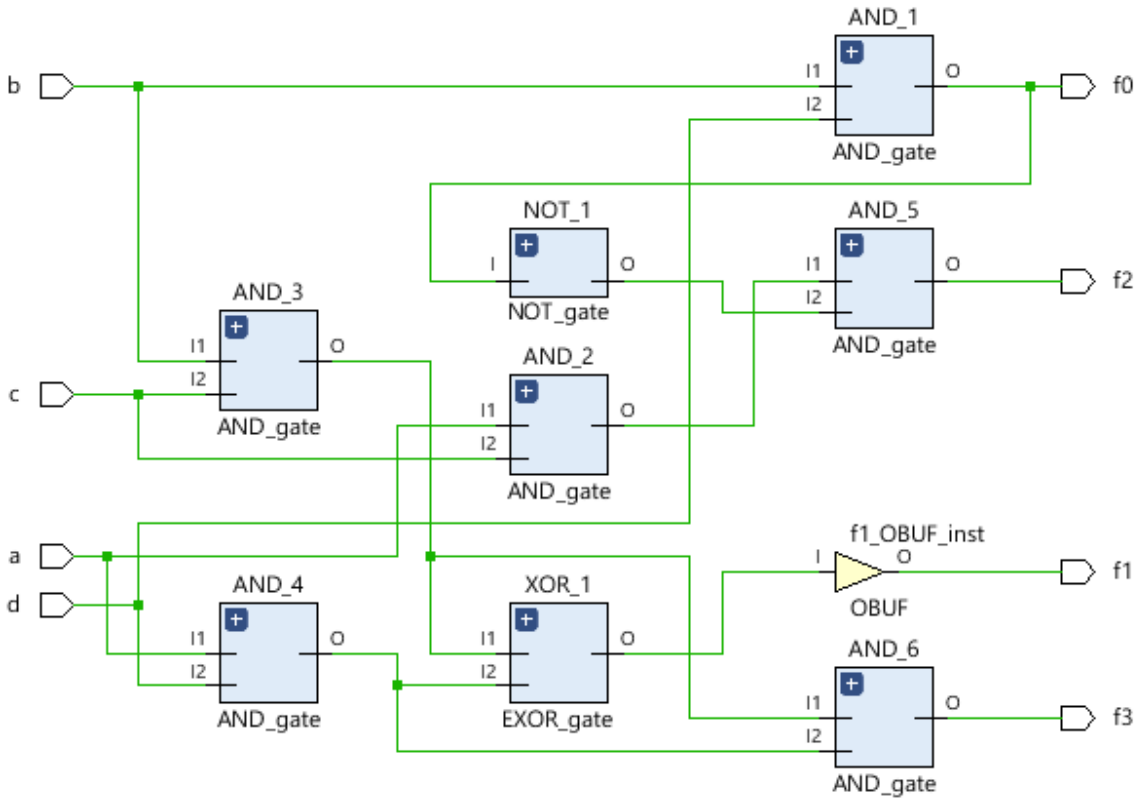
BEHAVIORAL SIMULATION

- TCL Console output is given below.

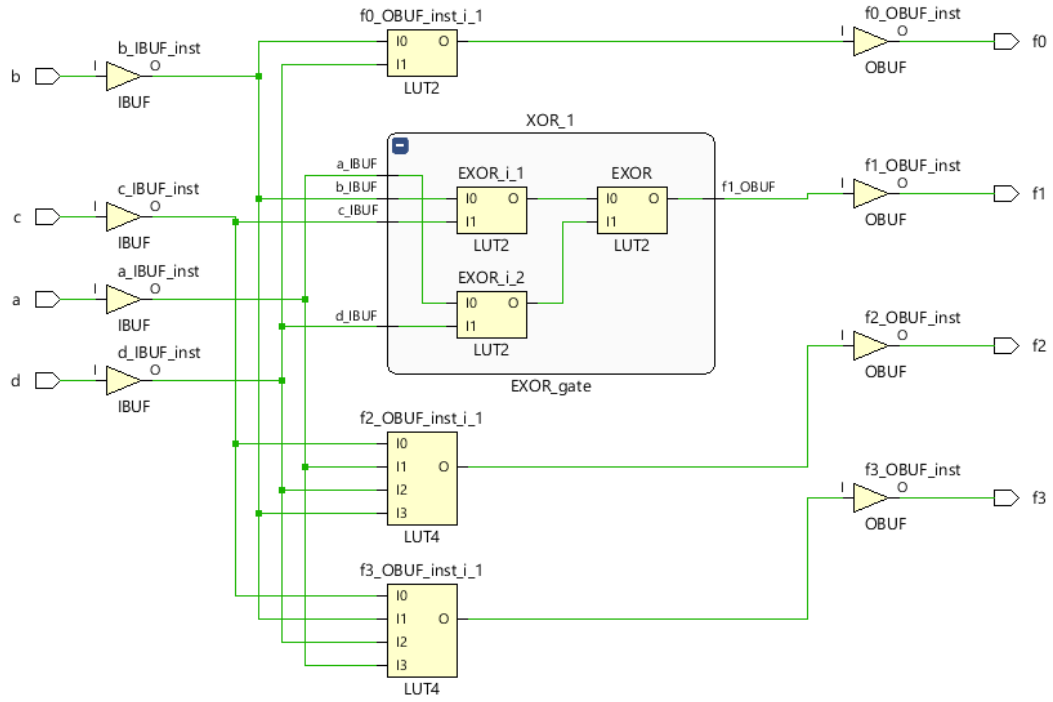
```
# run 1000ns
{a,b,c,d}=0000 => {f3,f2,f1,f0} = 0000 -- TRUE
{a,b,c,d}=0001 => {f3,f2,f1,f0} = 0000 -- TRUE
{a,b,c,d}=0010 => {f3,f2,f1,f0} = 0000 -- TRUE
{a,b,c,d}=0011 => {f3,f2,f1,f0} = 0000 -- TRUE
{a,b,c,d}=0100 => {f3,f2,f1,f0} = 0000 -- TRUE
{a,b,c,d}=0101 => {f3,f2,f1,f0} = 0001 -- TRUE
{a,b,c,d}=0110 => {f3,f2,f1,f0} = 0010 -- TRUE
{a,b,c,d}=0111 => {f3,f2,f1,f0} = 0011 -- TRUE
{a,b,c,d}=1000 => {f3,f2,f1,f0} = 0000 -- TRUE
{a,b,c,d}=1001 => {f3,f2,f1,f0} = 0010 -- TRUE
{a,b,c,d}=1010 => {f3,f2,f1,f0} = 0100 -- TRUE
{a,b,c,d}=1011 => {f3,f2,f1,f0} = 0110 -- TRUE
{a,b,c,d}=1100 => {f3,f2,f1,f0} = 0000 -- TRUE
{a,b,c,d}=1101 => {f3,f2,f1,f0} = 0011 -- TRUE
{a,b,c,d}=1110 => {f3,f2,f1,f0} = 0110 -- TRUE
{a,b,c,d}=1111 => {f3,f2,f1,f0} = 1001 -- TRUE
$finish called at time : 800 ns : File "C:/Users/yigit/Desktop/Okul/2022guz/Saysal sistem tasarm uygulamalar/sstu_odevler/Experiment3/sstu_odev3/sstu_odev3.srcs/sim_1/ne
INFO: [USF-XSim-96] XSim completed. Design snapshot 'experiment3_tb_behav' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
```

Design with NO Constraints

- RTL Schematic



- Technology Schematic



- Path Delays

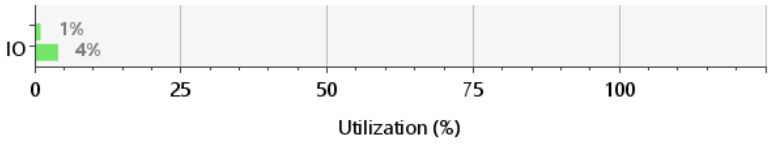
Combinational Delays

From Port	To Port	Max Delay	Max Process Corner	Min Delay	Min Process Corner
a	f1	7.643	SLOW	2.547	FAST
d	f1	7.438	SLOW	2.471	FAST
b	f1	7.395	SLOW	2.468	FAST
d	f2	7.241	SLOW	2.393	FAST
c	f1	7.173	SLOW	2.401	FAST
c	f2	7.030	SLOW	2.324	FAST
d	f3	7.008	SLOW	2.339	FAST
b	f2	6.906	SLOW	2.290	FAST
c	f3	6.799	SLOW	2.268	FAST
b	f0	6.781	SLOW	2.257	FAST
a	f2	6.675	SLOW	2.225	FAST
b	f3	6.674	SLOW	2.238	FAST
d	f0	6.537	SLOW	2.162	FAST
a	f3	6.475	SLOW	2.167	FAST

- Utilization Summary

Summary

Resource	Utilization	Available	Utilization %
LUT	5	32600	0.02
IO	8	210	3.81



Design with Time Constraints

- Path Delays
  - As seen in the photo above, I saw delays close to and above 7ns, so I set the time constraints maximum delay to 7ns. The results are as follows.

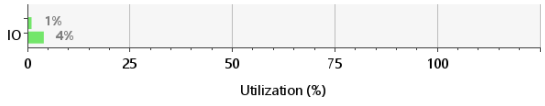
Combinational Delays

From Port	To Port	Max Delay	Max Process Corner
b	f1	6.907	SLOW
a	f1	6.848	SLOW
c	f1	6.787	SLOW
d	f1	6.688	SLOW
a	f3	6.667	SLOW
b	f3	6.613	SLOW
b	f2	6.606	SLOW
b	f0	6.552	SLOW
a	f2	6.522	SLOW
c	f3	6.311	SLOW
d	f2	6.297	SLOW
d	f0	6.269	SLOW
d	f3	6.203	SLOW
c	f2	6.190	SLOW

- Utilization Summary
  - If we look at the previous utilization summary, this result is 1 LUT more.

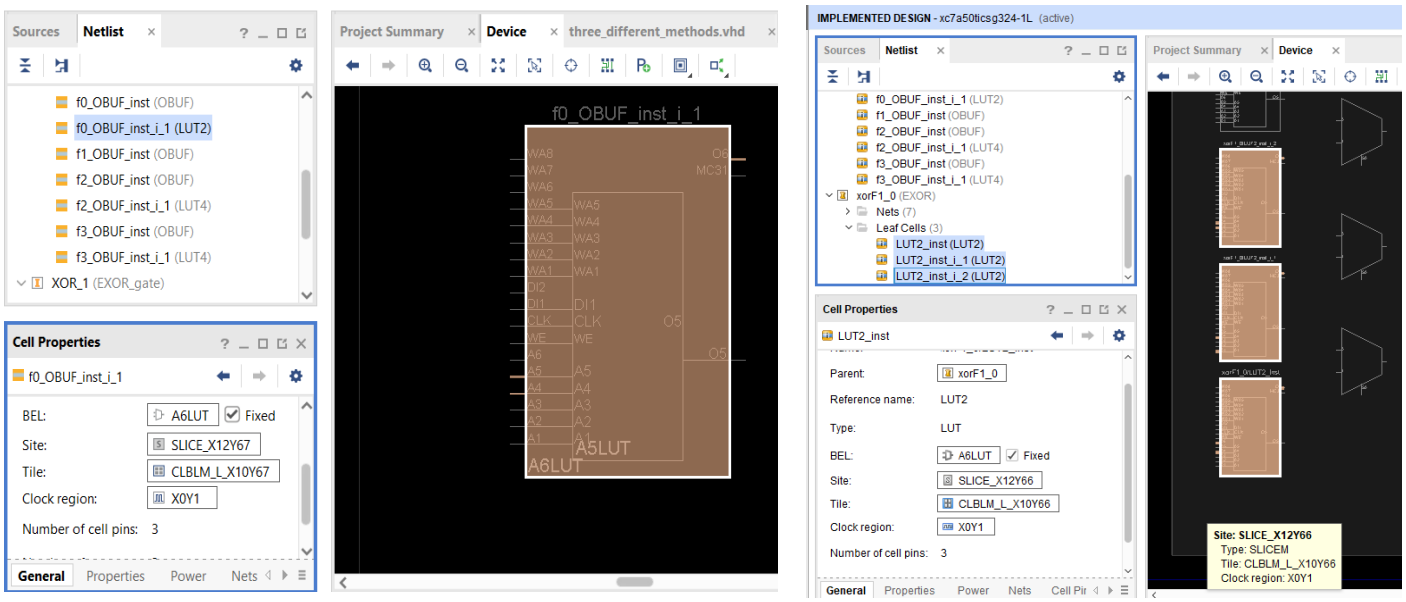
Summary

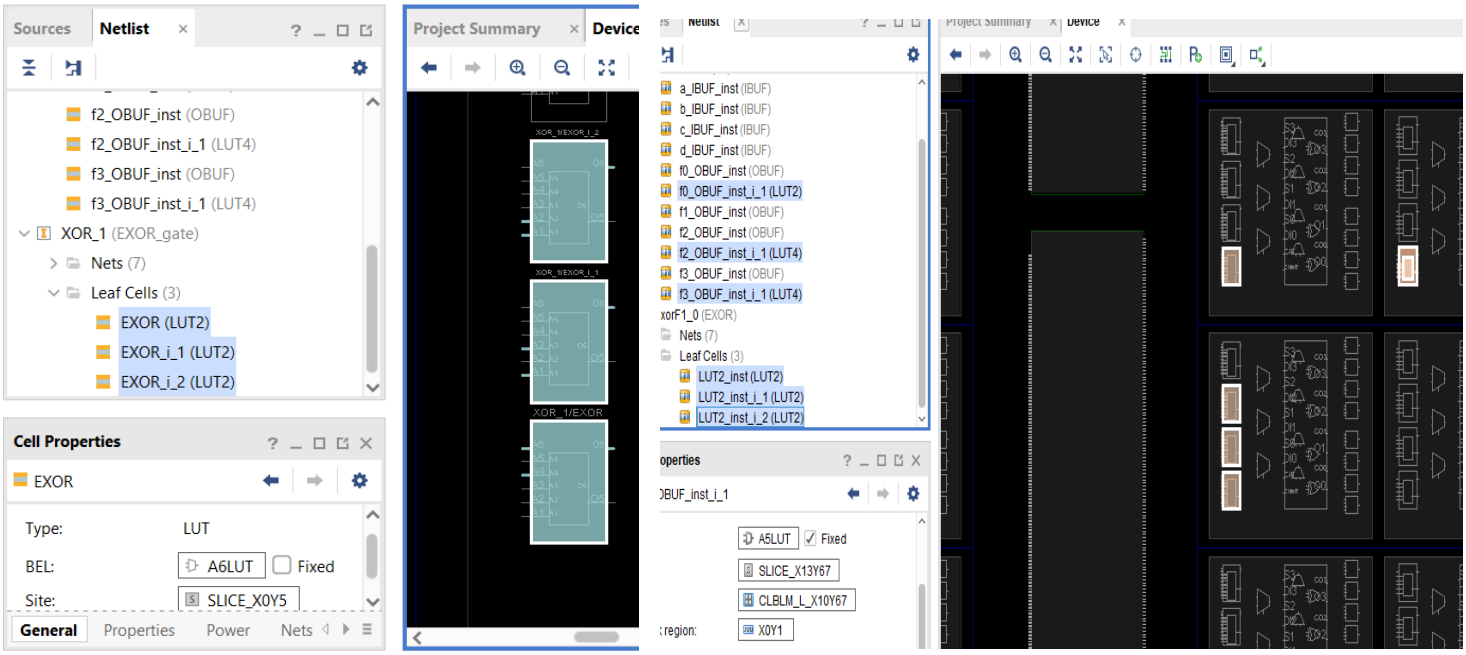
Resource	Utilization	Available	Utilization %
LUT	6	32600	0.02
IO	8	210	3.81



Design with LOC Constraints

- Placement f0,f1,f2,f3 respectively.





- Placed the LUTs on the device as stated in the assignment. As a result of these placements, our delays have almost doubled.

```
256 #f0 LUT
257 set_property LOC SLICE_X12Y67 [get_cells f0_OBUF_inst_i_1]
258 #f1 LUTS
259 set_property LOC SLICE_X12Y66 [get_cells xorF1_0/*]
260 #f2 LUT
261 set_property LOC SLICE_X13Y67 [get_cells f2_OBUF_inst_i_1]
262 #f3 LUT
263 set_property LOC SLICE_X14Y64 [get_cells f3_OBUF_inst_i_1]
```

- Path Delays

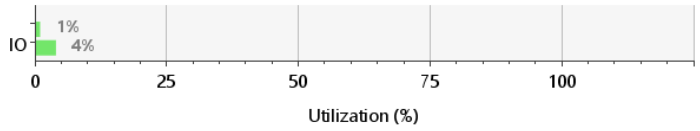
Combinational Delays

From Port	To Port	M ... 1	Max Process Corner	Min Delay	Min Process Corner
c	f3	11.627	SLOW	4.411	FAST
b	f0	11.620	SLOW	4.440	FAST
b	f3	11.576	SLOW	4.406	FAST
c	f2	11.544	SLOW	4.372	FAST
b	f2	11.491	SLOW	4.368	FAST
d	f0	11.385	SLOW	4.286	FAST
a	f3	11.380	SLOW	4.253	FAST
a	f2	11.293	SLOW	4.214	FAST
d	f3	11.237	SLOW	4.212	FAST
d	f2	11.150	SLOW	4.171	FAST
b	f1	7.562	SLOW	2.615	FAST
a	f1	7.103	SLOW	2.381	FAST
c	f1	7.093	SLOW	2.358	FAST
d	f1	6.918	SLOW	2.304	FAST

- Utilization

Summary

Resource	Utilization	Available	Utilization %
LUT	5	32600	0.02
IO	8	210	3.81



Design with Time (LOC CONSTRAINTS)

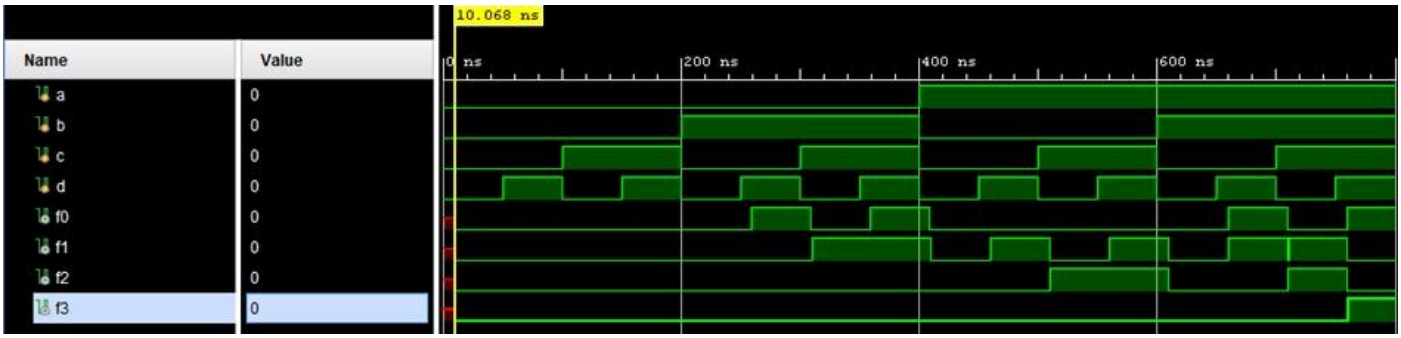
- Path Delays

I tried to reduce the maximum delay below 10ns. The output of my operation is as follows.

Combinational Delays

From Port	To Port	Max Delay	Max Process Corner
b	f3	10.507	SLOW
a	f3	10.348	SLOW
d	f3	10.276	SLOW
c	f3	10.160	SLOW
b	f2	10.134	SLOW
a	f2	9.975	SLOW
d	f2	9.905	SLOW
d	f0	9.865	SLOW
b	f0	9.856	SLOW
c	f2	9.821	SLOW
b	f1	7.254	SLOW
d	f1	7.000	SLOW
a	f1	6.872	SLOW
c	f1	6.868	SLOW

- Post-implementation Timing Simulation
  The red line above shows that there is a delay due to setup and hold time.



CONCLUSION

Implementation : Max Time Delay (ns)

Without any constraints : 7.643

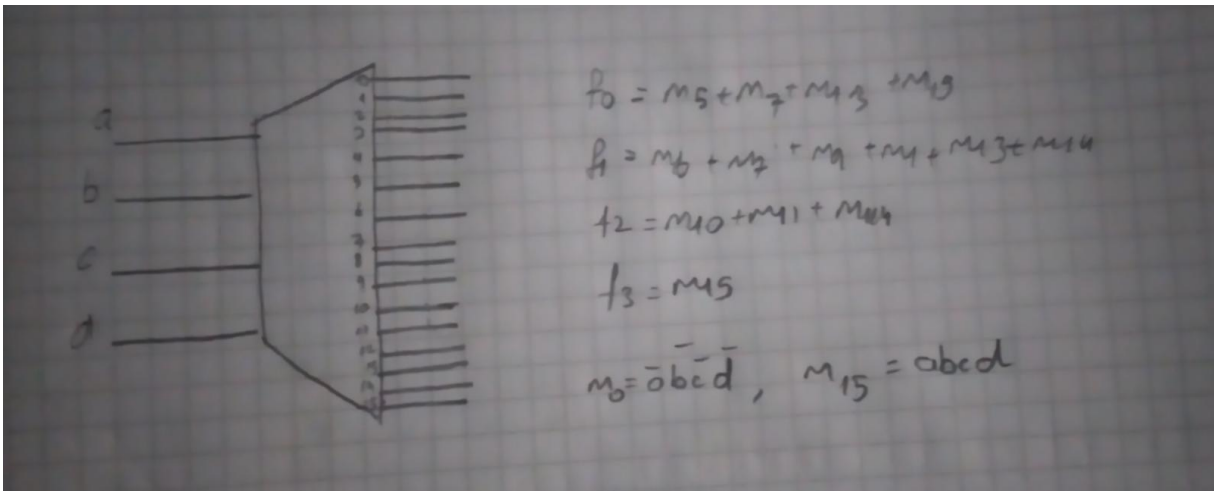
With time constraints (7ns) : 6.907

With LOC constraints : 11.627

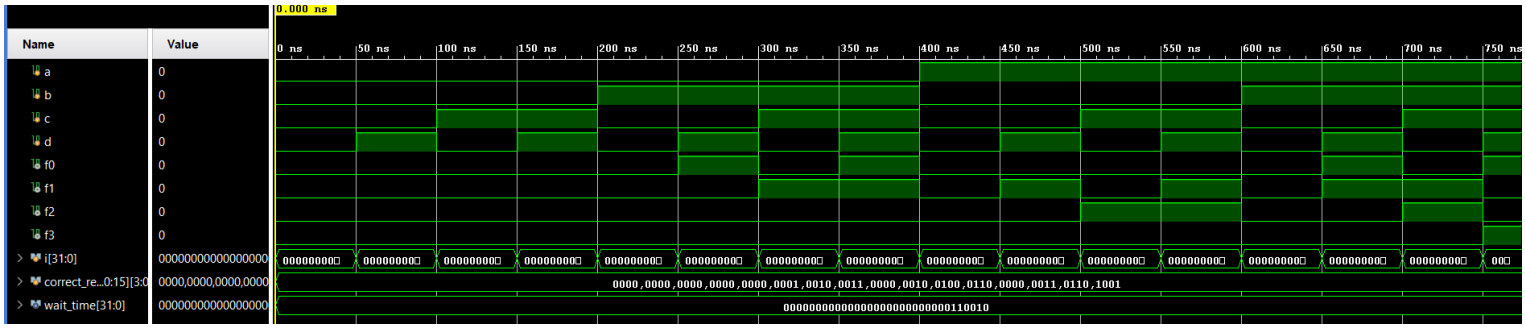
With time LOC constraints and set max delay (10ns) : 10.507

2. REALIZATION WITH DECODER

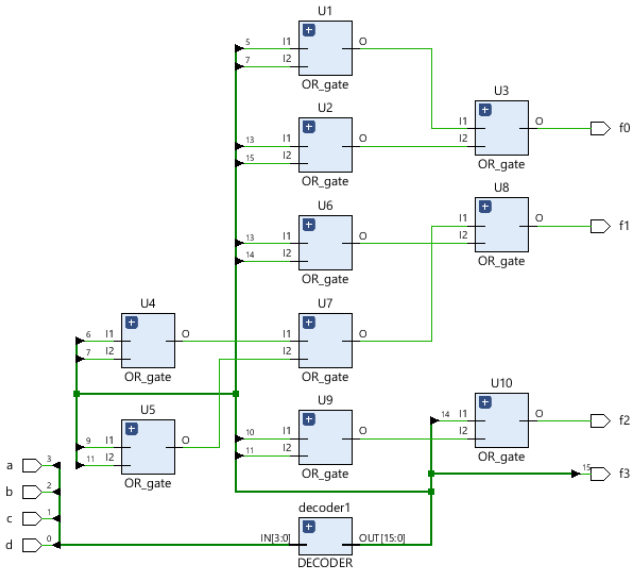
4x16 Decoder Representation



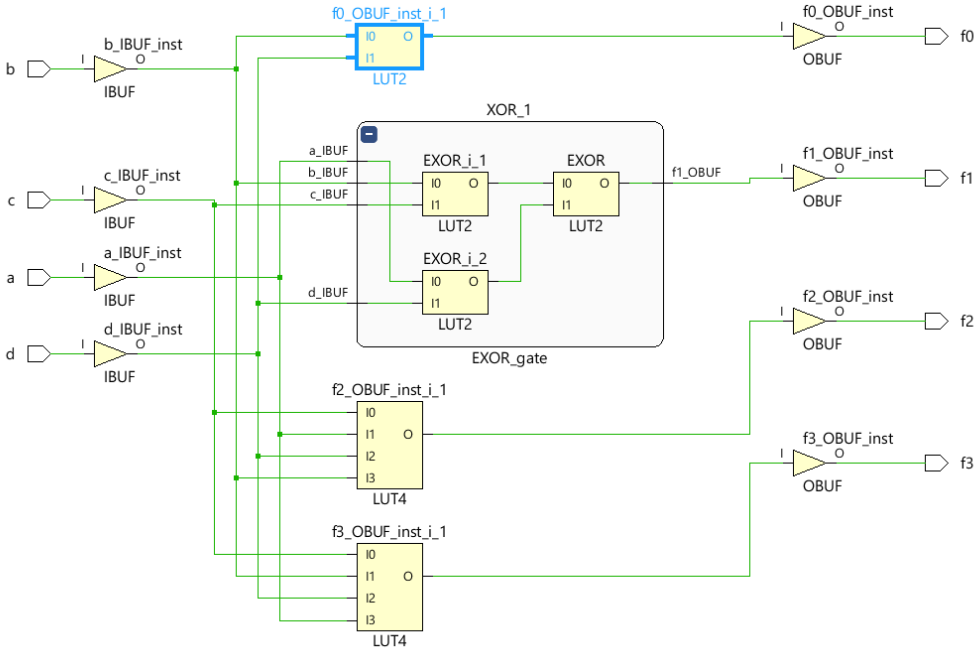
- Behavioral Simulation



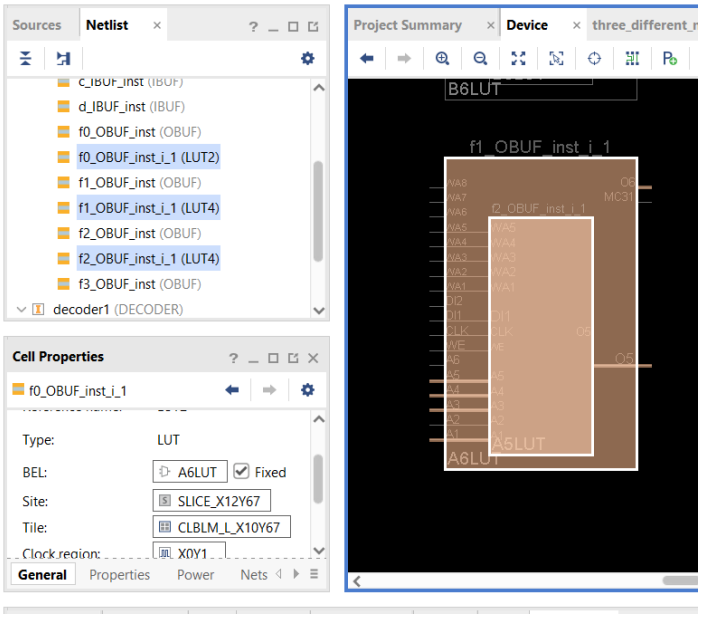
- RTL Schematic



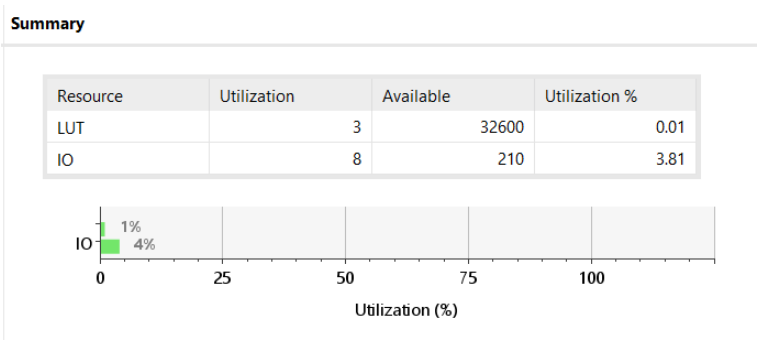
- Technology Schematic



- Device Placement



- Utilization Summary



Summary

Resource	Utilization	Available	Utilization %
LUT	3	32600	0.01
IO	8	210	3.81

- Path Delay
  - No time constraints

Combinational Delays

From Port	To Port	Max Delay	Max Process Corner	Min Delay	Min Process Corner
a	f1	7.271	SLOW	2.404	FAST
b	f0	7.067	SLOW	2.353	FAST
c	f3	6.979	SLOW	2.334	FAST
a	f2	6.940	SLOW	2.306	FAST
c	f1	6.929	SLOW	2.287	FAST
d	f1	6.852	SLOW	2.268	FAST
a	f3	6.796	SLOW	2.276	FAST
d	f0	6.777	SLOW	2.255	FAST
b	f1	6.747	SLOW	2.245	FAST
d	f3	6.680	SLOW	2.232	FAST
b	f3	6.618	SLOW	2.215	FAST
c	f2	6.600	SLOW	2.187	FAST
d	f2	6.523	SLOW	2.172	FAST
b	f2	6.449	SLOW	2.143	FAST

  - Adding time constraints

Max delay is set to 7 ns time constraints.

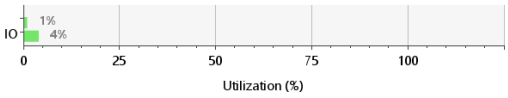
Combinational Delays

From Port	To Port	Max Delay	Max Process Corner
c	f2	6.673	SLOW
d	f3	6.620	SLOW
a	f2	6.613	SLOW
a	f1	6.578	SLOW
c	f3	6.543	SLOW
c	f1	6.529	SLOW
d	f2	6.498	SLOW
a	f3	6.489	SLOW
d	f0	6.398	SLOW
b	f0	6.332	SLOW
b	f2	6.314	SLOW
b	f3	6.305	SLOW
d	f1	6.251	SLOW
b	f1	6.192	SLOW

  - Utilization Summary

Summary

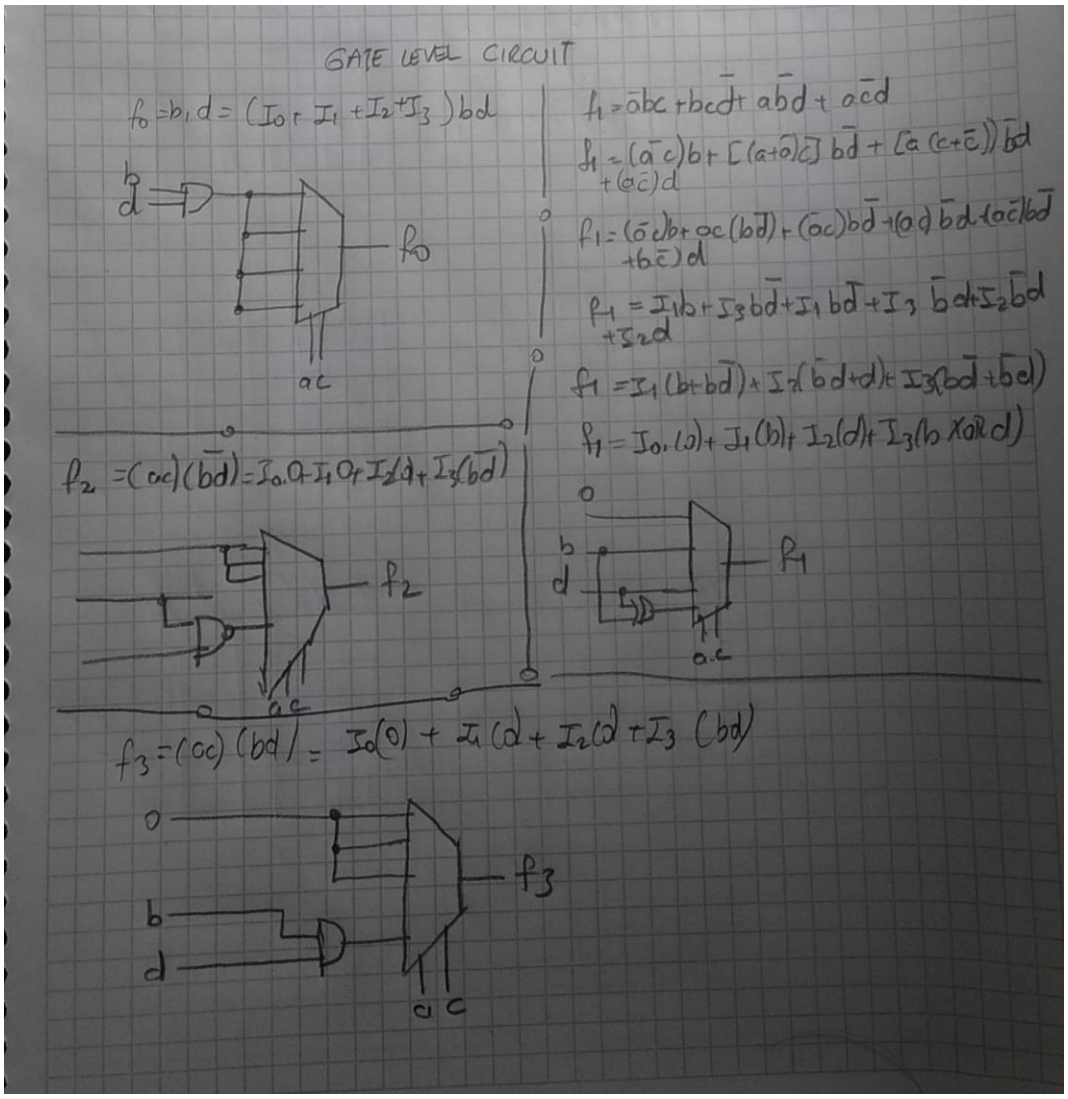
Resource	Utilization	Available	Utilization %
LUT	4	32600	0.01
IO	8	210	3.81



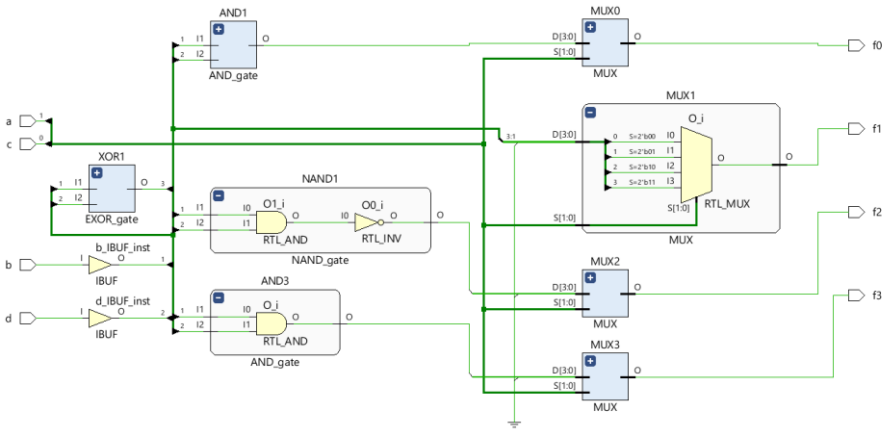
We reduced the delays below 7ns by adjusting the time constraint, but 1 LUT was added to our structure as an extra.

3. REALIZATION WITH MUX

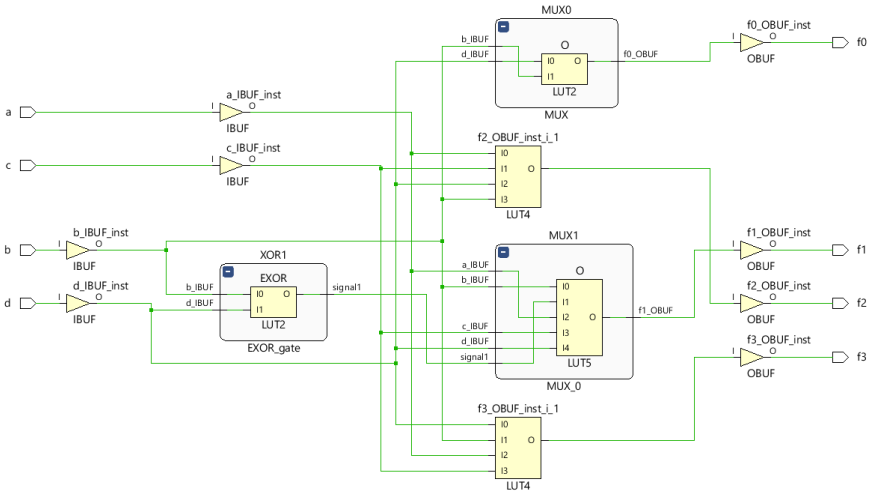
- Gate Level Circuit



- RTL Schematic



- Technology Schematic

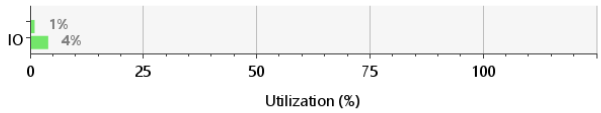


I saw the LUT5 build here, which I hadn't seen in previous assignments. LUT5 is a LookUpTable with 5 inputs and 1 output.

- Utilization Summary

Summary

Resource	Utilization	Available	Utilization %
LUT	4	32600	0.01
IO	8	210	3.81



- Path Delays
  - No time constraints

Combinational Delays

From Port	To Port	Max Delay	Max Process Corner	Min Delay	Min Process Corner
b	f1	7.731	SLOW	2.190	FAST
d	f1	7.451	SLOW	2.099	FAST
a	f2	7.184	SLOW	2.367	FAST
b	f0	7.076	SLOW	2.362	FAST
a	f3	6.950	SLOW	2.314	FAST
b	f2	6.922	SLOW	2.274	FAST
c	f2	6.842	SLOW	2.250	FAST
d	f0	6.790	SLOW	2.268	FAST
c	f1	6.774	SLOW	2.249	FAST
b	f3	6.690	SLOW	2.223	FAST
c	f3	6.610	SLOW	2.195	FAST
a	f1	6.591	SLOW	2.191	FAST
d	f2	6.516	SLOW	2.178	FAST
d	f3	6.316	SLOW	2.120	FAST

- With time constraints

With time constraints it is achieved to get below 7ns time constraints. Results are given below.

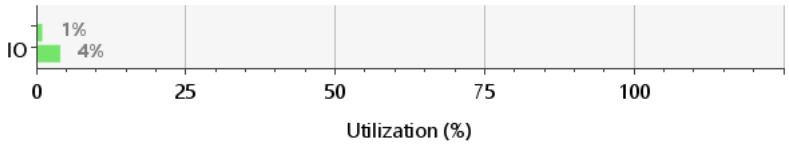
Combinational Delays

From Port	To Port	Max Delay 1	Max Process Corner
a	f1	6.803	SLOW
b	f1	6.748	SLOW
c	f3	6.619	SLOW
a	f2	6.601	SLOW
d	f1	6.571	SLOW
c	f1	6.559	SLOW
b	f2	6.548	SLOW
b	f3	6.546	SLOW
a	f3	6.448	SLOW
b	f0	6.415	SLOW
d	f2	6.403	SLOW
d	f0	6.275	SLOW
d	f3	6.197	SLOW
c	f2	6.190	SLOW

- Utilization Summary

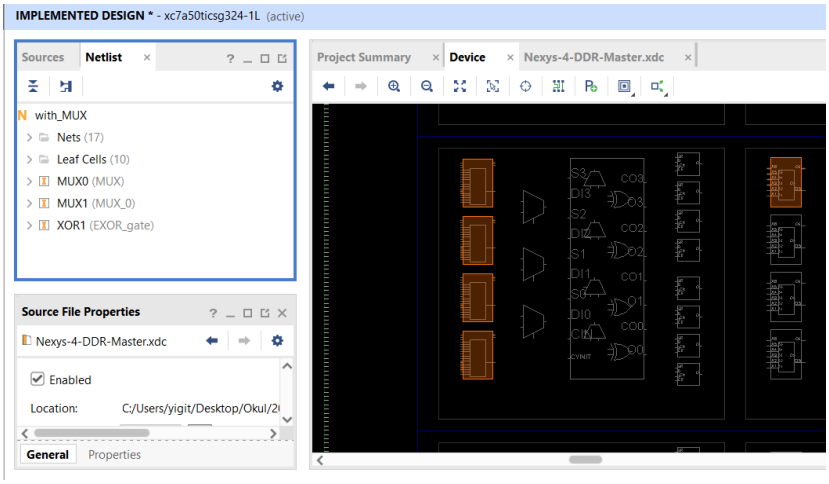
Summary

Resource	Utilization	Available	Utilization %
LUT	5	32600	0.02
IO	8	210	3.81



- Device placement and Combinational Delays

```
259 set_property BEL D6LUT [get_cells MUX0/O]
260 set_property LOC SLICE_X12Y63 [get_cells MUX0/O]
261 set_property BEL C6LUT [get_cells MUX1/O]
262 set_property LOC SLICE_X12Y63 [get_cells MUX1/O]
263 set_property BEL B6LUT [get_cells XOR1/EXOR]
264 set_property LOC SLICE_X12Y63 [get_cells XOR1/EXOR]
265 set_property BEL A6LUT [get_cells f2_OBUF_inst_i_1]
266 set_property LOC SLICE_X12Y63 [get_cells f2_OBUF_inst_i_1]
267 set_property BEL D6LUT [get_cells f3_OBUF_inst_i_1]
268 set_property LOC SLICE_X13Y63 [get_cells f3_OBUF_inst_i_1]
```



Combinational Delays

From Port	To Port	Max Delay	Max Process Corner	Min Delay	Min Process Corner
b	f1	11.575	SLOW	4.347	FAST
b	f0	11.556	SLOW	4.331	FAST
d	f1	11.549	SLOW	4.225	FAST
a	f1	11.528	SLOW	4.405	FAST
d	f3	11.480	SLOW	4.346	FAST
b	f3	11.303	SLOW	4.243	FAST
d	f0	11.216	SLOW	4.251	FAST
a	f3	11.126	SLOW	4.270	FAST
c	f3	11.086	SLOW	4.142	FAST
d	f2	10.886	SLOW	4.042	FAST
b	f2	10.711	SLOW	3.941	FAST
c	f1	10.662	SLOW	4.006	FAST
a	f2	10.566	SLOW	3.961	FAST
c	f2	10.492	SLOW	3.837	FAST

➢ Our combinational delays have increased noticeably due to random placement of locations within the device. The relevant outputs are shown in the figure above.

LUT Usage

Decoder : 3 (Best LUT Usage)
MUX : 4
SSI: 5 (Worst LUT Usage)

Path Delays

Decoder : 7.271ns (Best delay)
MUX : 7.731ns (Worst delay)
SSI : 7.643ns

Final comments

- Decoder is the simpliler than the other structures , with_SSI and MUX, it is need to be used the decoder and OR_gates the necessary outputs together..

- MUX is more complex to design than the other structures , with_SSI and MUX, the design of the design was more difficult to think through and more time was spent than others.

- If we look at the coding side, I used less submodules in the MUX structure compared to other modules, while the decoder was the structure where I used the most submodules.