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EHB322E Digital Electronic Circuits MIDTERM I

Duration: 120 Minutes

Grading: 1) 30%, 2) 30%, 3) 40%

Exam is in closed-notes and closed-books format; calculators are allowed

For your answers please use the space provided in the exam sheet

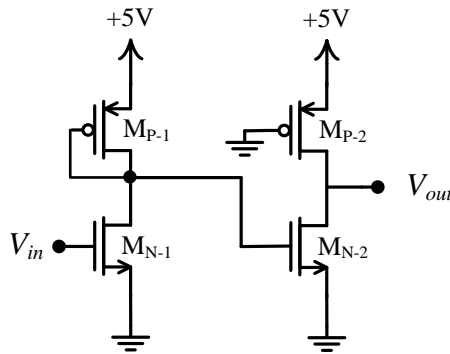
GOOD LUCK!

- 1) Consider a buffer shown below. Use the following equations for your calculations.

Saturation region current-voltage equation: $I_D = \frac{1}{2} k'_{p,n} \frac{W}{L} (V_{GS} - V_{T0p,n})^2$

Linear region current-voltage equation: $I_D = \frac{1}{2} k'_{p,n} \frac{W}{L} [2(V_{GS} - V_{T0p,n})V_{DS} - V_{DS}^2]$

Transistor parameters: $k_p' = \mu_p c_{ox} = 35 \mu\text{A/V}^2$, $k_n' = \mu_n c_{ox} = 98 \mu\text{A/V}^2$, $V_{TN} = 1\text{V}$, $V_{TP} = -0.5\text{V}$, $W_{N-1} = 5\mu$, $W_{N-2} = 5\mu$, $L_P = L_N = 1\mu$.



Buffer

- Find the maximum value of W_{P-1} satisfying that $V_{in} = 5\text{V}$ results in $V_{out} = 5\text{V}$.
- Find the value of W_{P-2} if $V_{in} = 0\text{V}$ results in $V_{out} = 1\text{V}$.
- Find the buffer's static power consumption values when $V_{in} = 0\text{V}$ and $V_{in} = 5\text{V}$.

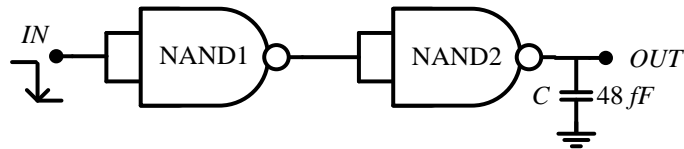
- 2) Consider a buffer circuit consisting of two CMOS NAND gates, shown below. An external capacitor of $48fF$ is connected to the output. A signal switching from high to low is applied to the input.

Equivalent resistor for an NMOS transistor: $R_N = (12k\Omega) / (W/L)_N$

Equivalent resistor for a PMOS transistor: $R_P = (24k\Omega) / (W/L)_P$

Gate capacitors $C_{GS-N} = c_{ox}W_NL_N$ and $C_{GS-P} = c_{ox}W_PL_P$; neglect C_{GD} capacitors.

Transistor parameters: $c_{ox} = 1 \text{ fF}/\mu\text{m}^2$, $L_N = L_P = 1\mu$, $W_{N1} = 2\mu$, $W_{P1} = 3\mu$, $W_{N2} = 4\mu$, $W_{P2} = 6\mu$.



Digital circuit with two CMOS NAND gates

- Implement a NAND gate with a Boolean function $f = \overline{x_1 x_2}$ using CMOS transistors. If inputs of a NAND gate are shorted, as we use in our circuit, then find its Boolean function. Draw the CMOS implementation of the above circuit.
- Find the **total propagation delay value** between the input and the output.
 - You should consider C_{GS} capacitors as well as the external $C = 48fF$ capacitor
 - Do not consider capacitors at nodes other than the node of gate inputs/outputs.

- 3) For a specific technology and a specific supply voltage, a CMOS inverter with parameters $W_P=1\mu$, $W_N=1\mu$, $L_P=1\mu$, $L_N=1\mu$, and a total output load capacitor of 1 fF has $t_{PHL}=1\text{ ns}$ and $t_{PLH}=2\text{ ns}$. By considering the same technology and the supply voltage,
- Implement $f = x_1x_2\bar{x}_3 + x_1\bar{x}_2x_3 + \bar{x}_1x_2x_3 + \bar{x}_1x_4$ with a **CMOS circuit** using **minimum** number of transistors. Draw the circuit. How many PMOS and NMOS transistors do you use?
 - Select $W_P=4\mu$ for all PMOS transistors and $W_N=2\mu$ for all NMOS transistors of your CMOS circuit. Find the **worst case (largest)** and the **best case (smallest)** t_{PHL} and t_{PLH} values if a total output load capacitor is 2 fF . Neglect internal node capacitors. You should report 4 delay values.