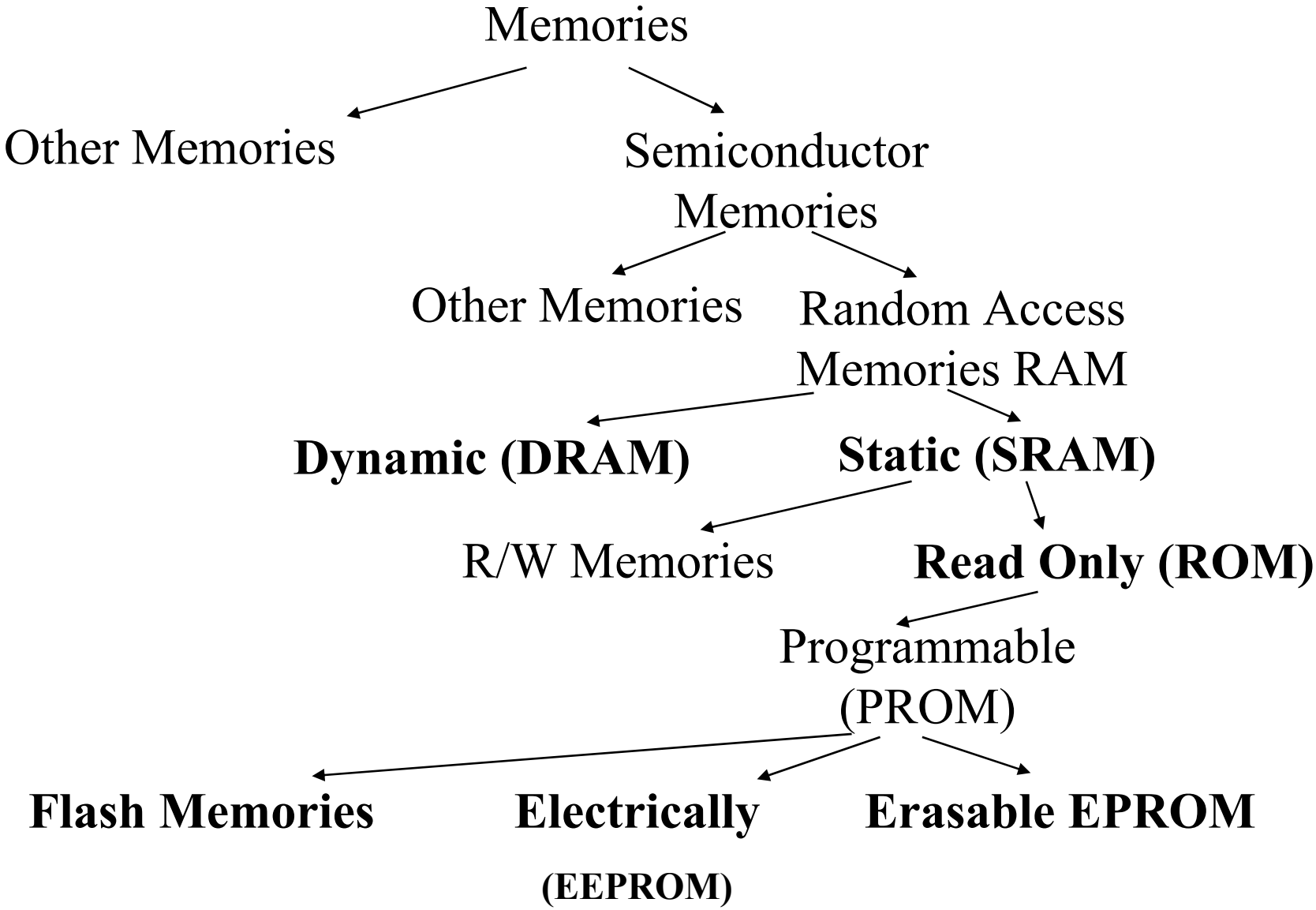
Memory I: Overview of Semiconductor Memories

- **Random Access Memories**
- **ROMs;**
  - **ROM**
  - **Decoders**
  - **PLA's**
  - **EEPROM**

Static Random Access

- **Memory Classification**
- **CMOS Static Memory**
  - **Six transistor memory cell**
  - **Memory architecture**
  - **Decoders**
  - **Read/write cirtcuitry**
- **RMOS Static Memory**
  - **Four transistor memory cell**
  - **Technology**
  - **Memory cell layout**

Memory Classification



Memory Classification

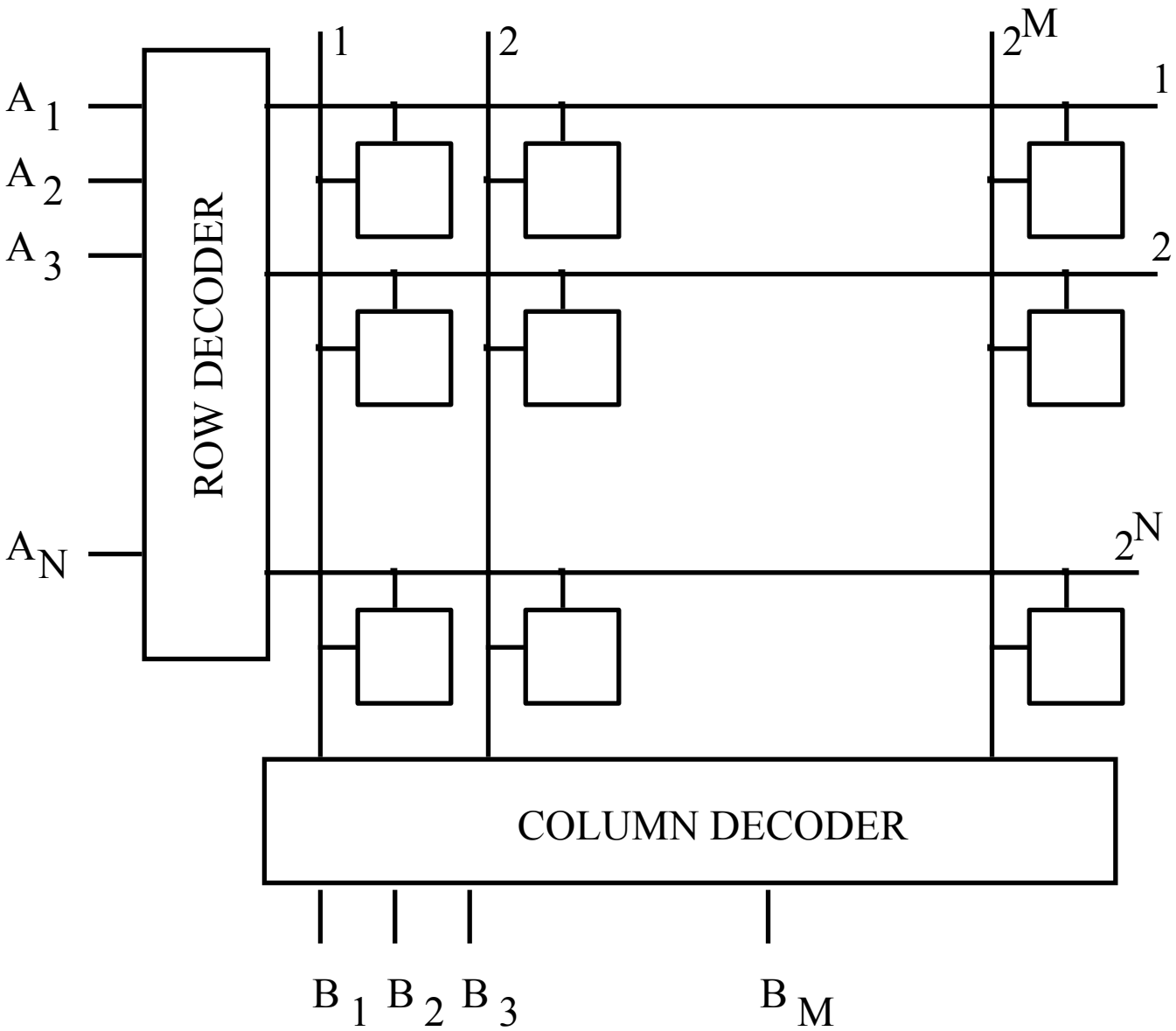
Semiconductor Memories

Read Only (ROM) L 23

Static (SRAM) L 23/24

Dynamic (DRAM) L 24

Random Access Memories



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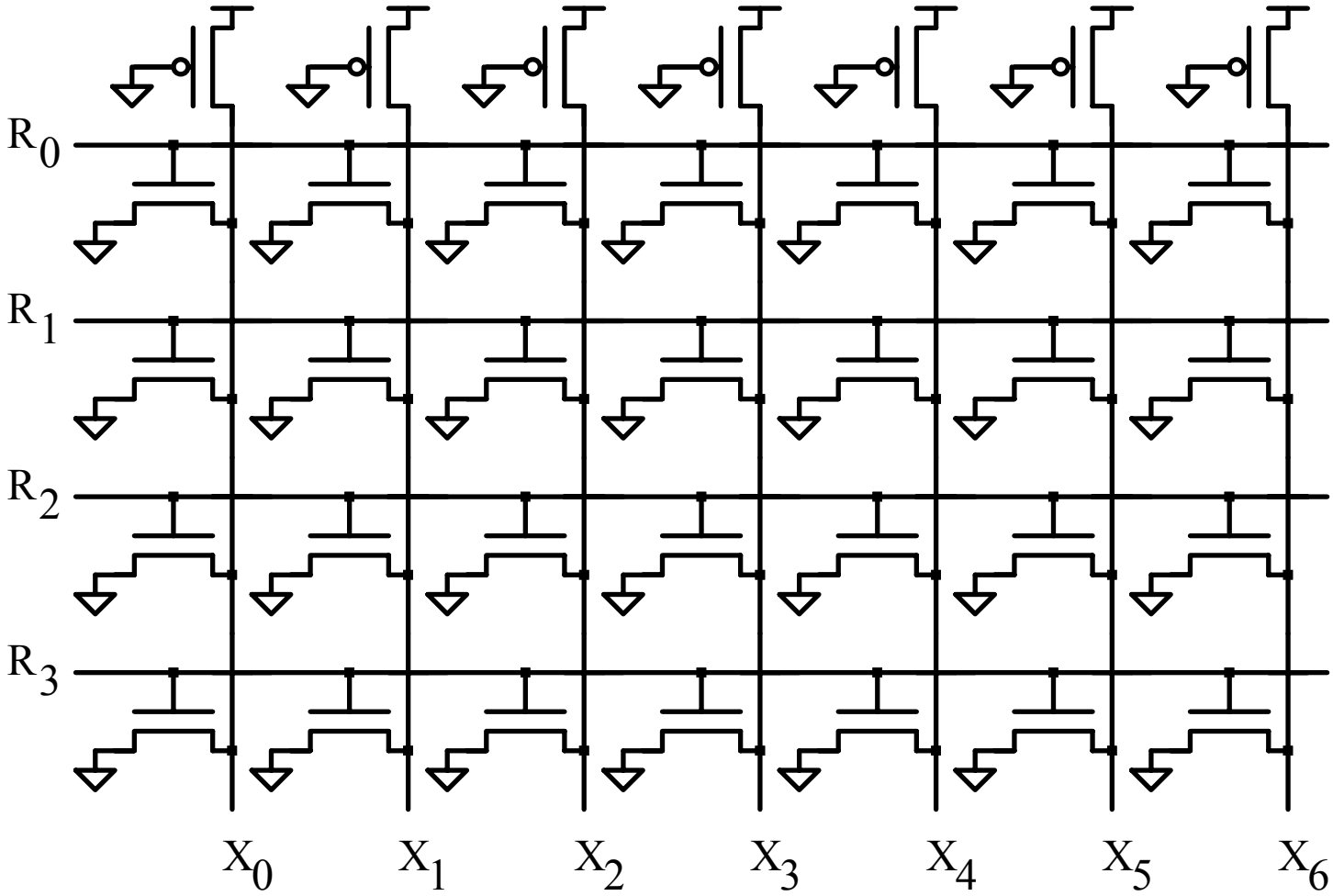
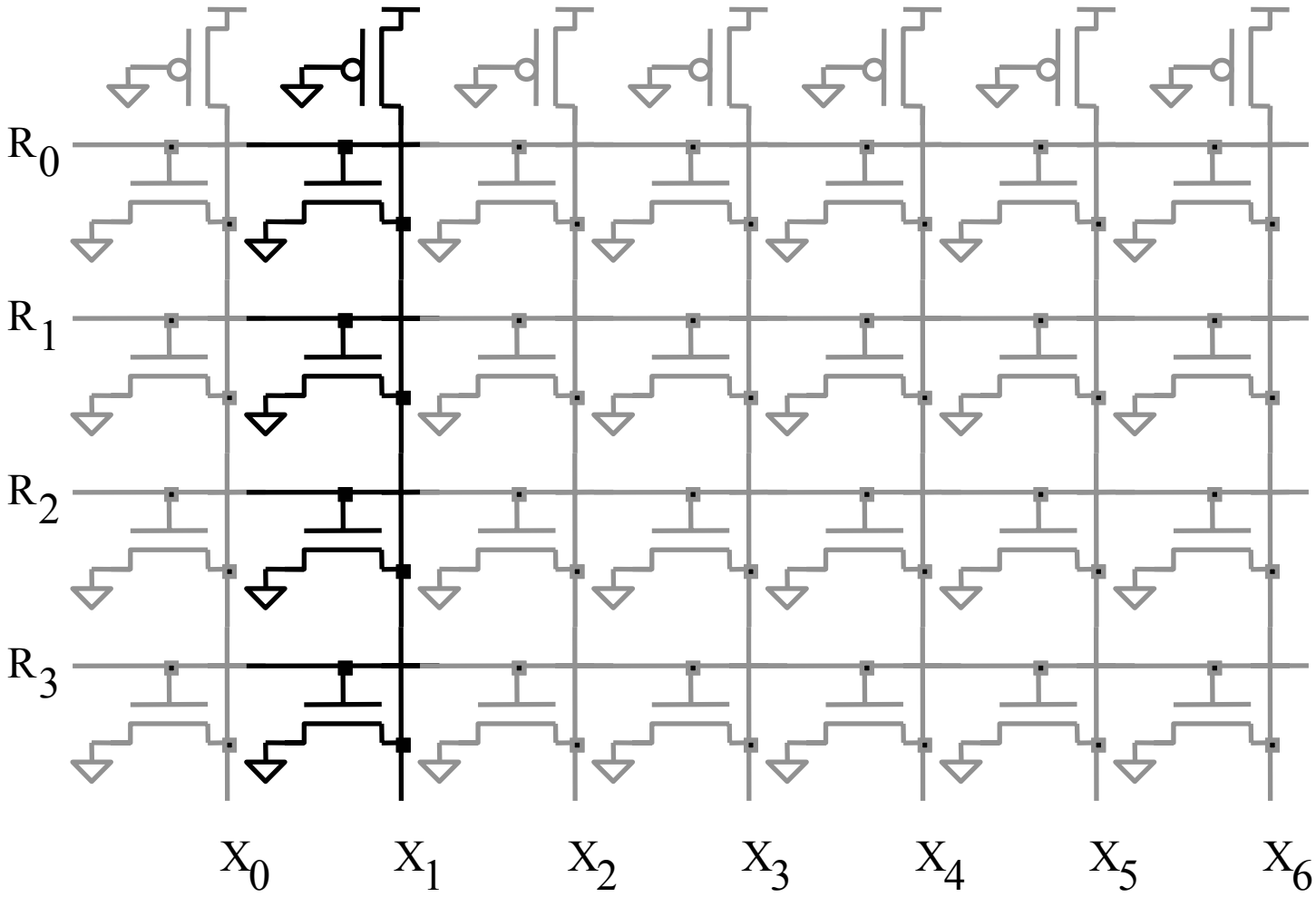
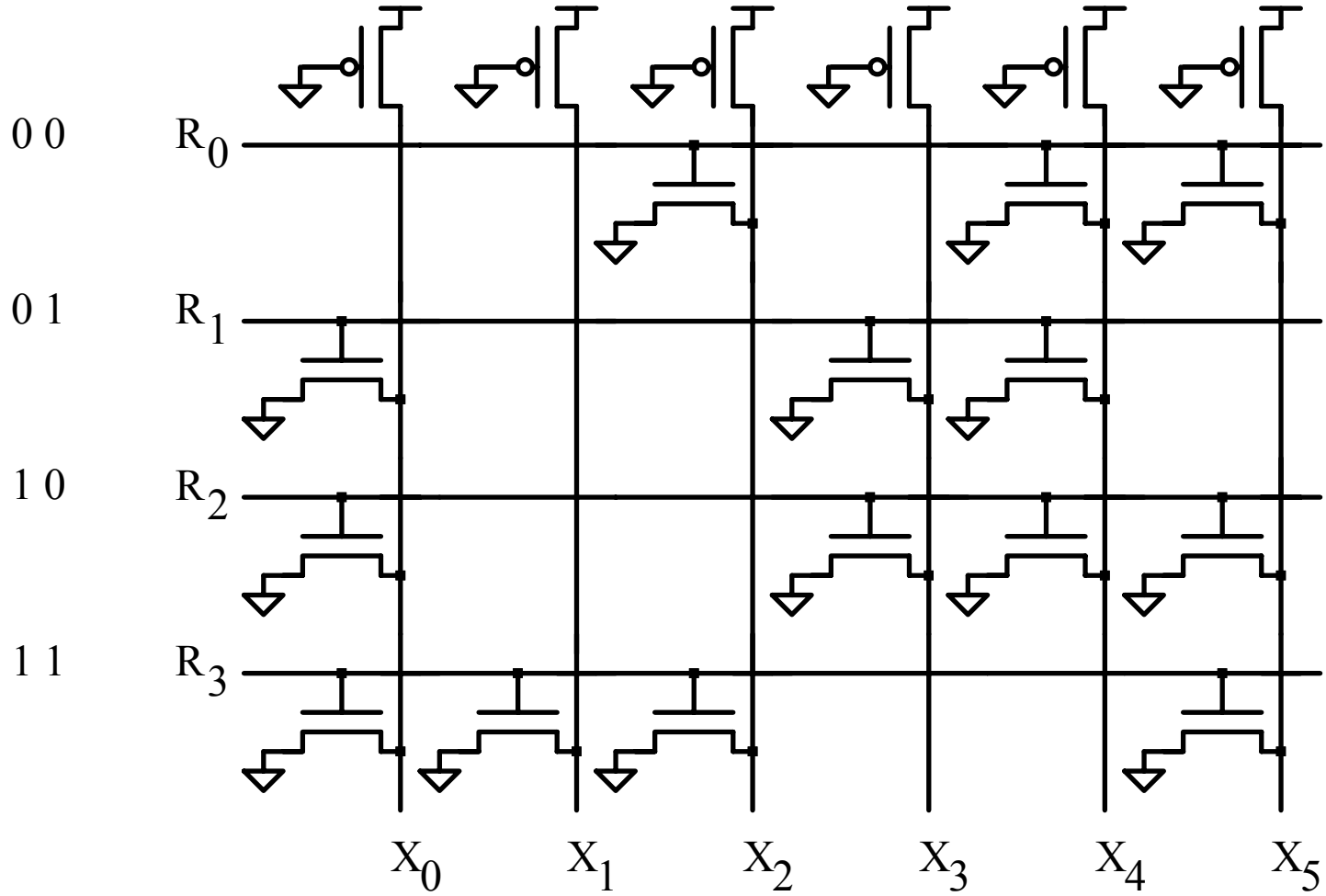
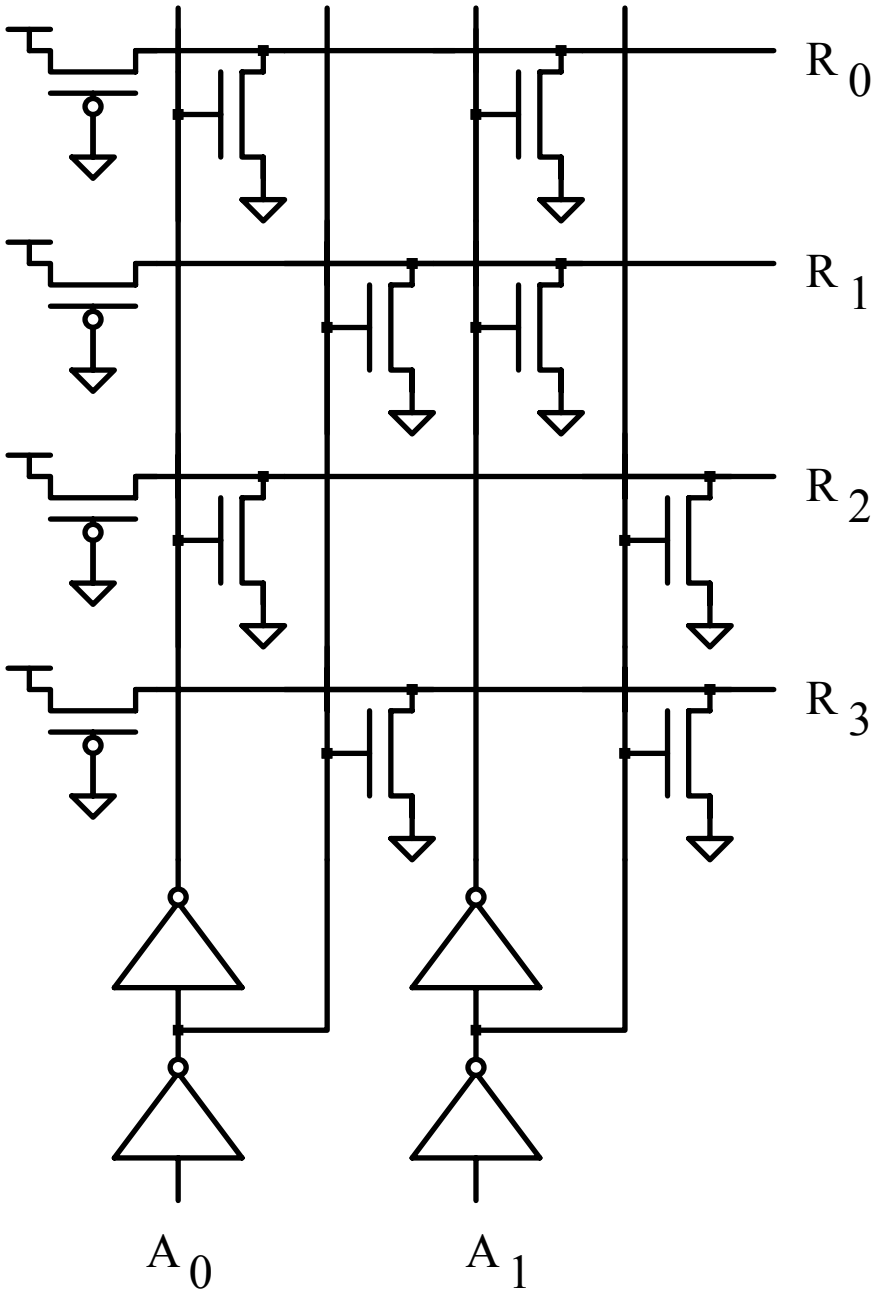


Read Only Memory (ROM)



Read Only Memory (ROM)

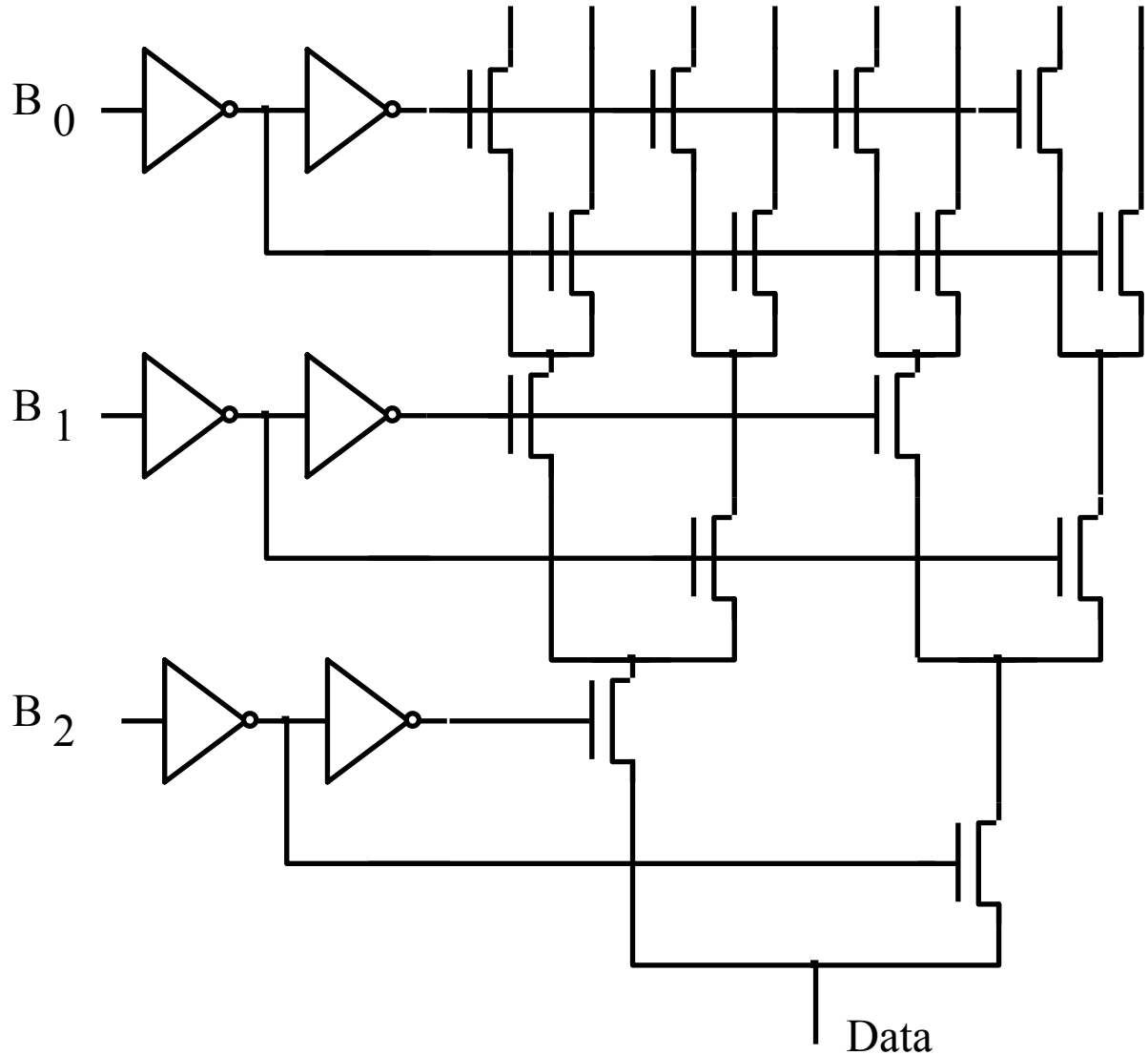




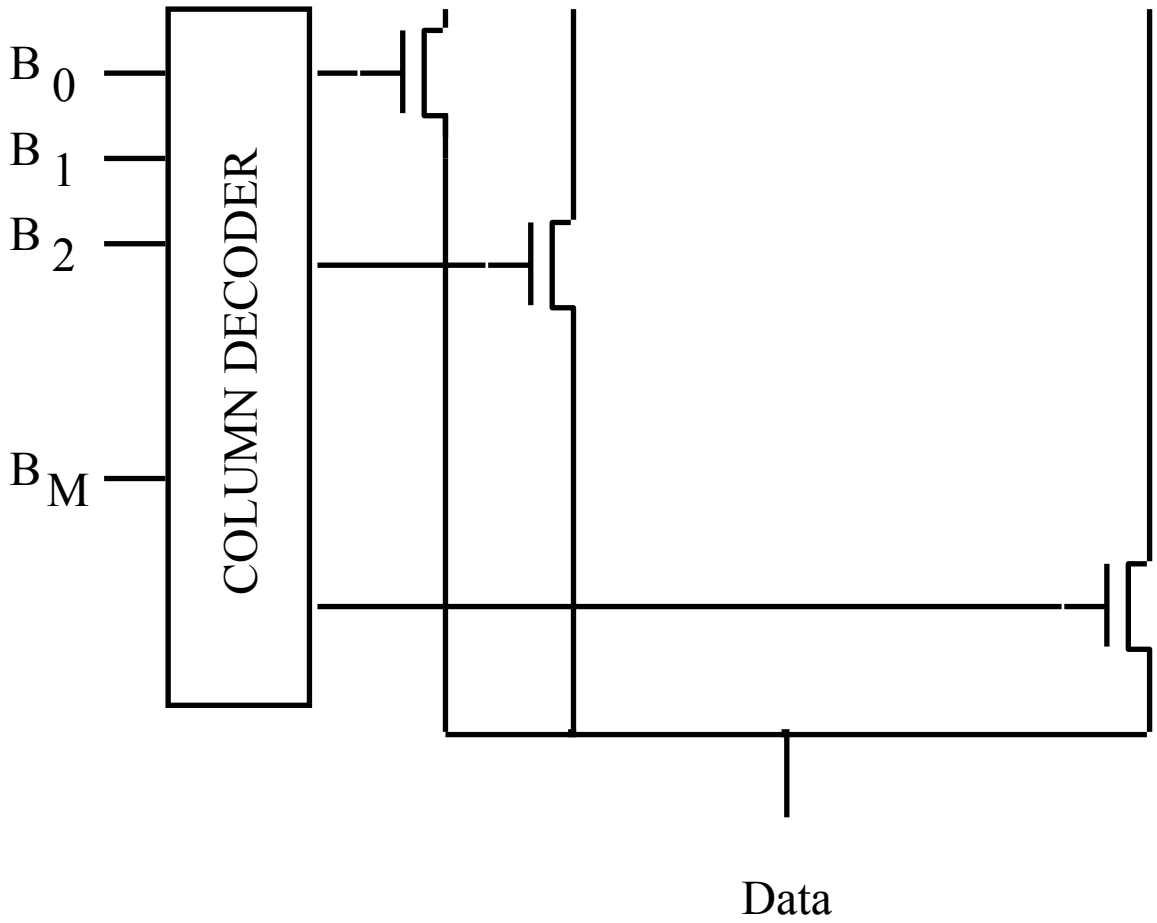
Row Decoder

$A_0\ A_1 \quad R_0\ R_1\ R_2\ R_3$

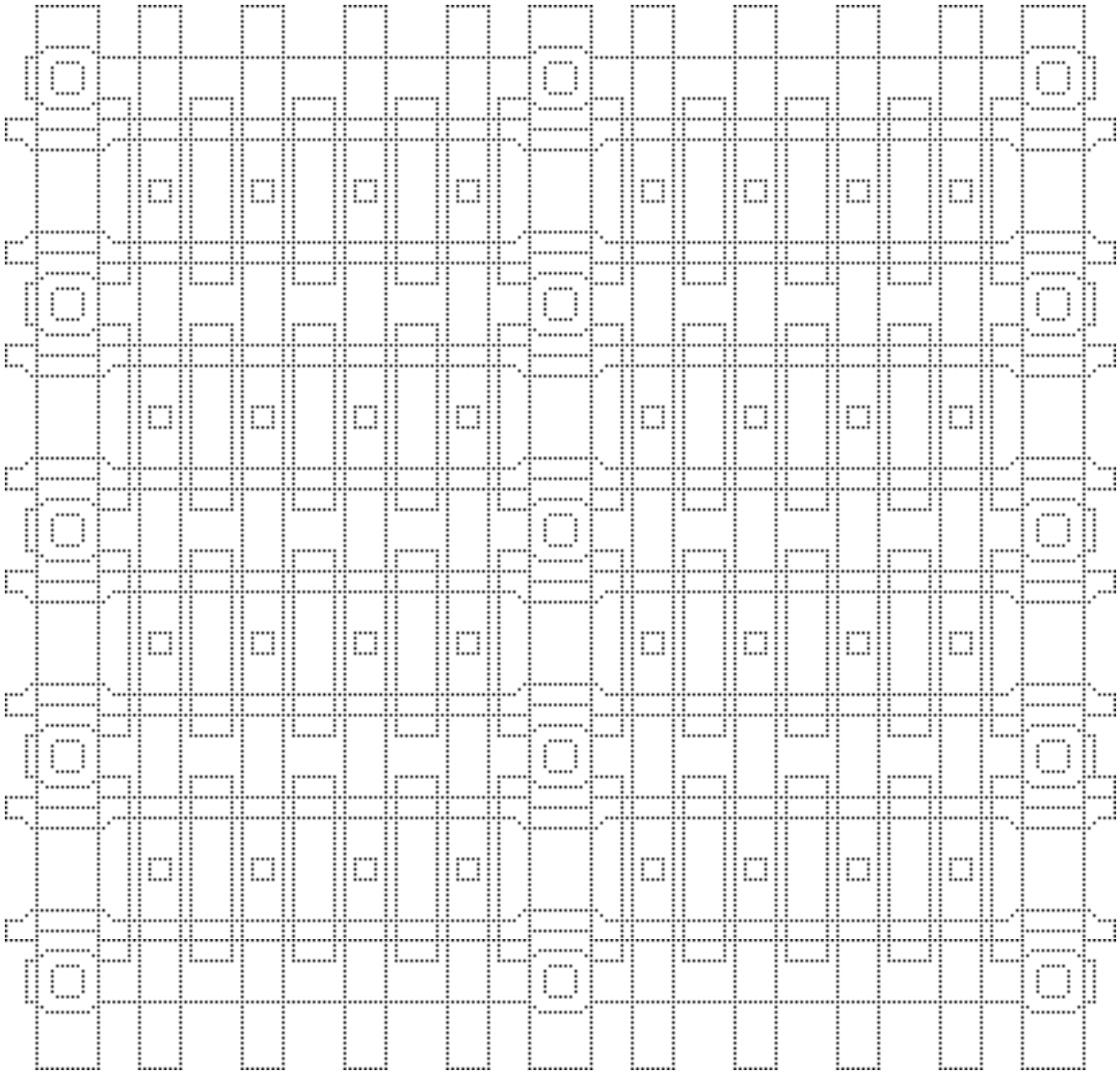
Column Decoder

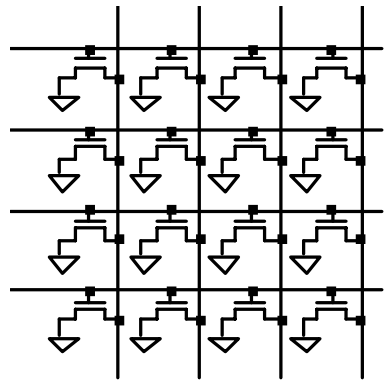


Column Decoder



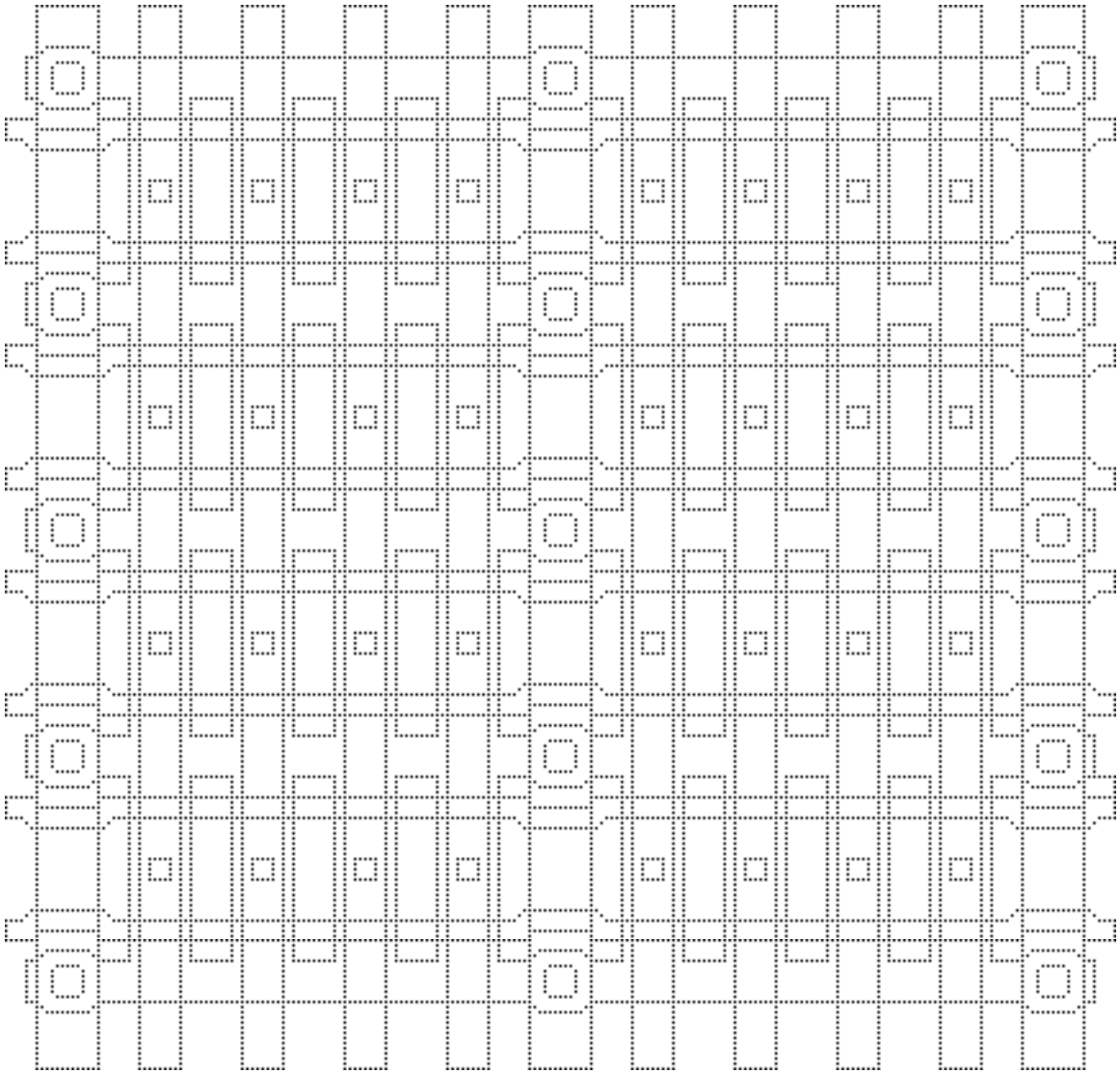
Read Only Memory (ROM)





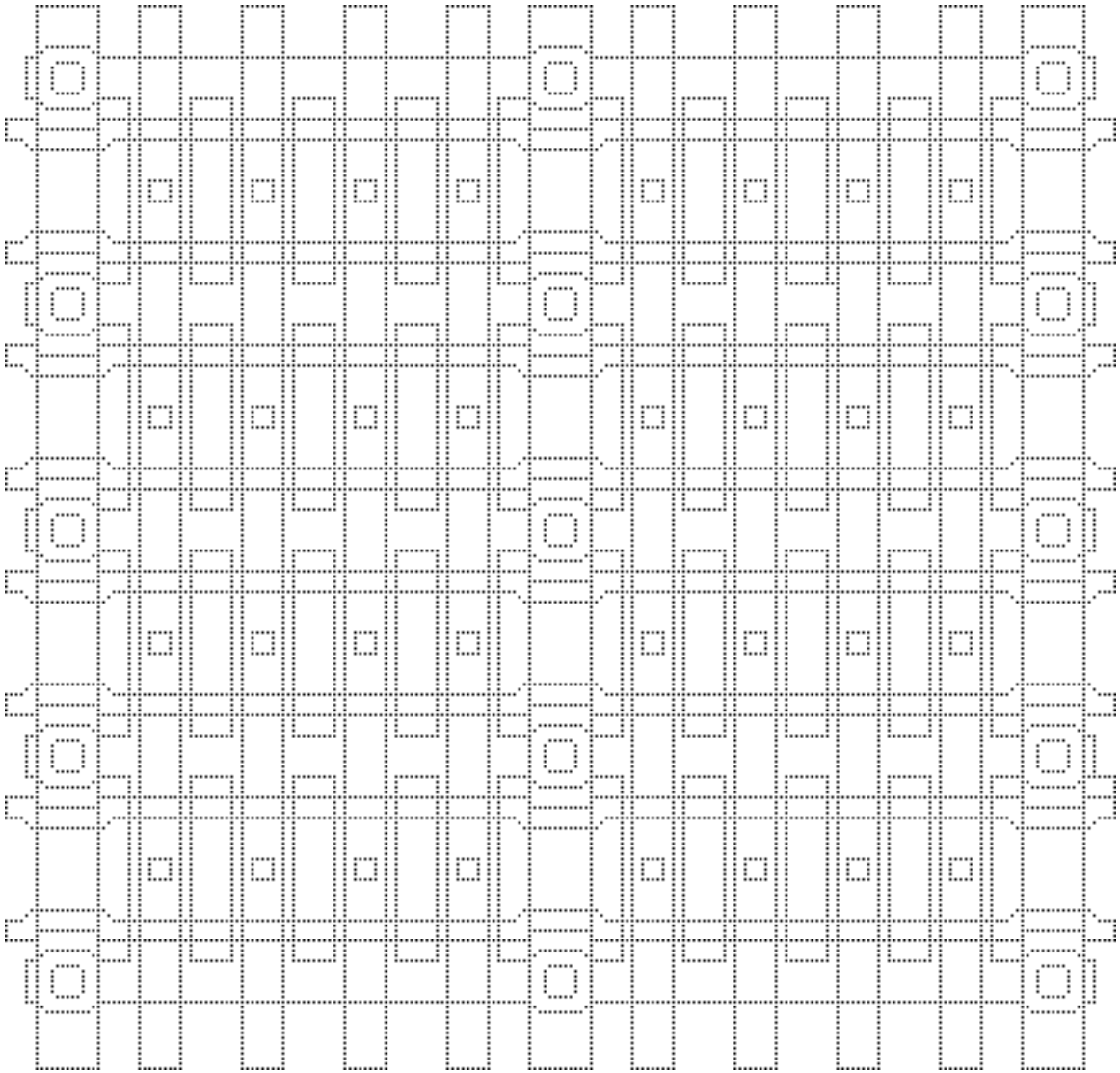
Read Only Memory (ROM)

Active



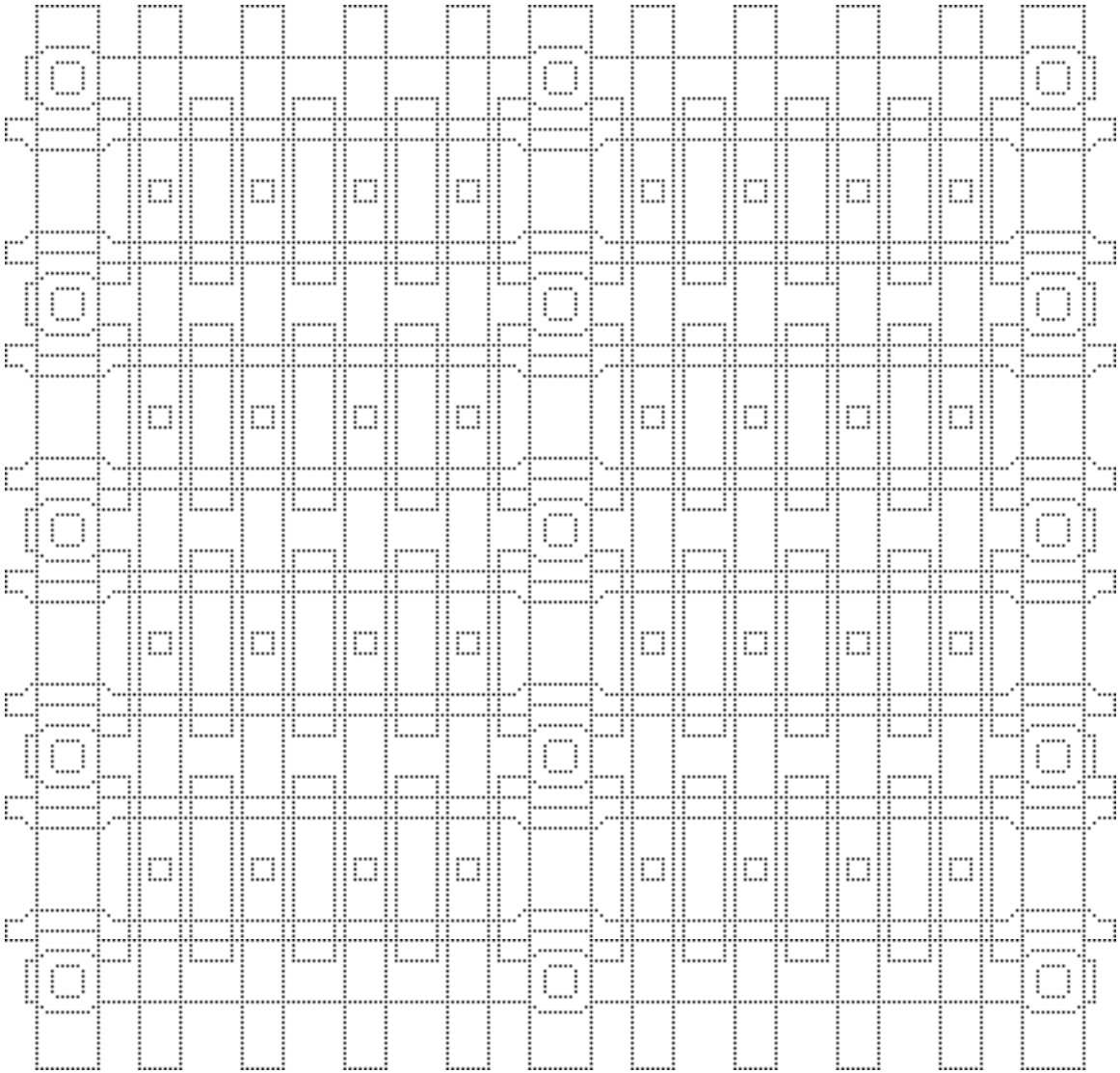
Read Only Memory (ROM)

Poly

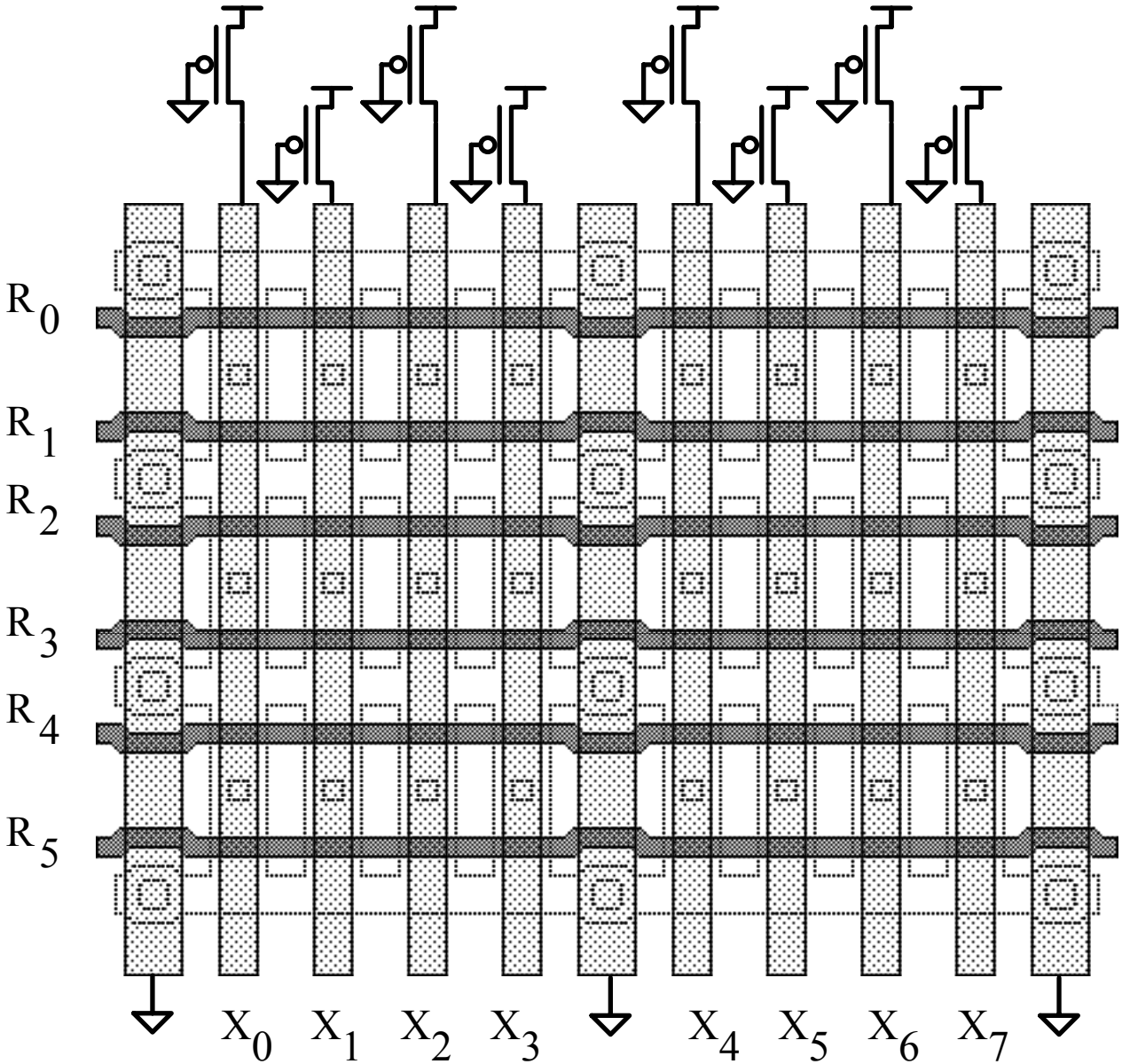


Read Only Memory (ROM)

Metal



Read Only Memory (ROM)



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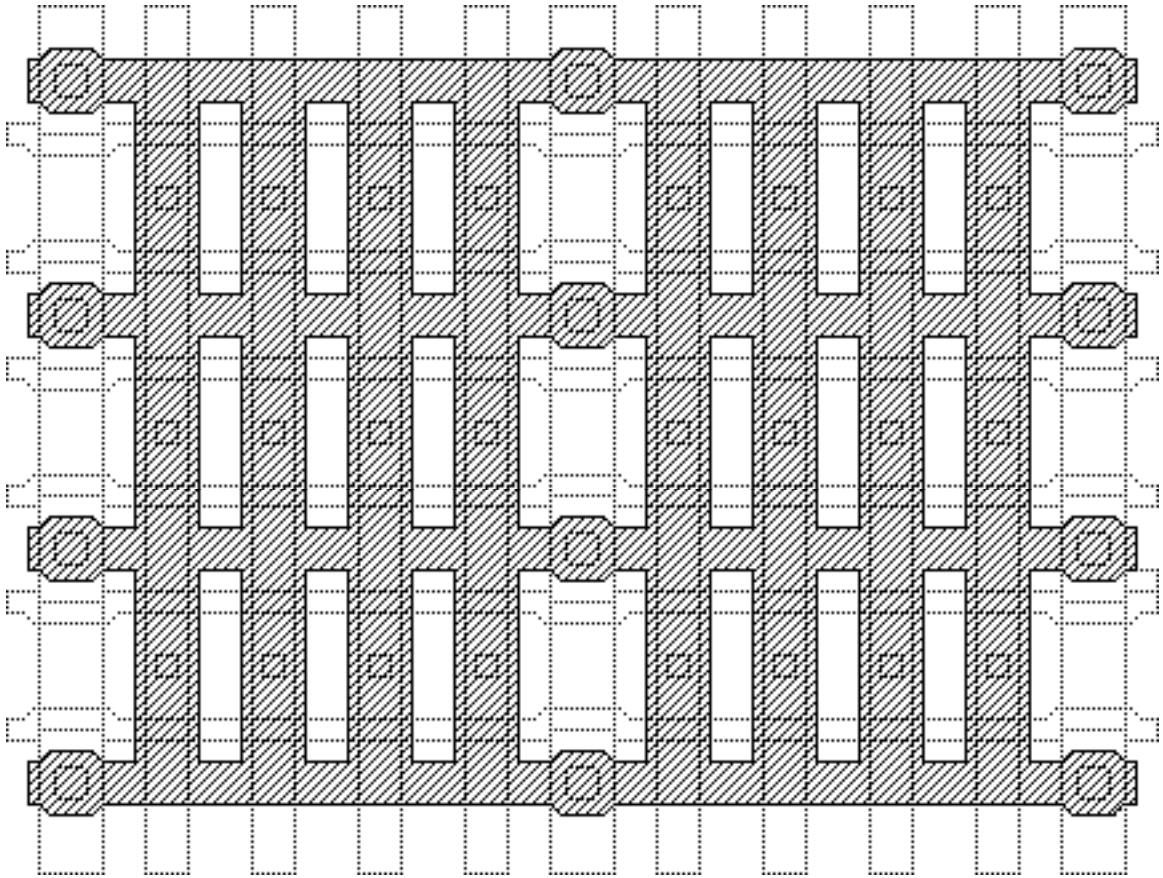
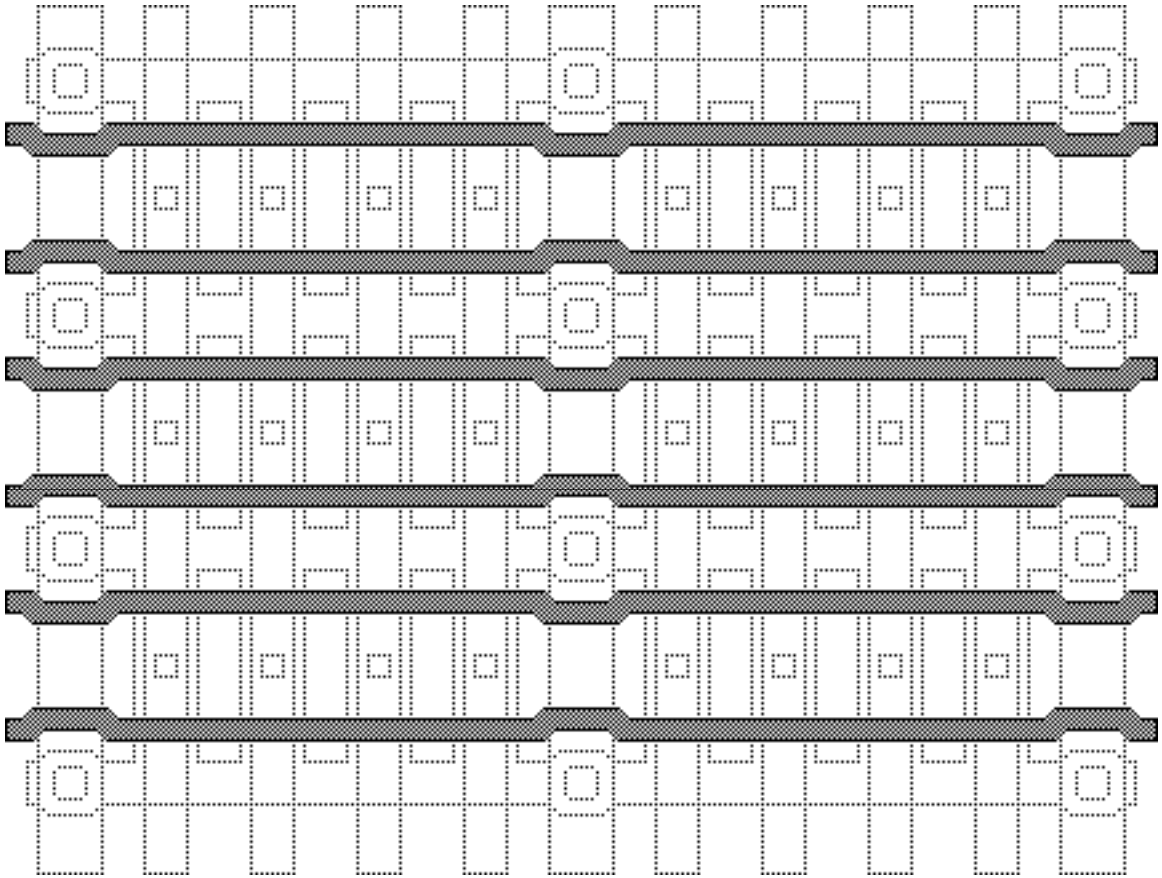
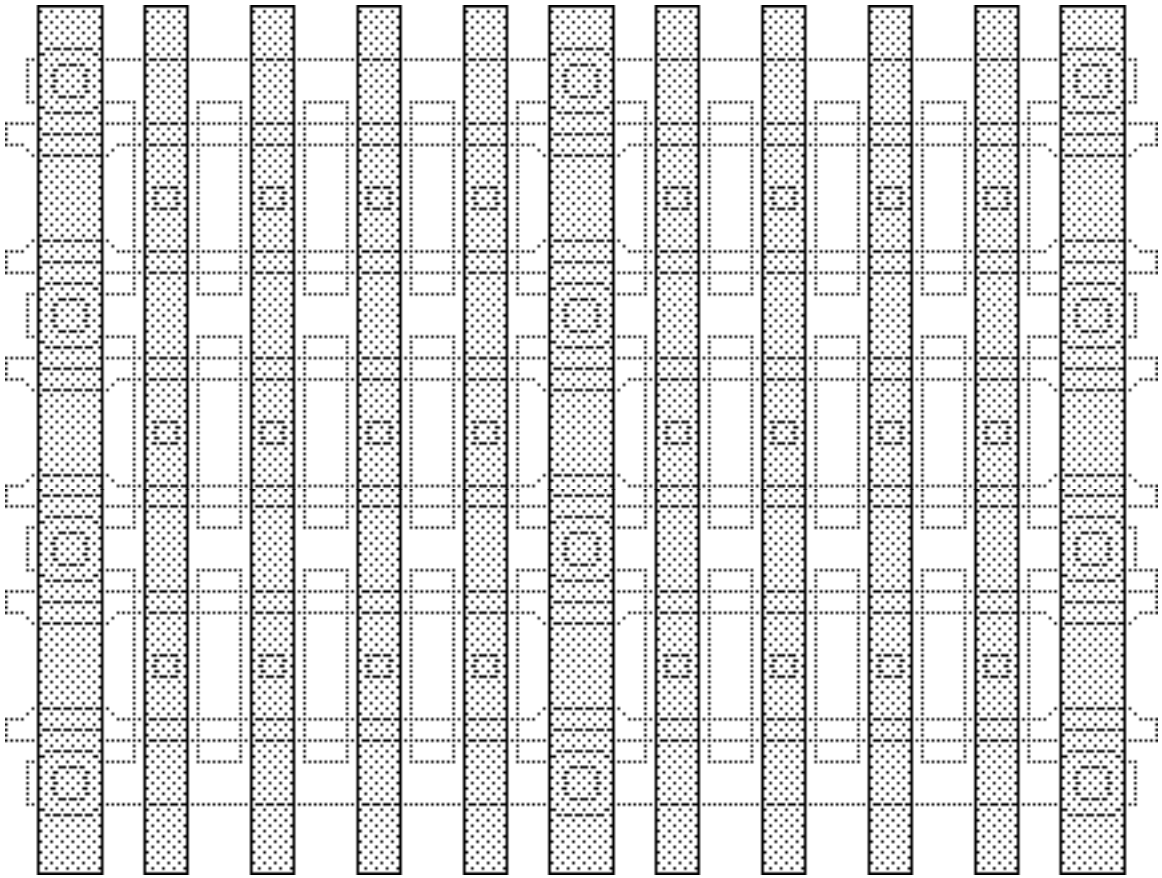


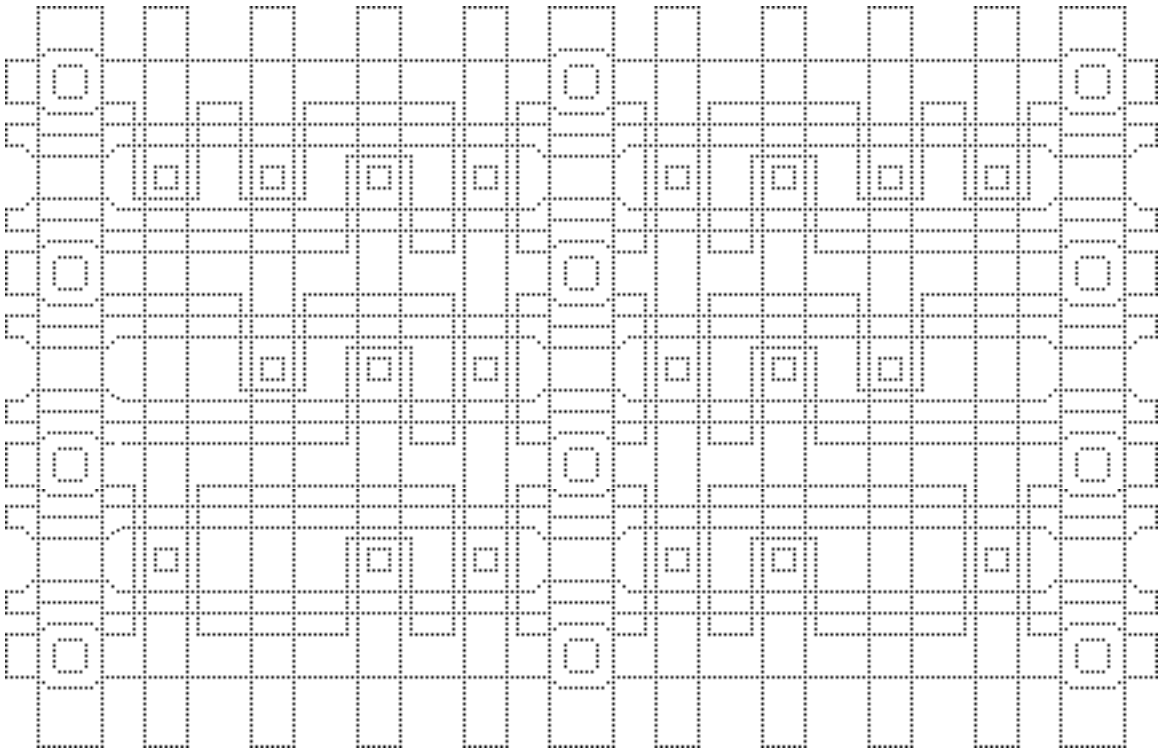
Read Only Memory (ROM)



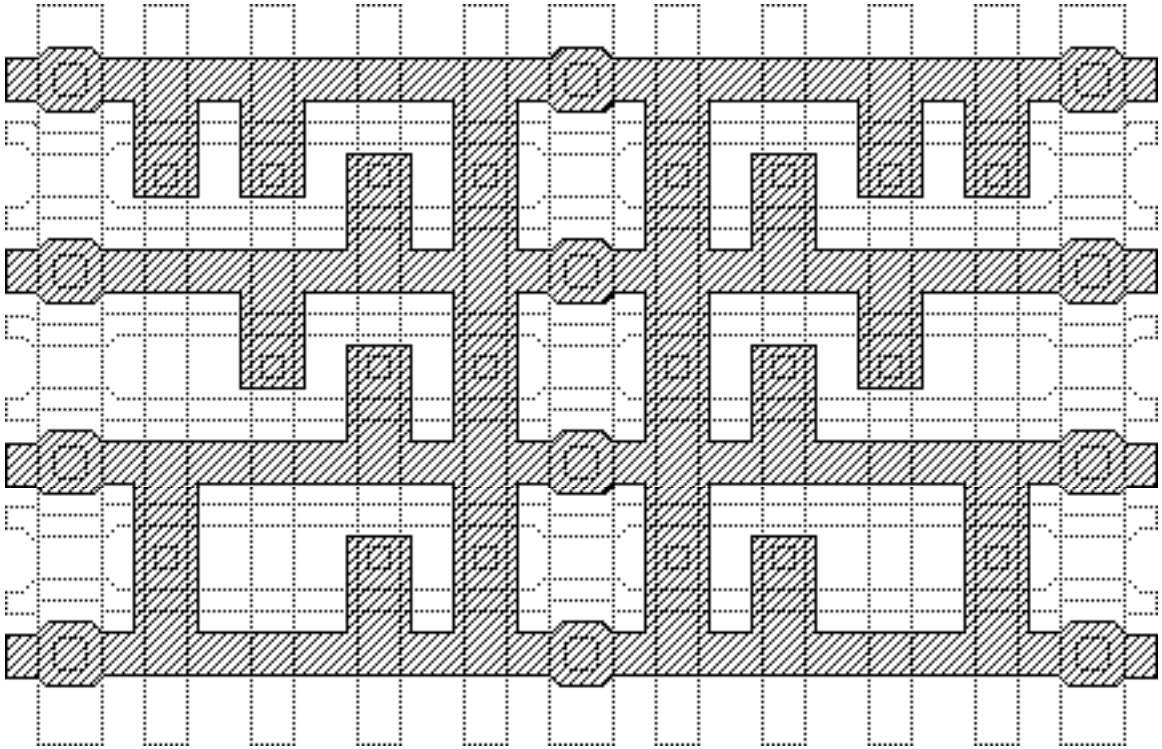
Read Only Memory (ROM)



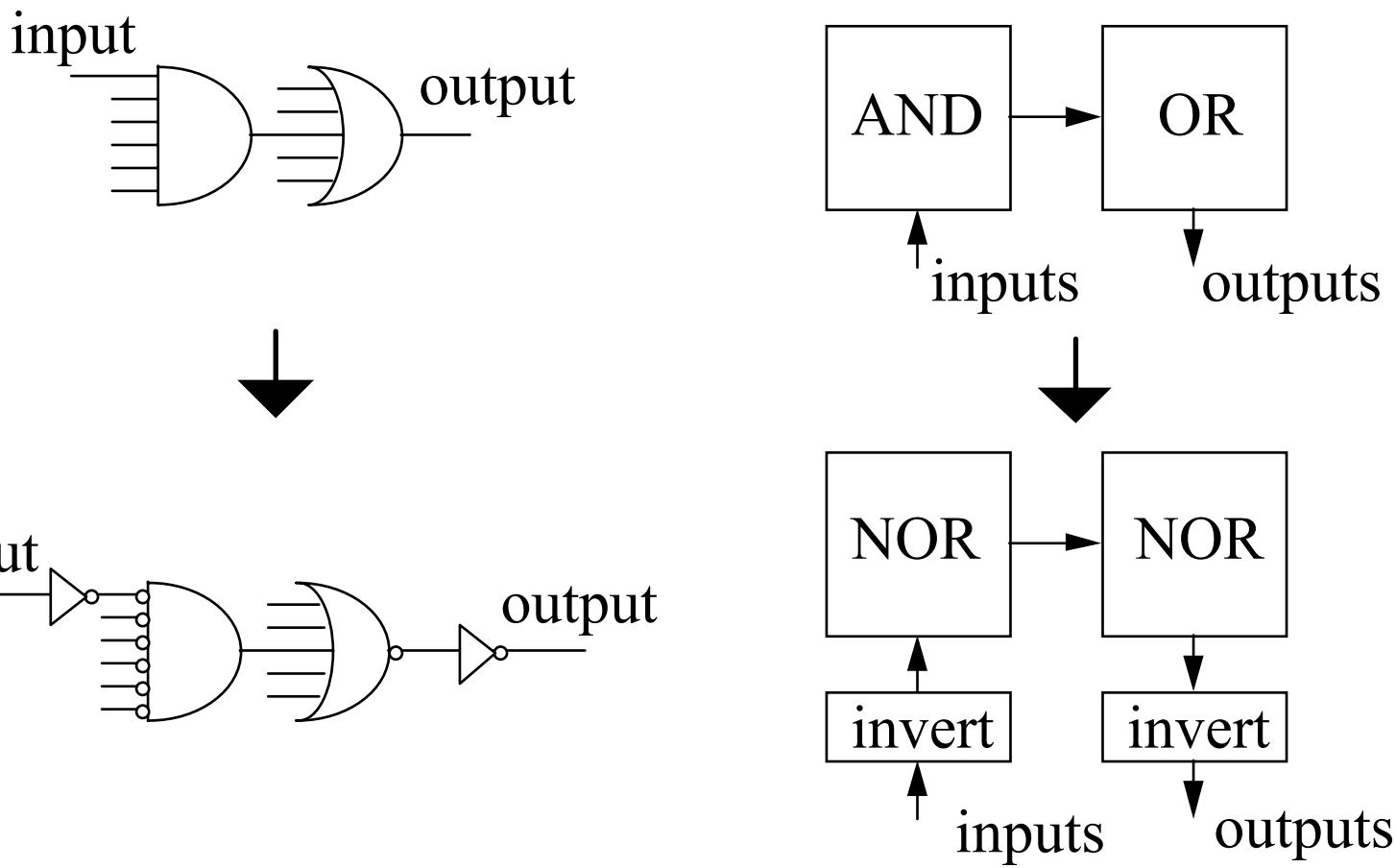
Read Only Memory (ROM)

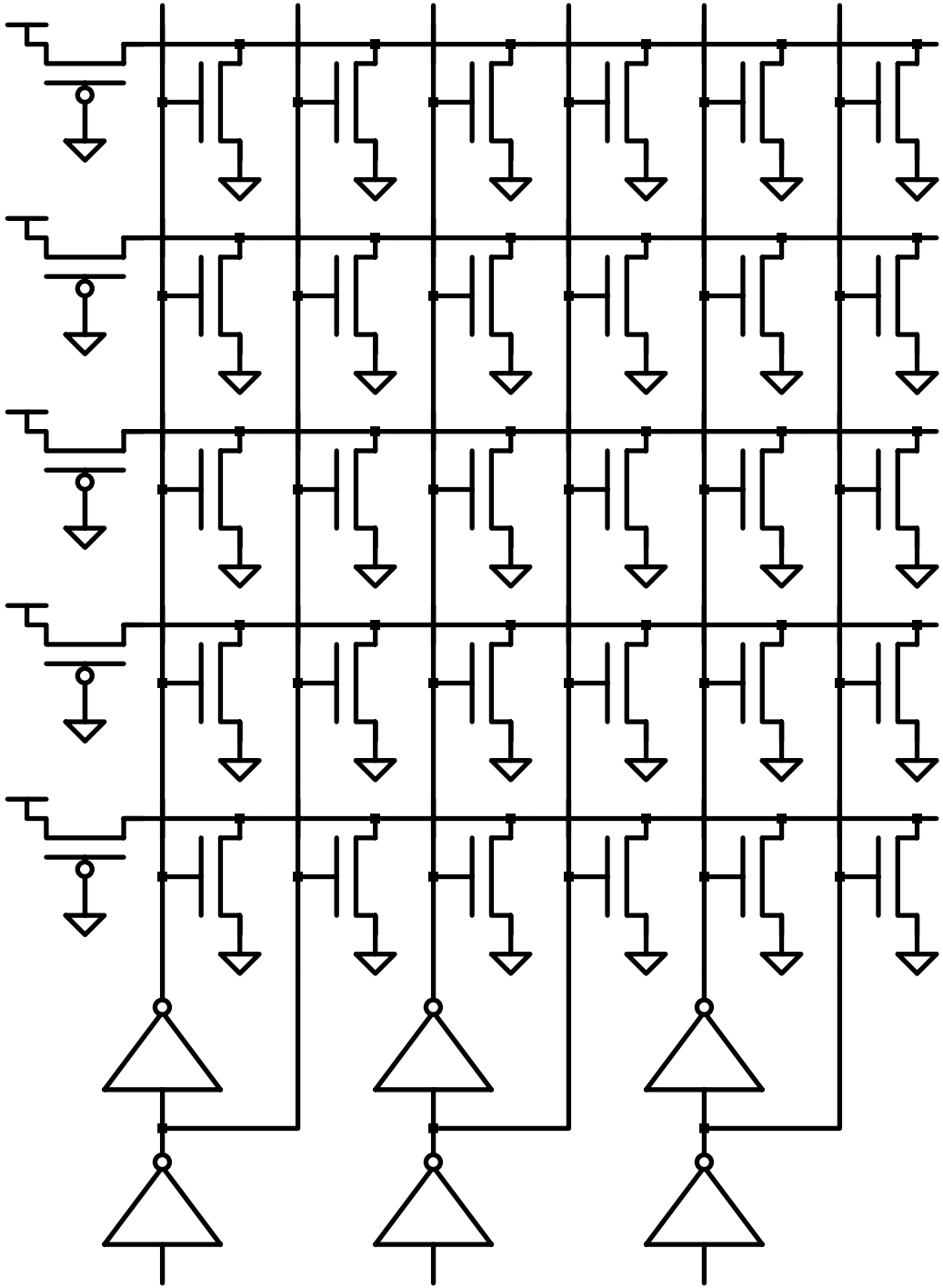


Read Only Memory (ROM)



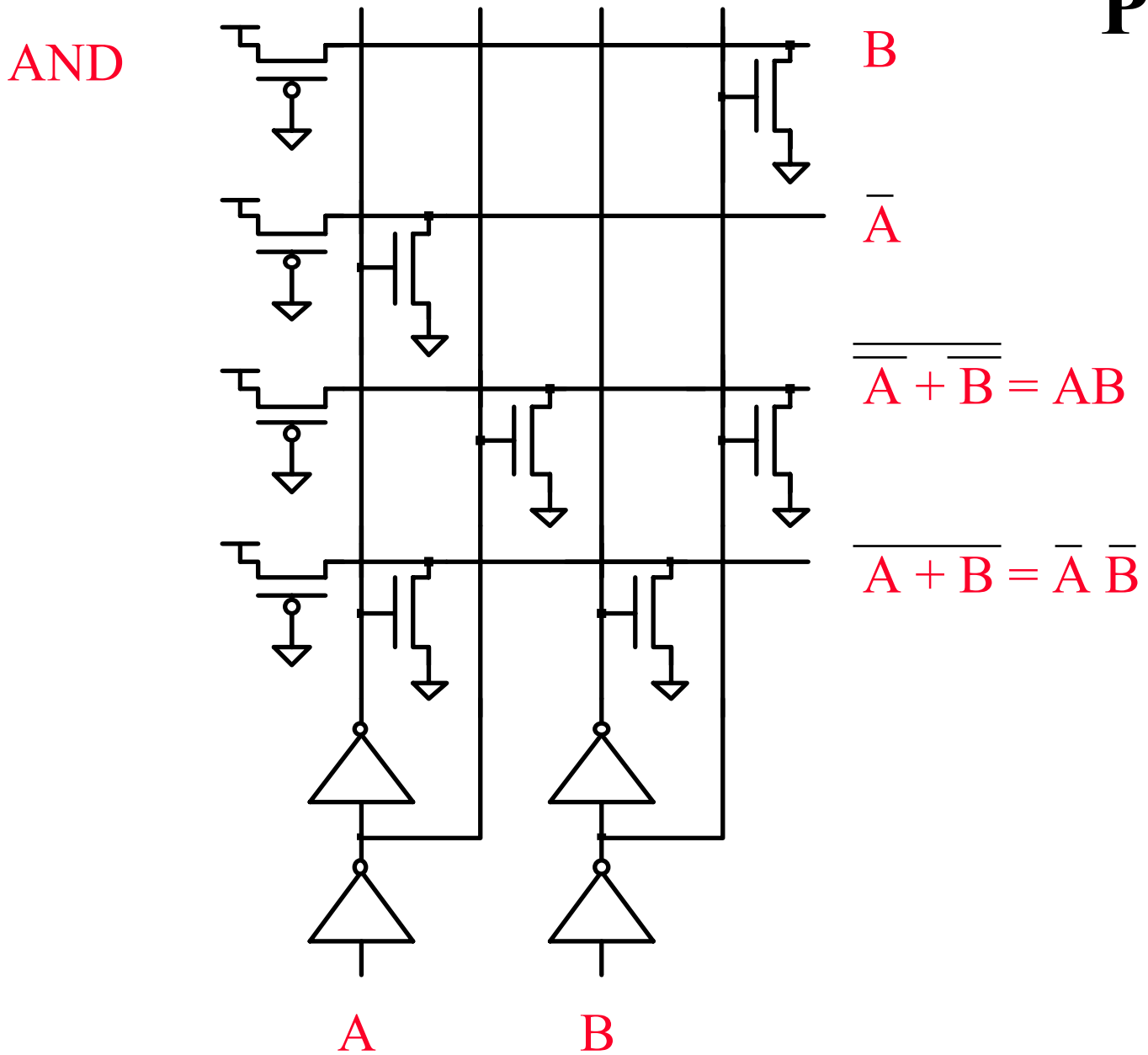
Programmable Logic Array (PLA)



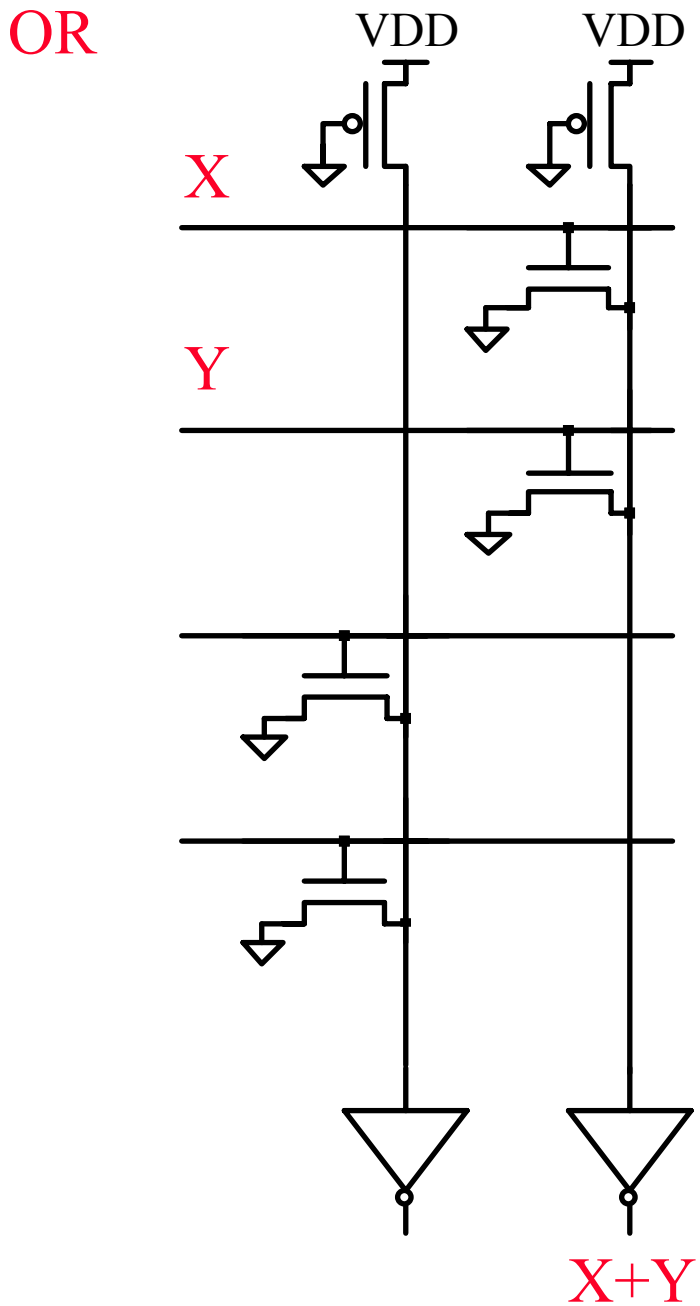


Programmable Logic Array (PLA)

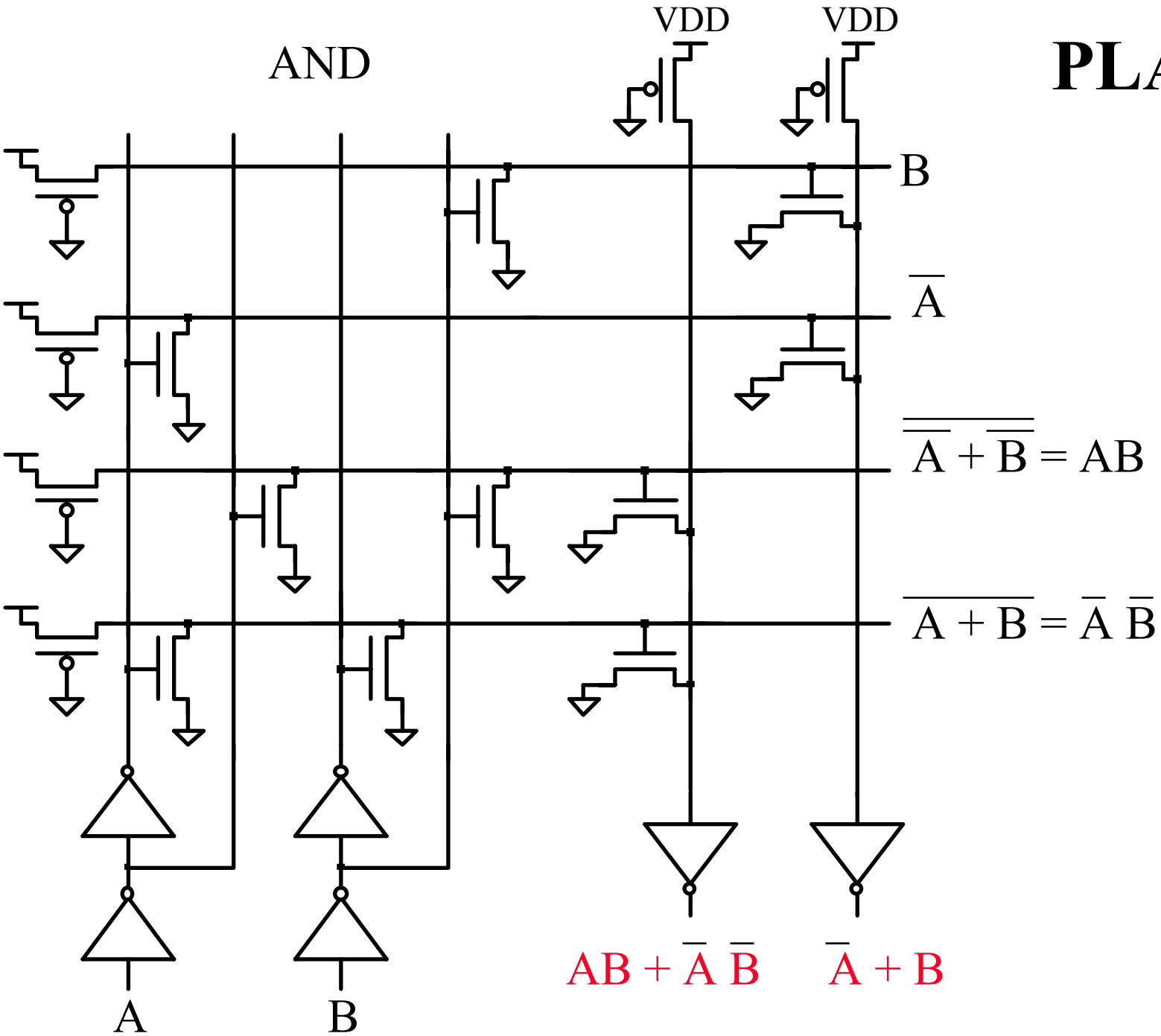
PLA


AND
B
$\bar{A}$
$\overline{\overline{A} + \overline{B}} = AB$
$\overline{A + B} = \bar{A}\,\bar{B}$
A
B

PLA

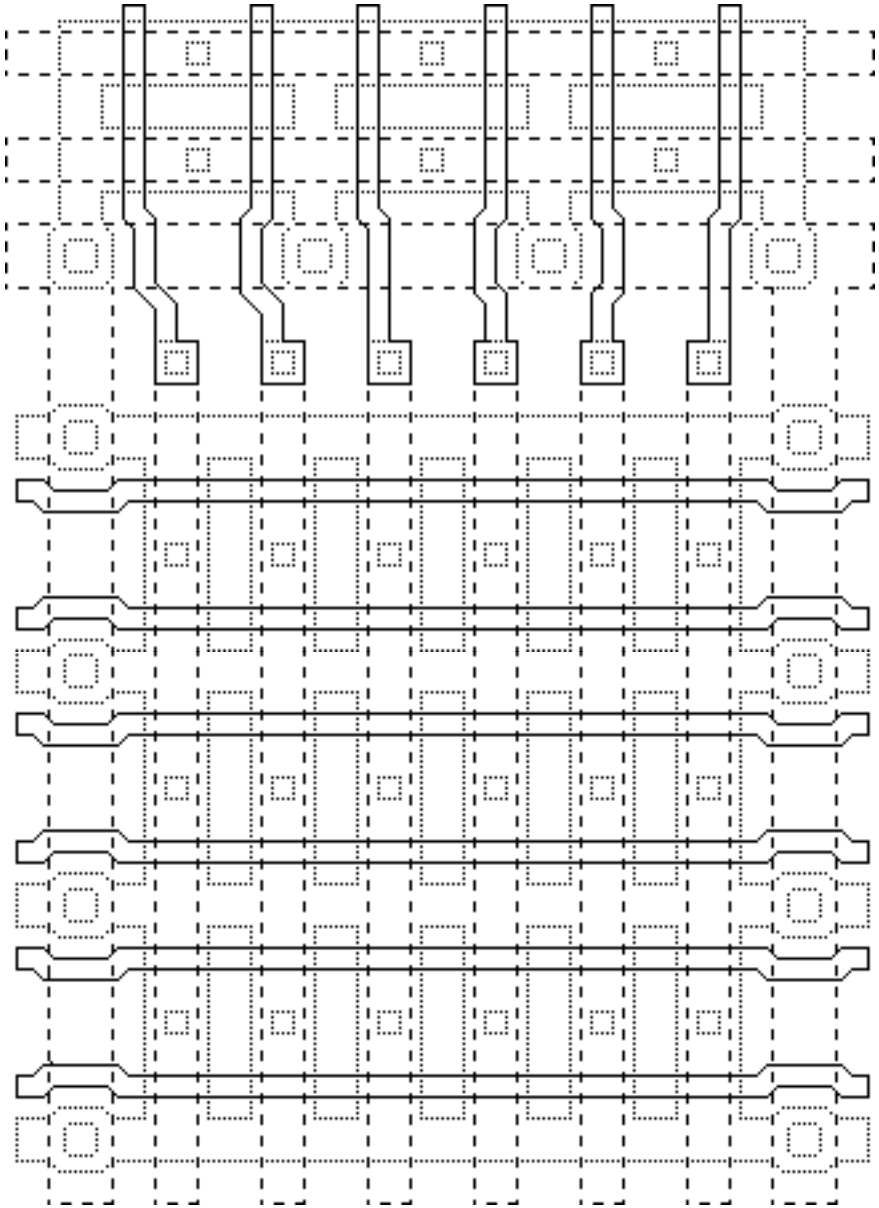


PLA


AND
VDD
VDD
B
$\overline{A}$
$\overline{\overline{A} + \overline{B}} = AB$
$\overline{A + B} = \overline{A}\,\overline{B}$
A
B
$AB + \overline{A}\,\overline{B}$
$\overline{A} + B$

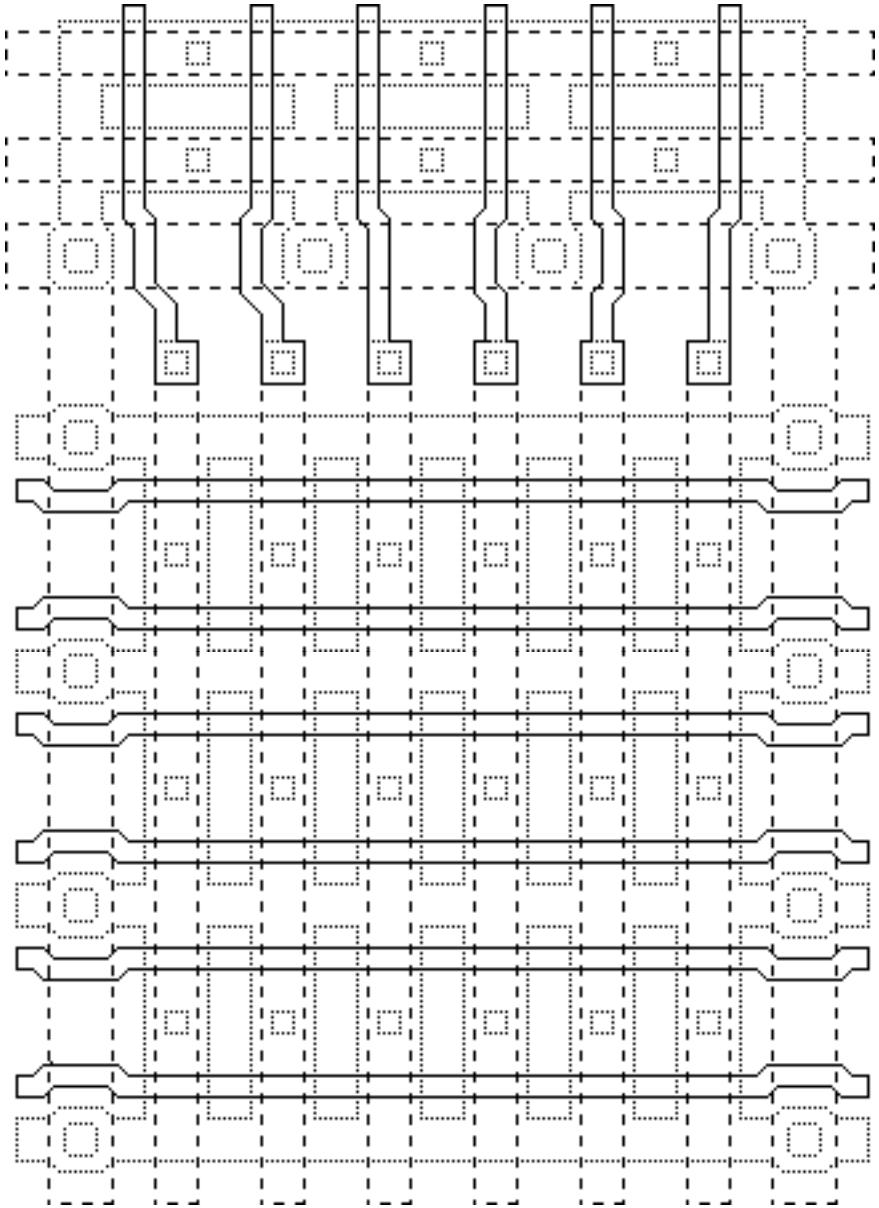
PLA

Active



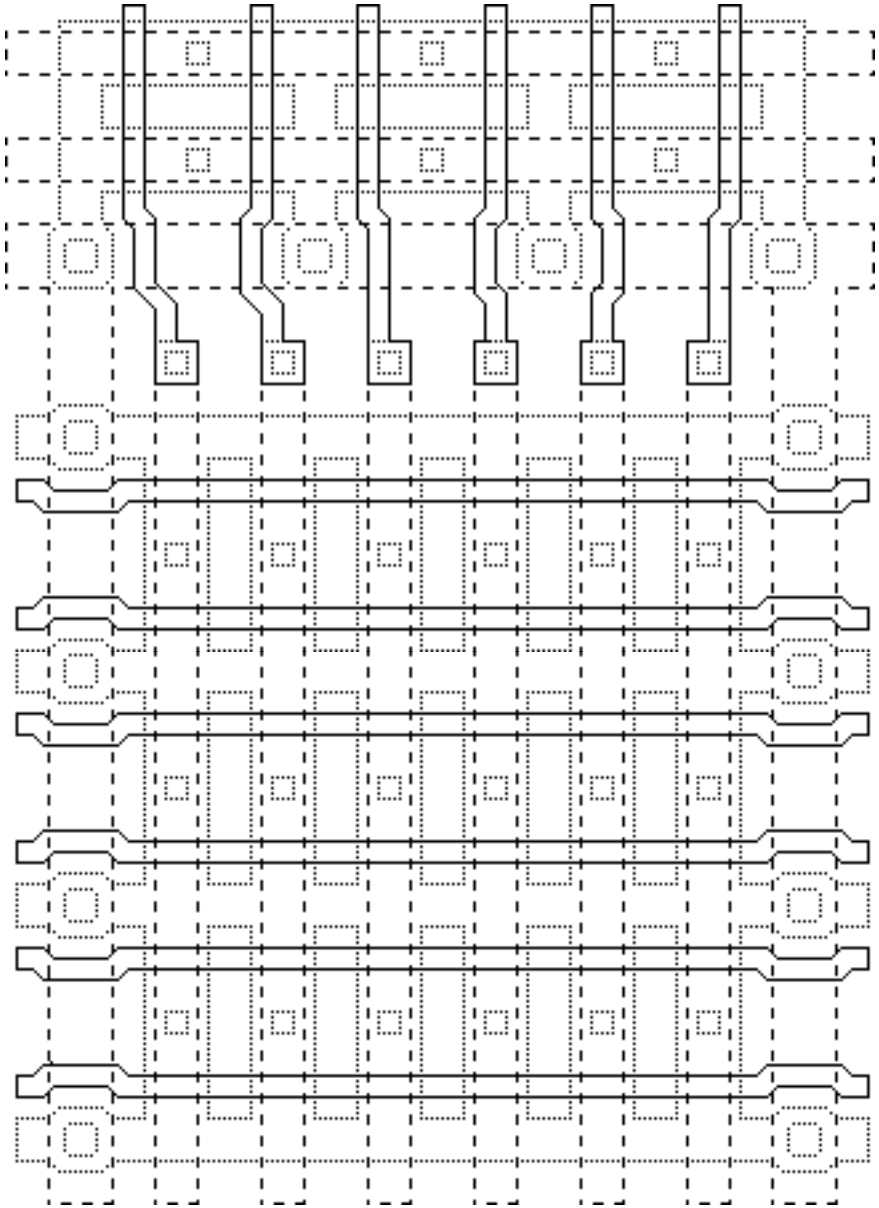
PLA

Poly

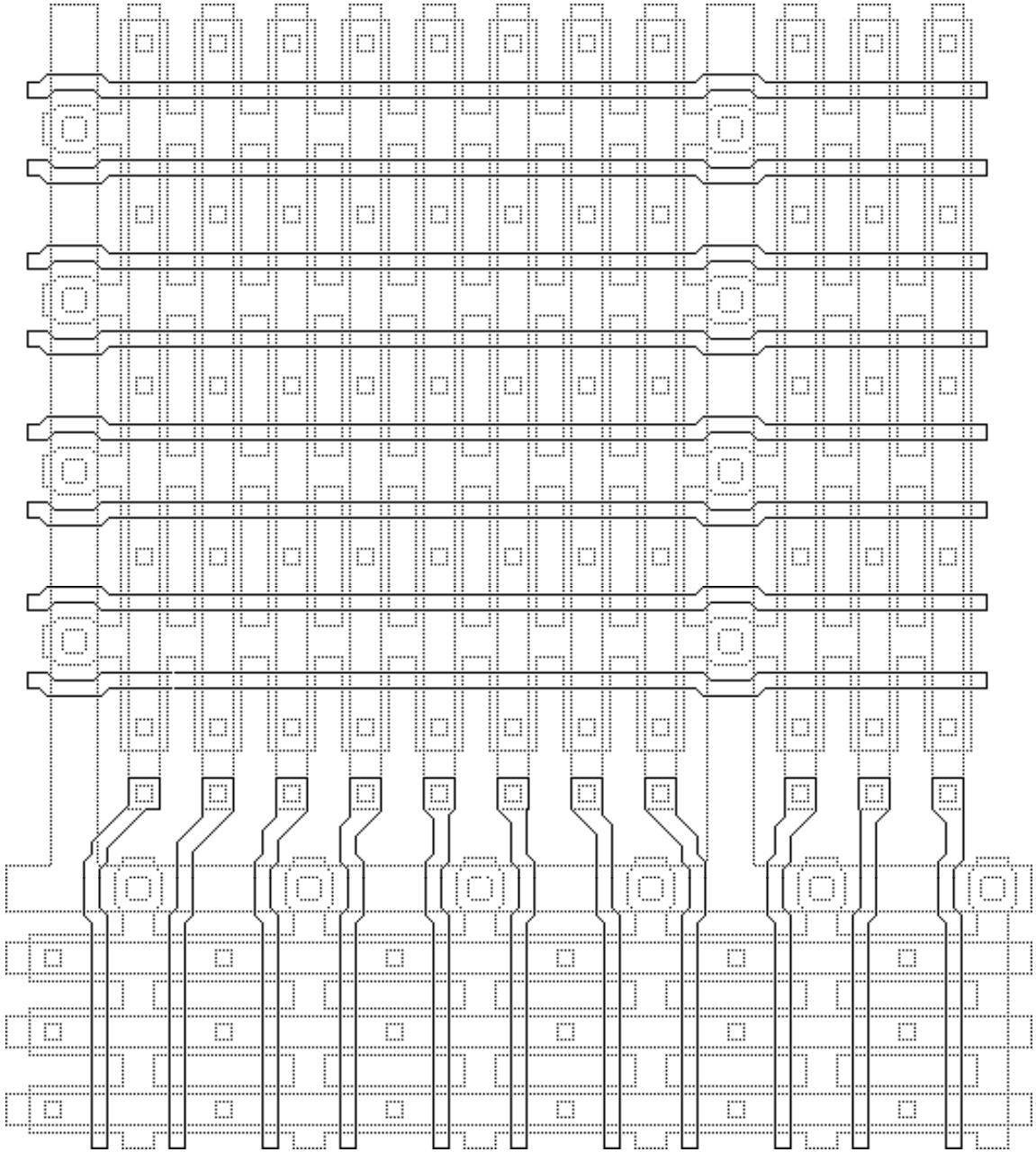


PLA

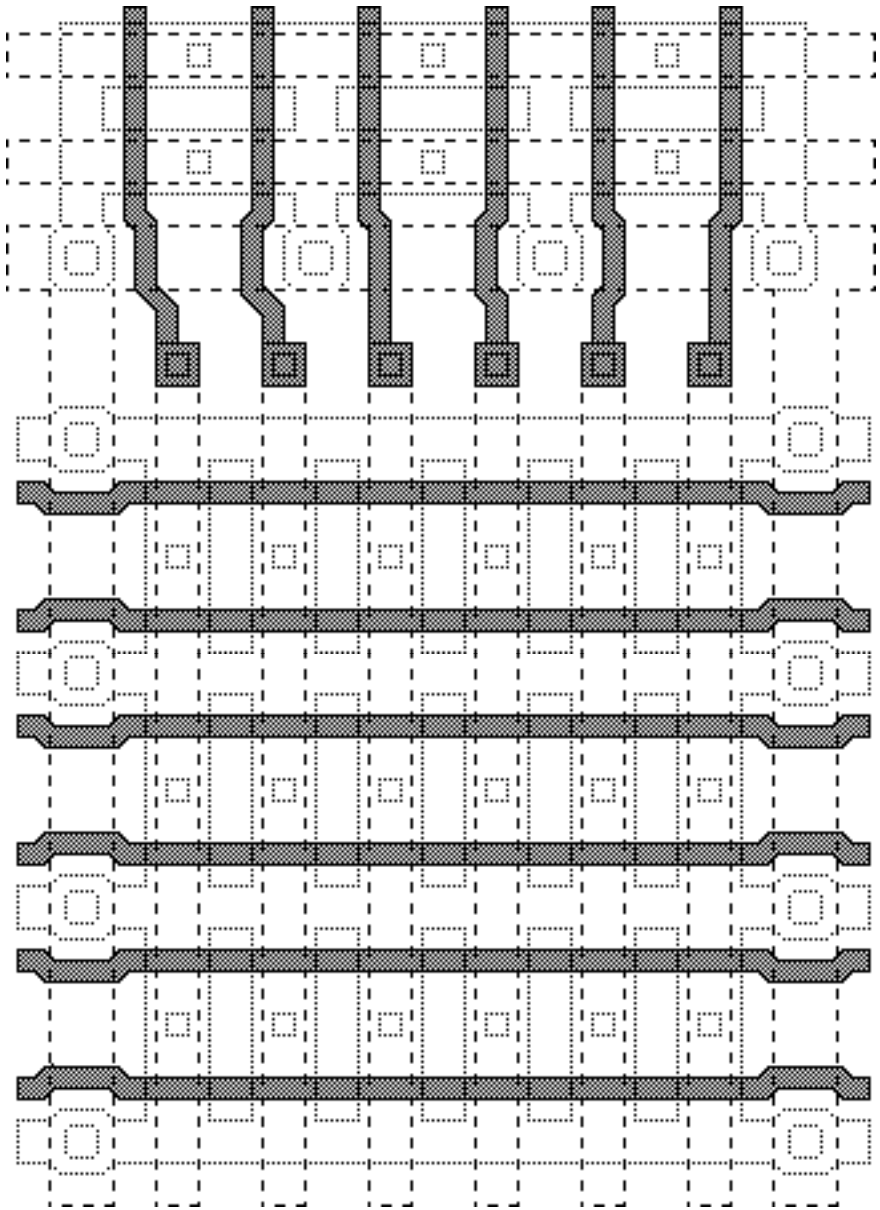
Metal



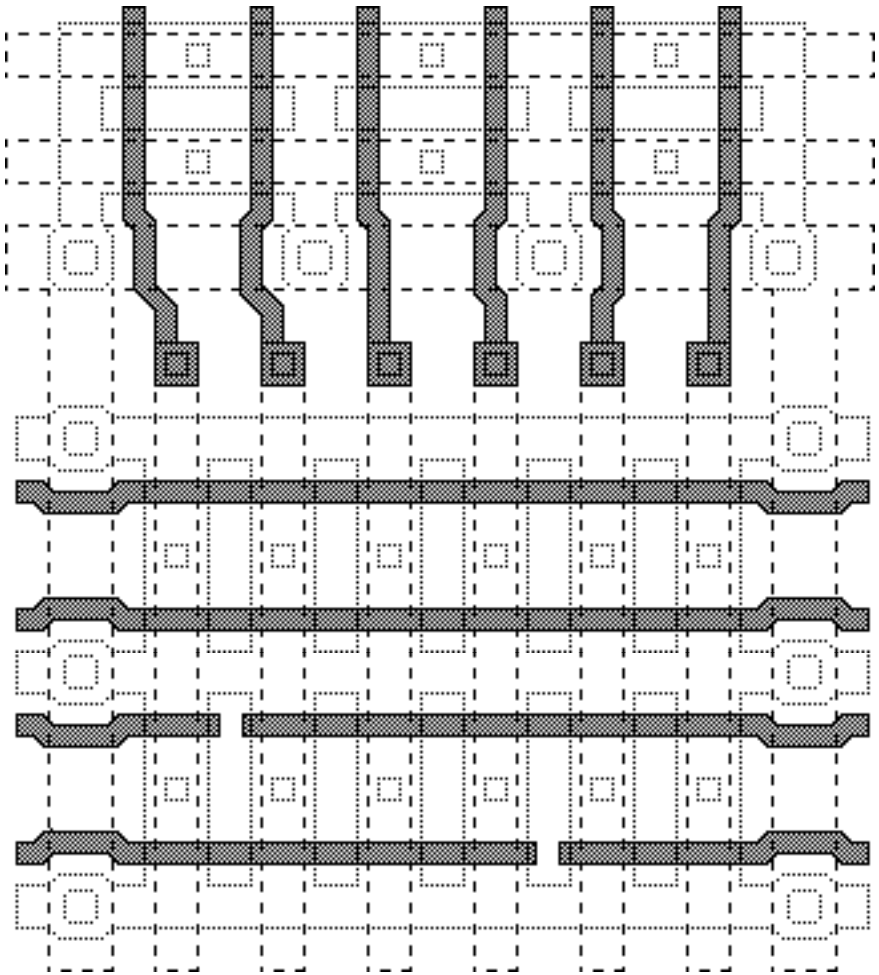
PLA



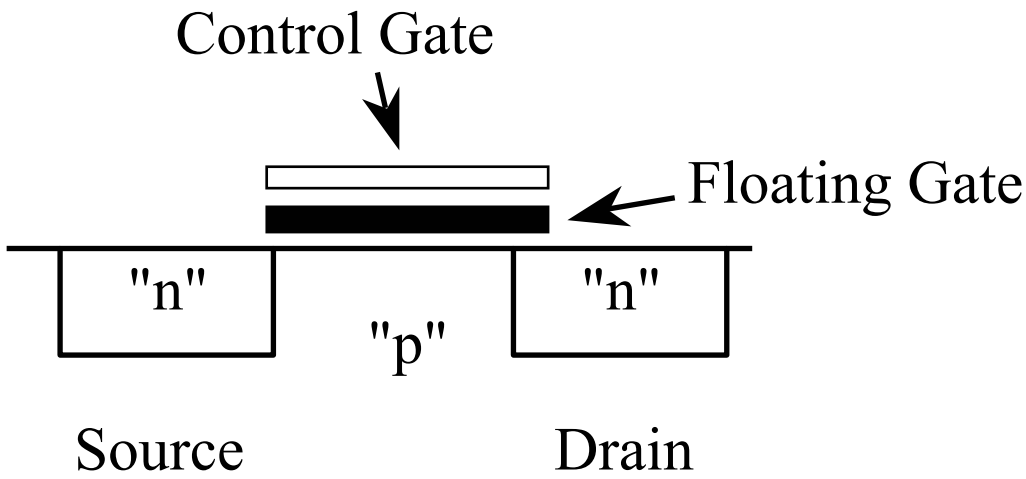
PLA

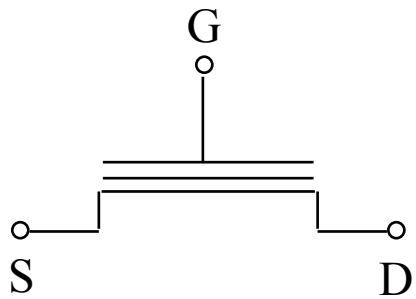


PLA



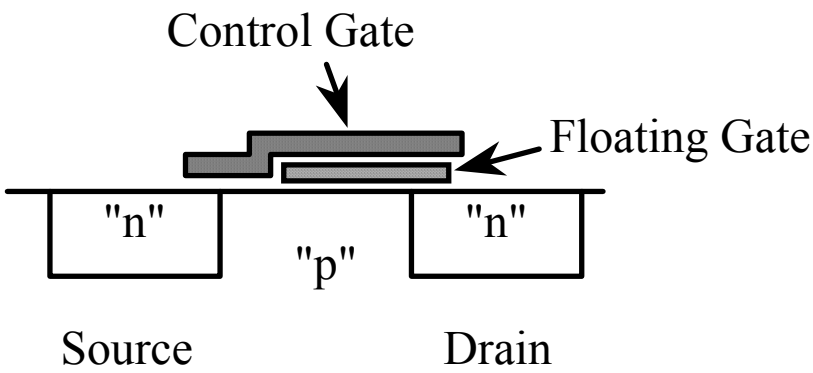
Electrically Programmable

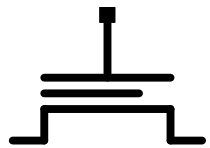




Erase --> Apply UV
--> Low Vt --> Transistor ON when Selected
Program --> CG = High, Drain = High, Source = Low
--> High Vt --> Transistor OFF when Selected

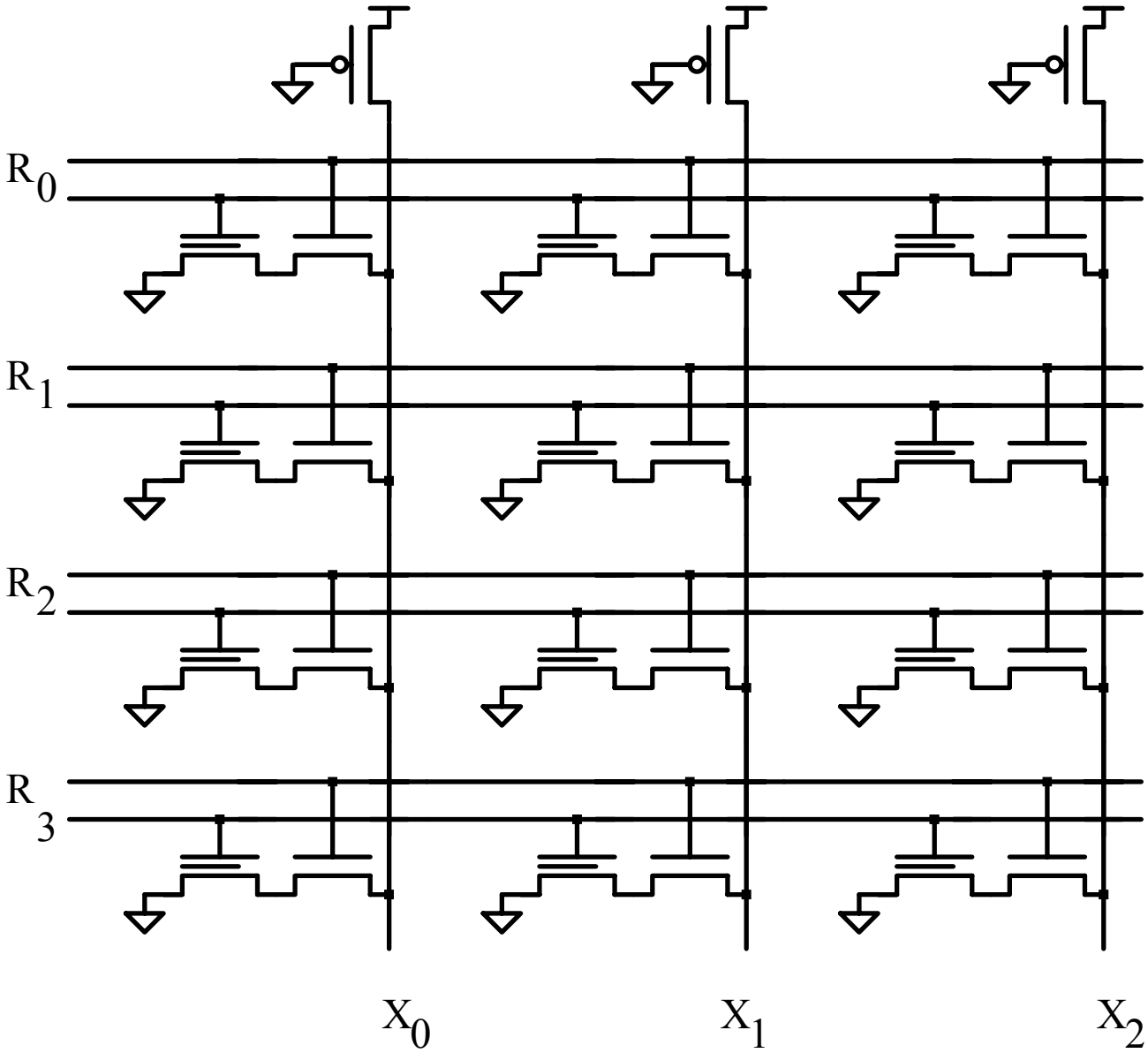
Electrically Programmable





Erase --> CG = High, Drain = Low, Source = Low
--> High Vt --> Transistor OFF when Selected
Program --> CG = Low, Drain = High, Source = Low
--> Low Vt --> Transistor ON when Selected

Electrically Programmable



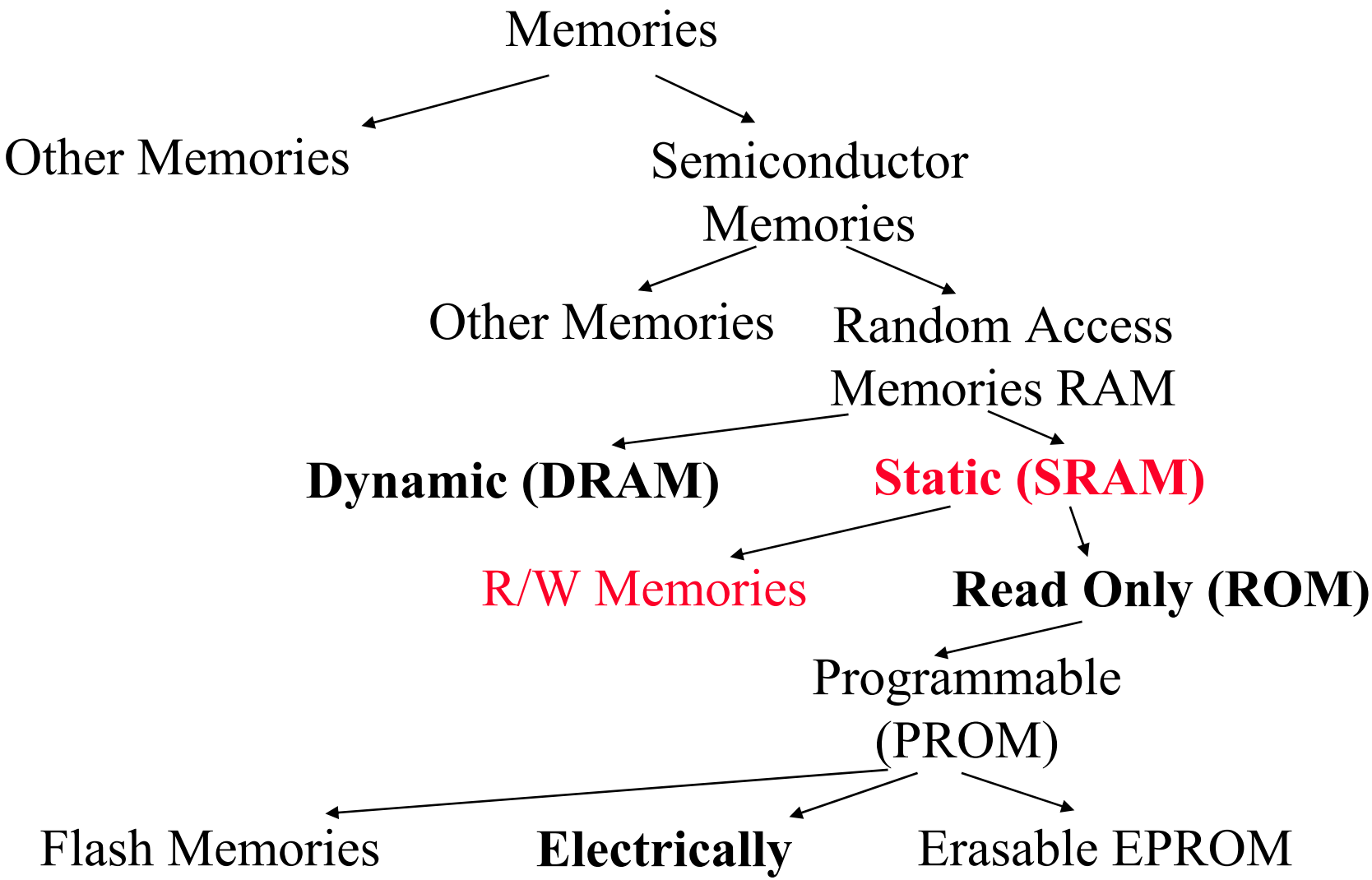
Flash EEPROM

- Same as EEPROMs
- Erased in Single Cycle
- Relatively low number of erase/program cycles

Static Random Access Memories

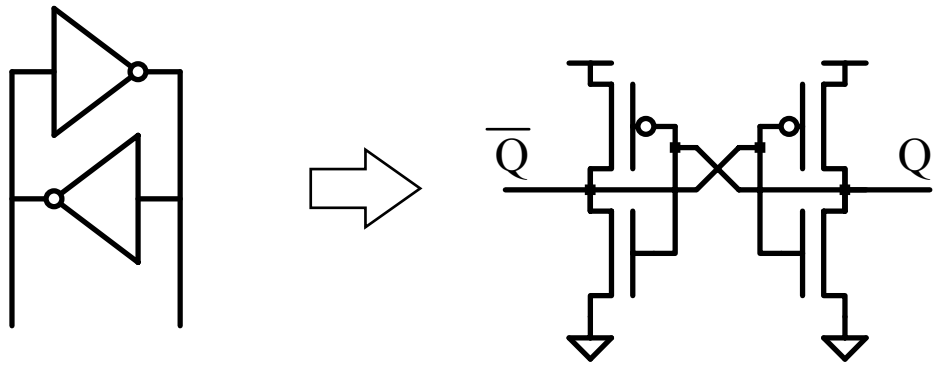
- **Memory Classification**
- **CMOS static memory**
  - **Six transistor memory cell**
  - **Memory architecture**
  - **Decoders**
  - **Read/Write circuitry**

Memory Classification



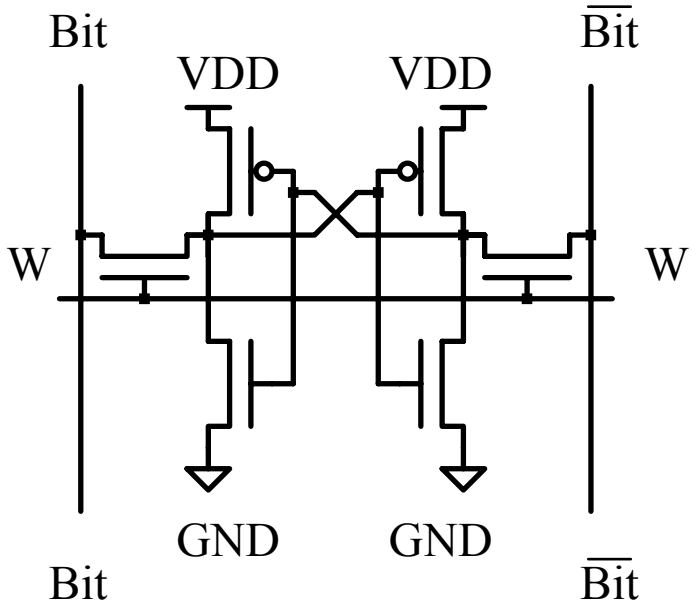
CMOS static memory

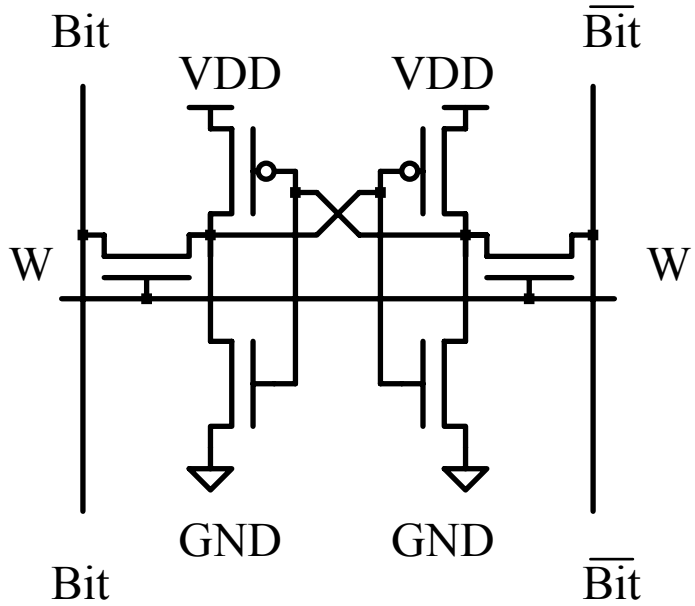
Six transistor memory cell

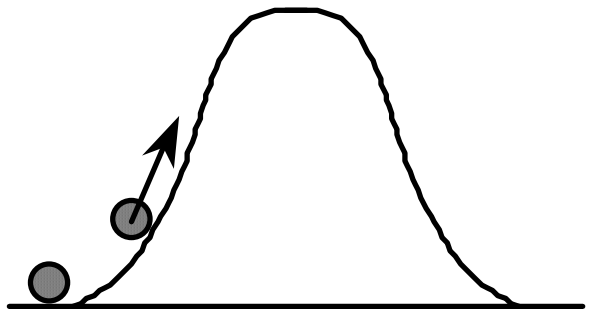


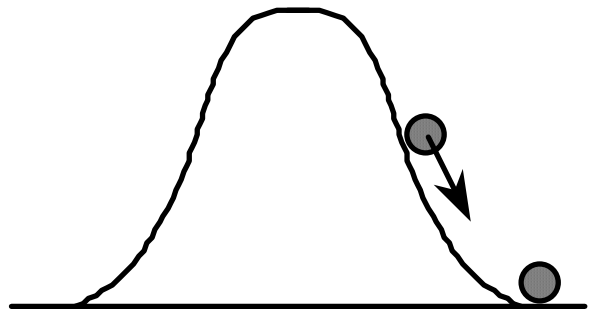
CMOS static memory

Six transistor memory cell



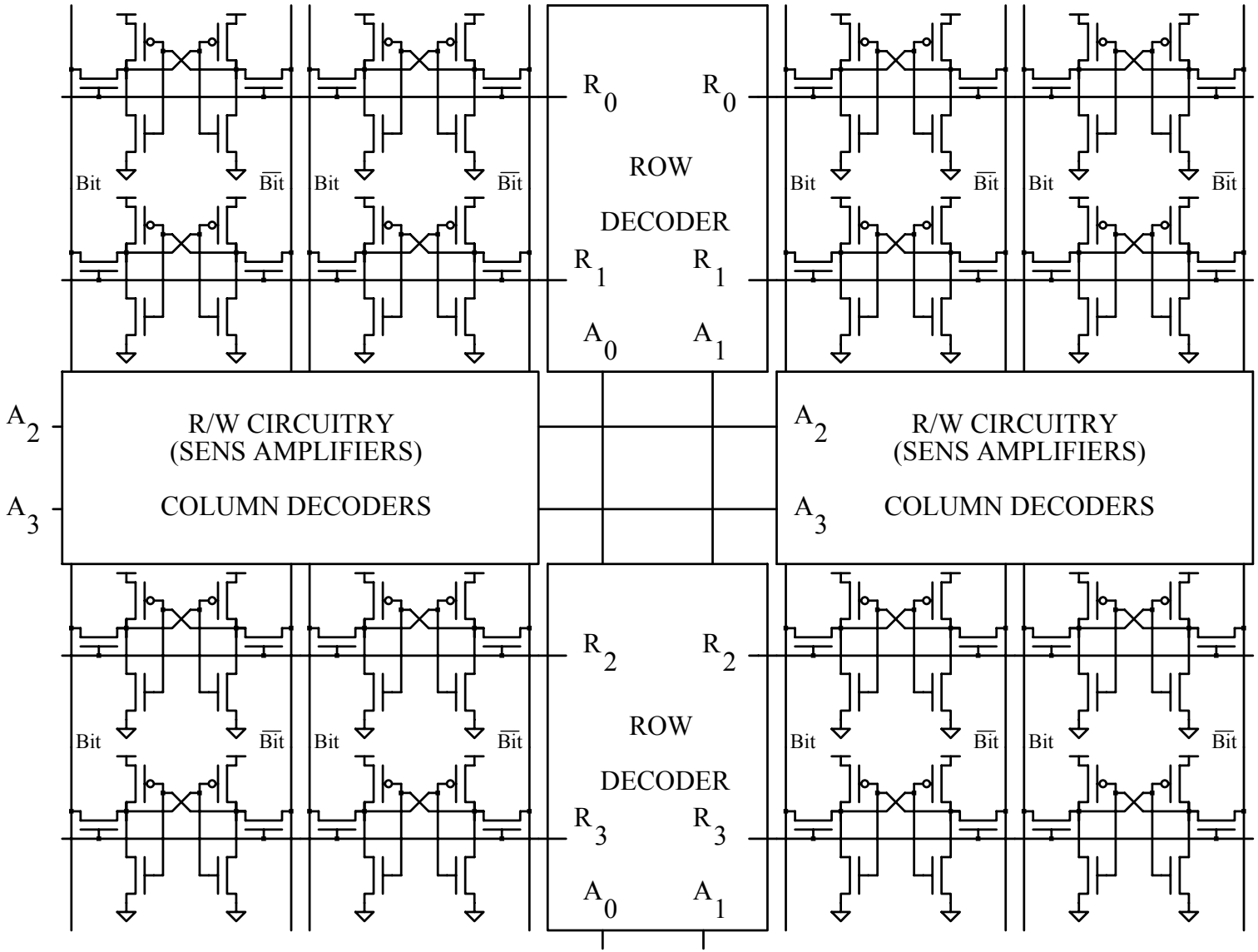






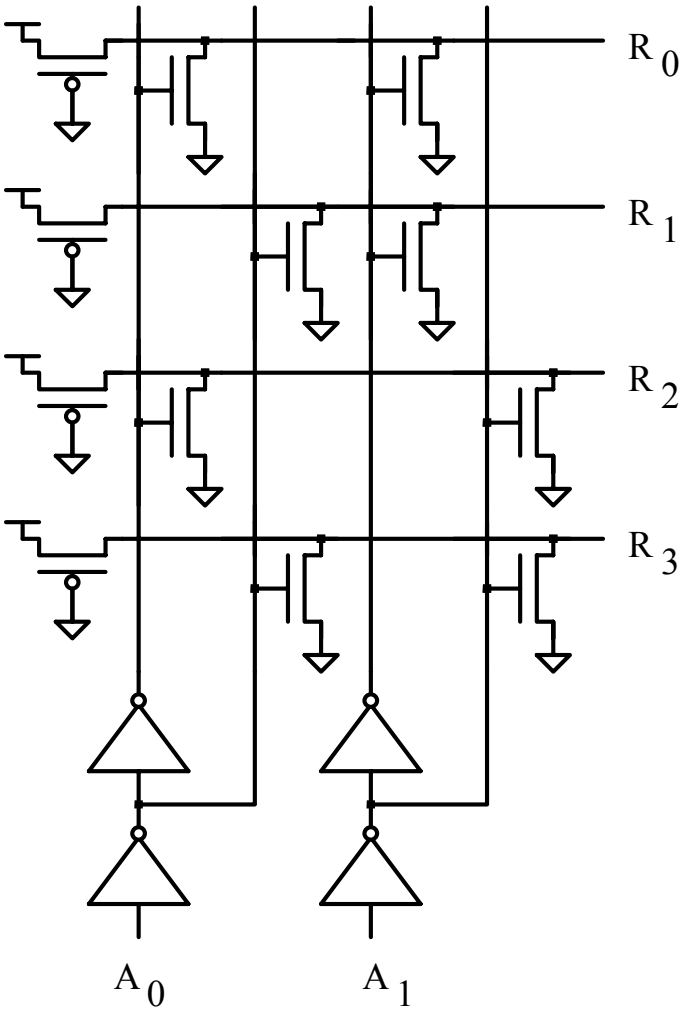
CMOS static memory

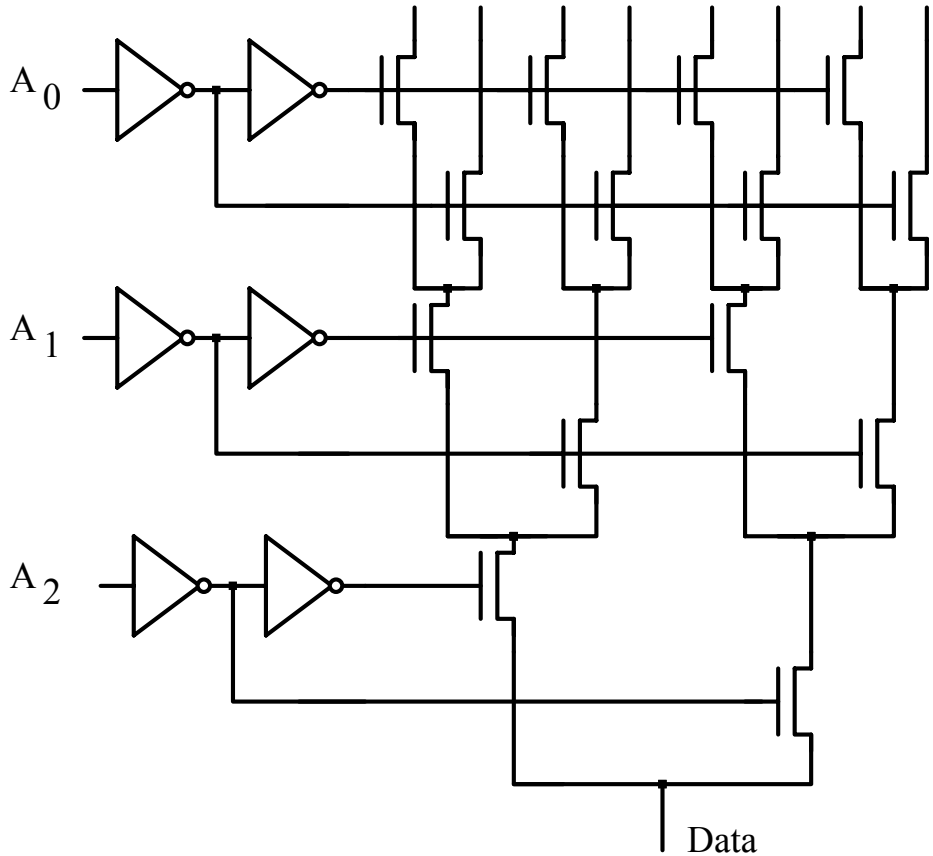
Memory architecture



CMOS static memory

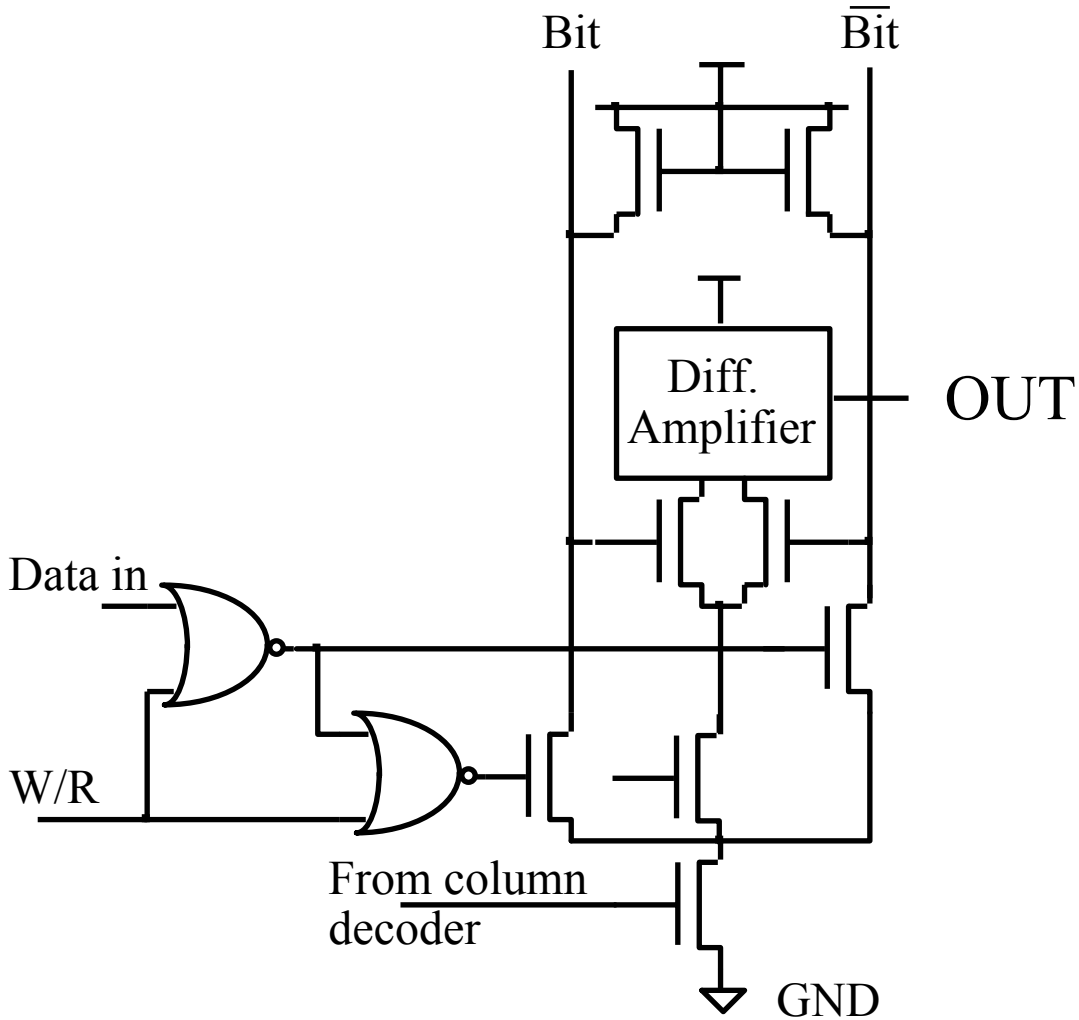
Decoders





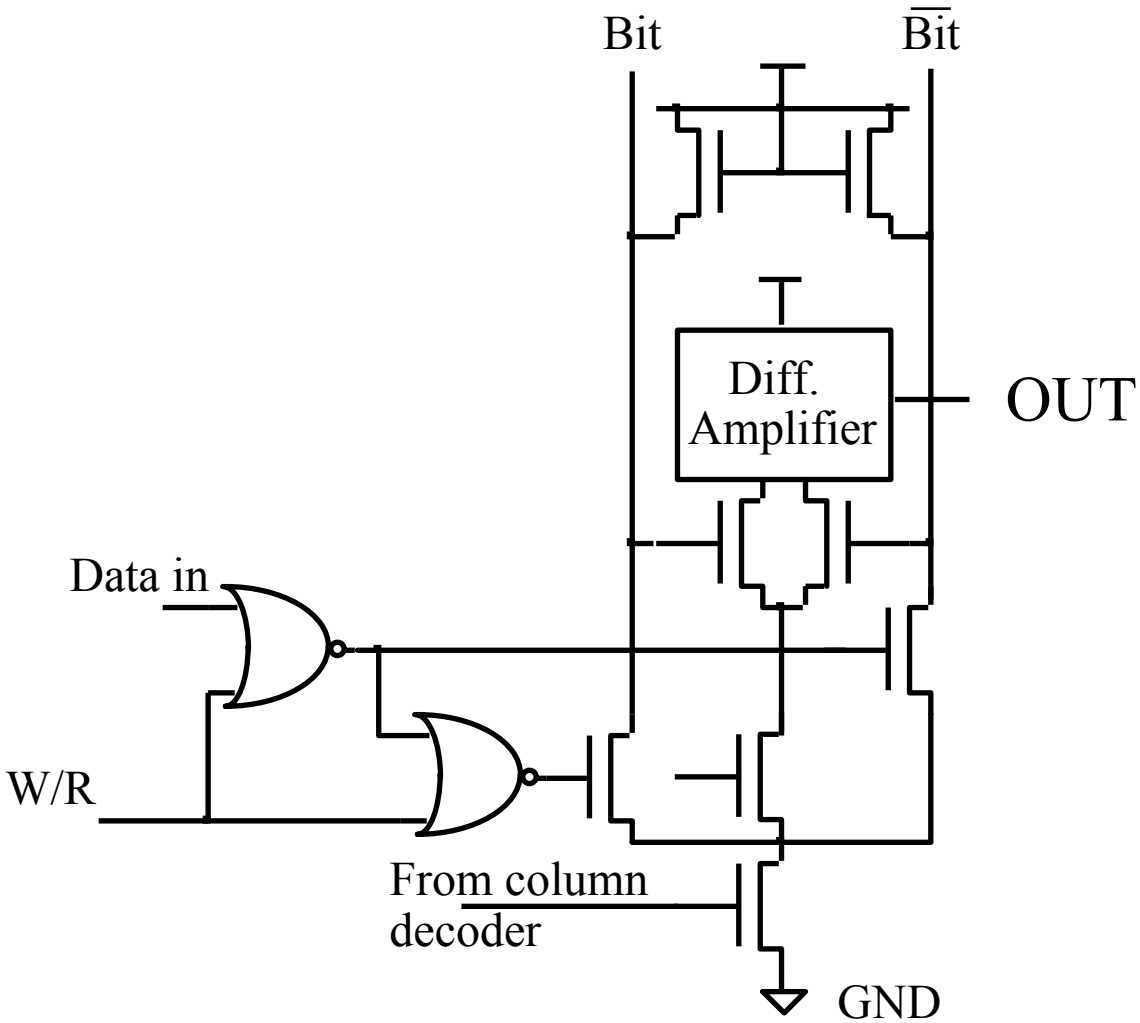
CMOS static memory

Read/Write circuitry



CMOS static memory

Read



CMOS static memory

Write