QUESTION 1) [15 points]
F:Fetch, D:Decode, E:Execute, W:Write

PHASES (INSTRUCTION CYCLES)

Instruction Number	1	2	3	4	5	6	7	8
1	F	D	E					
2		F	D	E				
3			F	D	E			
4				F	D	E		
5					F	D	E	W
6						F	D	E

Total instruction cycles = 8

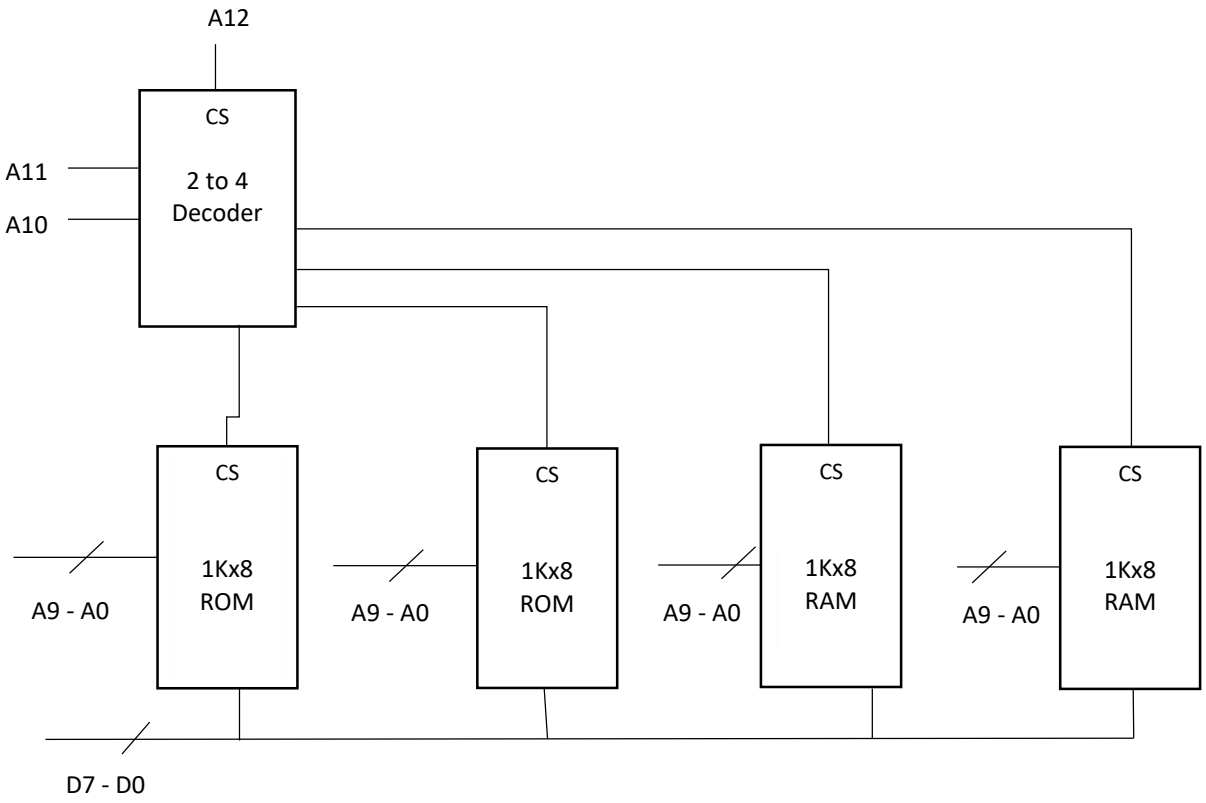
QUESTION 2) [55 points]
a) [25 points] Address bus is 13 bits, total capacity is $= 2^{13} = 2^3 * 2^{10} = 8$ KB
Total used memory = 4 KB

Address Map:

Memory	Module type	Smallest Address	Biggest Address
ROM1	1 K x 8	$0000	$03FF
ROM2	1 K x 8	$0400	$07FF
RAM1	1 K x 8	$0800	$0BFF
RAM2	1 K x 8	$0C00	$0FFF

1K chip ---> 2^{10}
10 address lines are used for location selection. ---> A0-A9
Range: 00 0000 0000 - 11 1111 1111 ---> $000 - $3FF
3 address lines are used for chip selection (decoder). ---> A10-A12

b) [30 points]



QUESTION 3) [30 points]

```
SIZE  EQU  5
EVEN_COUNT  RMB 1
ARRAY   RMB  SIZE
    ORG  ARRAY
    DAT  10,3,8,6,7

START
   STA 0, EVEN_COUNT ;Reset even counter to 0.
   LDA  SK, ARRAY         ;Get beginning address of array
   LDA  B, 0              ;Loop counter

* Loop through the array.
DEVAM1
   LDA  A, <SK+0>         ;Get next number from array
   LSR  A           ; Logical Shift Right (Get rightmost bit to Carry flag)
   BNC  EVEN    ; Branch if Not Carry (If carry flag is 0, data is even)
   BRA DEVAM2    ;Goto label

EVEN
   INC  <EVEN_COUNT>  ;Increment count of even numbers
DEVAM2
    INC  SK          ; Increment SK
    INC  B           ; Increment loop counter
    CMP B, SIZE  ; Compare with array size
    BLT  DEVAM1             ; Goto loop if CD is less than size

    INT
```