30/03/2015 - W9

EHB 322E Digital Electronic Circuits

SPRING 2015

Pass-Transistor Logic (PTL)

Goals 1) No resistors

2) No static power

3) Using fewer transistors compared to CMOS

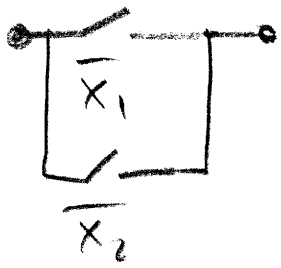
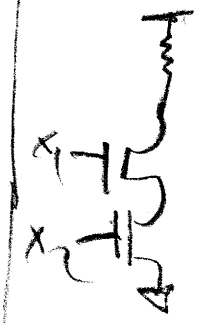
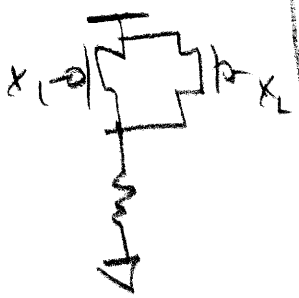
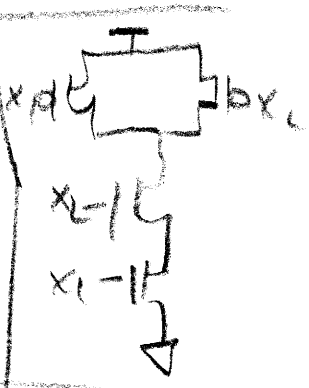
Target function: f with a linked count n factored form

Implementation / f	Pseudo NMOS	Pseudo PMOS	CMOS	PTL
Area	n NMOS transistors + 1 load (resistor)	n PMOS transistors + 1 load (resistor)	$2n$ transistors (n NMOS, n PMOS)	$\approx n$ transistors best
Power	$SP \geq 0$	$SP \geq 0$	$SP = 0$ best	$SP = 0$ best
Signal quality and integration	average	average	best	restoration is needed worst

Ex

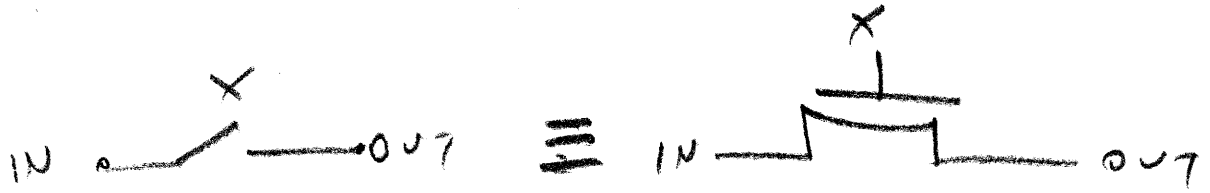
$f = \overline{x_1 x_2} = \overline{x_1} + \overline{x_2}$ (NAND)

x_1	x_2	f
0	0	1
0	1	1
1	0	1
1	1	0

Switching network	Pseudo NMOS	Pseudo PMOS	CMOS
			

How about RTL

Main idea is using a single transistor for a switch



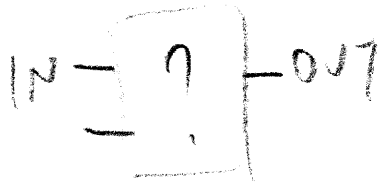
$X = 0$ (0V) — OUT is not known (floating)

$X = 1$ (V_{DD}) — OUT = IN

$X = 0$ — OUT is floating

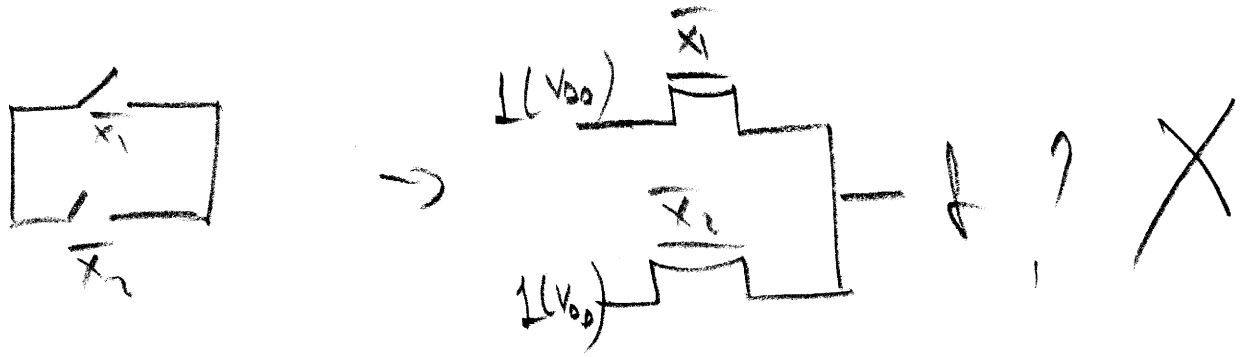
$X = 1$ — OUT ≅ IN ($V_D = 0$)

How to implement $f = \overline{x_1} + \overline{x_2}$



$f = \overline{x_1} + \overline{x_2}$

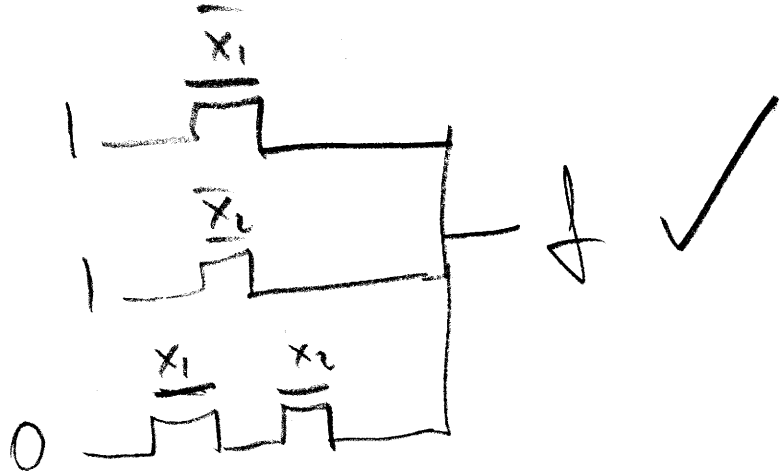
1) Replacing each switch with a transistor



x_1	x_2	f	
0	0	1	✓
0	1	1	✓
1	0	1	✓
1	1	0	floating X

- output should not be open (floating)

2)

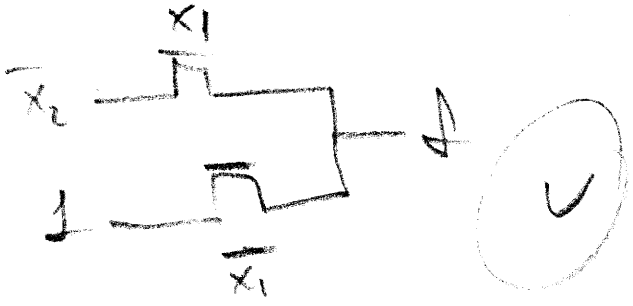


3.) $f = \overline{x_1} + \overline{x_2}$

$= \overline{x_1}(x_2 + \overline{x_2}) + \overline{x_2}(x_1 + \overline{x_1})$

$= \overline{x_1}x_2 + \overline{x_1}\,\overline{x_2} + x_1\overline{x_2} + \overline{x_1}\,\overline{x_2}$

$f = x_1\overline{x_2} + \overline{x_1}$ (Shannon's expansion)



x_1	x_2	f	
0	0	1	✓
0	1	1	✓
1	0	1	✓
1	1	0	✓

2 versions

How to design a PTL circuit

Rule: Output should always be connected to either GND or VDD

(0) (1)

- Output should not be open
- Output should not be connected to both VDD and GND

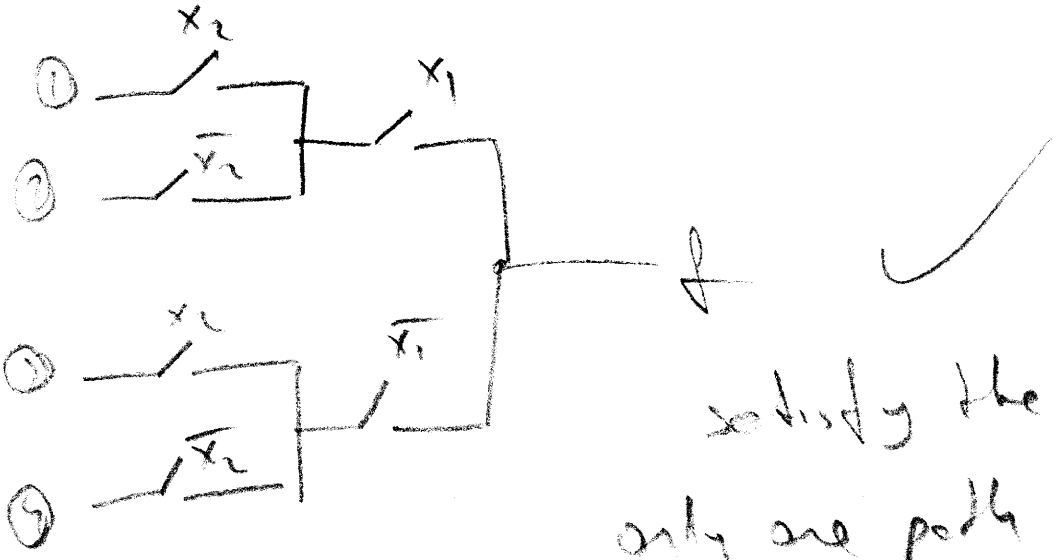
out is open if $x_1 = 0$ and $x_2 = 0$

out is connected to 1 and 0 if $x_1 = 1$ and $x_2 = 1$

How to satisfy the rule?

With Shannon's expansion:

$$f = x_1\left(x_2(\text{①}) + \bar{x}_2(\text{②})\right) + \bar{x}_1\left(x_2(\text{③}) + \bar{x}_2(\text{④})\right)$$



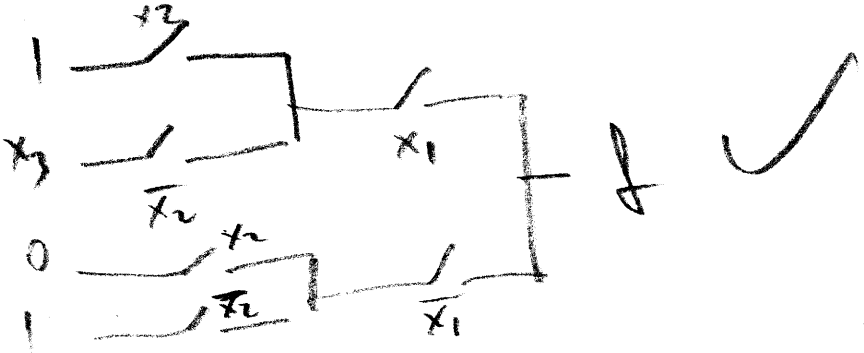
satisfy the rule

only one path exists between input and output.

ex $f = x_1 x_2 \bar{x}_3 + x_1 x_3 + \bar{x}_1 \bar{x}_2$ ordering $x_1 - x_2 - x_3$

$= x_1(x_2\bar{x}_3 + x_3) + \bar{x}_1(\bar{x}_2)$

$f = x_1\left(x_2\bar{x}_3 + x_3(x_2+\bar{x}_2)\right) + \bar{x}_1(x_2 \cdot 0 + \bar{x}_2 \cdot 1)$

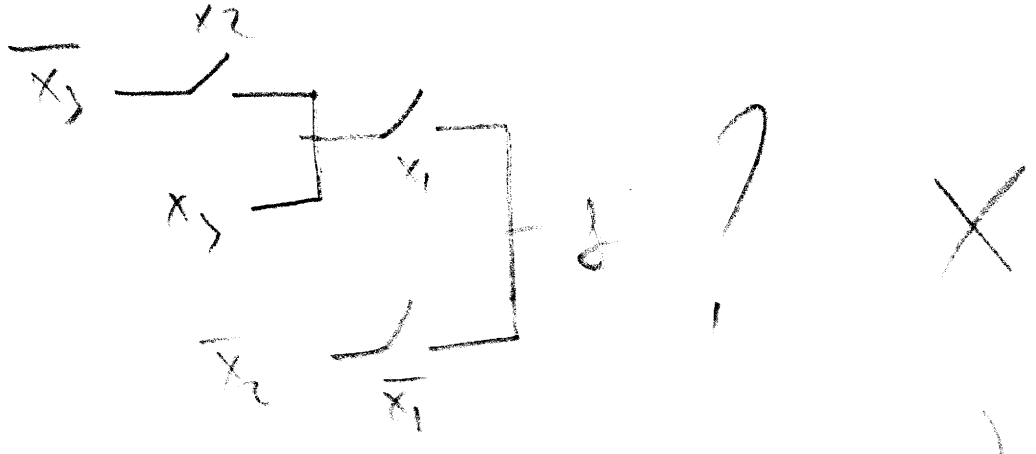


not the optimum solution in terms of the # of switches

How to find the optimum sol. (6)

$$f = x_1(x_2\bar{x}_3 + x_3) + \bar{x}_1(\bar{x}_2)$$

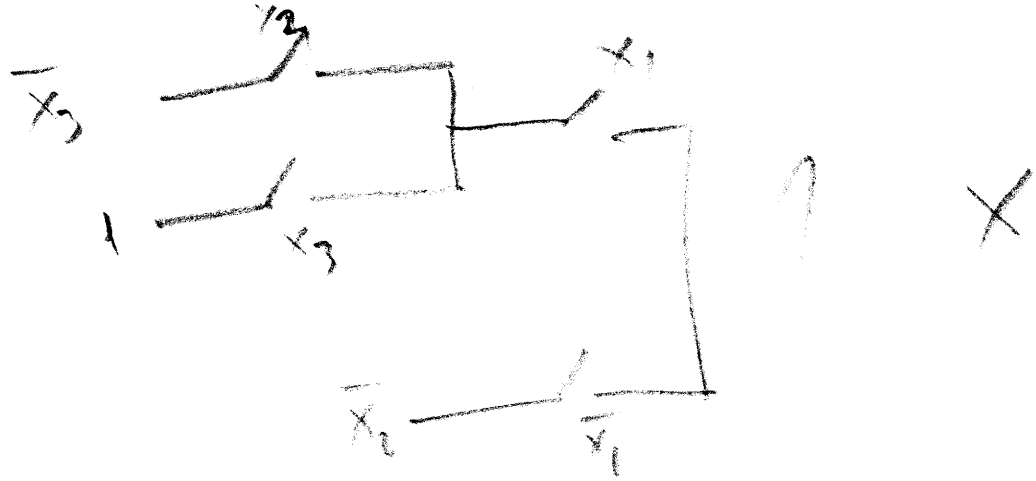
1)



$(x_1 = 1,\ x_2 = 1,\ x_3 = (0 \text{ or } 1))$

makes the output connected to both 0 and 1
- static power consumption is not zero

2)



$(x_1 = 1,\ x_2 = 0,\ x_3 \geq 0)$

makes the output open

3) $f = x_1(x_2\bar{x}_3 + x_3) + \bar{x}_1(\bar{x}_2)$

ordering $x_1 - x_2 - x_3$

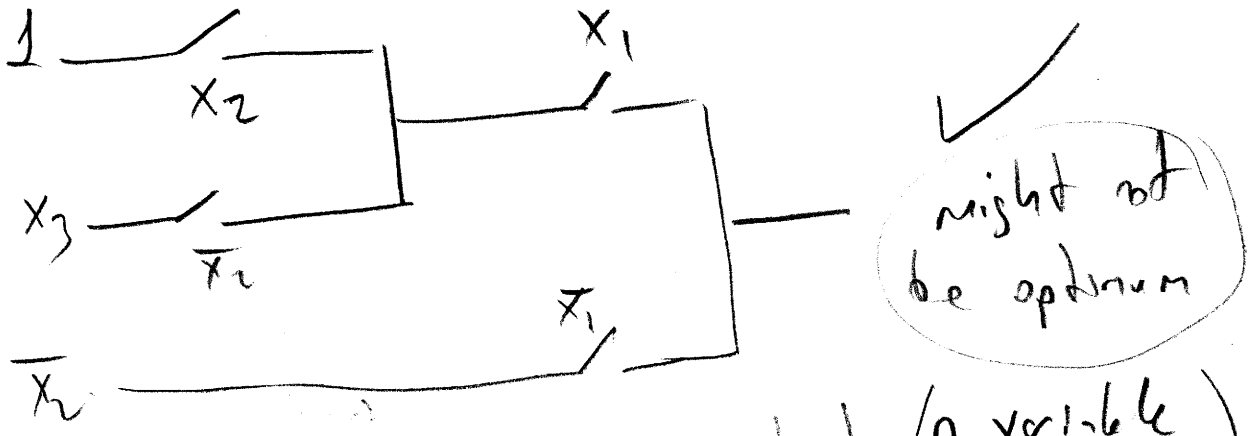
$f = x_1(x_2\bar{x}_3 + x_3) + \bar{x}_1(\bar{x}_2)$ → done

↙ no x_2 not done

$f = x_1(x_2\bar{x}_3 + x_2x_3 + \bar{x}_2x_3) + \bar{x}_1(\bar{x}_2)$

$= x_1(x_2 1 + \bar{x}_2x_3) + \bar{x}_1(\bar{x}_2)$

done done

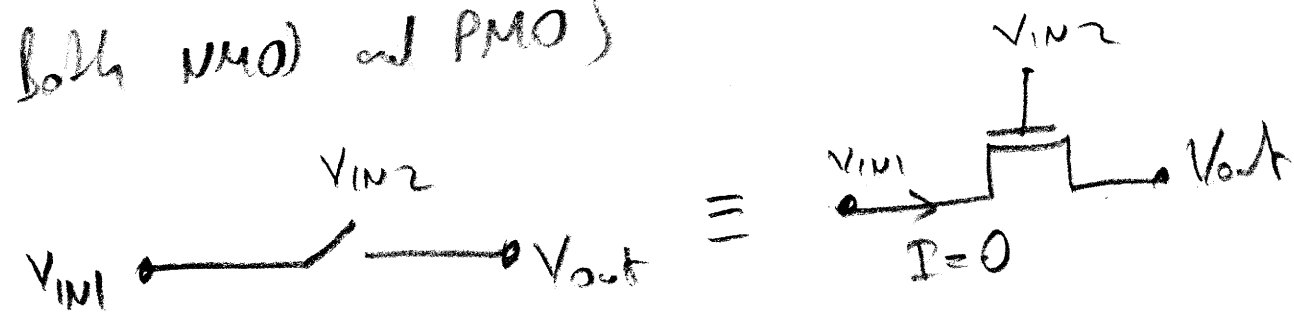


Note that ordering is important (n variable → n! orderings)

- Ordering is important
- Shannon's expansion does not necessarily result in an optimum solution.
- Finding an optimum solution is an NP complete problem in circuit complexity.

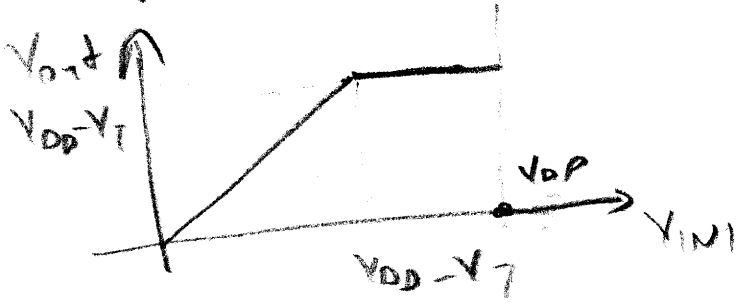
How to implement switches in PTL

1. NMOS
2. PMOS
3. Both NMOS and PMOS

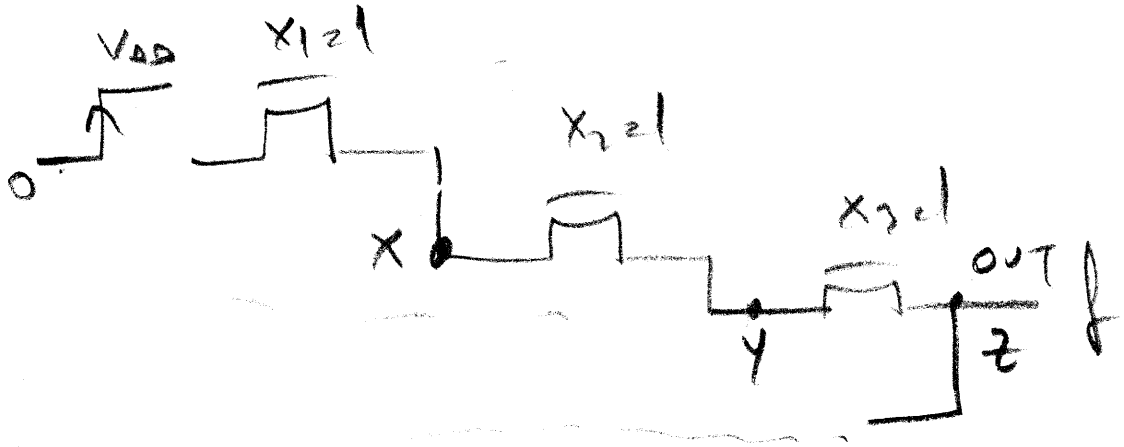
4. 

If $V_{IN2}=0$ then open circuit

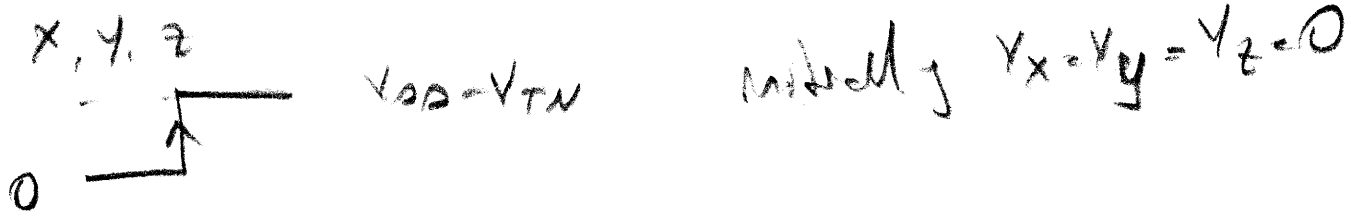
If $V_{IN2}=1$ then wire $I=0$



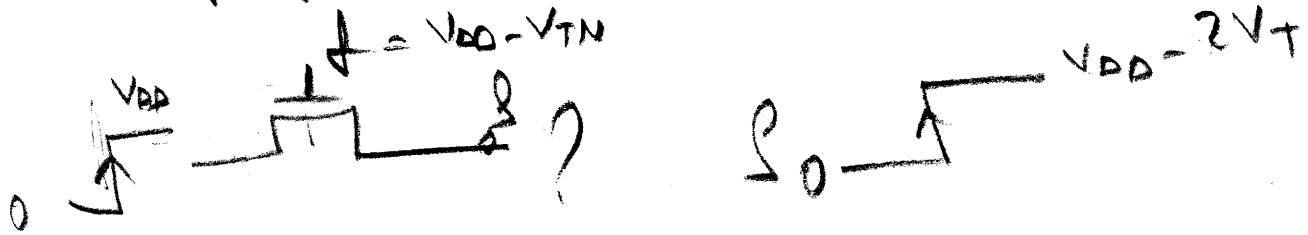
Ex



Draw X, Y, and Z (out)



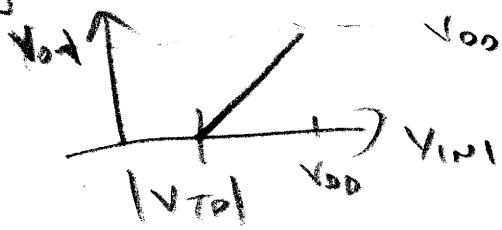
If f used as input



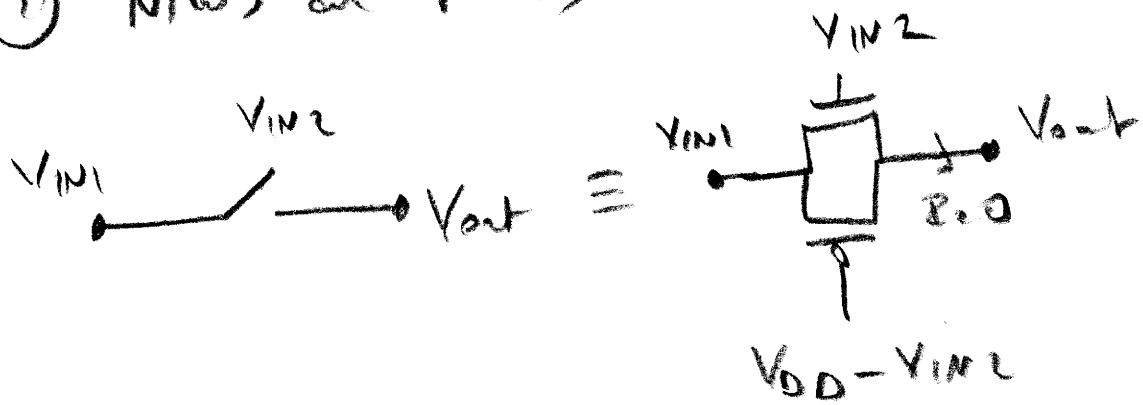
② PMOS

If $V_{IN2}=1$ open

If $V_{IN2}=0$ to make $R=0$

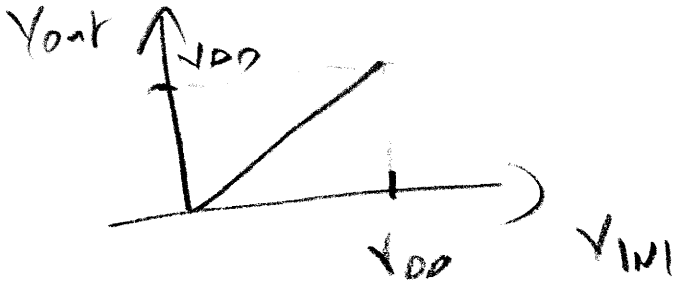


(3) NMOS & PMOS



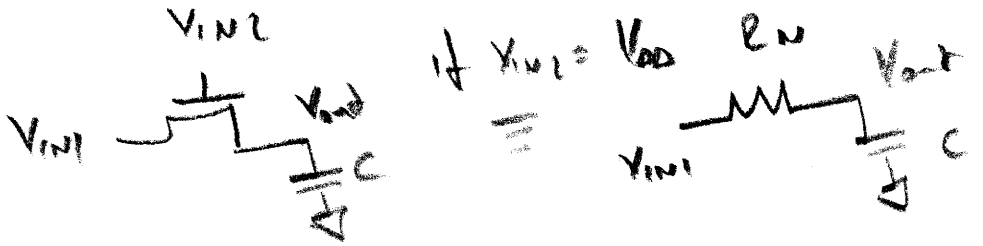
If $V_{IN2} = 0$ transistors are open

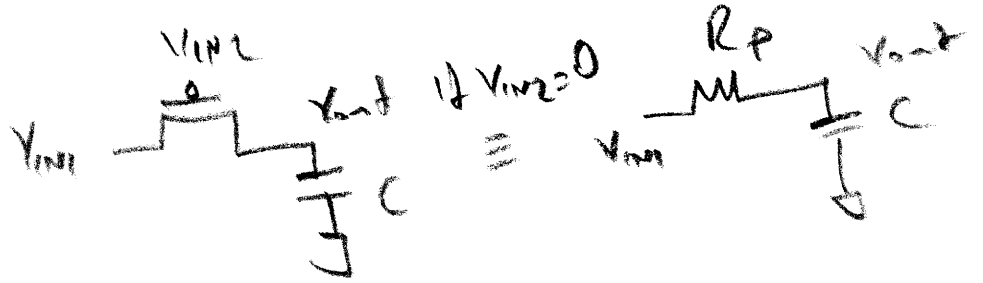
If $V_{IN2} = V_{DD}$ do make R.O

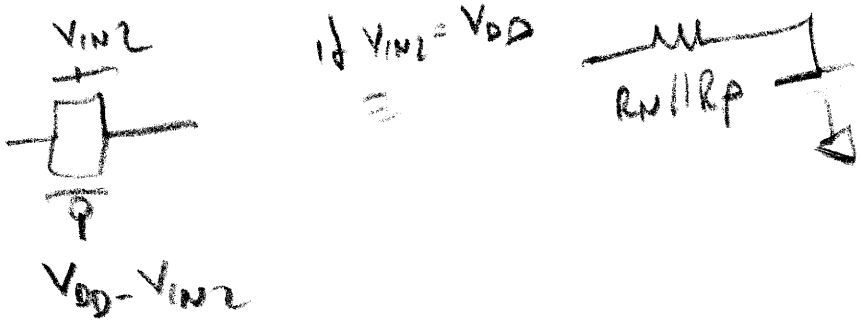


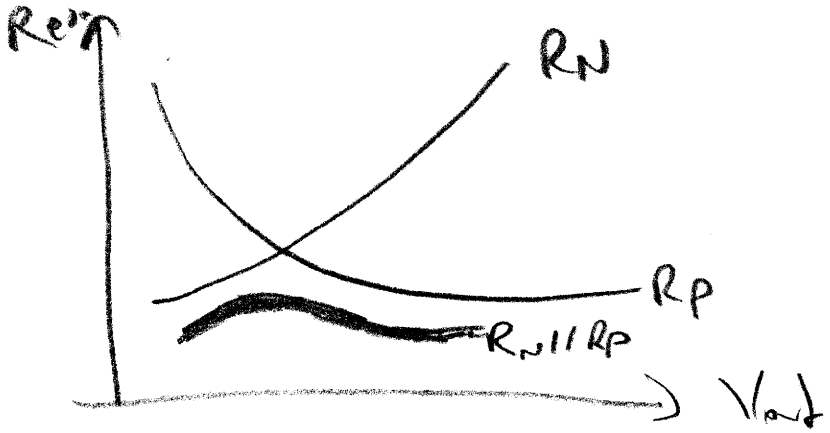
best one at the cost of using doubled # of them.

Delay of PTL



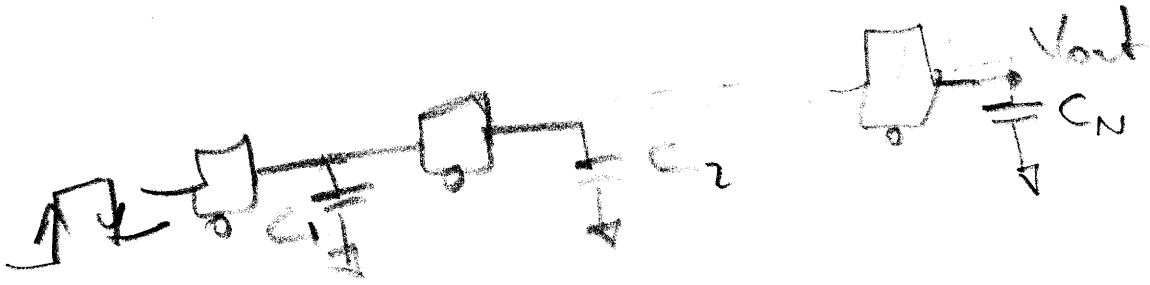




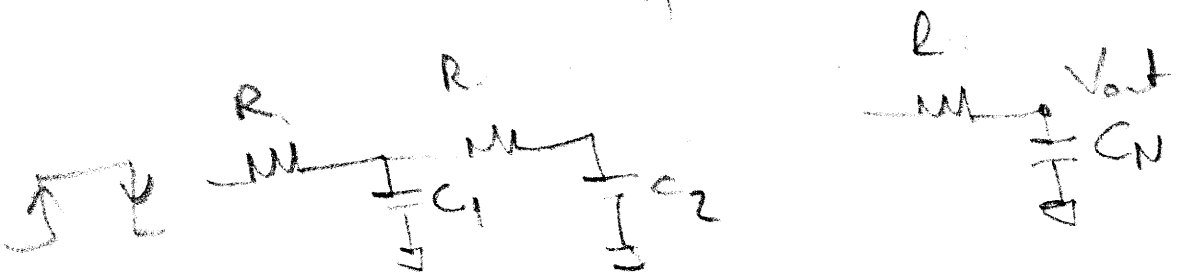


$V_{IN1} = 0$, transistors are ON

$R_N \| R_P$ is relatively constant



M



Delay at V_{out}

$$t_{PHL} = t_{PLH} = 0.69 \{C_1(R) + C_2(2R) + C_N(NR)\}$$

If $C_1 = C_2 = \cdots = C_N = C$ then

$$t_{PHL} = t_{PLH} = 0.69\ C.R\left(\frac{N(N+1)}{2}\right)$$

Ex $f = x_1x_2 + x_1x_3 + x_2x_3$

Implement f with PTL using NMOS and PMOS transistors. Determine WC and BC t_{PHL} and t_{PLH}. Each node has an equivalent cap. of 1fF.

$R_{n1} = 4k\Omega$, $R_{p2} = 8k\Omega$

ordering $x_1 - x_2 - x_3$

$f = x_1x_2 + x_1x_3 + x_2x_3$

all the terms should include x_1 or $\bar{x}_1$ — next

$f = x_1x_2 + x_1x_3 + (x_1 + \bar{x}_1)x_2x_3$

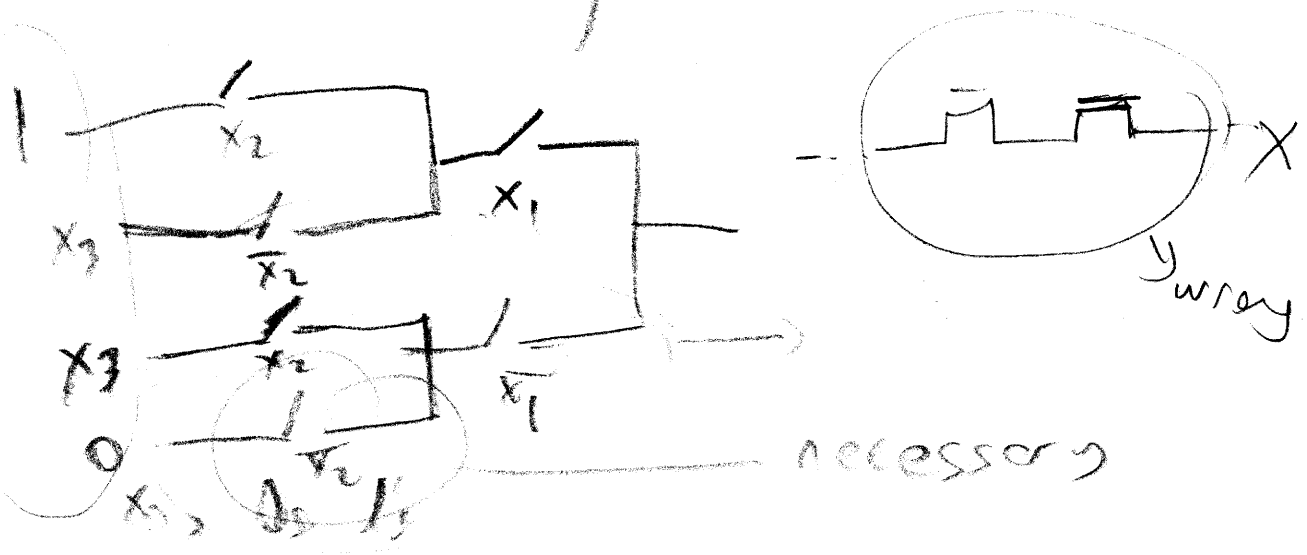
$f = x_1(x_2 + x_3) + \bar{x}_1(x_2x_3)$

x_2 ✓

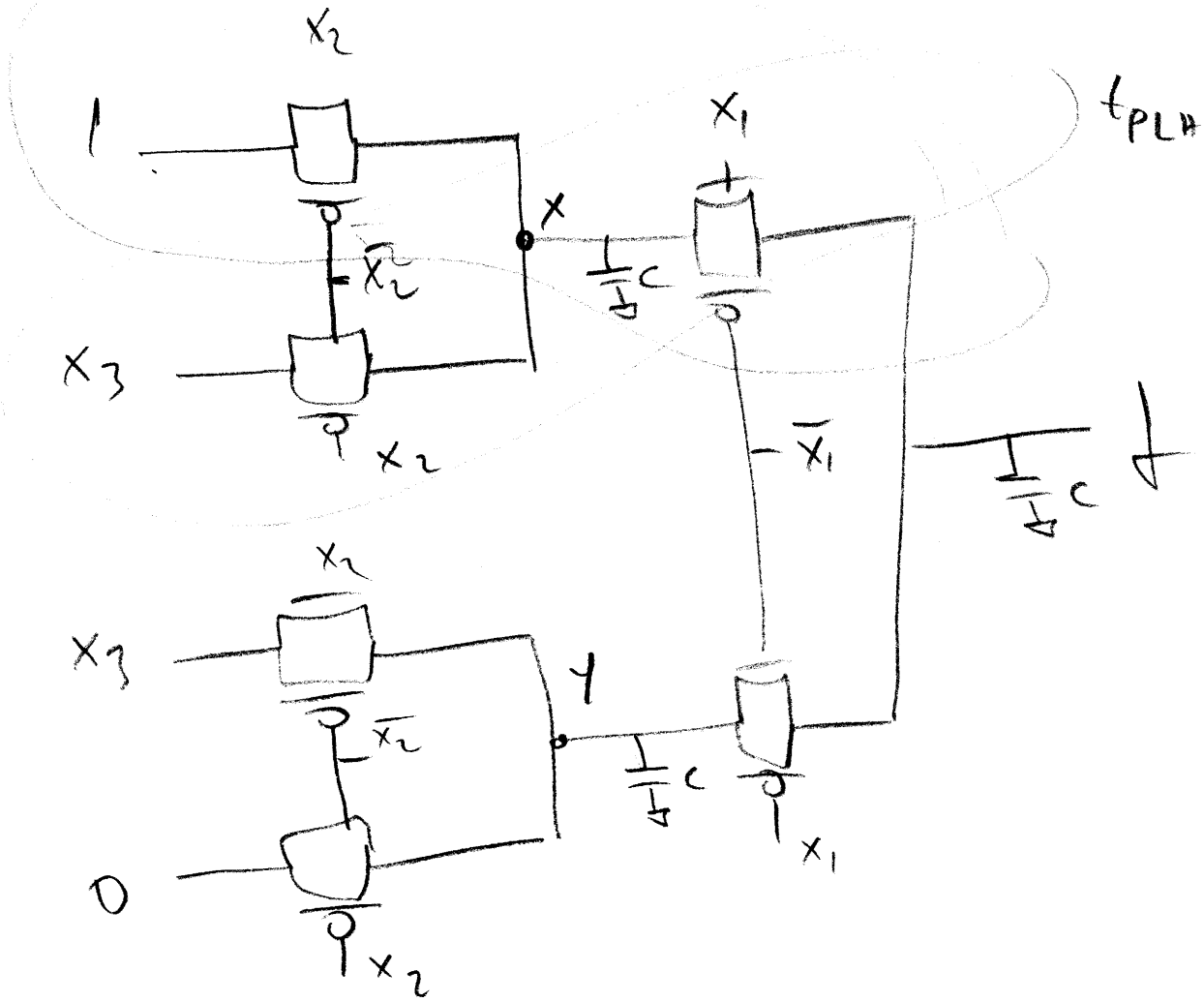
x_2 ✓ — no x_2

$f = x_1(x_2 + (x_2 + \bar{x}_2)x_3) + \bar{x}_1(x_2x_3)$

$= x_1(x_2(1) + \bar{x}_2(x_3)) + \bar{x}_1(x_2(x_3) + \bar{x}_2(0))$



t_{PLH-BC}



t_{PLH-WC}

t_{PLH}

① Best Case
- $X_1 = 0 \rightarrow 1$
- $X_2 = 1$ •
- $X_3 = 0$ •
- $V_{X\text{-initial}} = V_{DD}$

② Worst case
- X_1 1 •
- $X_2 = 0$ •
- $X_3 = 0 \rightarrow 1$
- $V_{X\text{-initial}} = 0$

t_{PHL}

① Best case
- $X_1 = 1 \rightarrow 0$
- $X_2 = 0$ •
- $X_3 = 1$ •
- $V_{Y\text{-initial}} = 0$

② Worst case
- $X_1 = 0$
- $X_2 = 1$
- $X_3 = 1 \rightarrow 0$
- $V_{Y\text{-initial}} = V_{DD}$

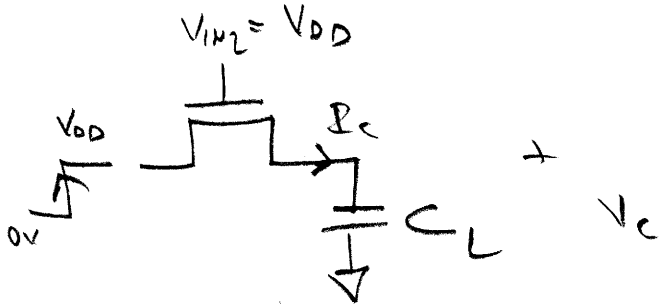
$t_{PLH-BC} = 0{,}69(2R_{eq}C)$ $t_{PLH-WC} = 0{,}69(R_{eq}C + 2R_{eq}C)$ $R_{eq} = 4\,k$

$t_{PHL-BC} = 0{,}69(2R_{eq}C)$ $t_{PHL-WC} = 0{,}69(R_{eq}C + 2R_{eq}C)$ $C = 1\,fF$

$= 5{,}52\,ps$ $= 8{,}28\,ps$

PTL power consumption

(1) Energy consumed in charging for NMOS PTL



$$E_{supp} = \int_0^\infty I_c(t) \cdot V_{DD}\, dt$$

$$I_c(t) = C_L \frac{dV_c(t)}{dt} \qquad V_c = V_{out}$$

$$\Rightarrow E_{supp.} = C_L V_{DD} \int_0^{V_{DD}-V_{TN}} dV_{out}$$

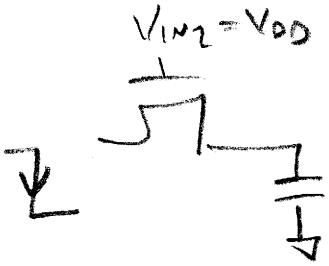
$$\Rightarrow \boxed{E_{supp.} = C_L V_{DD} (V_{DD} - V_{TN})}$$

$$E_{st} = \int_0^\infty I_c(t)\, V_c(t)\, dt = C_L \int_0^{V_{DD}-V_{TN}} V_{out}\, dV_{out}$$

$$\Rightarrow E_{st} = \boxed{C_L \frac{(V_{DD}-V_{TN})^2}{2}}$$

$$E_{consumed} = E_C = E_{ps} - E_{st} = C_L \cdot (V_{DD}-V_{TN}) \left(V_{DD} - \frac{V_{DD}-V_{TN}}{2} \right)$$

(2) Energy consumed in discharging for NMOS PTL



$$P_{s-pp} = E_{st\,(charging)} = C_L \frac{(V_{DD} - V_{TN})^2}{2}$$

$$E_{st} = 0$$

$$E_C = P_{s-pp} = \frac{C_L (V_{DD} - V_{TN})^2}{2}$$

$$E_{C\text{-}total} = C_L V_{DD} (V_{DD} - V_{TN})$$

$$P_{av} = E_{C\text{-}total} \cdot f \rightarrow \text{input signal frequency}$$

PMOS PTL

$$E_{C\text{-}total} = C_L V_{DD} (V_{DD} + V_{TP}) \qquad P_{av} = E_{C\text{-}total} \cdot f$$

NMOS and PMOS PTL

$$E_{C\text{-}total} = C_L V_{DD}^2$$

$$P_{av} = E_{C\text{-}total} \cdot f$$