VLSI Circuit Design II– EHB 425E

HOMEWORK IV

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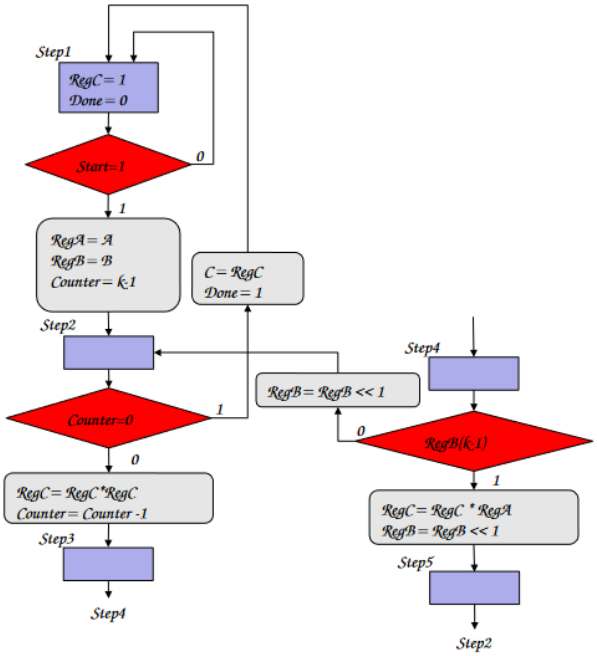
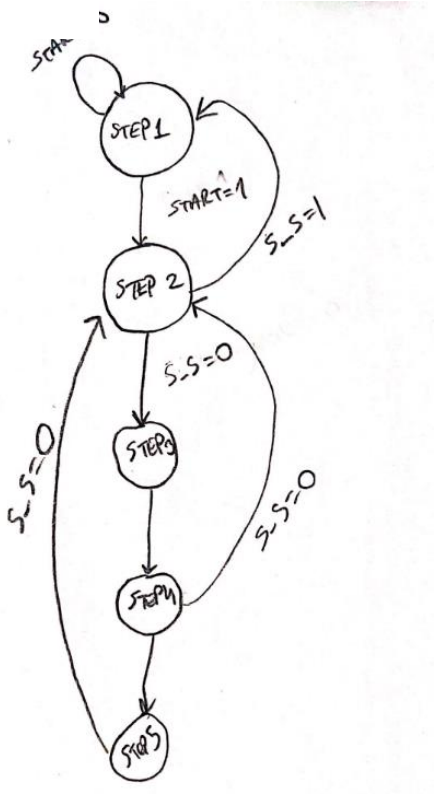
1- Controller

- **State Diagram**

  The state diagram of the figure whose ASM is given below is as shown in the figure. Controller is written according to the diagram in the figure.



		Status Signals		Control Signals						
State	Start	=	RegB (k-1)	Load A	Load Coun	Load B	Shift B	Load C	S Coun	S C
Step1	0	X	X	0	0	0	0	1	X	0
Step1	1	X	X	1	1	1	0	1	0	00
Step2	X	0	X	0	1	0	0	0	1	01
Step2	X	1	X	0	1	0	0	0	1	X
Step3	X	X	X	0	0	0	0	0	X	X
Step4	X	X	0	0	0	0	1	0	X	X
Step4	X	X	1	0	0	0	1	1	X	10
Step5	X	0	X	0	0	0	0	0	X	X



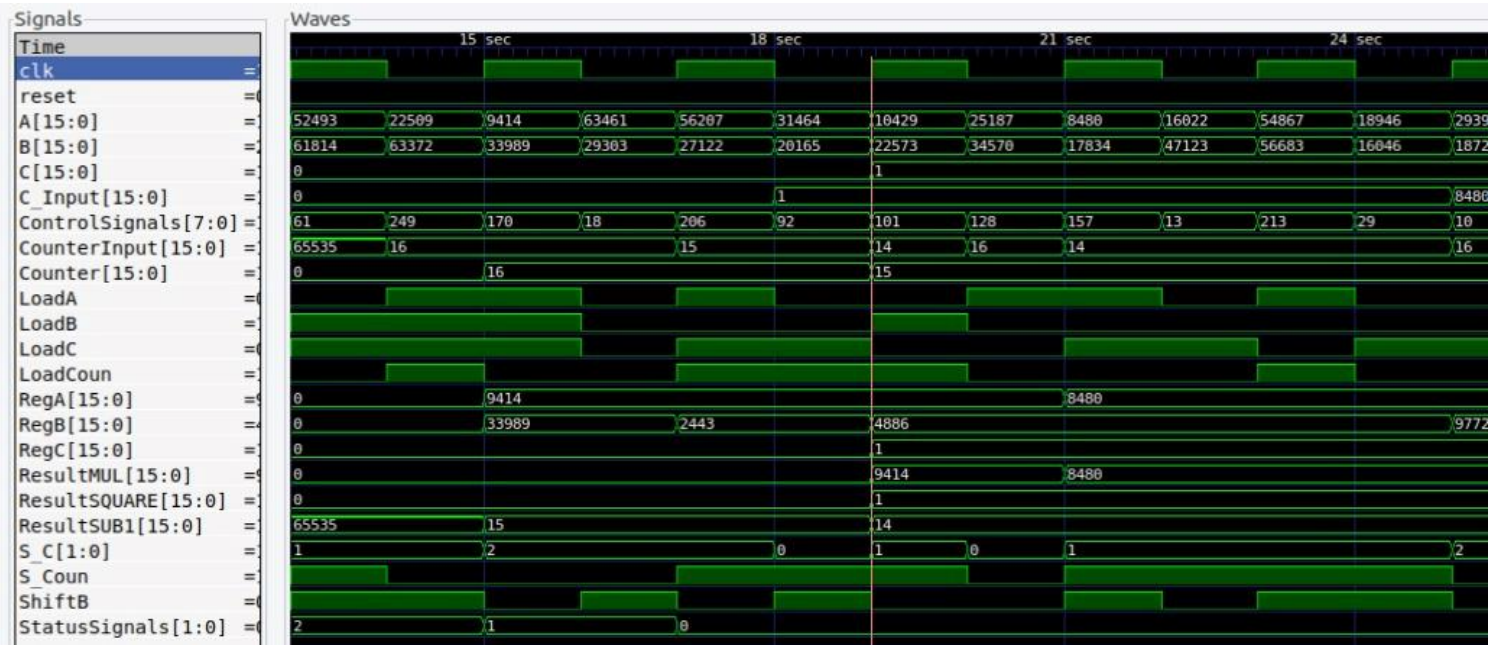
- **GTK Waveform**

As you can see, the code designed according to the state diagram works correctly. The simulation above shows this.

2- Datapath

As it was said in the assignment, the datapath was designed based on the k parameter and using the MUL block in HW3. The codes are zipped and put into the assignment file.

- **GTK Waveform**

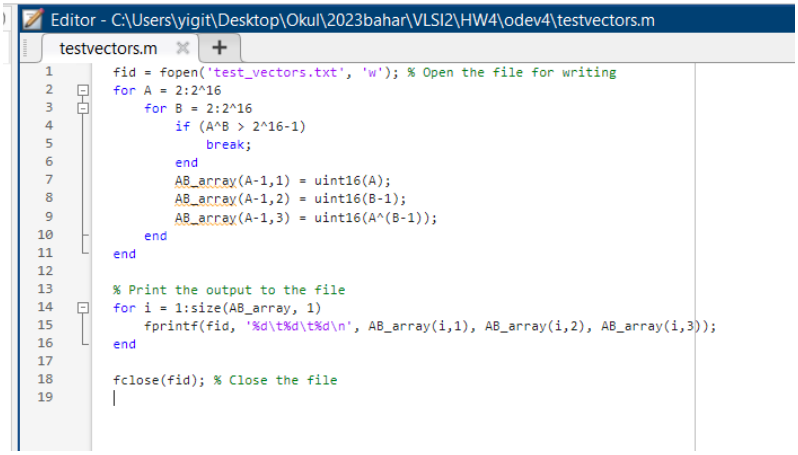


3- Top Module

By combining Controller and Datapath, a top module is created.

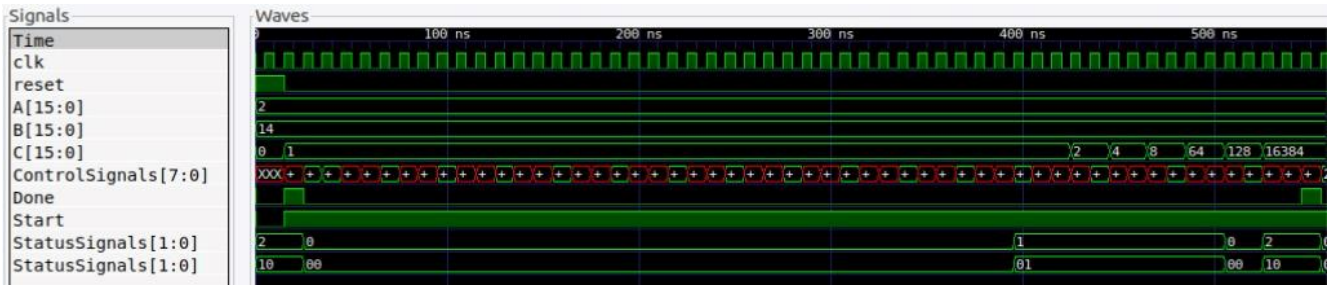
- **MATLAB**

  Test vectors were obtained using the following MATLAB code.

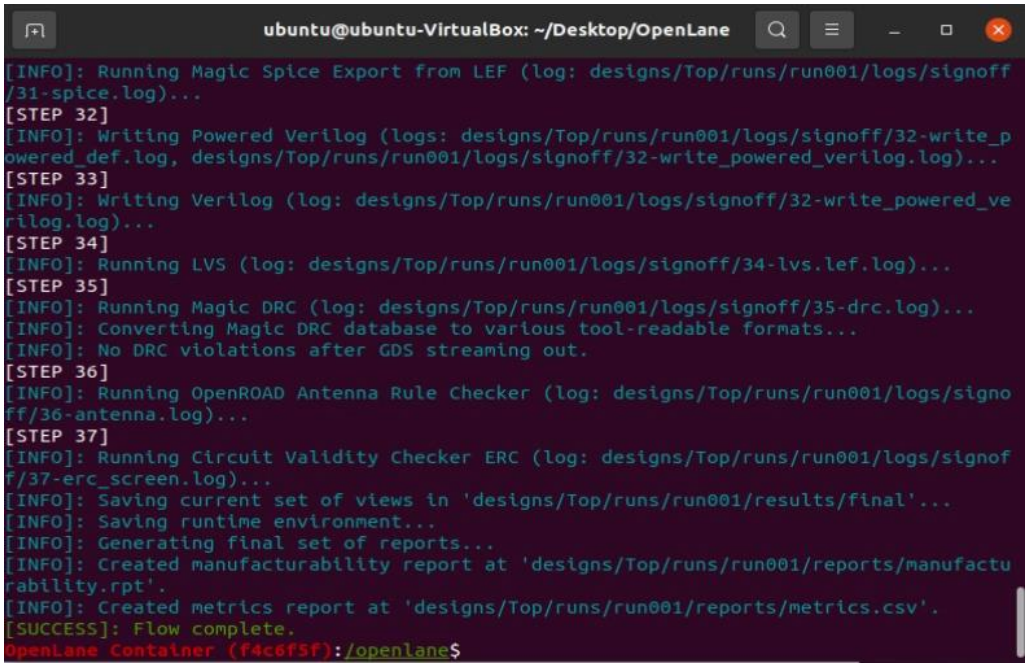


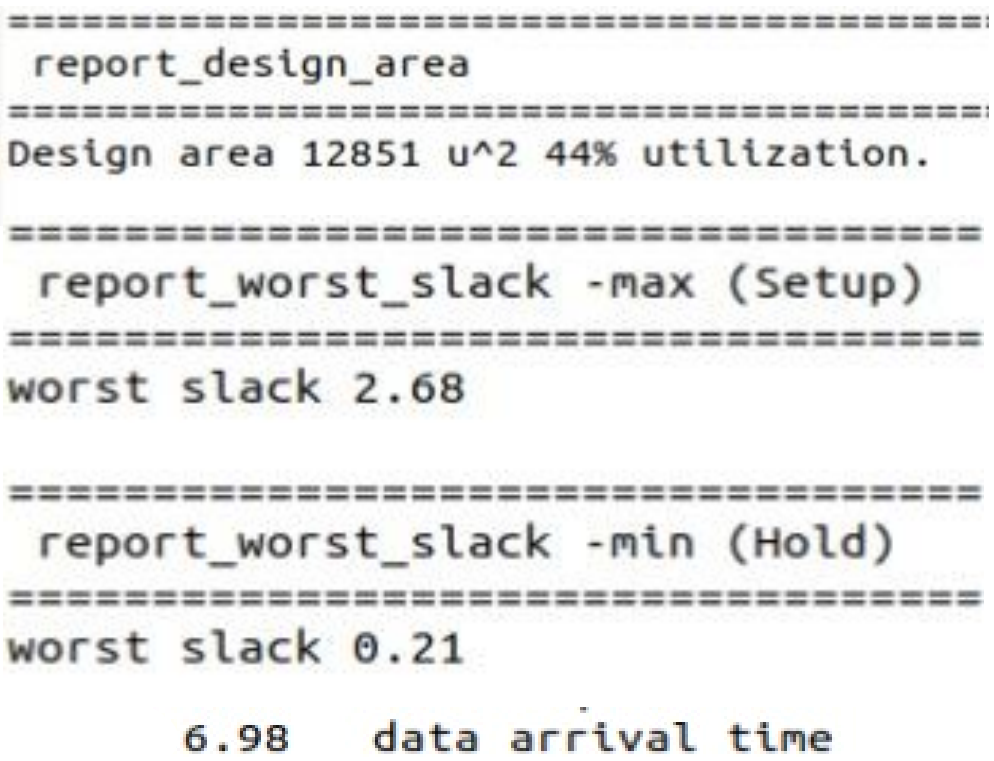
- **GTK Waveform**

  where A is the value to be powered. B is the power of A. By looking at the power of 2 here, it can be understood whether the circuit is working correctly. The powers of 2 confirm that the circuit is working correctly. After 2^14 is finally received, the done signal 1 appears to be lit. Indicates that the process is finished.



4- Openlane Section





As can be seen, no errors were encountered while synthesizing. The desired outputs are mentioned above. Max Frequency ➔ 1/6.98*10^-9 = 143.266 MHz

All verilog source codes and files with .dot extension are in the archive.