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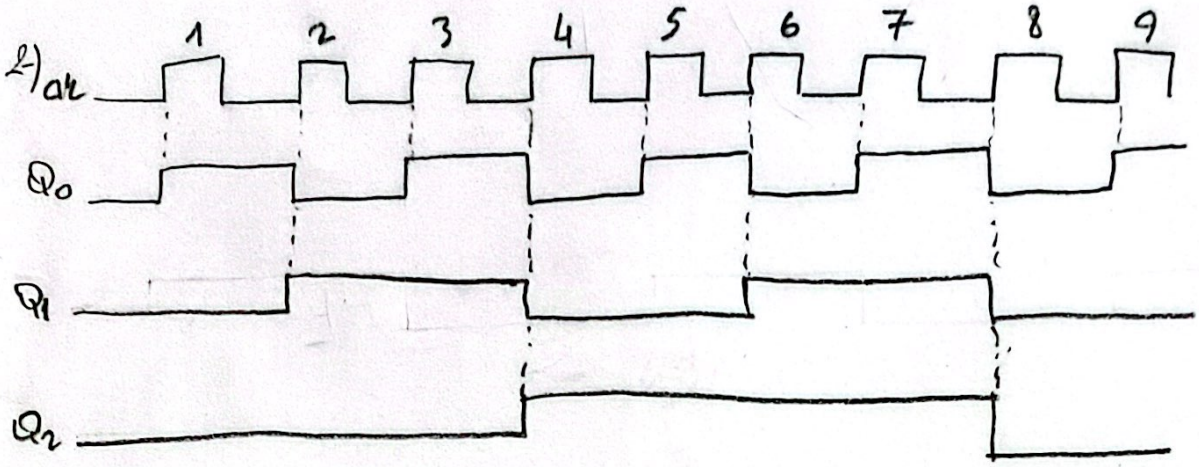
1) $Q_0 = T_0 \oplus q_0$ $T_0 = 1 \Rightarrow Q_0 = q_0'$

$Q_1 = T_1 \oplus q_1$ $T_1 = 1 \Rightarrow Q_1 = q_1'$

$Q_2 = T_2 \oplus q_2$ $T_2 = 1 \Rightarrow Q_2 = q_2'$

2)



Q_1 depends on $\overline{Q_0}$'s posedge $\Rightarrow$ Q_0's negedge

Q_2 " " $\overline{Q_1}$' posedge $\Rightarrow$ Q_1's negedge

Uses as clocks

3-)

No of posedge clk	Q_2	Q_1	Q_0
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
8	0	0	0
9	0	0	1

This circuit is a 3-bit binary up counter. As can be see in truth table on the left, the 3-bit binary counter increases by 1 for each posedge of the clock signal, when the value reaches 7, it returns to 0 again.