A pattern detector which gives 1 at its 1-bit output when the last four values of its 2-bit inputs are 11-11-01 will be designed. The detected streams will not overlap. T type rising edge triggered flip-flops, AND (VE), OR (VEYA) and NOT (TÜMLEME) gates will be used for the implementation. ($Q = T \oplus q$)

1) Draw the Mealy type state diagram.
2) Draw the state transition table using binary encoding of the states (00, 01, 10, …).