



Very Large Scale Integration II - VLSI II

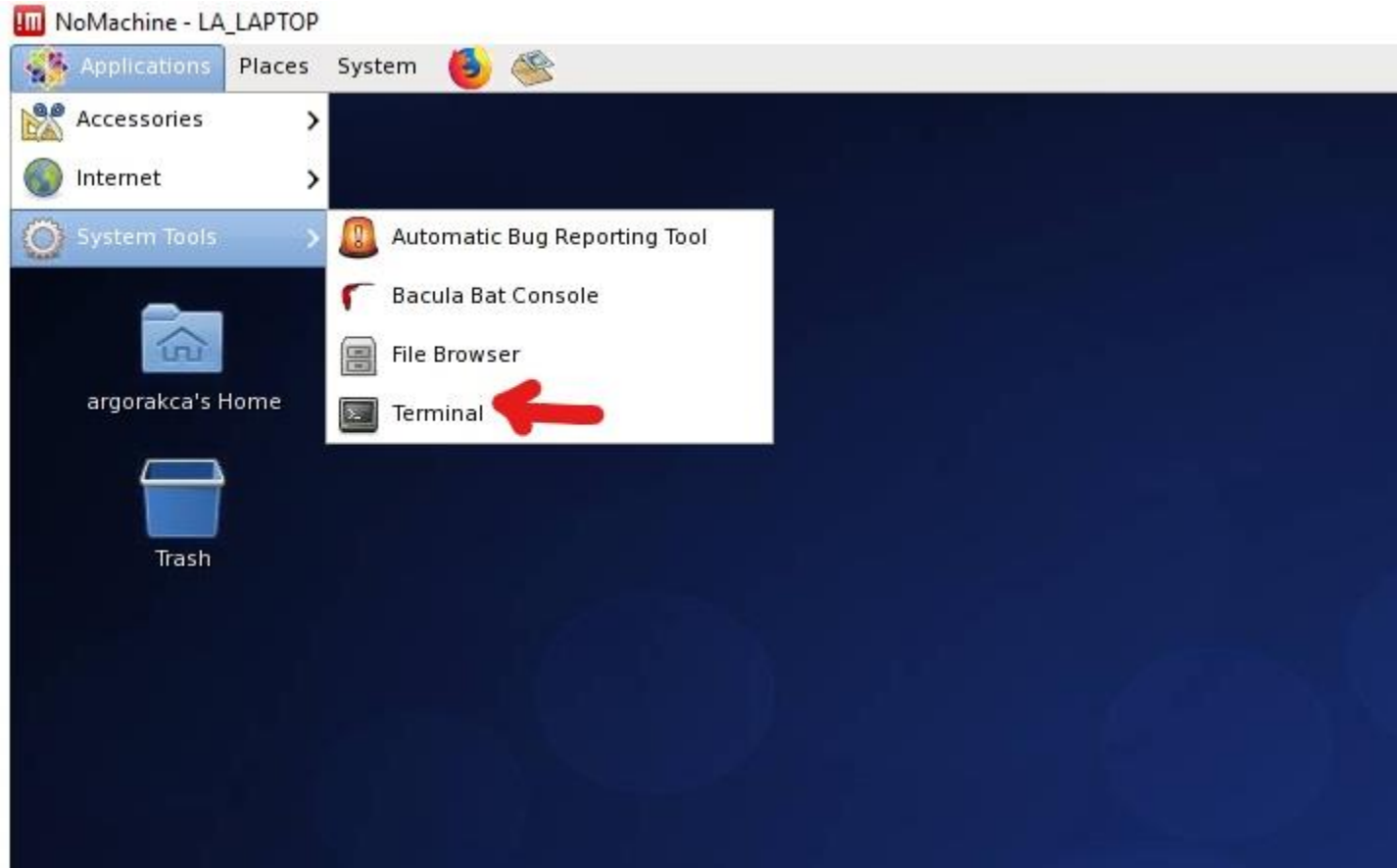
Full Custom Gate Design

ITU VLSI Laboratories

Istanbul Technical University



Full Custom Gate Design with Cadence



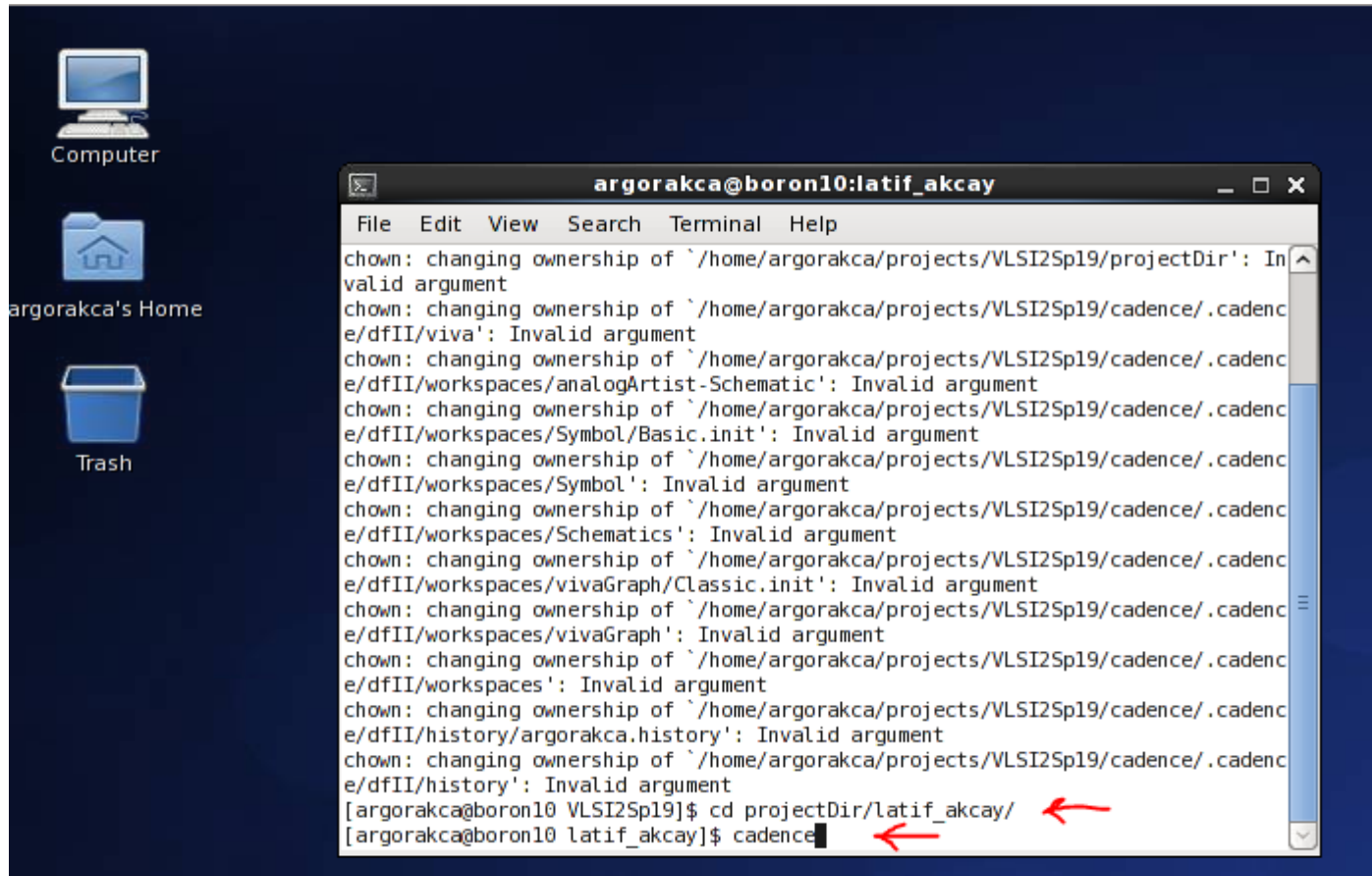


Full Custom Gate Design with Cadence

```
argorakca@boron10:latif_akcay
File Edit View Search Terminal Help
[argorakca@silicon ~]$ ssh boron10
argorakca@boron10's password:
Last login: Fri Feb 15 21:16:24 2019 from silicon.comp.vlsi.labs
[argorakca@boron10 ~]$ VLS
VLSI2Sp17 VLSI2Sp18 VLSI2Sp19
[argorakca@boron10 ~]$ VLSI2Sp19
chown: changing ownership of `/home/argorakca/projects/VLSI2Sp19/projectDir': In
valid argument
chown: changing ownership of `/home/argorakca/projects/VLSI2Sp19/cadence/.cadenc
e/dfII/viva': Invalid argument
chown: changing ownership of `/home/argorakca/projects/VLSI2Sp19/cadence/.cadenc
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chown: changing ownership of `/home/argorakca/projects/VLSI2Sp19/cadence/.cadenc
e/dfII/workspaces/Symbol/Basic.init': Invalid argument
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e/dfII/workspaces/Symbol': Invalid argument
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e/dfII/workspaces': Invalid argument
```

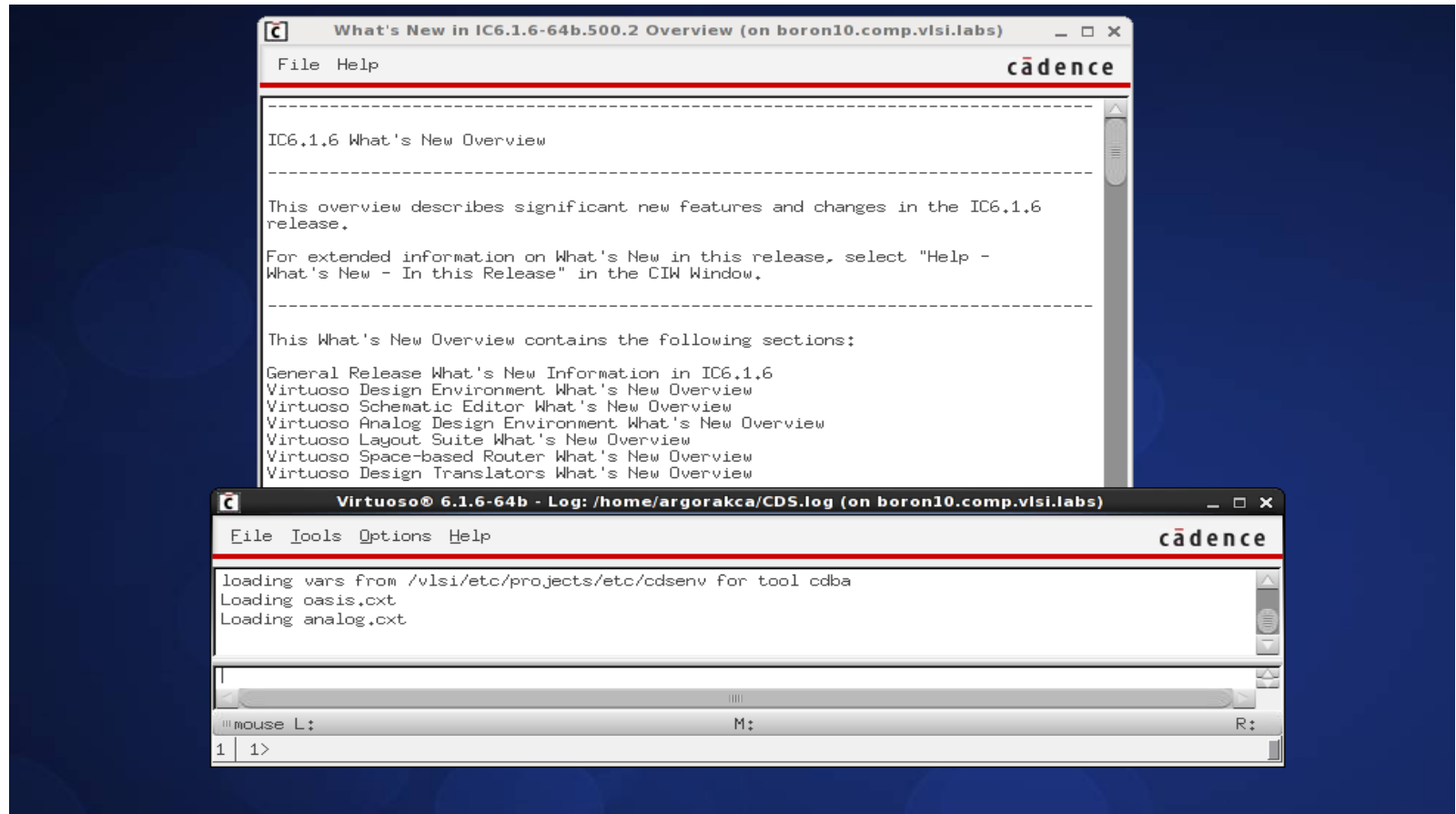


Full Custom Gate Design with Cadence



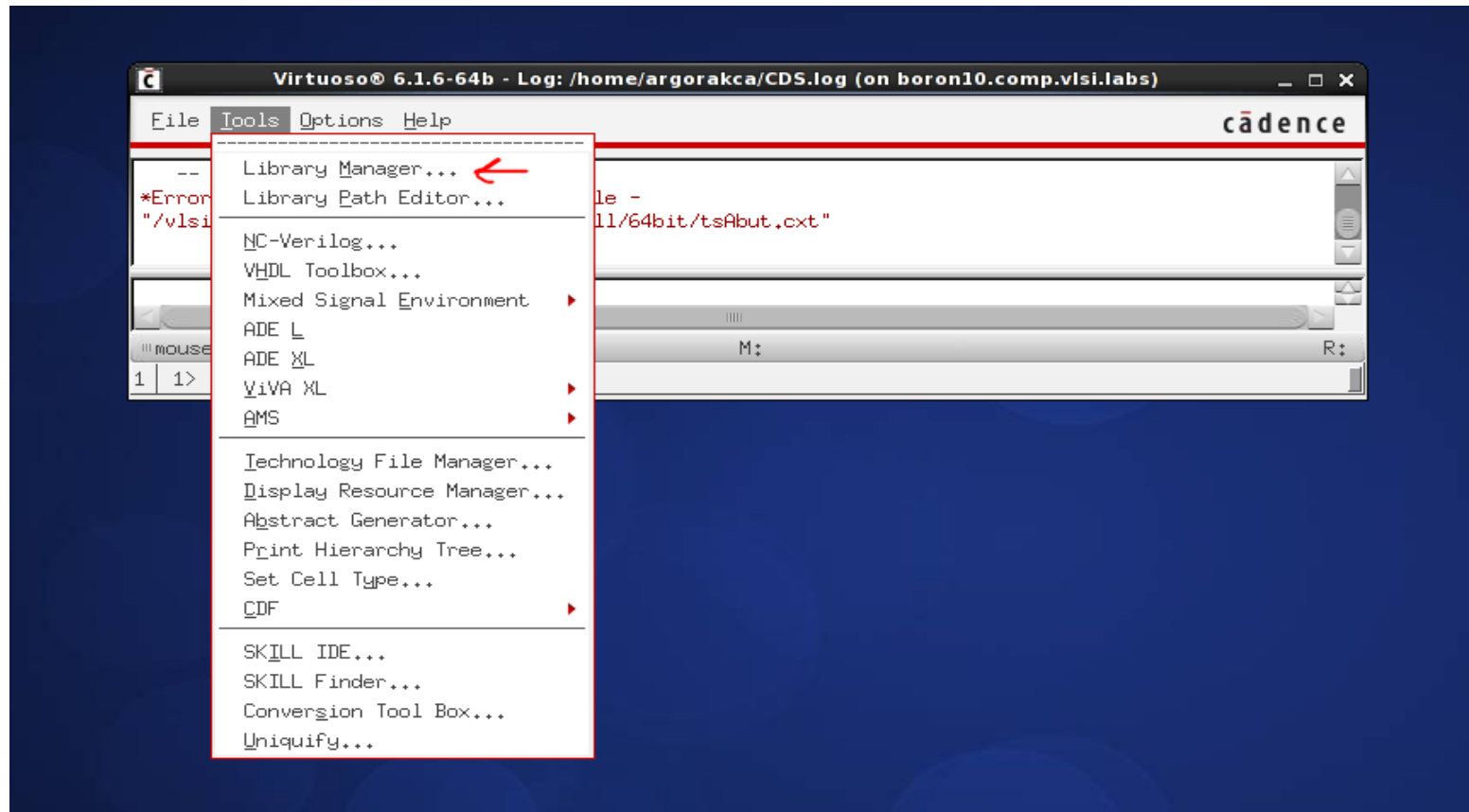


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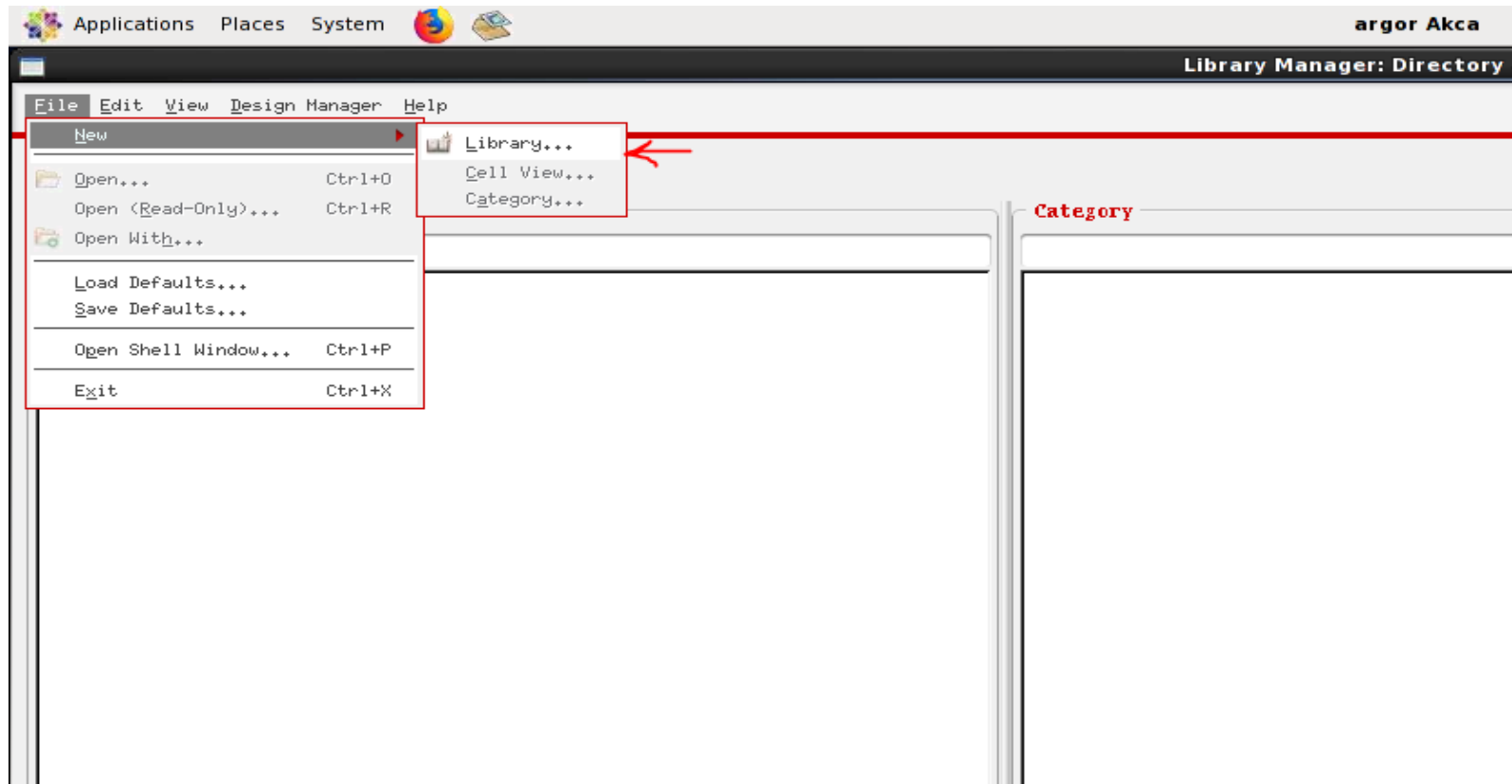


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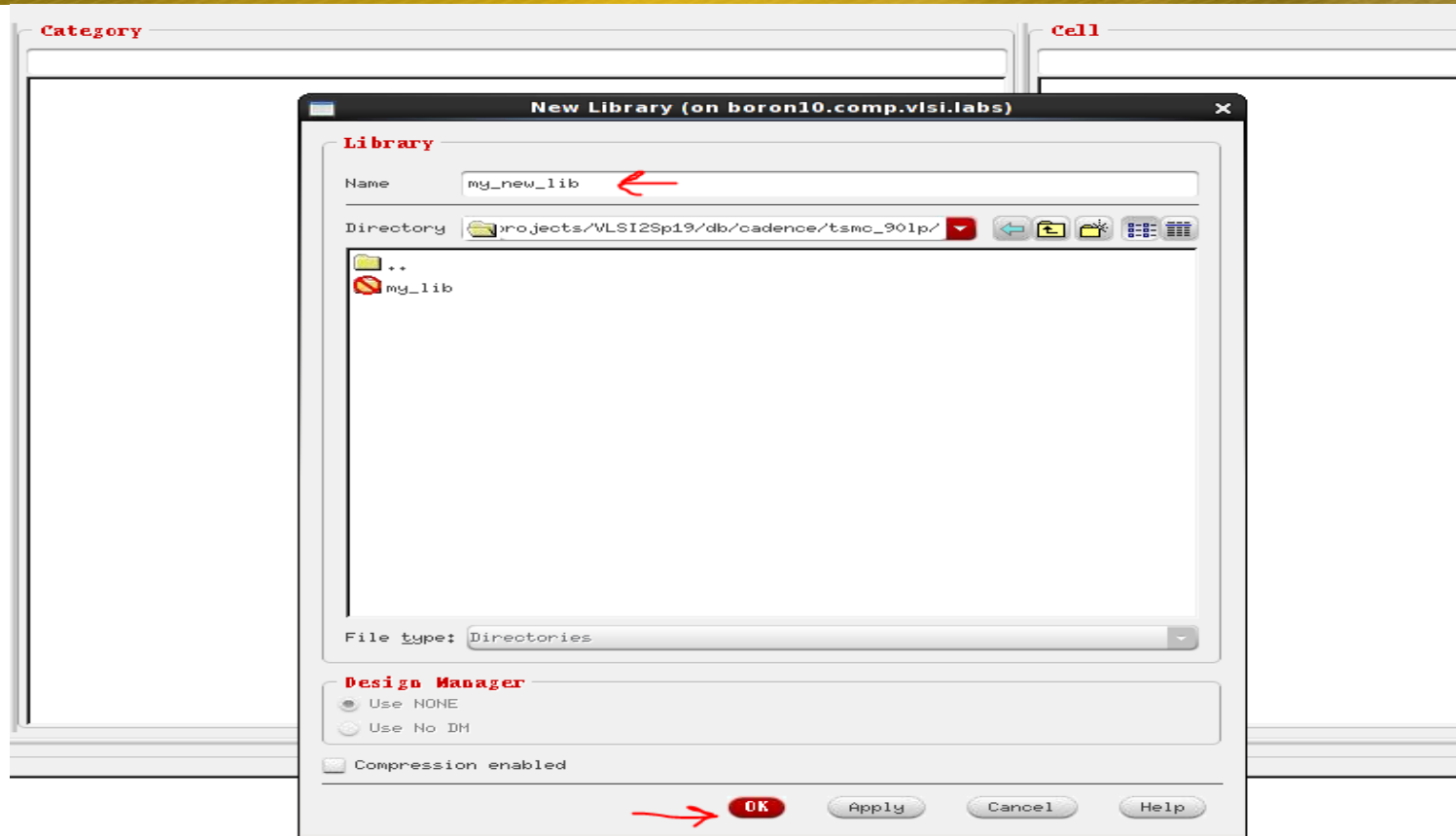


Full Custom Gate Design with Cadence



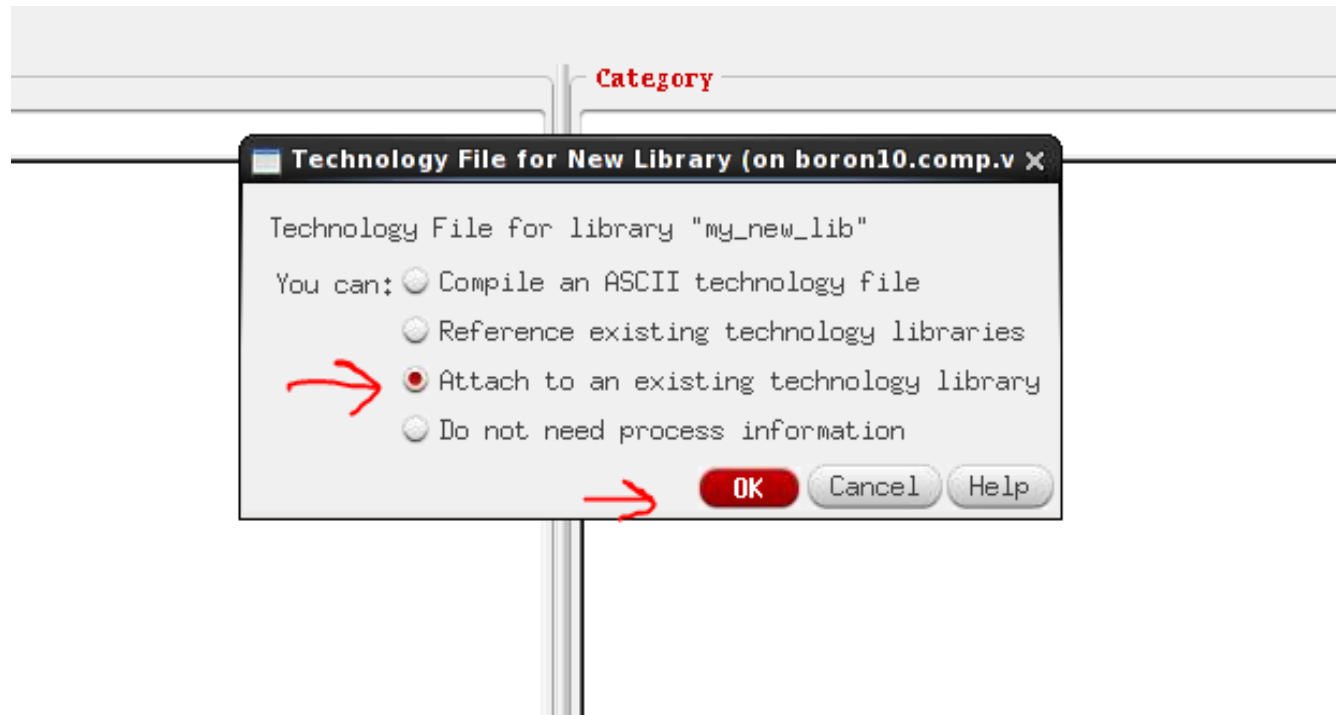


Full Custom Gate Design with Cadence



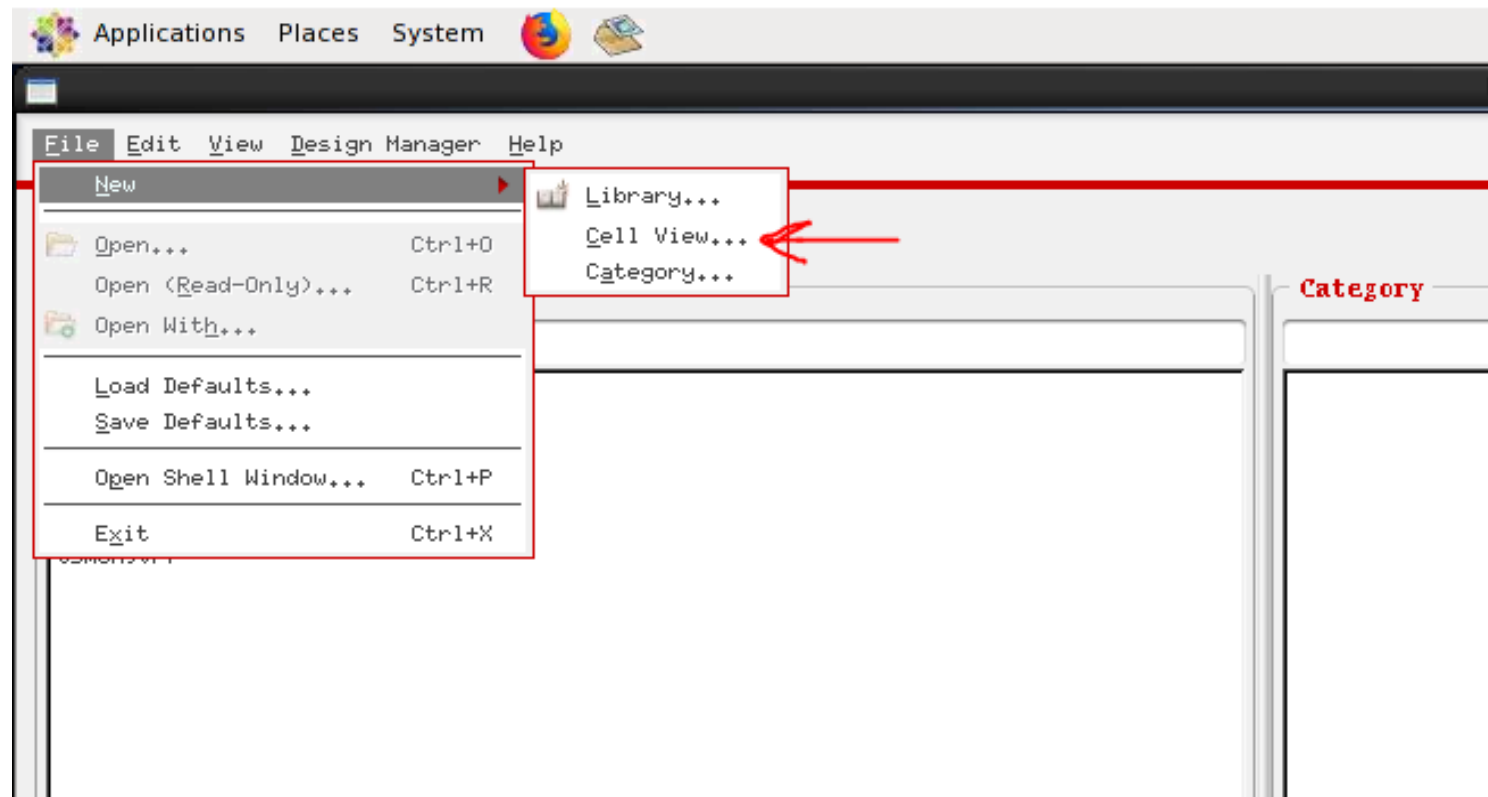


Full Custom Gate Design wiht Cadence



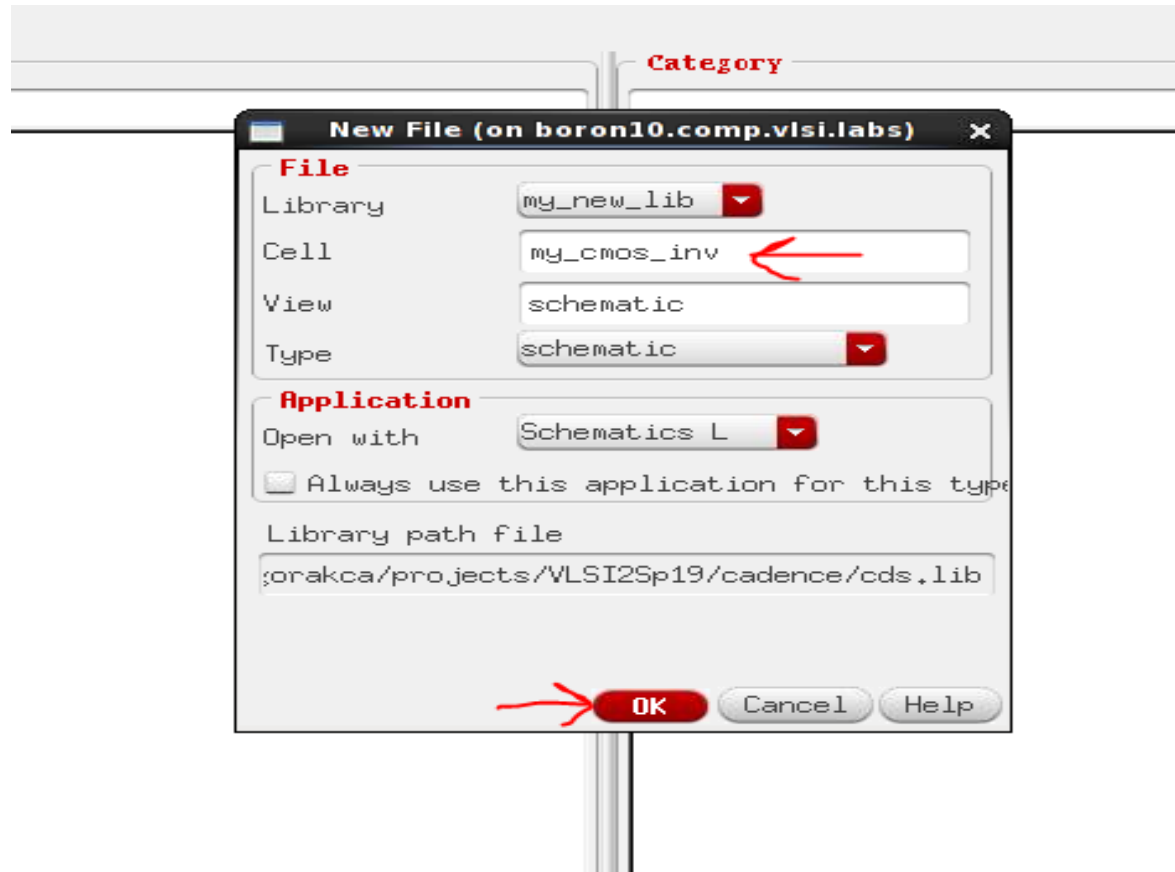


Full Custom Gate Design wiht Cadence



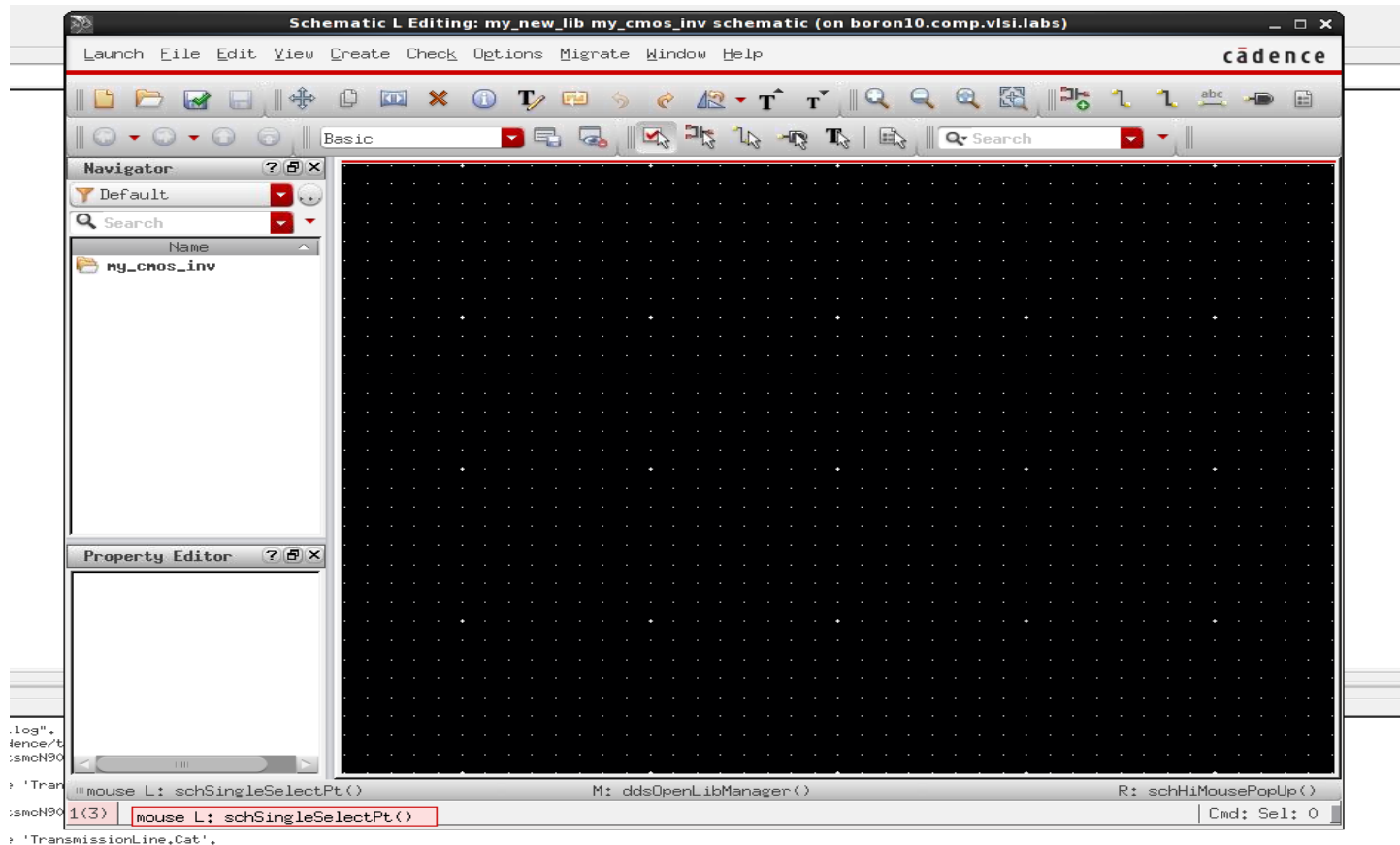


Full Custom Gate Design with Cadence



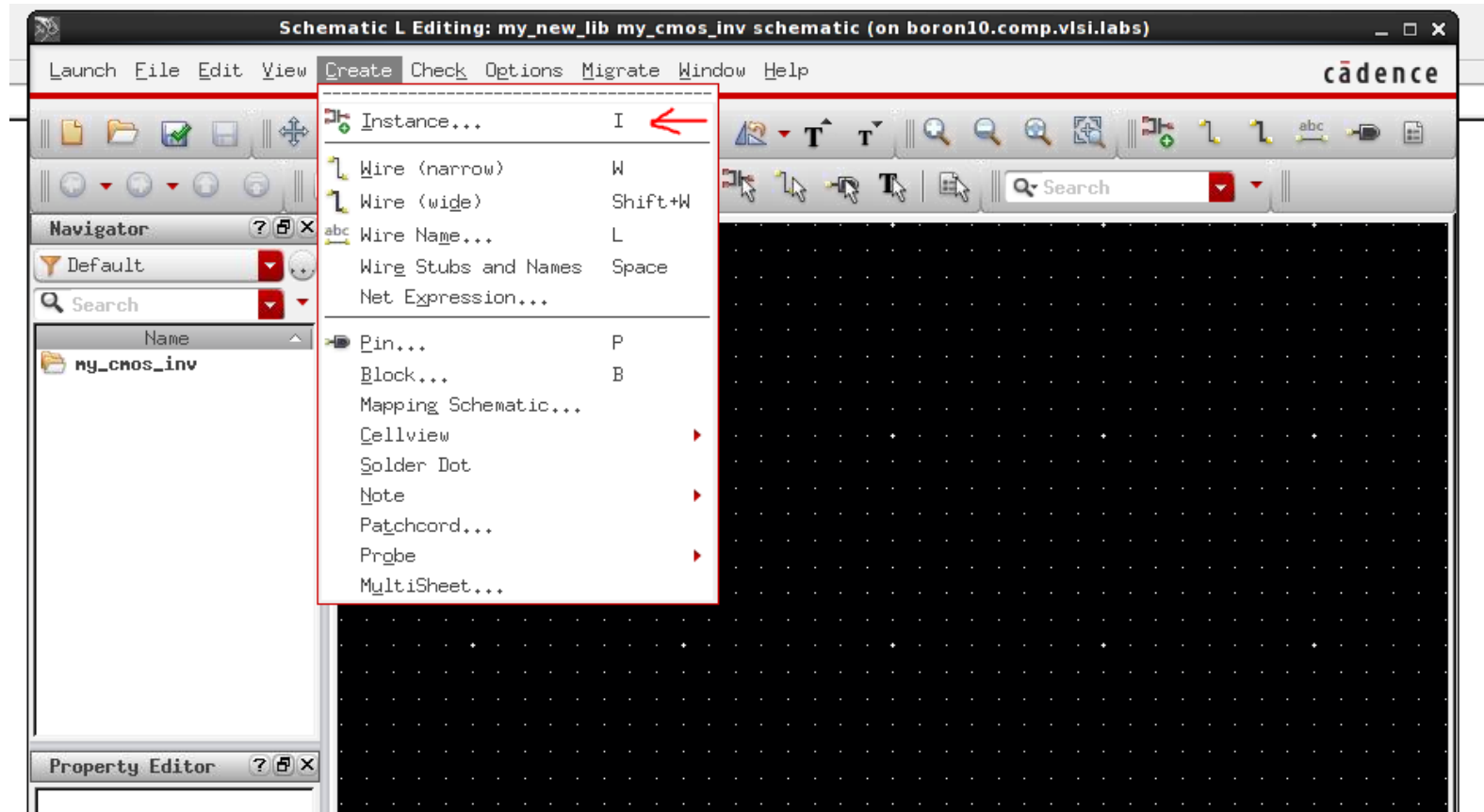


Full Custom Gate Design with Cadence



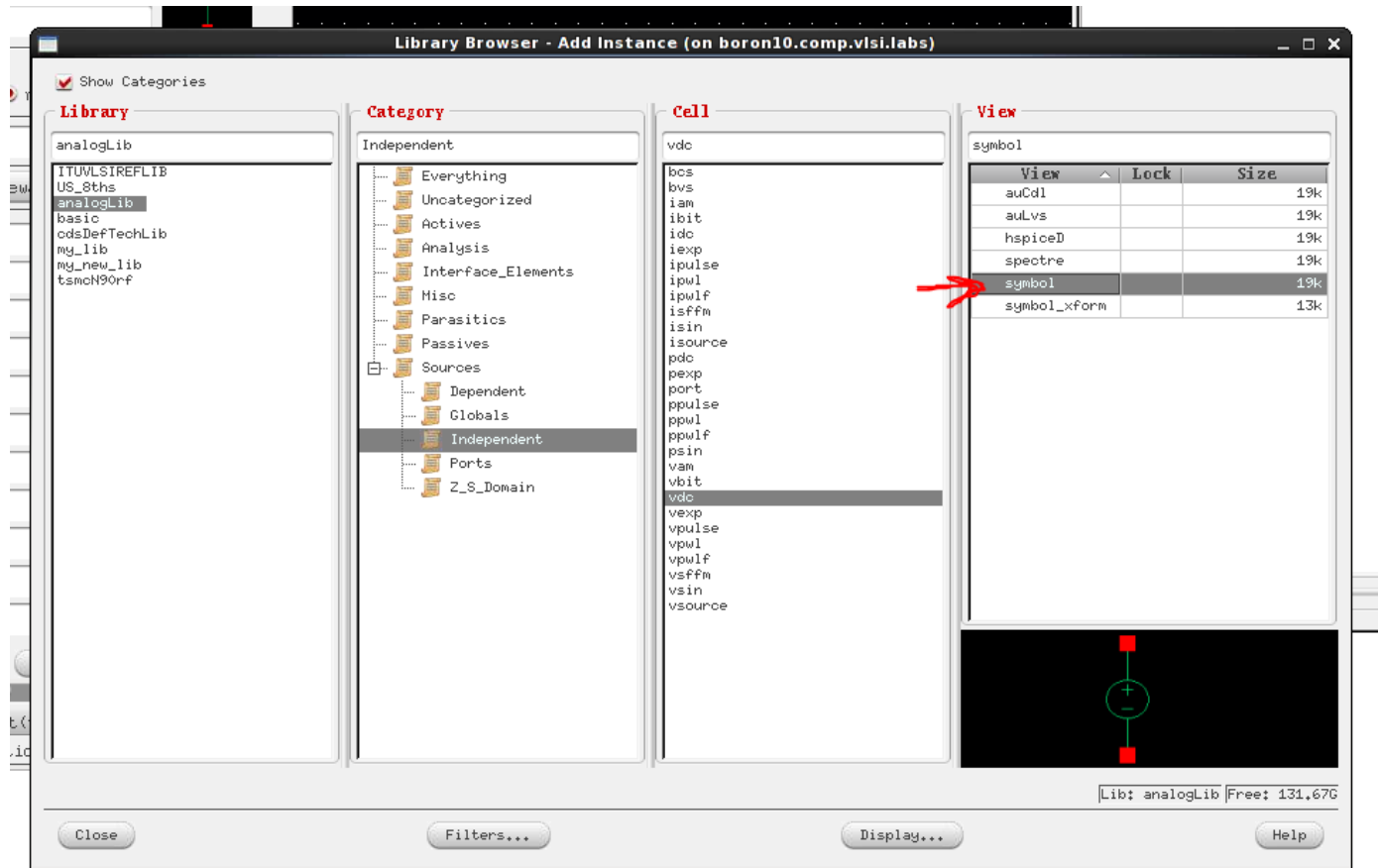


Full Custom Gate Design with Cadence



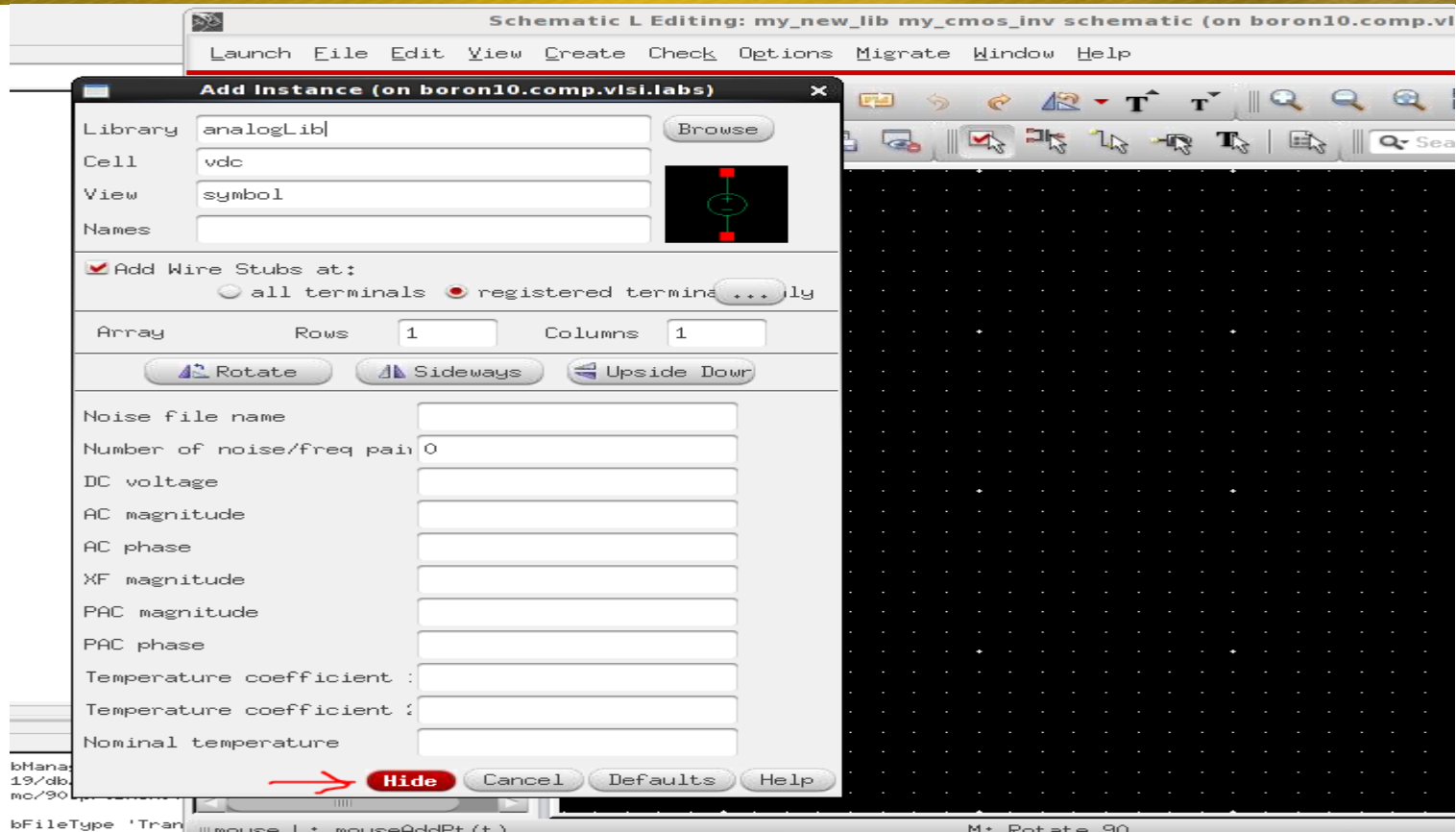


Full Custom Gate Design with Cadence



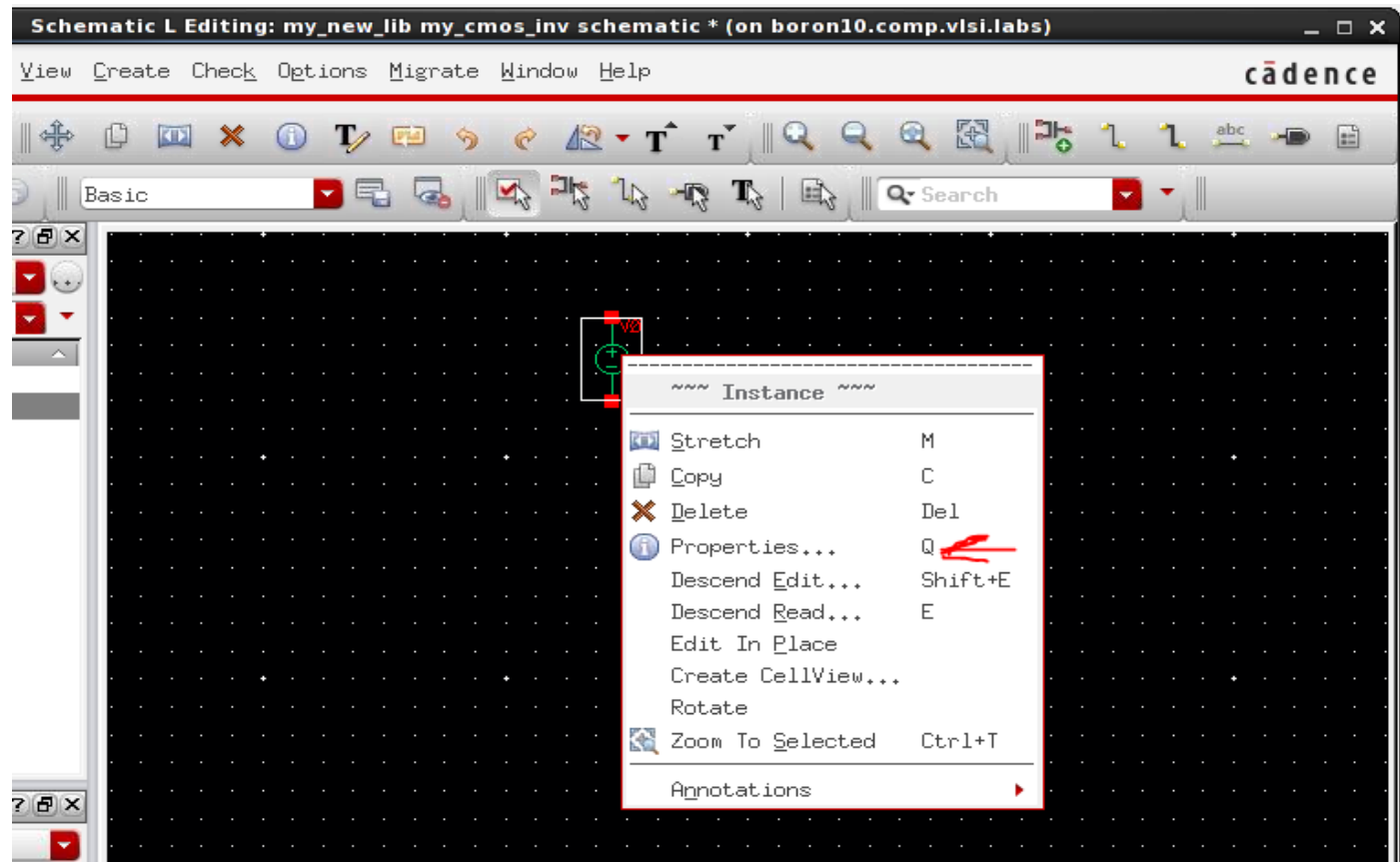


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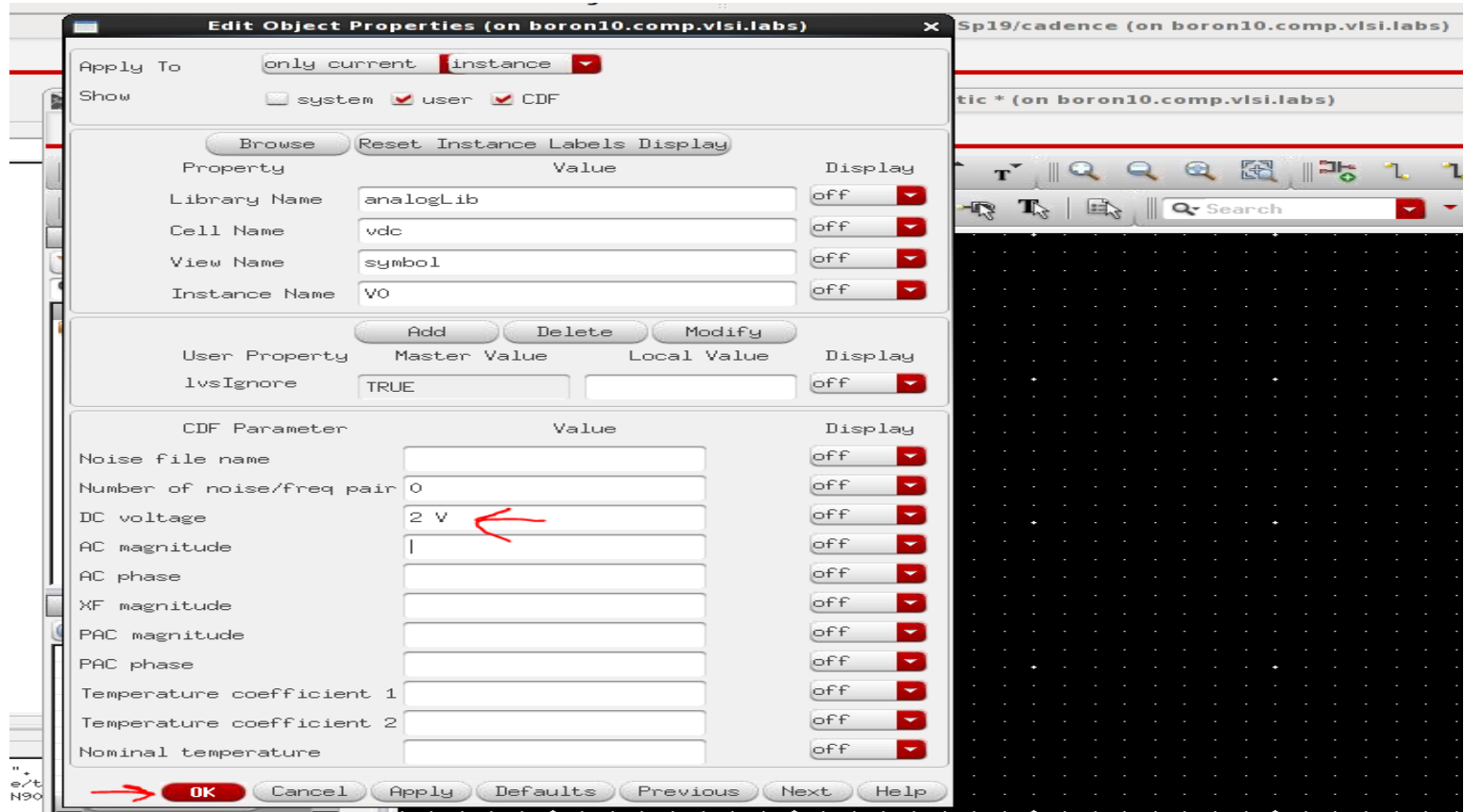


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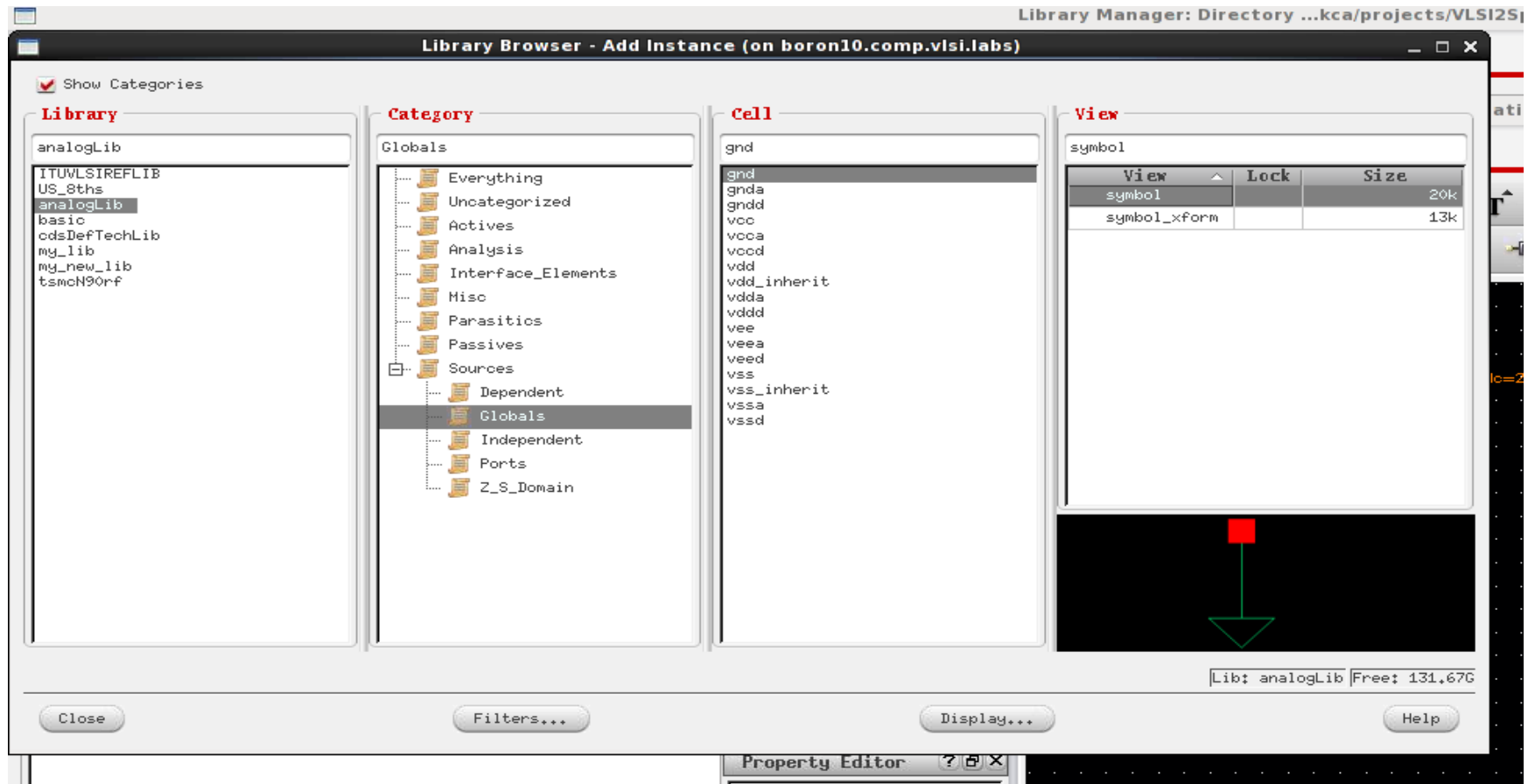


Full Custom Gate Design with Cadence





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Full Custom Gate Design with Cadence

Library Manager: Directory ...kca/projects/VLSI2Sp19/cadence (on boron10.comp.vlsi.labs)

File Edit View Design Manager Help

☒ Show Categories ☐ Show Files

Library

- tsmcN90rf
- ITUVLSIREFLIB
- US_8ths
- analogLib
- basic
- cdsDefTechLib
- my_lib
- my_new_lib
- tsmcN90rf**

Category

- MosFets
- Everything
- Uncategorized
- BJTS
- Capacitors
- Diodes
- Inductors
- LogicGates
- MetalRes
- MosFets**
- MosFets_mac
- Pad_layout
- Parasitic_RC
- Resistors
- Symbolic
- TransmissionLine
- TurboToolbox
- Varactors
- do_not_use

Cell

- pch
- nch
- nch_25
- nch_25_dnw
- nch_25_dnwX
- nch_25x
- nch_dnw
- nch_dnwX
- nch_hvt
- nch_hvt_dnw
- nch_hvt_dnwX
- nch_hvtX
- nch_lvt
- nch_lvt_dnw
- nch_lvt_dnwX
- nch_lvtX
- nch_na
- nch_na25
- nch_na25x
- nch_nax
- nch_ulvt
- nch_ulvt_dnw
- nch_ulvt_dnwX
- nch_ulvtX
- nchX
- nmos_rf
- nmos_rf25
- pch**
- pch_25
- pch_25x
- pch_hvt
- pch_hvtX

View

View	Lock	Size
Advance_HS		19k
ads		19k
ams		19k
auCdl		19k
auLvs		19k
eldoD		19k
hspiceD		19k
ivpCell		23k
layout		32k
spectre		19k
symbol		19k

Messages

Log file is "/home/argorakca/projects/VLSI2Sp19/cadence/libManager.log".
Warning: Couldn't get an exclusive lock for "/vlsi/kits/tsmc/90lp/tsmcN90rf/TransmissionLine.Cat"
Permission denied
Warning: ddDeleteDeep: Couldn't get exclusive lock on ddLibFileType 'TransmissionLine.Cat'.
Warning: ddCatRemove: unable to remove category TransmissionLine.
Warning: Couldn't get an exclusive lock for "/vlsi/kits/tsmc/90lp/tsmcN90rf/TransmissionLine.Cat"
Permission denied
Warning: ddDeleteDeep: Couldn't get exclusive lock on ddLibFileType 'TransmissionLine.Cat'.
Warning: ddCatRemove: unable to remove category TransmissionLine.

Lib: tsmcN90rf Free: 131,67G



Full Custom Gate Design with Cadence

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File Edit View Design Manager Help

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- tsmcN90rf

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- Mosfets
- Everything
- Uncategorized
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- Capacitors
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- Mosfets_mac
- Pad_layout
- Parasitic_RC
- Resistors
- Symbolic
- TransmissionLine
- TurboToolbox
- Varactors
- do_not_use

Cell

nch

- nch
- nch_25
- nch_25_dnw
- nch_25_dnwxc
- nch_25x
- nch_dnw
- nch_dnwxc
- nch_hvt
- nch_hvt_dnw
- nch_hvt_dnwxc
- nch_hvtx
- nch_lvt
- nch_lvt_dnw
- nch_lvt_dnwxc
- nch_lvtx
- nch_na
- nch_na25
- nch_na25x
- nch_nax
- nch_ulvt
- nch_ulvt_dnw
- nch_ulvt_dnwxc
- nch_ulvtx
- nchx
- nmos_rf
- nmos_rf25
- pch
- pch_25
- pch_25x
- pch_hvt
- pch_hvtx
- ...

View

symbol

View	Lock	Size
ADVance_MS		19k
ads		19k
ans		19k
auCd1		19k
auLvs		19k
eldoD		19k
hspiceD		19k
ivpcell		23k
layout		32k
spectre		19k
symbol		19k

Messages

Log file is "/home/argorakca/projects/VLSI2Sp19/cadence/libManager.log".
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Full Custom Gate Design with Cadence

Library Manager: Directory ...kca/projects/VLSI2Sp19/cadence (on boron10.comp.vlsi.labs)

File Edit View Design Manager Help

cadence

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Library

- analogLib
- ITUMLSIREFLIB
- US_Sths
- analogLib
- basic
- cdsDefTechLib
- my_lib
- my_new_lib
- tsmcN90rf

Category

Independent

- Everything
- Uncategorized
- Actives
- Analysis
- Interface_Elements
- Misc
- Parasitics
- Passives
- Sources
 - Dependent
 - Globals
 - Independent
 - Ports
 - Z_S_Domain

Cell

vpulse

- bcs
- bvs
- iam
- ibit
- idc
- iepx
- ipulse
- ipul
- ipulf
- isffm
- isin
- isource
- pdc
- pexp
- port
- ppulse
- ppul
- ppulf
- psin
- vam
- vbit
- vdc
- vexp
- vpulse**
- vpul
- vpulf
- vsffm
- vsin
- vsource

View

symbol

View	Lock	Size
auCdl		19k
auLvs		19k
hspiceD		19k
spectre		19k
symbol		19k
symbol_xform		13k

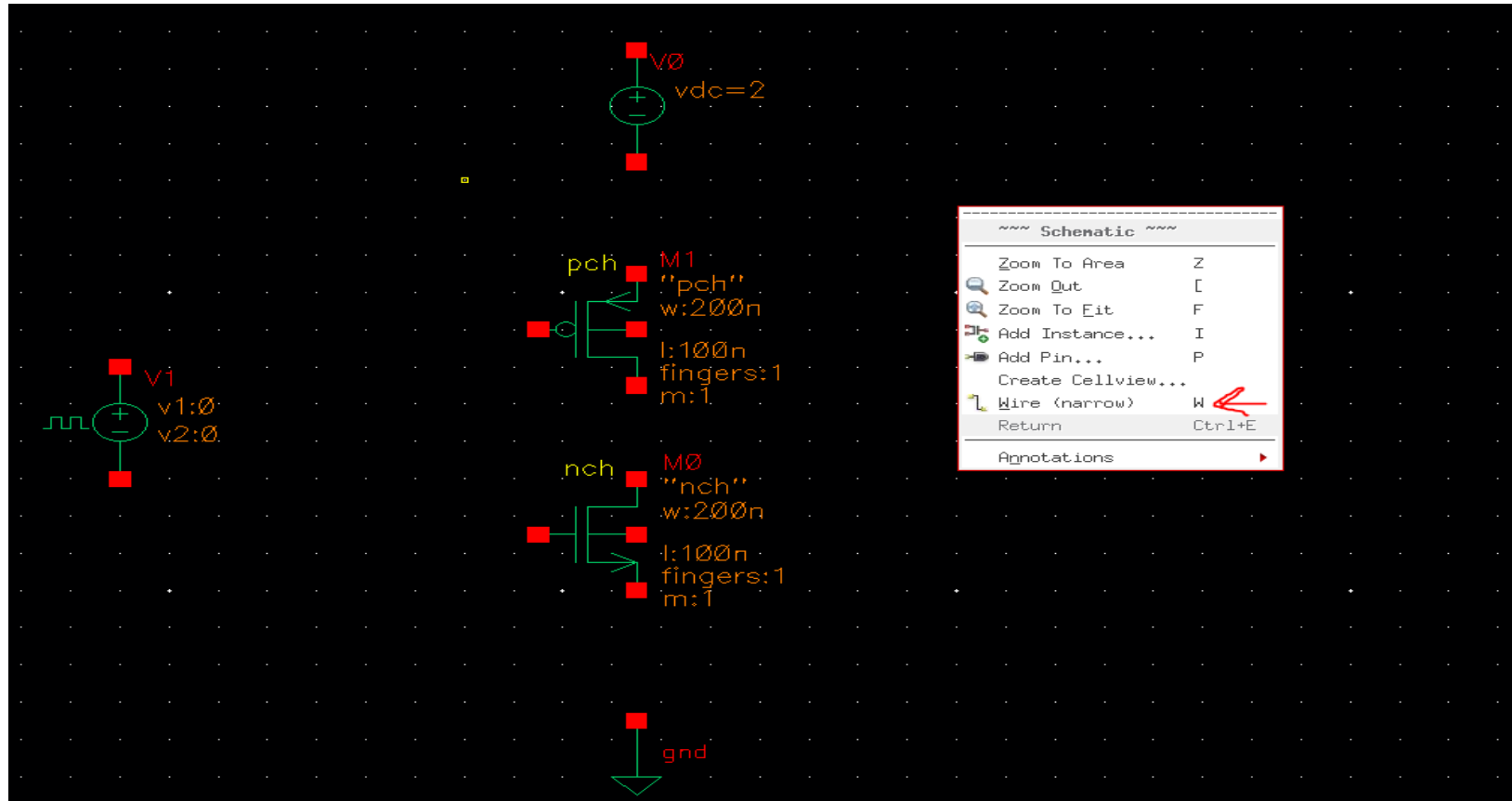
Messages

Log file is "/home/argorakca/projects/VLSI2Sp19/cadence/libManager.log".
Warning: Couldn't get an exclusive lock for "/vlsi/kits/tsmc/901p/tsmcN90rf/TransmissionLine.Cat"
Permission denied
Warning: ddDeleteDeep: Couldn't get exclusive lock on ddLibFileType 'TransmissionLine.Cat'.
Warning: ddCatRemove: unable to remove category TransmissionLine.
Warning: Couldn't get an exclusive lock for "/vlsi/kits/tsmc/901p/tsmcN90rf/TransmissionLine.Cat"
Permission denied
Warning: ddDeleteDeep: Couldn't get exclusive lock on ddLibFileType 'TransmissionLine.Cat'.
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Lib: analogLib Free: 131,67G

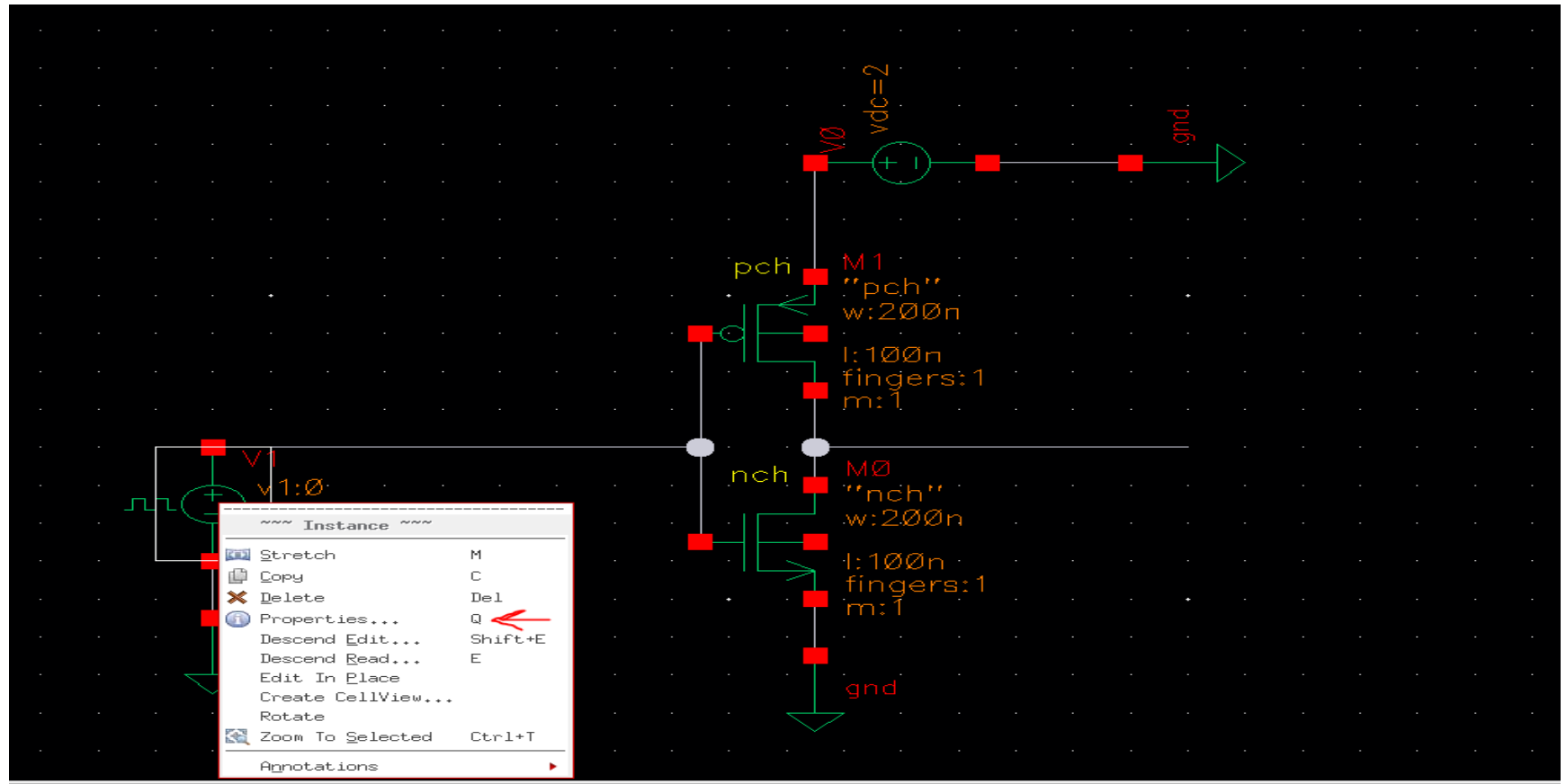


Full Custom Gate Design with Cadence





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Edit Object Properties (on boron10.comp.vlsi.labs)

Property	Value	Display
Library Name	analogLib	off
Cell Name	vpulse	off
View Name	symbol	off
Instance Name	V1	off
Add Delete Modify		
User Property	Master Value	Local Value
lvsIgnore	TRUE	off
CDF Parameter		
Frequency name for 1/peri		off
Noise file name		off
Number of noise/freq pair	0	off
DC voltage		off
AC magnitude		off
AC phase		off
XF magnitude		off
PAC magnitude		off
PAC phase		off
Voltage 1	0 V	off
Voltage 2	2 V	off
Period	2u s	off
Delay time		off
Rise time		off
Fall time		off
Pulse width		off
Temperature coefficient	1	off

Circuit Diagram:

The diagram shows a pulse source (V1) connected to a load. The source is labeled with $vdc=2$ and gnd . The load is labeled with $M1$ and $M0$. The source is also labeled with $+1$ and gnd .

Model Parameters:

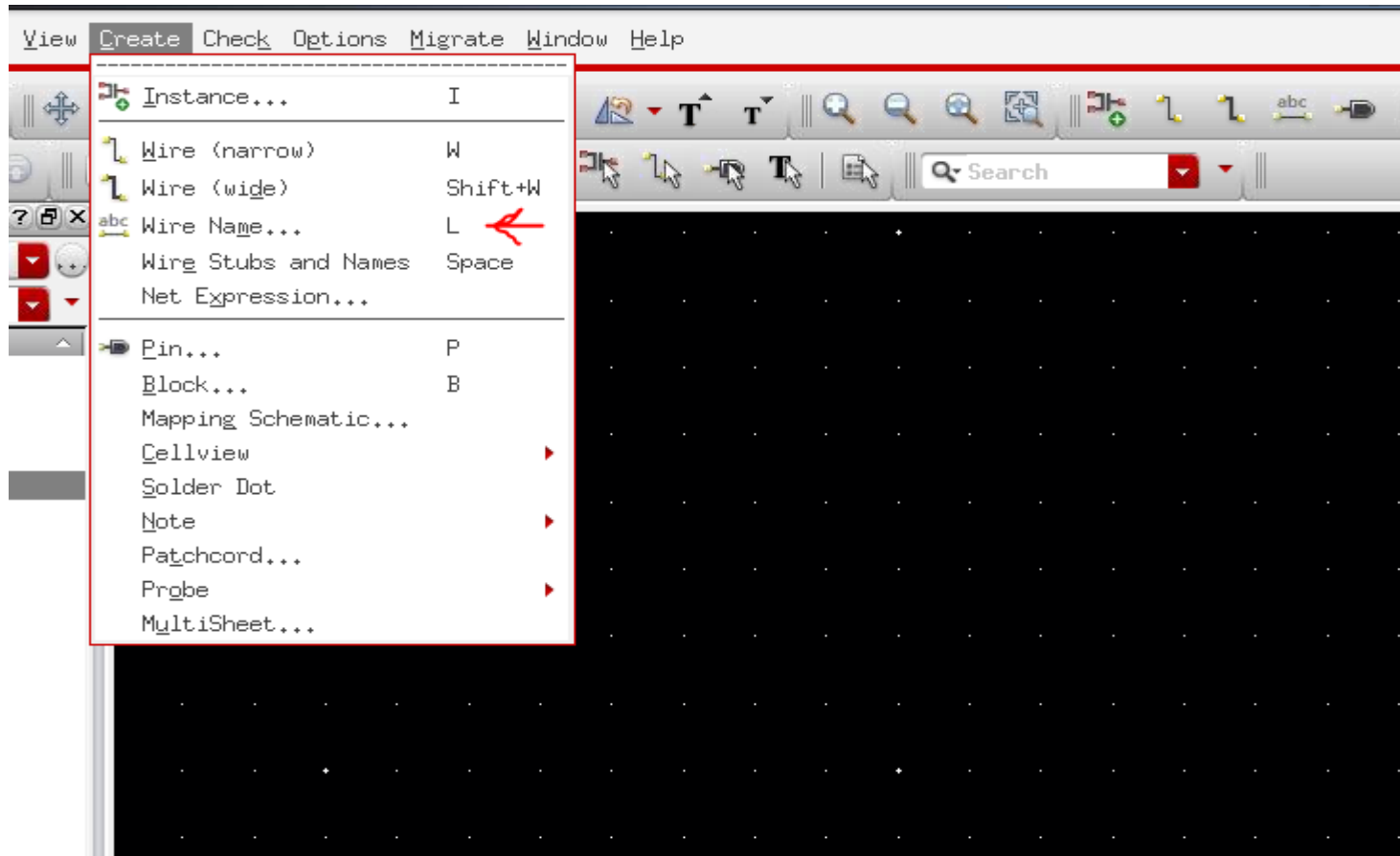
M1
"pch"
w:200n
l:100n
fingers:1
m:1

M0
"nch"
w:200n
l:100n
fingers:1
m:1

gnd

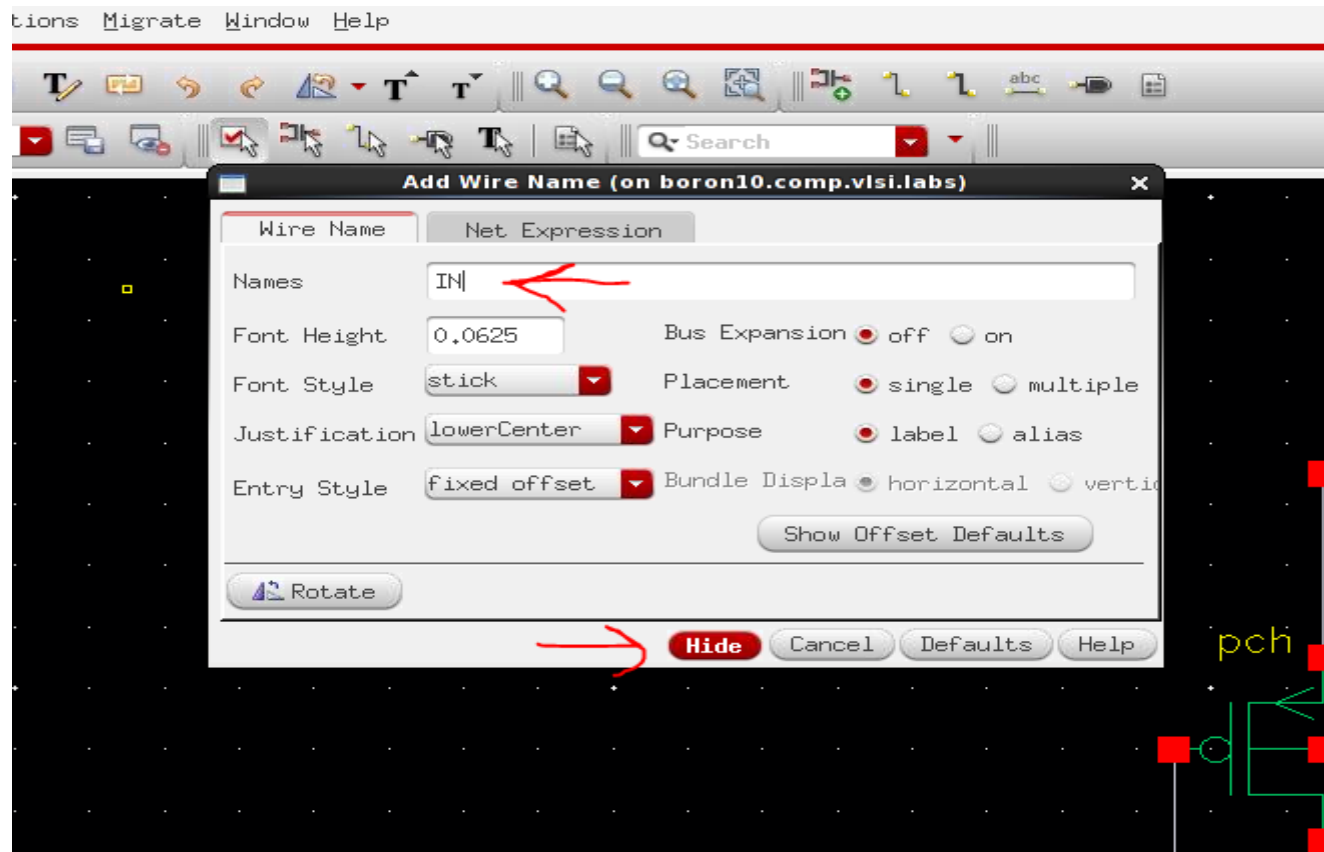


Full Custom Gate Design with Cadence



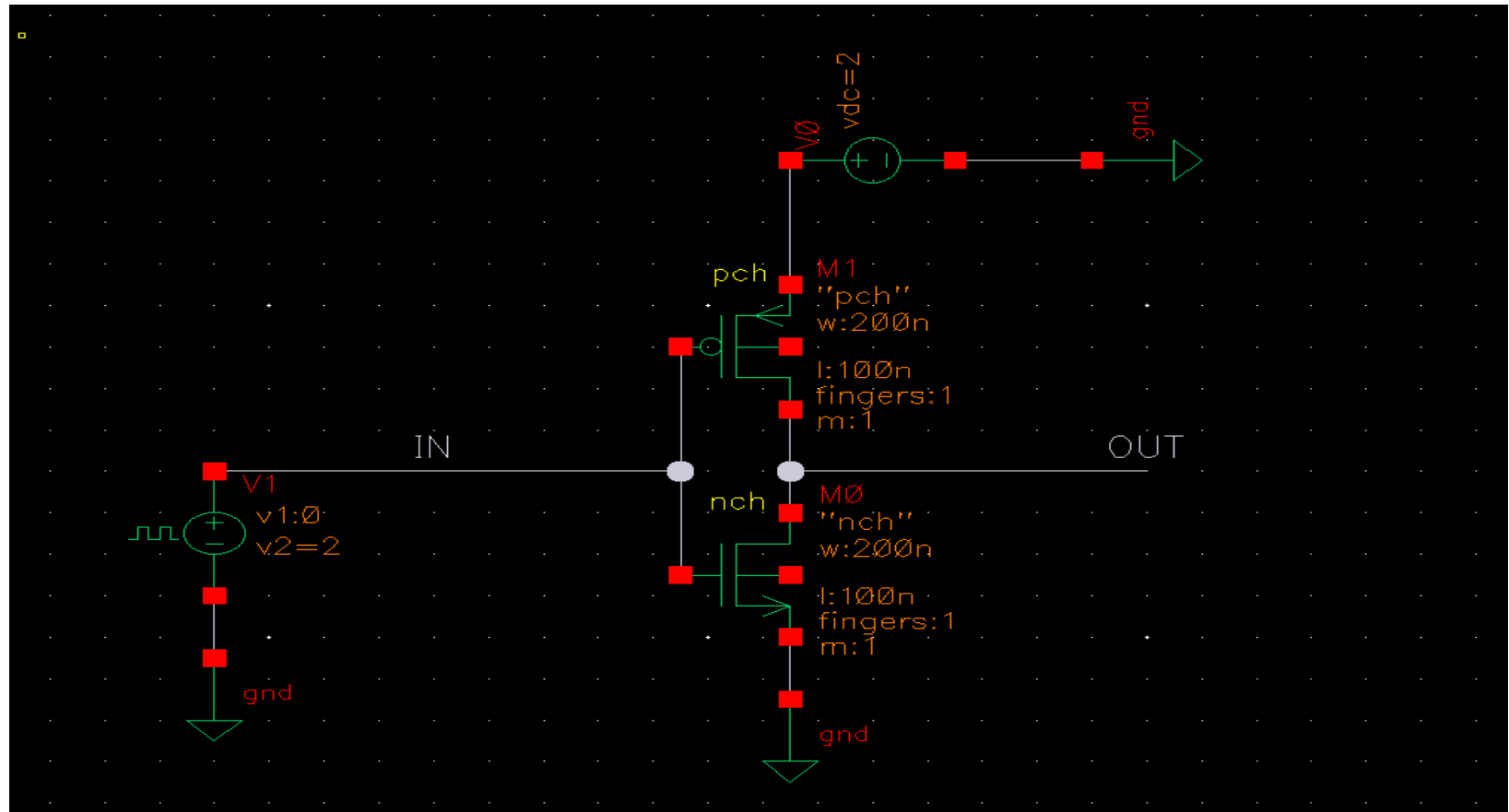


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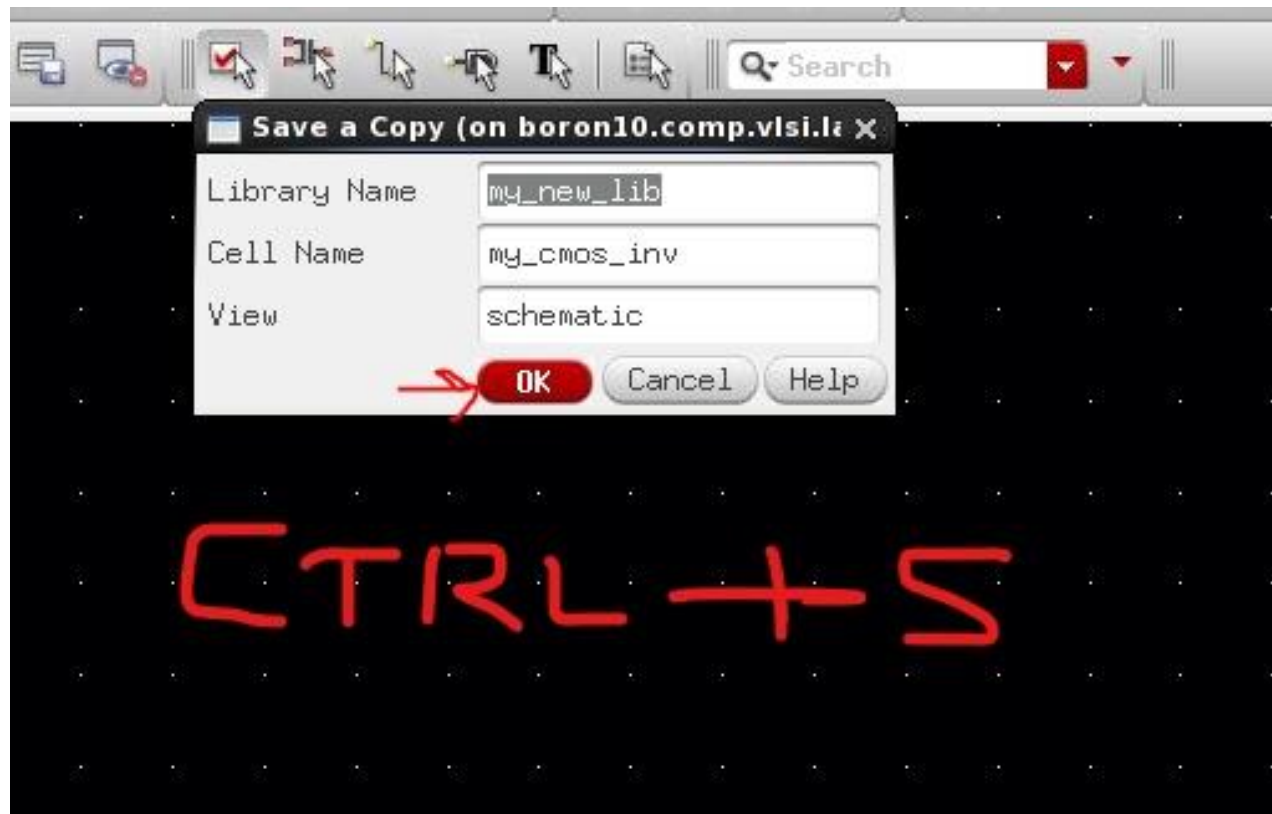


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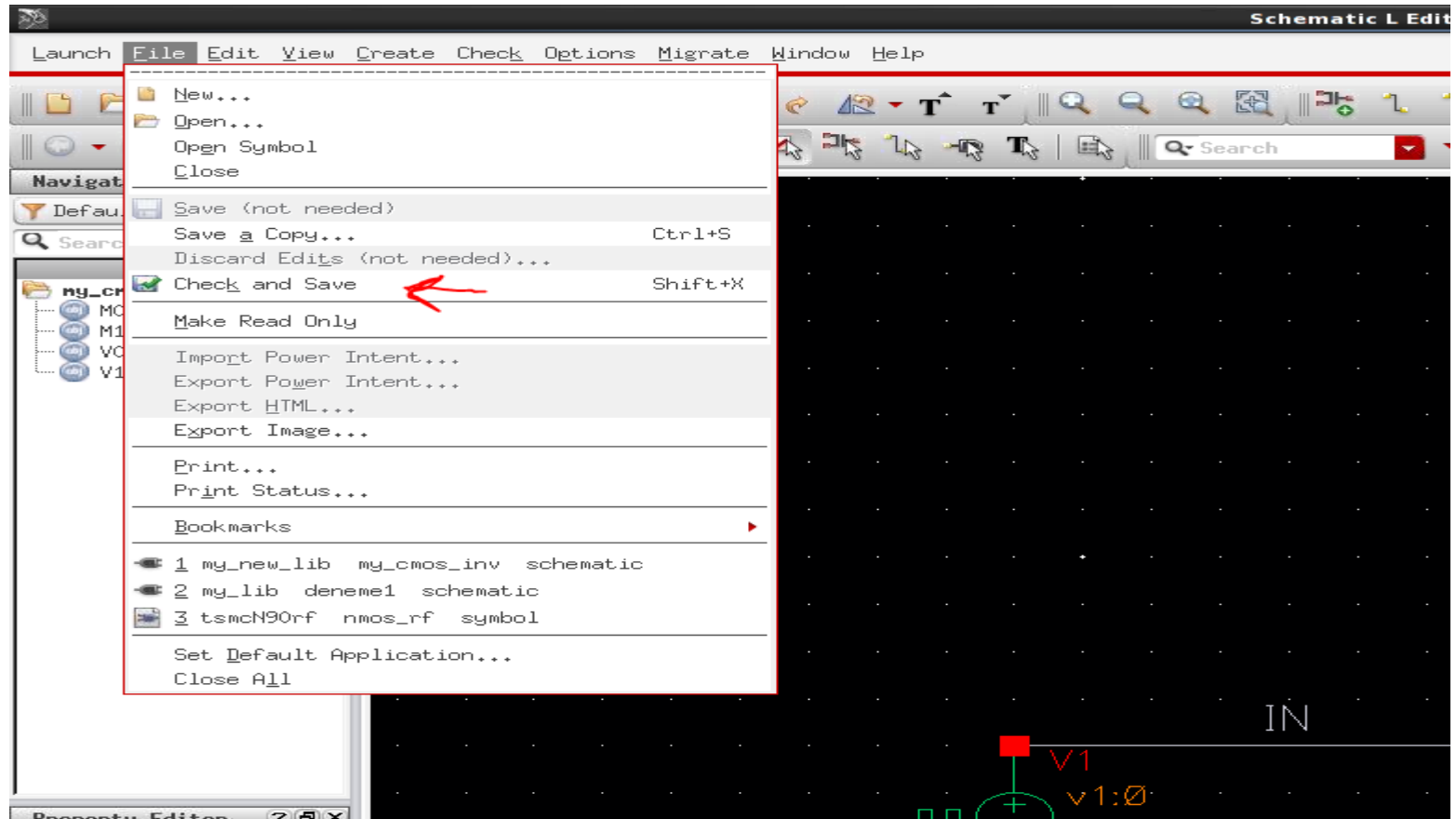


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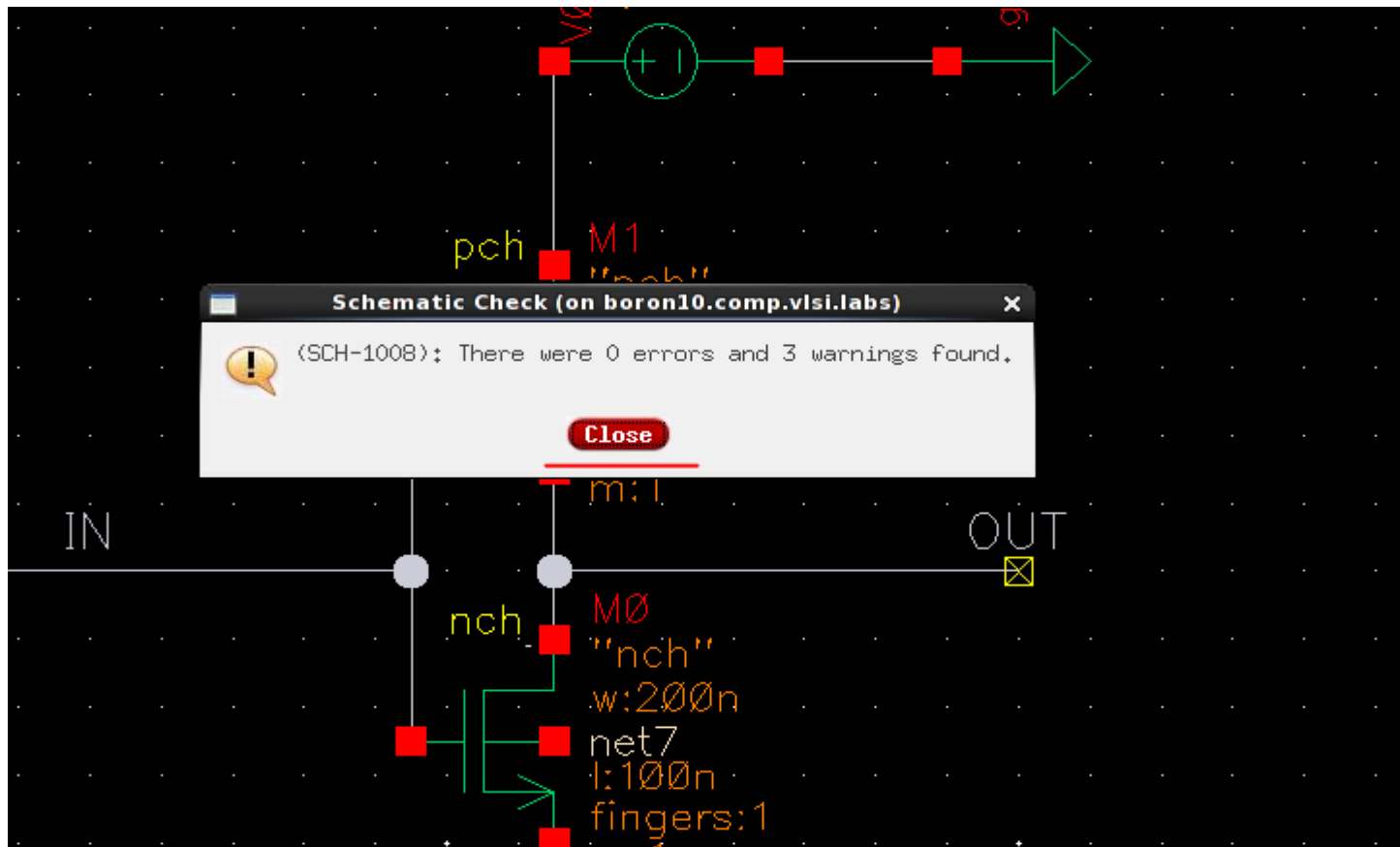


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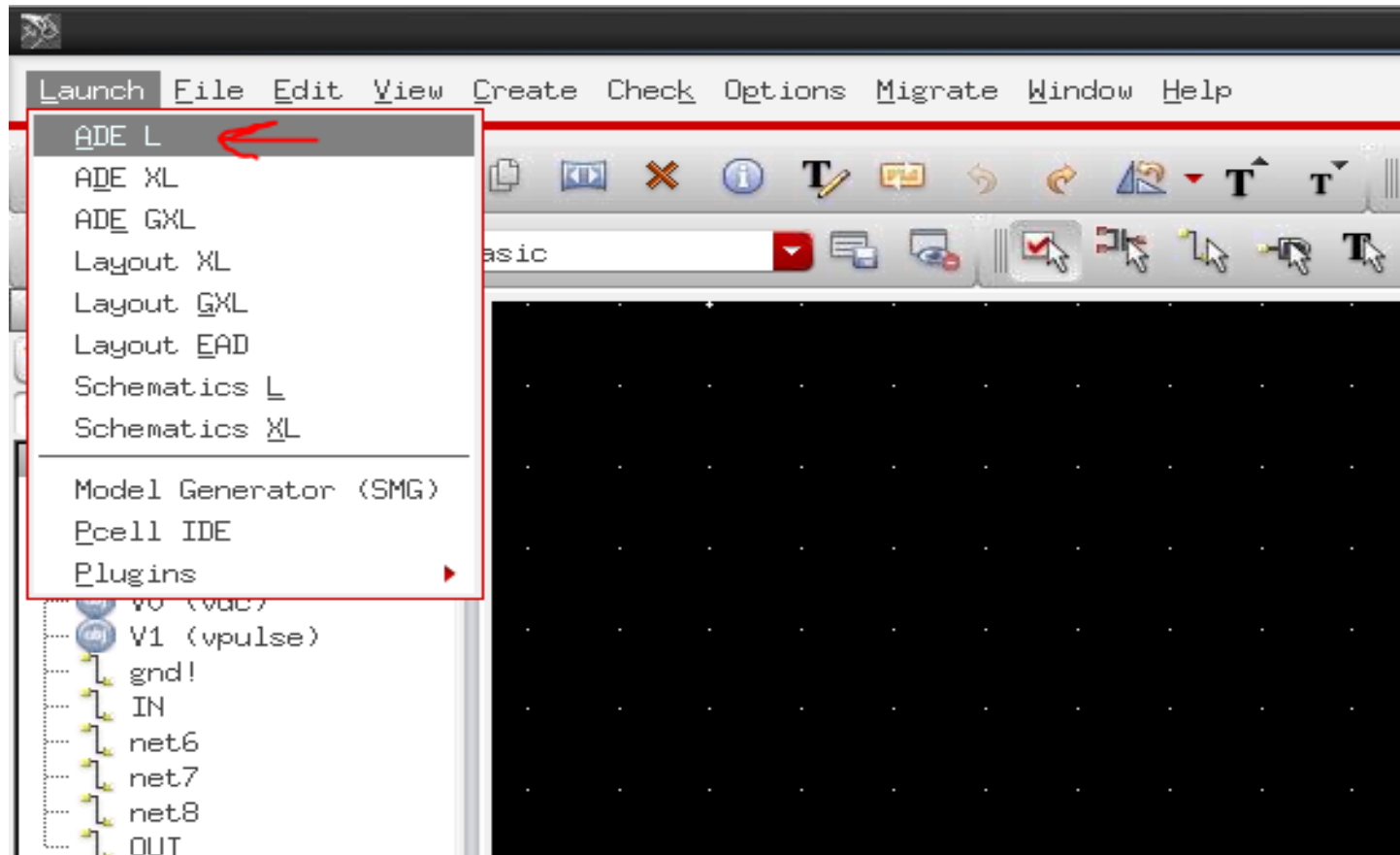


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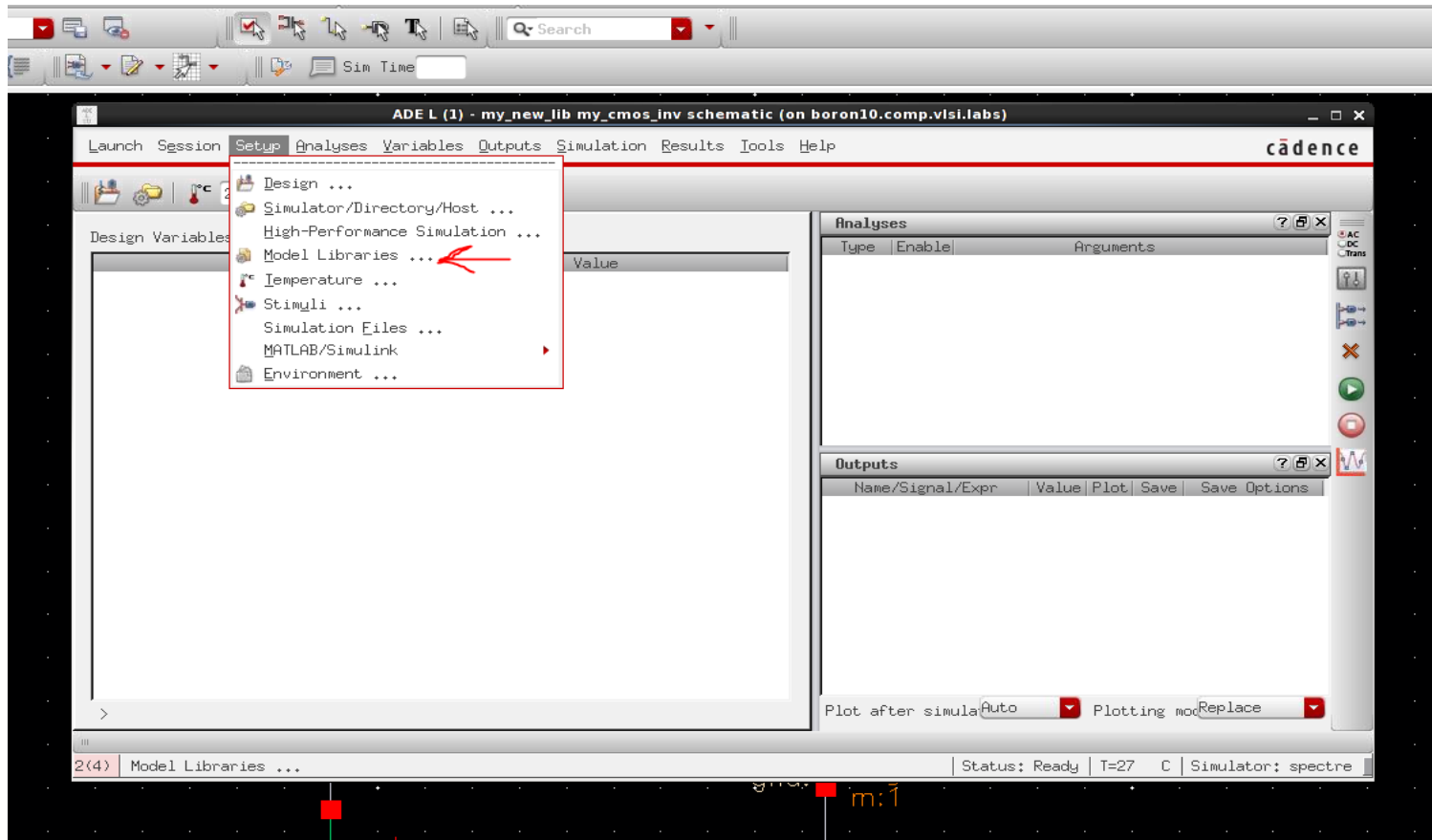


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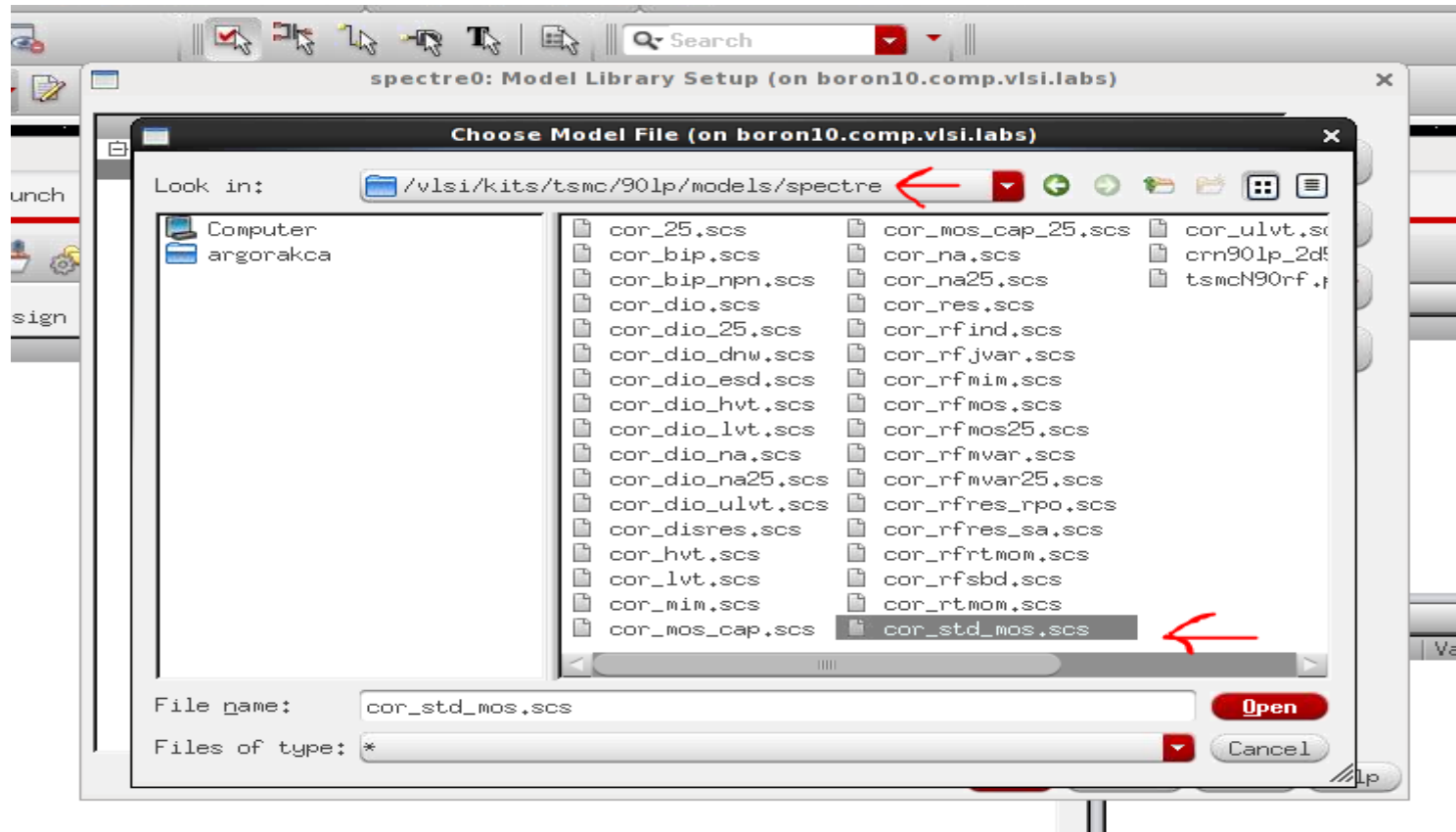


Full Custom Gate Design with Cadence



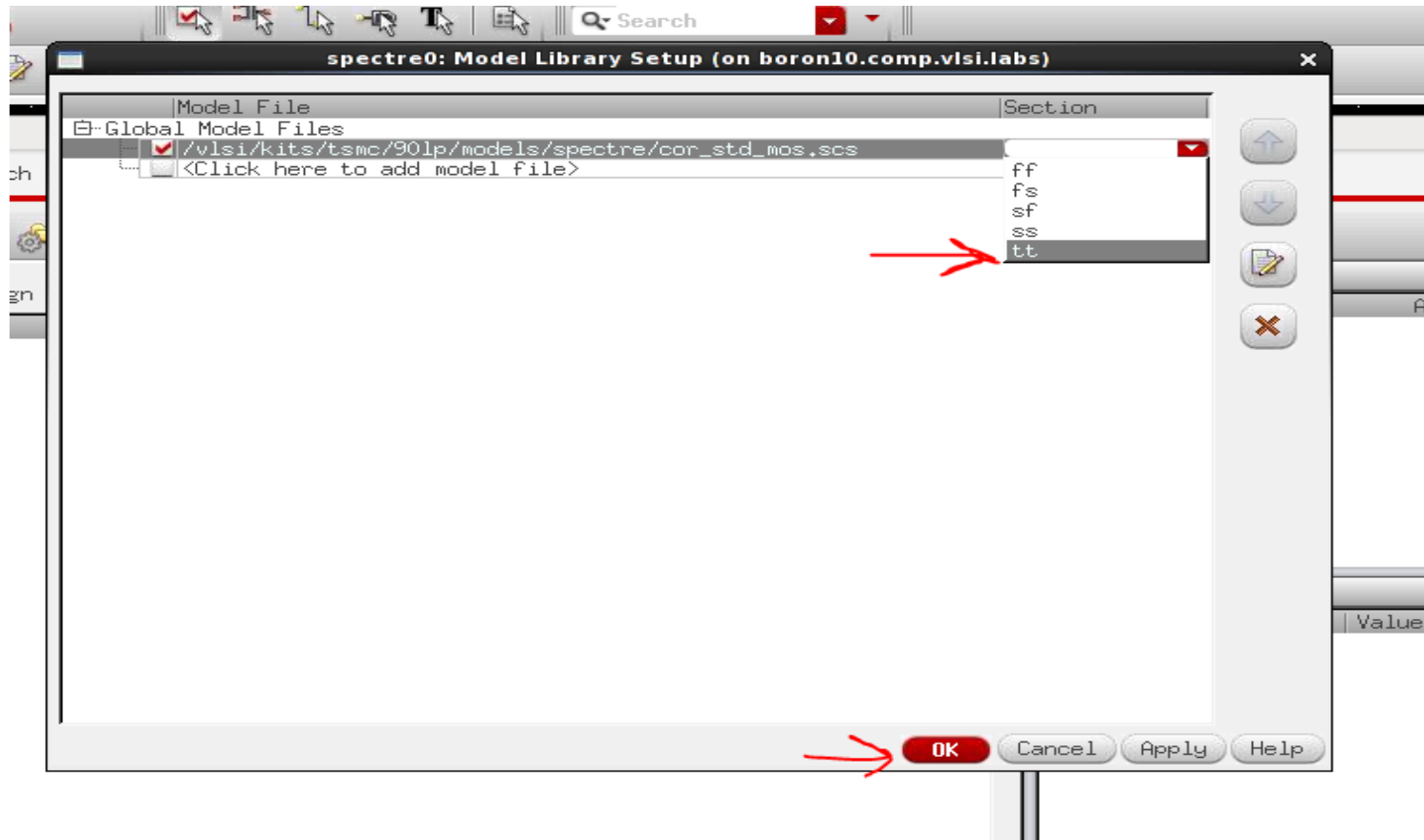


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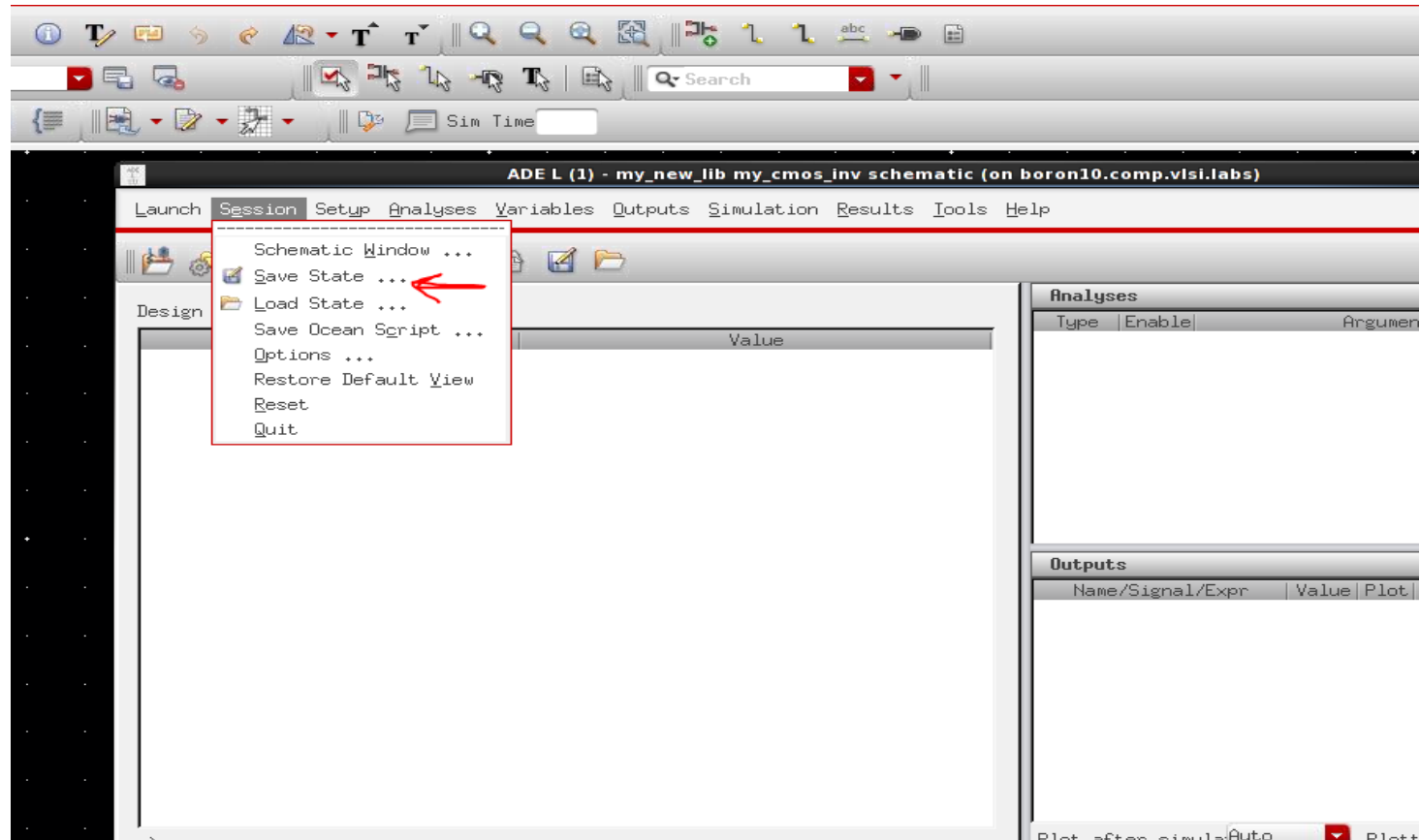


Full Custom Gate Design with Cadence



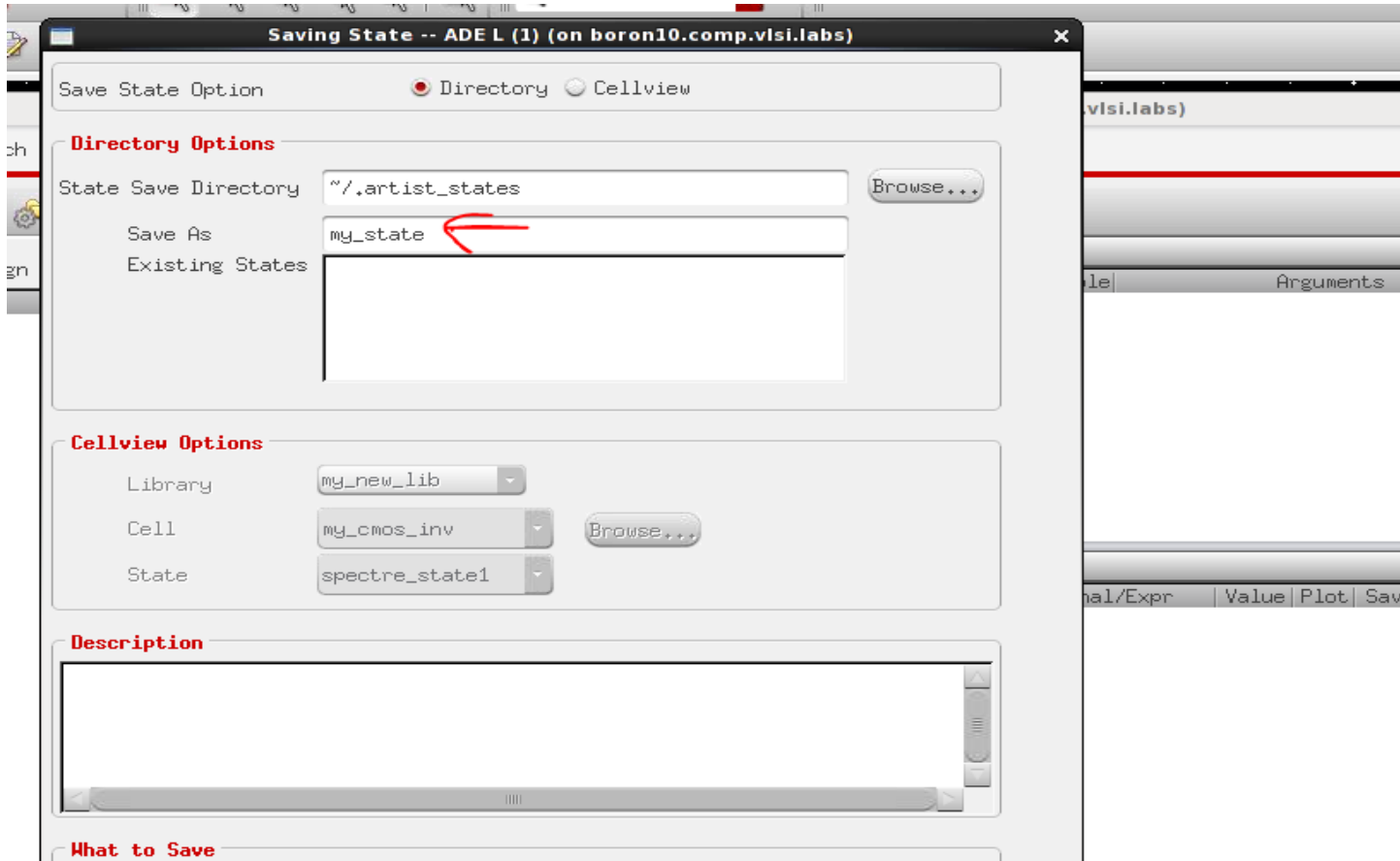


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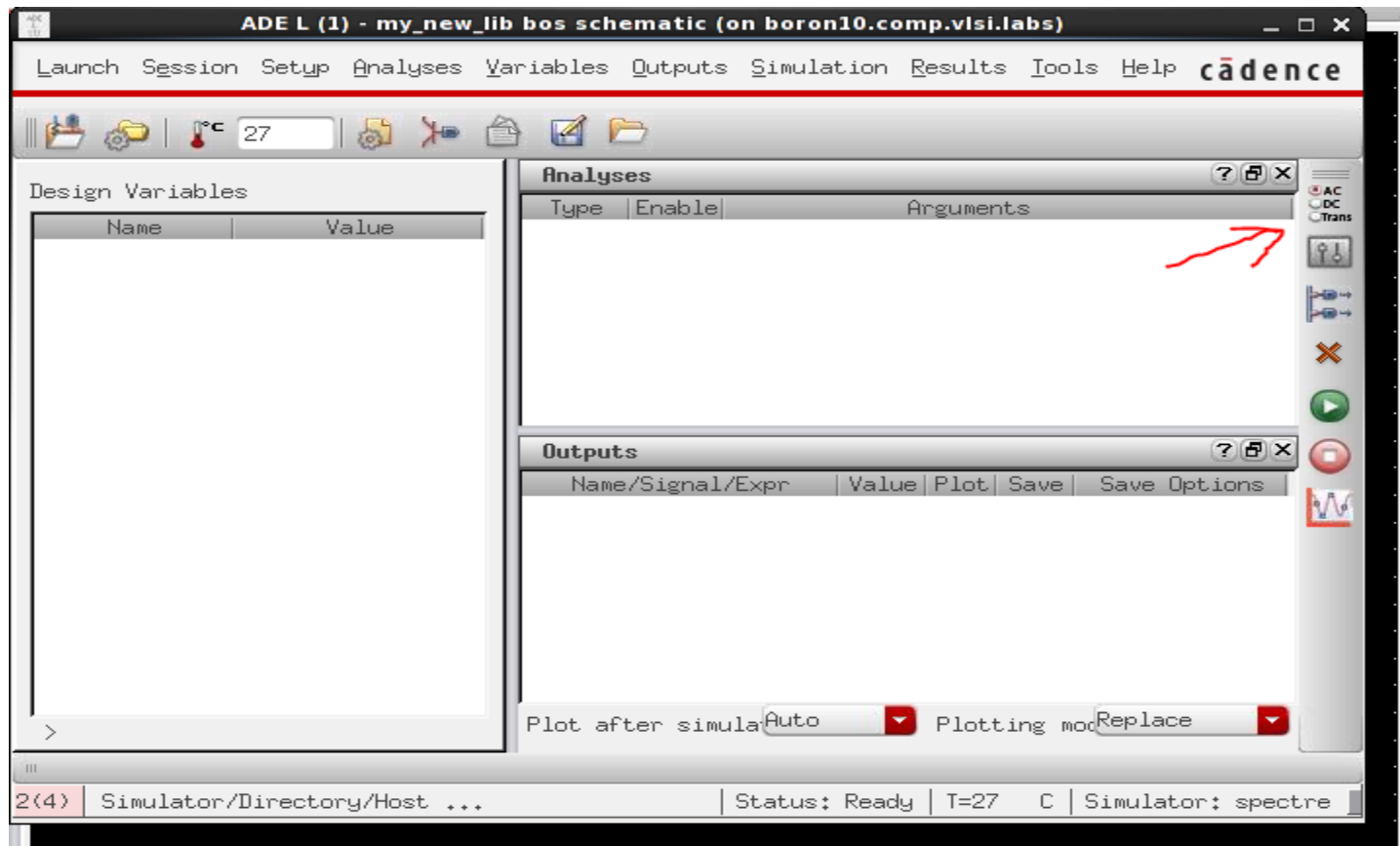


Full Custom Gate Design with Cadence



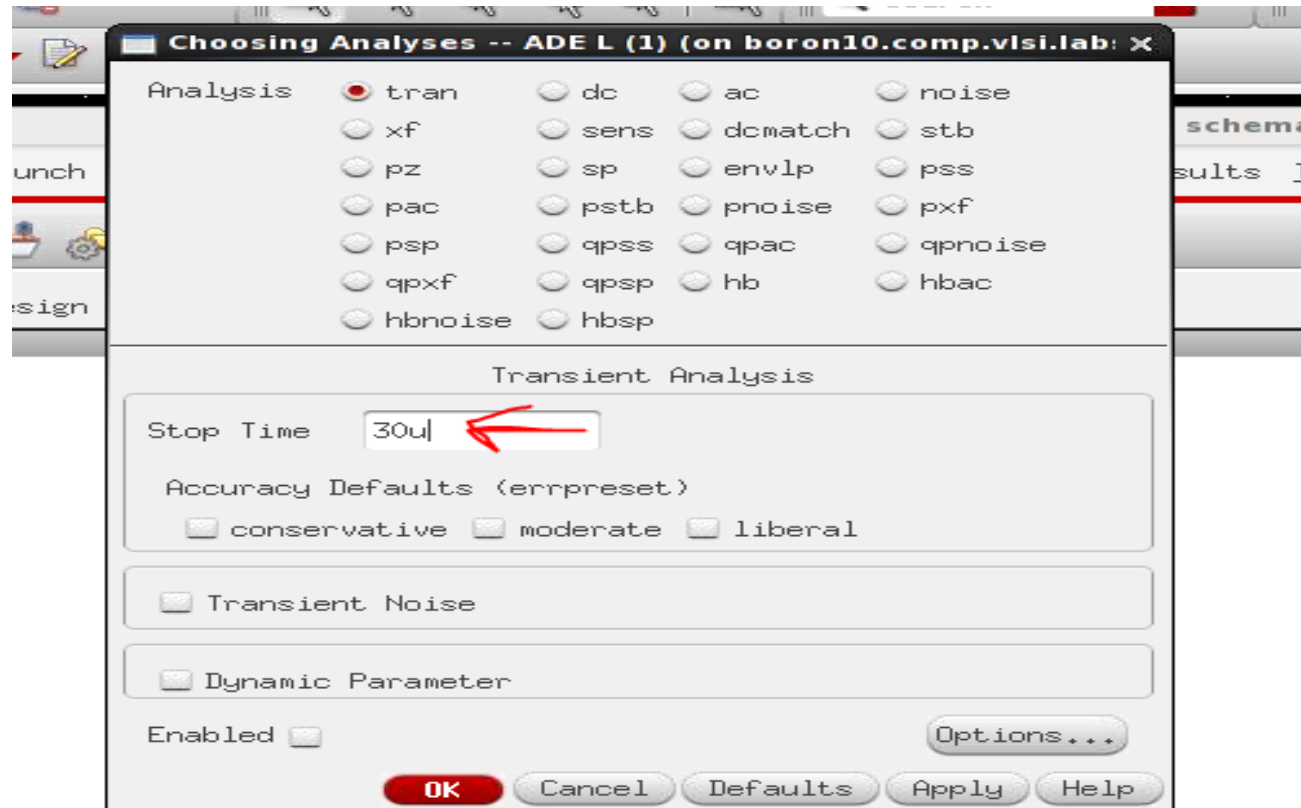


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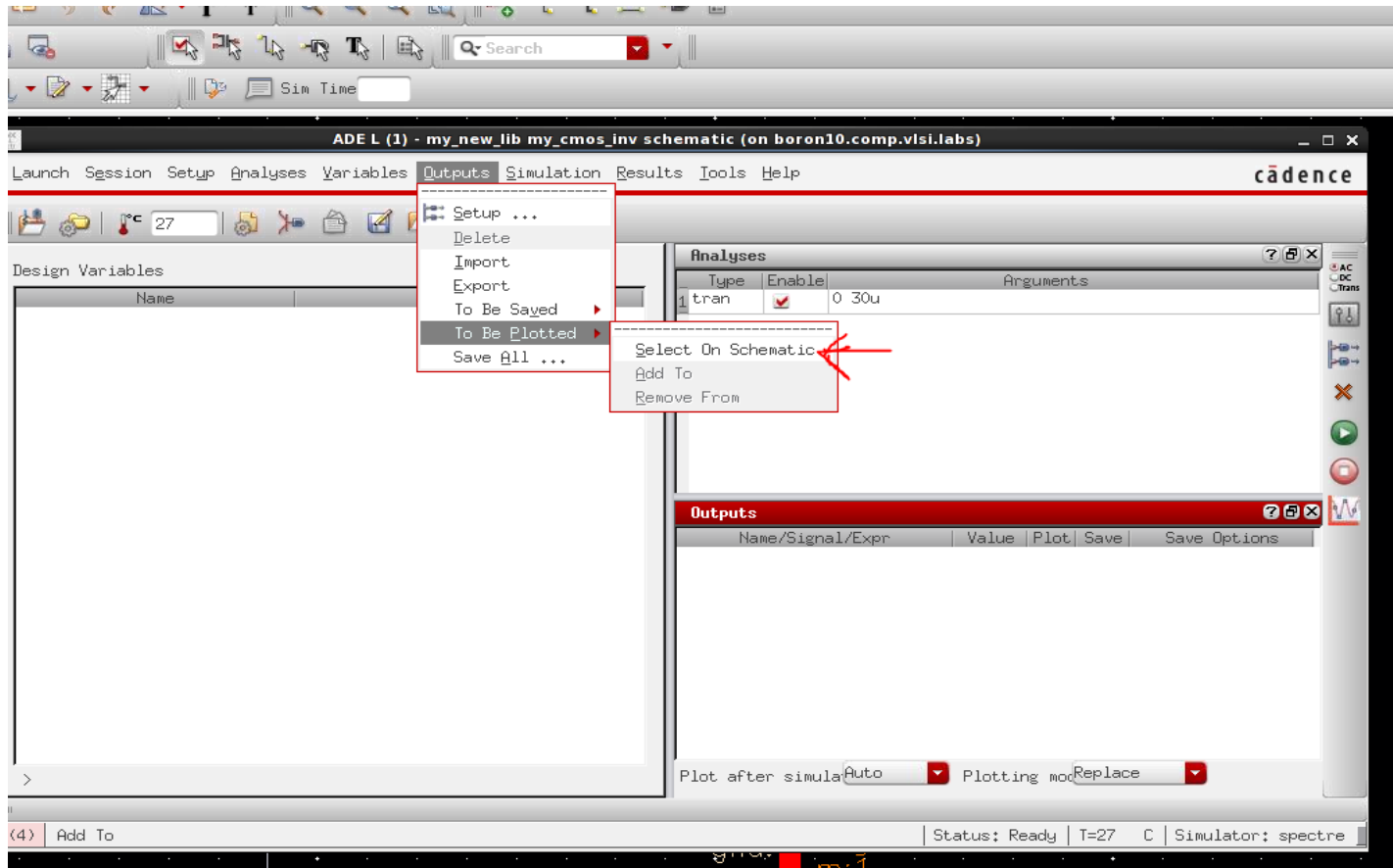


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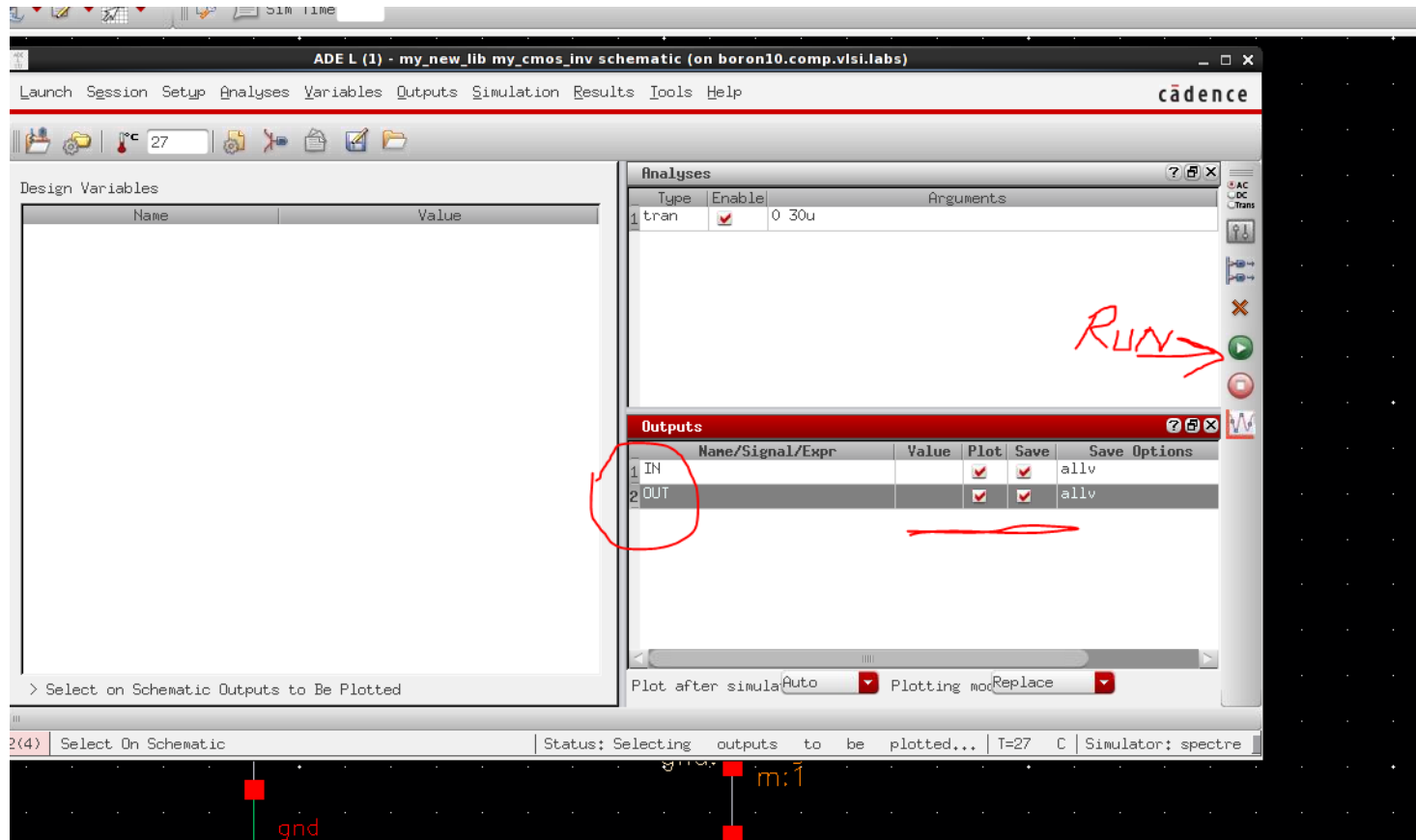


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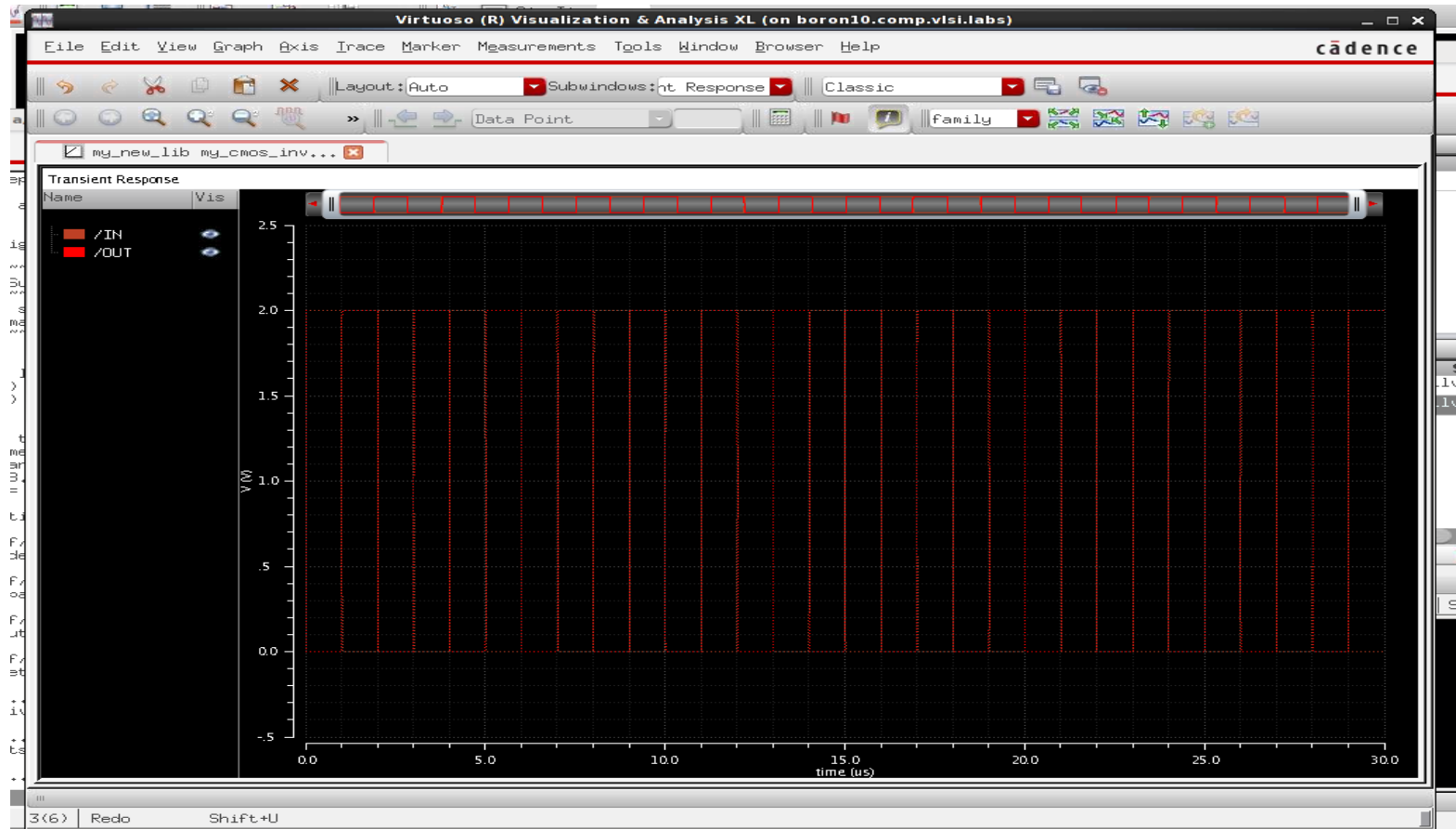


Full Custom Gate Design wiht Cadence



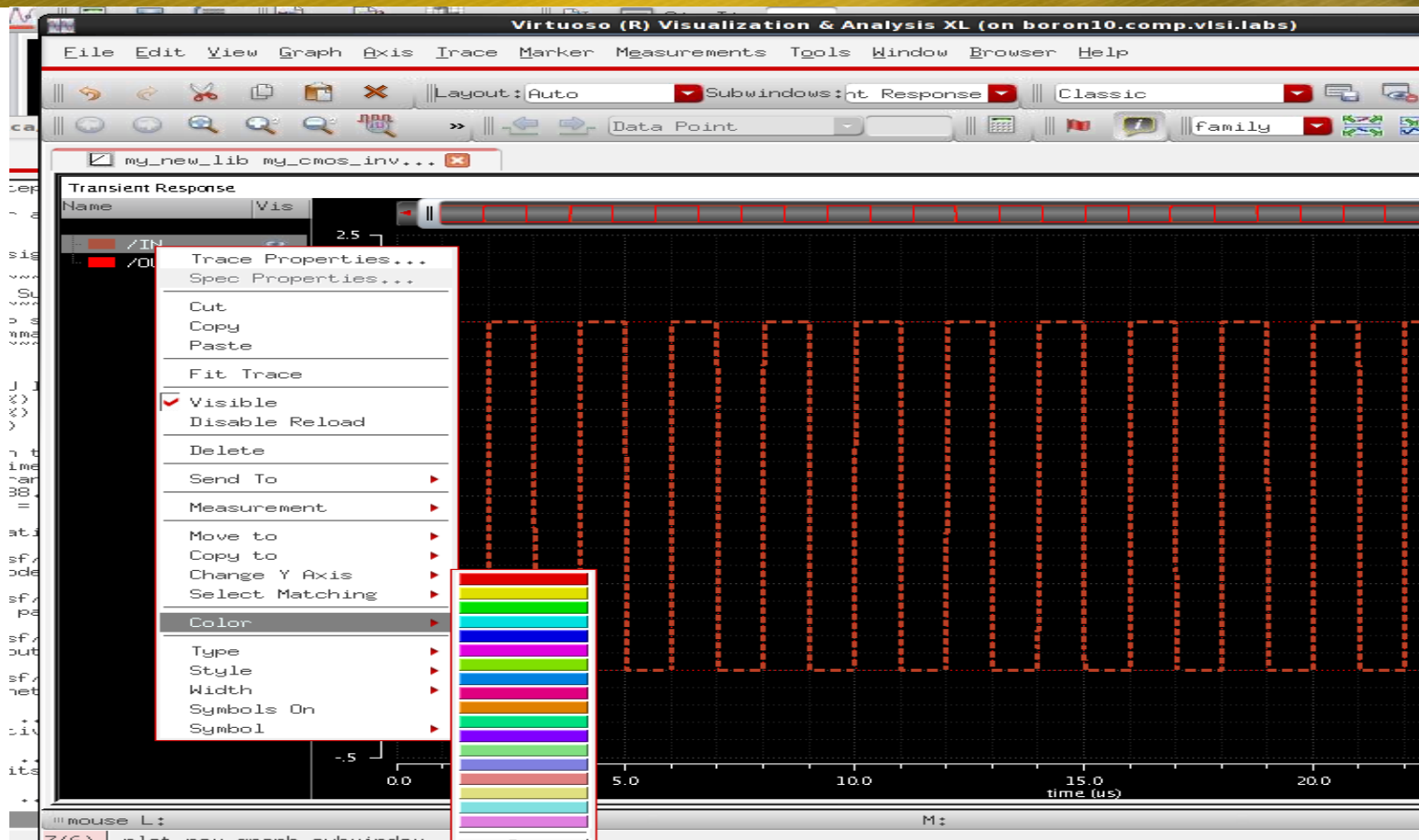


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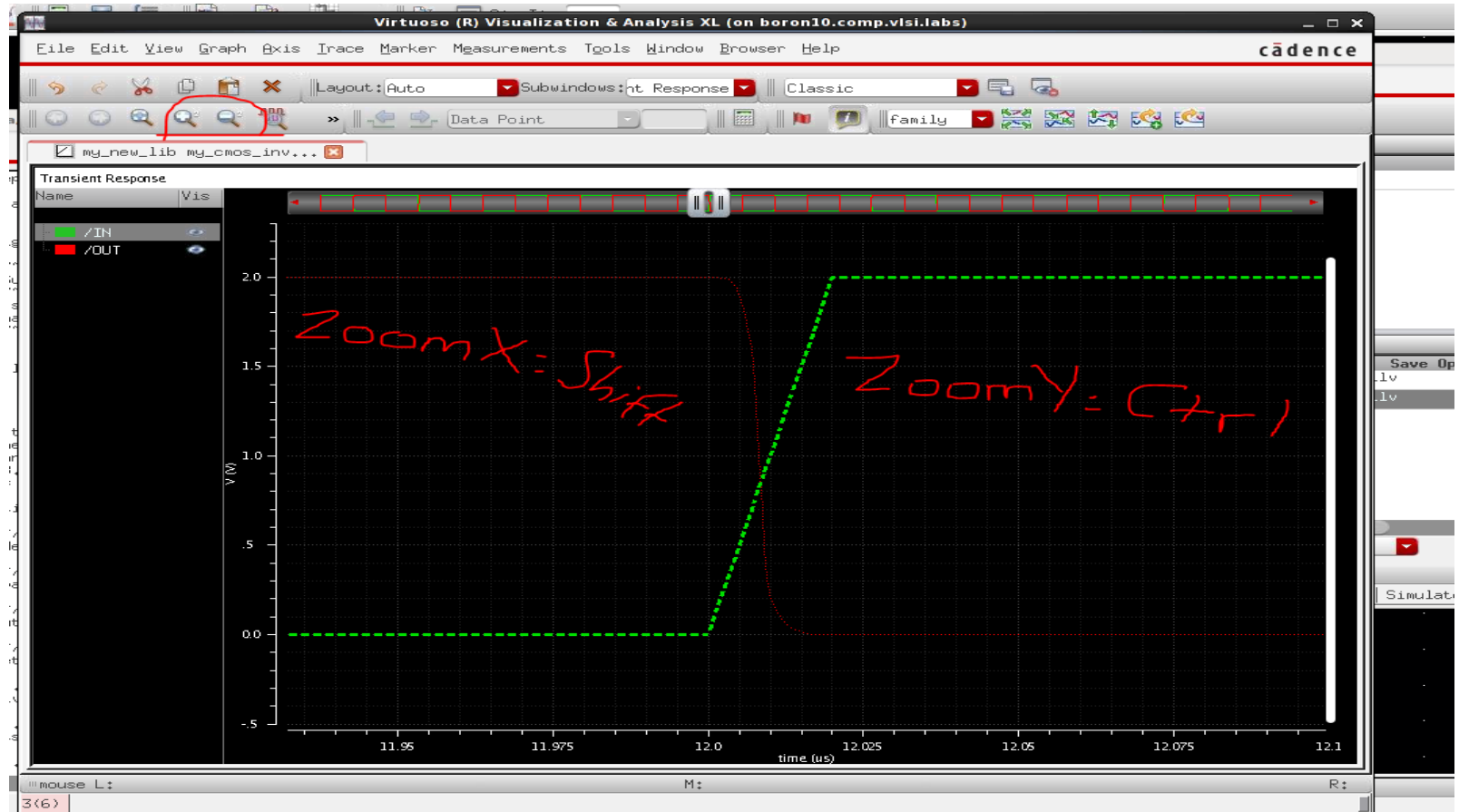


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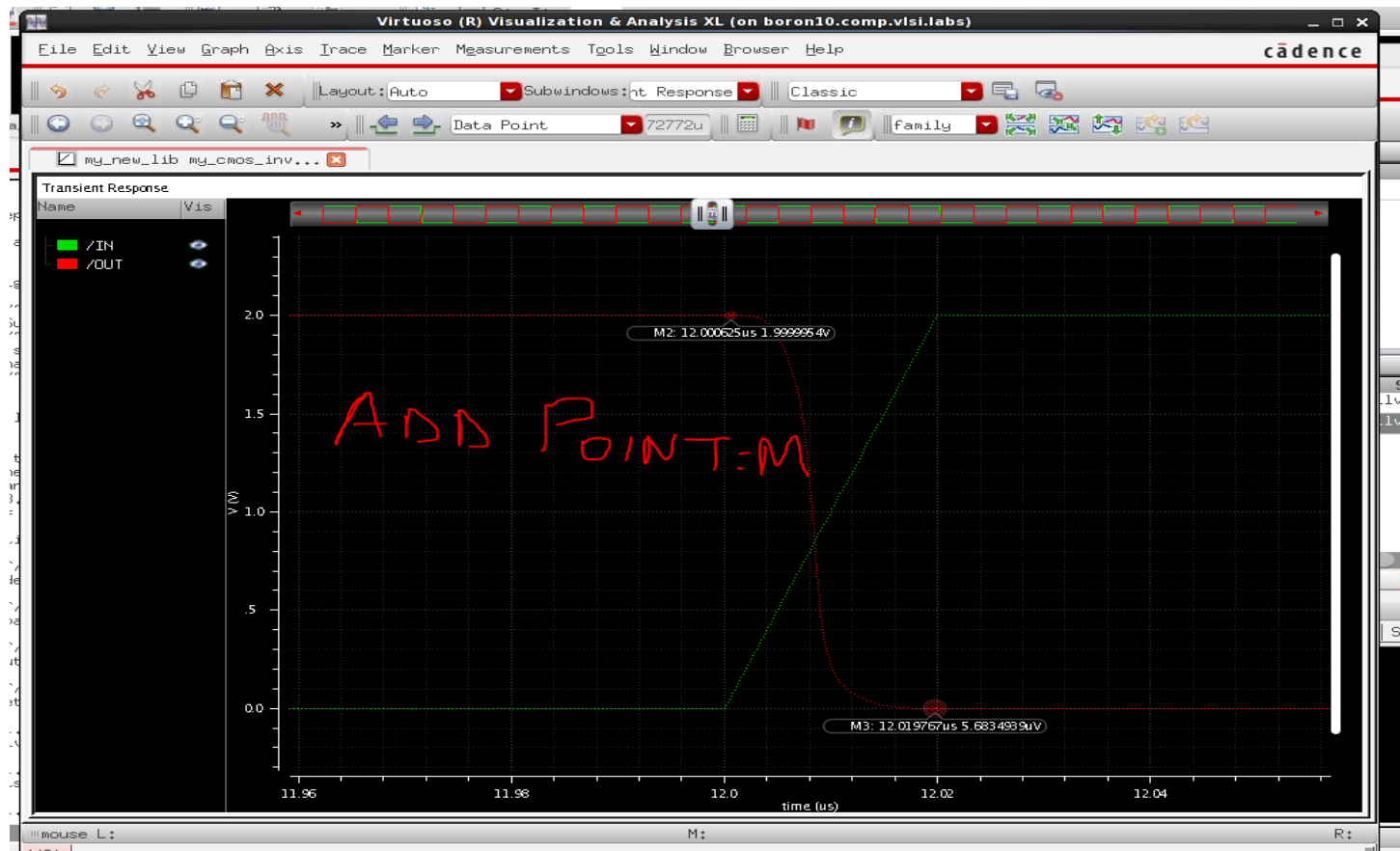


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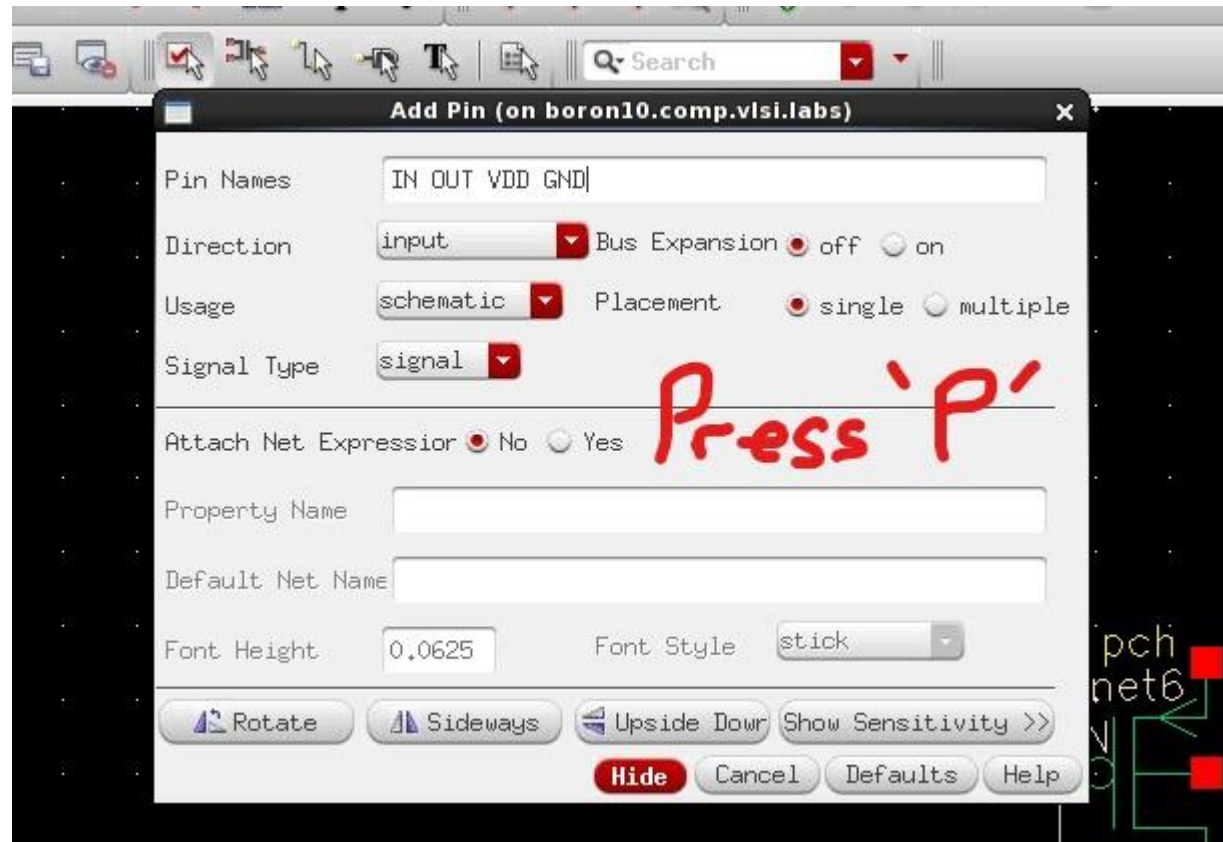


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