VLSI Circuit Design II– EHB 425E

HOMEWORK I

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1- RIPPLE CARRY ADDER

A digital circuit called a ripple carry adder is used to add binary values. Because each bit addition "ripples" a carry bit to the following stage of the adder, it is known as a ripple carry adder. Each bit of the input operands and the carry from the previous stage are added together using a complete adder in a ripple carry adder. The carry bit is propagated to the following stage, and the output of the current stage is the sum bit of the entire adder. The ripple carry adder's main drawback is the length of time required for carry propagation from one stage to the next.

Ripple Carry Adder Advantages[1]:

- With simple digital logic gates, designs and implementations are simple.
- Since the circuit is modular, more bits can be readily added.
- Designers can readily comprehend and alter the circuit.

Ripple Carry Adder Disadvantages[1]:

- With high numbers of bits, the time delay in carry propagation can become significant, slowing down the circuit's overall speed.
- The output may experience glitches as a result of the carry propagation delay, which may require additional circuitry to filter out.
- Due to the necessity to propagate carry bits throughout the circuit, ripple carry adders may have higher power requirements than other adder types.

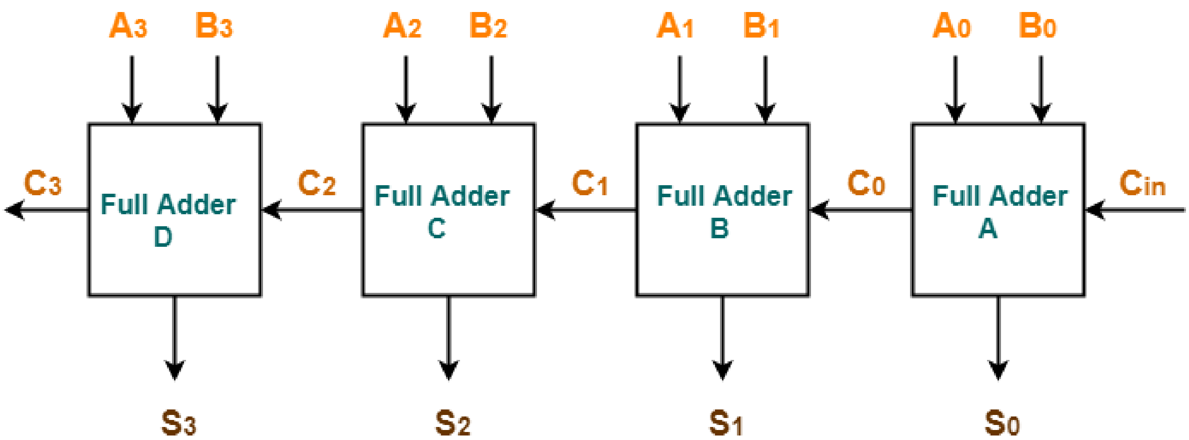

Figure 1 Ripple Carry Adder [1]

2- CARRY LOOKAHEAD ADDER

A digital circuit called a carry lookahead adder (CLA) is used to add binary digits. It is known as a lookahead adder because it generates the carry signals for each stage of the adder using a lookahead mechanism rather than relying on the carry from the stage before. In a CLA, a succession of logic gates that examine the input operands and produce the carry signals based on the carry lookahead equations generate the carry signals for each stage. Based on the input operands and the carry signals from the preceding stages, the carry lookahead equations calculate the carry signal for each stage.

Carry Lookahead Adder Advantages[1]:

- The circuit can run more quickly than a ripple carry adder since the carry signals for each step are generated in parallel.
- The propagation latency of the circuit is fixed and unaffected by the number of bits being added.
- Adding more bits to the circuit is a simple process that won't influence the propagation delay.

Carry Lookahead Adder Disadvantages[1].

- It takes more logic gates to create the circuit since it is more complicated than a ripple carry adder.
- Due to the extra logic gates and interconnects, the circuit may use more power than a ripple carry adder.
- For adding small numbers of bits, the circuit might not be the most effective since the overhead of the lookahead method might balance the advantages of the fixed propagation delay.

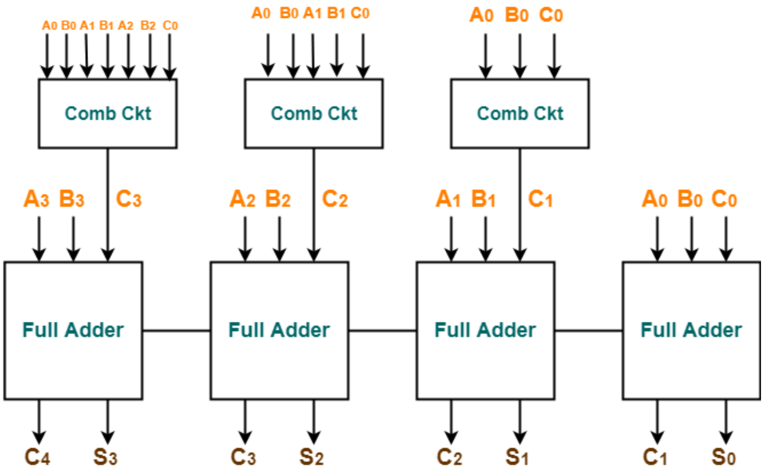

Figure 2 Carry Lookahead Adder [1]

$P_i = A_i \oplus B_i$ ➔ where P is called carry propagator $S_i = P_i \oplus C_i$

$G_i = A_i * B_i$ ➔ where G is called carry generator $C_{i+1} = G_i + P_i C_i$

3- CARRY SELECT ADDER

A digital circuit called a Carry Select Adder (CSA) is used to add binary digits. Because it generates the carry signals at each stage of the adder using a carry select mechanism, the device is known as a carry select adder. In a CSA, the input operands are split into two groups and added using different ripple carry adders for each group. The right sum output is then chosen from a group of multiplexers using the carry output from each of these adders. Depending on the carry input to the multiplexer, the multiplexers output the sum from either the first or second ripple carry adder.

Carry Select Adder Advantages:

- The propagation latency in the circuit is fixed and unaffected by the number of bits being added. [2]
- Adding more bits to the circuit is a simple modification that won't alter propagation delay. [2]
- By splitting the input operands into two groups and adding them in parallel, the circuit can work more quickly than a ripple carry adder.[3]

Carry Select Adder Disadvantages:

- Due to the extra logic gates and interconnects, the circuit may use more power than a ripple carry adder. [2]
- It takes more logic gates to create the circuit since it is more complicated than a ripple carry adder. [3]
- For adding small numbers of bits, the circuit might not be the most effective since the overhead of the carry choose mechanism might outweigh the advantages of the fixed propagation delay. [3]

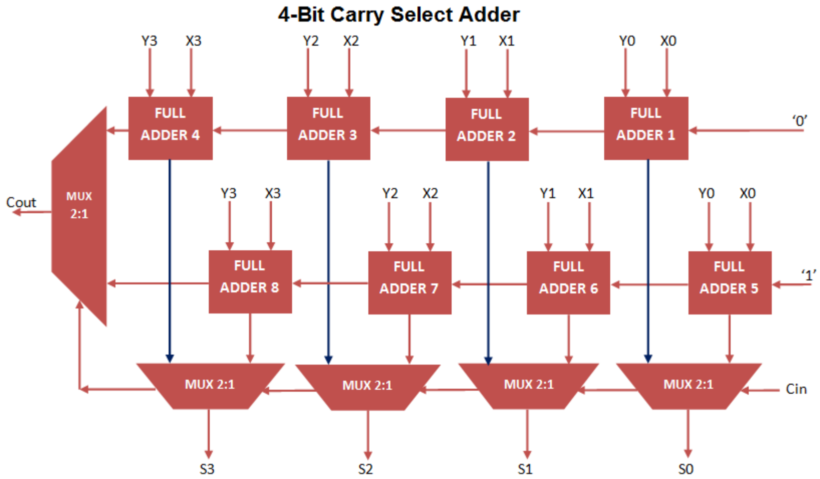

Figure 3 Carry Select Adder[4]

4- CARRY SKIP ADDER

A digital circuit called a carry skip adder (CSA) is used to add binary values. The device is also known as a Kogge-Stone adder or a Carry Bypass Adder. By allowing carry signals to skip over intermediate stages in the adder, the CSA's main goal is to decrease the delay of a ripple carry adder. With a CSA, the input operands are split up into various groups of bits that can all be processed simultaneously. The carry signals for the following group of bits are produced by a carry look-ahead adder at the end of each group. The final sum is then calculated by combining each group of bits' output.

Carry Skip Adder Advantages:

- Because carry signals can skip through intermediate stages of the adder, the circuit processes data more quickly than a ripple carry adder. [3]
- Because it uses fewer logic gates and multiplexers than a carry select adder, the circuit is simpler. [2]

Disadvantages of a Carry Skip Adder:

- Even with a carry select adder, the circuit may still have a longer propagation delay, especially if there are many bits being added. [3]
- Because there are additional gates and interconnects, the circuit might use more power than a ripple carry adder. [2]

Overall, the Carry Skip Adder strikes a fair balance between a carry select adder's complexity and fixed propagation time and a ripple carry adder's efficiency and speed. The specific application needs and design limitations determine the adder to use.

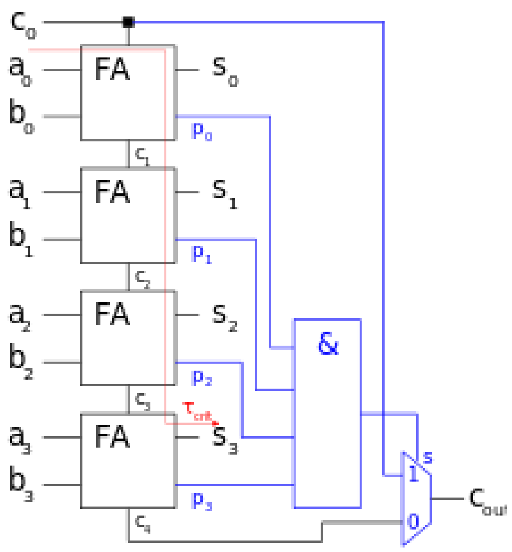

Figure 4 Carry Skip Adder[5]

5- CARRY SAVE ADDER

A digital circuit called a carry save adder (CSA) is used to add many binary values simultaneously. The main benefit of CSA is that it decreases the number of stages necessary to do addition, which leads to a quicker processing time and less power usage. With a CSA, the input operands are split up into various groups of bits that can all be processed simultaneously. Then, for each group, a separate register is used to store the sum and carry output. The final adder, which is coupled to these registers, computes the total sum of all the input operands.

Carry Save Adder Advantages :

- CSA is more effective than a ripple carry adder because it cuts the number of stages needed to conduct addition, which decreases processing time. [3]
- By obviating the necessity for intermediate carry propagation, CSA also lowers the adder's power consumption.[3]
- To minimize the number of operations necessary to complete the computation, CSA can also be utilized as an intermediate stage in circuits with greater complexity, such as multipliers and filters. [2]

Carry Save Adder Disadvantages:

- To store the intermediate findings, the circuit needs extra registers, which might lengthen the circuit's latency and expand its area. [3]
- The additional logic needed by CSA to integrate the output from the intermediate registers can make the circuit more complex. [2]

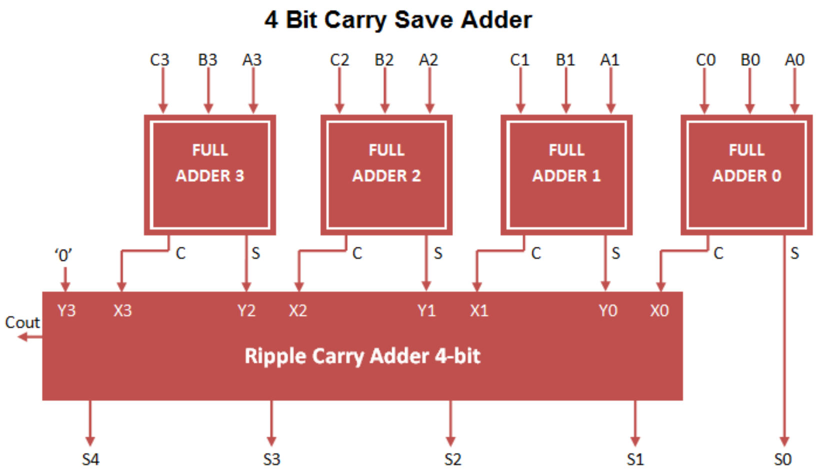

Figure 5 Carry Save Adder[6]

6- CARRY INCREMENT ADDER

A digital circuit called a carry increment adder (CIA) is used to quickly add binary values. It is a variation of the Carry Select Adder (CSA) that makes the circuit simpler by lowering the quantity of AND gates needed to produce the carry lookahead signals. In a CIA, a partial adder is used to process each set of bits first, producing a sum and carry-out bit. After that, a succession of carry increment gates process each group's carry-out bit to produce a carry-in bit for the following group. The carry-in and sum bits from the previous group are added to get the final sum.

Carry Increment Adder Advantages :

- CIA uses fewer gates than the Carry Select Adder and is faster and more power-efficient than the Ripple Carry Adder (RCA) (CSA). [7]
- In high-performance computing systems like CPUs and digital signal processors, CIA is well suited for arithmetic operations. [7]

Carry Increment Adder Disadvantages:

- Additional carry increment gates are needed for CIA, which can complicate and enlarge the circuit. [7]
- CIA might not be appropriate for all addition operations, especially when multiplying values with a lot of bits. [7]

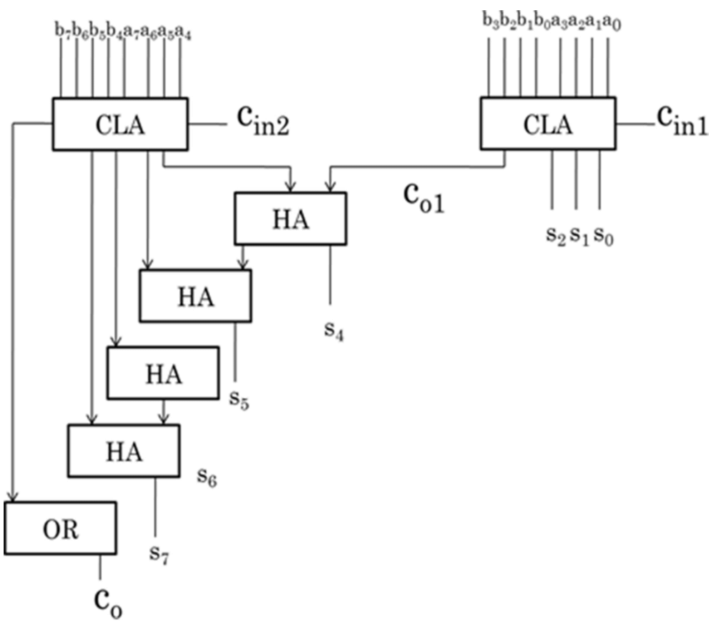

Figure 6 Carry Increment Adder[8]

7- PREFIX ADDER

A sort of digital circuit called a prefix adder is used to quickly add binary values. A Sklansky Adder or a Logarithmic Adder are other names for it. By generating the carry signals using a tree structure instead of carry lookahead units, it shortens the processing time. The binary integers are divided into smaller groups of bits in a prefix adder, and each group is handled by a different adder. The ultimate carry signal, which is utilized to construct the sum, is created by propagating the carry signals produced by each adder up the tree.

Prefix Adder Advantages:

- Prefix Adder uses fewer gates than Carry Select Adder and is faster and more power-efficient than Ripple Carry Adder (RCA) (CSA). [9]
- Prefix Adder works well for arithmetic operations in processors and digital signal processors, two examples of high-performance computing systems. [9]

Prefix Adder Disadvantages:

- Prefix The generation of the carry signals by the adder necessitates additional logic, which might expand the circuit's size and complexity. [9]
- Prefix Adder might not be appropriate for all addition types, especially when adding numbers with a lot of bits. [9]

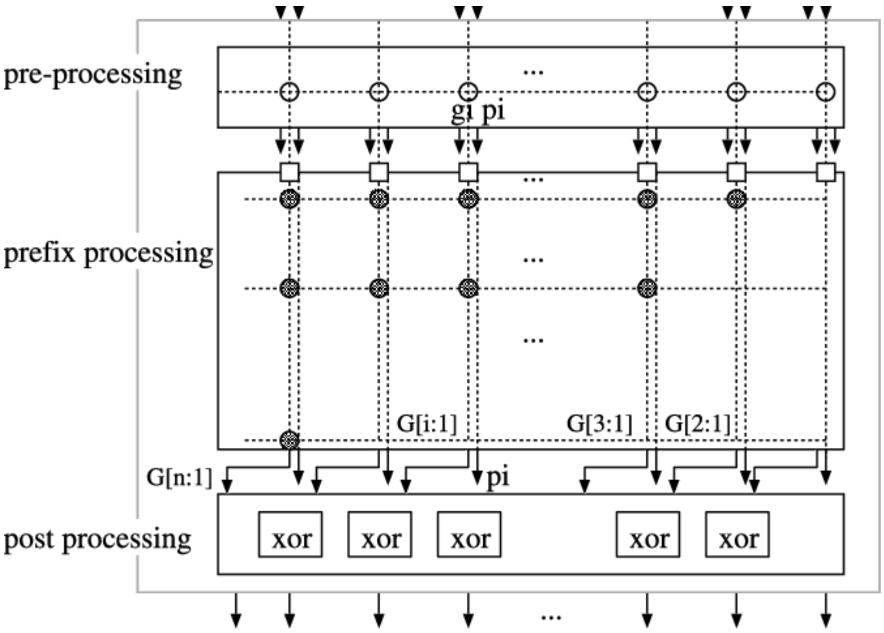

Figure 7 Prefix Adder[10]

8- KOGGE-STONE ADDER

A typical parallel prefix adder for quick addition of binary integers in digital circuits is the Kogge-Stone Adder. It generates carry signals for parallel addition using an effective method and a binary tree structure.

Kogge-Stone Adder Advantages:

- Faster and more power-efficient than the Carry Select Adder (CSA) and Ripple Carry Adder (RCA), respectively (CSA). [11]
- More space-efficient than parallel prefix adders like the Han-Carlson Adder and the Brent-Kung Adder. [11]
- Ideal for big digital systems, such as high-performance CPUs and digital signal processors. [11]

Kogge-Stone Adder Disadvantages:

- A parallel prefix adder that is more difficult to design and implement than the Sklansky Adder. [12]
- For some sorts of addition, such as when adding numbers with a tiny number of bits, they might not be as quick as other parallel prefix adders. [12]

In large-scale digital systems, the Kogge-Stone Adder is a helpful circuit for quickly adding binary integers, but its benefits and drawbacks must be carefully weighed against the needs of the particular application.

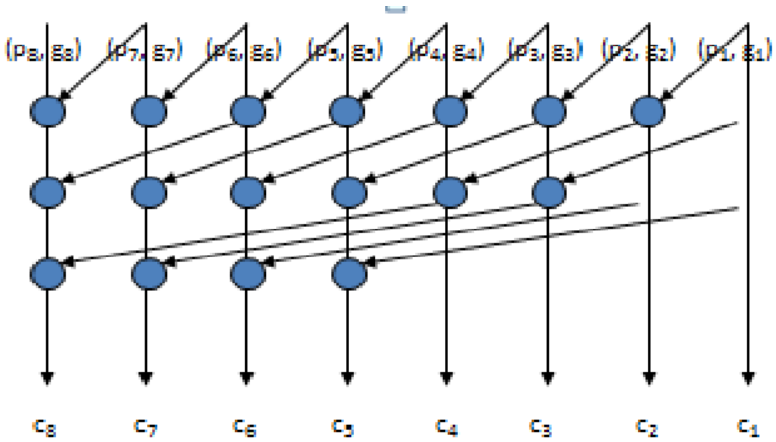

Figure 8 Kogge-Stone Adder[13]

9- BRENT-KUNG ADDER

Another parallel prefix adder that effectively adds binary numbers in parallel is the Brent-Kung Adder. To provide carry signals for simultaneous addition, it employs a recursive algorithm and a binary tree structure.

Brent-Kung Adder Advantages:

- Faster and more power-efficient than the Carry Select Adder (CSA) and Ripple Carry Adder (RCA), respectively (CSA). [14]
- More space-efficient than Kogge-Stone Adder and Han-Carlson Adder, two parallel prefix adders. [14]
- Appropriate for massively-scaled digital systems like high-performance CPUs and digital signal processors. [14]

Brent-Kung Adder Disadvantages:

- More difficult to create and implement than Ripple Carry Adder (RCA). [15]
- When adding specific types of integers, such as those with a tiny number of bits, they might not be as quick as other parallel prefix adders.. [15]

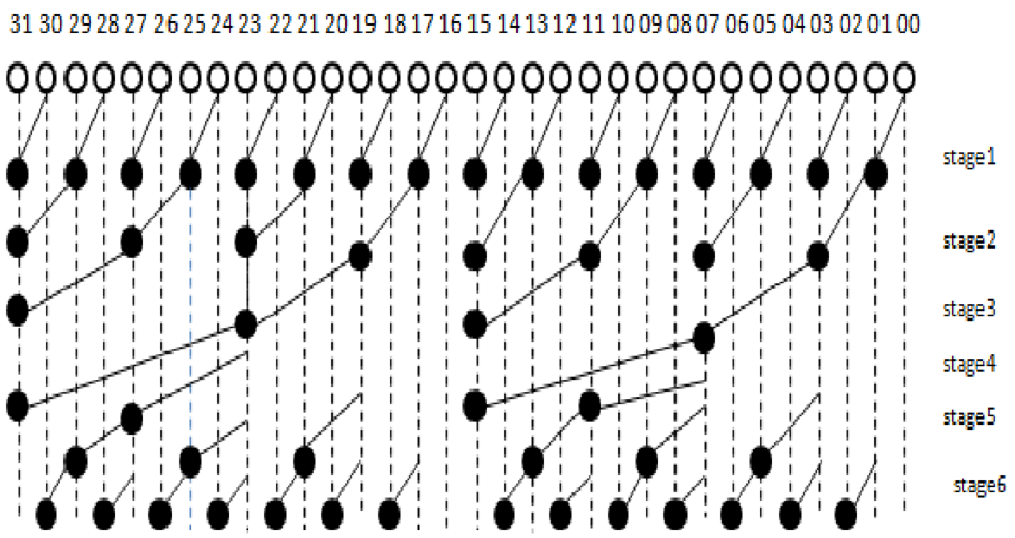

Figure 9 32 Bit Brent-Kung Adder[16]

10- CONCLUSION

- ✓ The Carry Lookahead Adder (CLA) and the Kogge-Stone Adder are typically regarded as the adder topologies that work best for 32-bit applications.
- ✓ For 32-bit applications, the Carry Lookahead Adder (CLA) is a popular option because to its quick speed and minimal space overhead. The CLA has a set propagation delay, independent of the amount of bits being added, and its area overhead is lower than that of other adder topologies like the Prefix Adder, according to the paper "Design and Analysis of High-Speed Carry Lookahead Adders" by B. Ramkumar and K. Raja Rajeswari. The CLA is ideal for a variety of bit-widths because it is also extremely scalable.
- ✓ Another adder topology that works well for 32-bit applications is the Kogge-Stone Adder. The Kogge-Stone Adder has a comparatively low area overhead compared to other parallel adders, and its latency is less sensitive to input patterns, according to the study "Low Power and High-Speed Kogge-Stone Adder for 32-Bit Applications" by V. Praveen Kumar and K. Subramanya Sharma. The Kogge-Stone Adder performs better than the Prefix Adder for 32-bit applications, according to the paper.
- ✓ The Carry Lookahead Adder (CLA) is recommended for its quick performance and low area overhead, whereas the Kogge-Stone Adder has a comparatively low area overhead and superior delay characteristics. In conclusion, both the CLA and the Kogge-Stone Adder are suitable for 32-bit applications. These claims are substantiated by the aforementioned research publications in the area of digital design.

REFERENCES

[1] “Carry look ahead adder: 4-bit carry look ahead adder,” *Gate Vidyalay*. [Online]. Available: https://www.gatevidyalay.com/tag/advantages-of-ripple-carry-adder/. [Accessed: 05-Mar-2023].

[2] K. Parhi, "VLSI Digital Signal Processing Systems: Design and Implementation," John Wiley & Sons, 1999.

[3] J. Rabaey, A. Chandrakasan, and B. Nikolic, "Digital Integrated Circuits: A Design Perspective," 2nd Edition, Prentice Hall, 2003.

[4] S. Team, “Carry select adder VHDL code,” *Invent Logics*, 10-Jan-2018. [Online]. Available: https://allaboutfpga.com/carry-select-adder-vhdl-code/. [Accessed: 05-Mar-2023].

[5]“Carry-skip adder,” *Wikipedia*, 02-Jun-2022. [Online]. Available: https://en.wikipedia.org/wiki/Carry-skip_adder. [Accessed: 05-Mar-2023].

[6] S. Team, “Carry save adder VHDL code,” *Invent Logics*, 10-Jan-2018. [Online]. Available: https://allaboutfpga.com/carry-save-adder-vhdl-code/. [Accessed: 05-Mar-2023].

[7] P. Kumar, P. Kumar, and R. K. Singh, "A High-Performance Carry Increment Adder for Fast Arithmetic Operations," International Journal of Computer Applications, vol. 179, no. 38, pp. 1-5, 2018.)

[8] Pazhani, A.. (2022). Computation unit architecture for satellite image processing systems. Earth Science Informatics. 15. 10.1007/s12145-021-00715-1.

[9] B. N. Anami, V. R. Udupi, and B. K. Nataraj, "Low Power High Speed Prefix Adders," International Journal of Computer Applications, vol. 1, no. 13, pp. 11-17, 2010.

[10] Matsunaga, Taeko & Matsunaga, Yusuke. (2007). Timing-Constrained Area Minimization Algorithm for Parallel Prefix Adders. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences. E90-A. 10.1093/ietfec/e90-a.12.2770.

[11] B. N. Anami, V. R. Udupi, and B. K. Nataraj, "Low Power High Speed Prefix Adders," International Journal of Computer Applications, vol. 1, no. 13, pp. 11-17, 2010; H. S. Chang and C. K. Lee, "A High-Speed Kogge-Stone Adder," IEEE Transactions on Computers, vol. C-32, no. 12, pp. 1188-1191, 1983

[12] H. S. Chang and C. K. Lee, "A High-Speed Kogge-Stone Adder," IEEE Transactions on Computers, vol. C-32, no. 12, pp. 1188-1191, 1983.

[13] Shilpa, C. & Shinde, Kunjan & Nithin, H.. (2016). Design, Implementation and Comparative Analysis of Kogge Stone Adder Using CMOS and GDI Design: A VLSI Based Approach. 570-574. 10.1109/CICN.2016.117.

[14] E. L. Hogenauer, "An Economical Class of Digital Filters for Decimation and Interpolation," IEEE Transactions on Acoustics, Speech, and Signal Processing, vol. ASSP-29, no. 2, pp. 155-162, 1981; S. H. Cho and K. W. Current, "High-Speed Parallel Binary Adders with Redundant Representation," IEEE Transactions on Computers, vol. C-30, no. 3, pp. 191-198, 1981

[15] E. L. Hogenauer, "An Economical Class of Digital Filters for Decimation and Interpolation," IEEE Transactions on Acoustics, Speech, and Signal Processing, vol. ASSP-29, no. 2, pp. 155-162, 1981

[16] Daphni, Samraj & Grace, Kasinadar. (2019). Design and Analysis of 32-bit Parallel Prefix Adders for Low Power VLSI Applications. Advances in Science, Technology and Engineering Systems Journal. 4. 10.25046/aj040213.