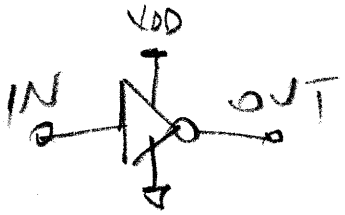
16/02/15 - W3

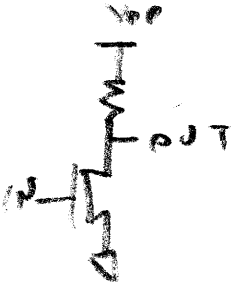
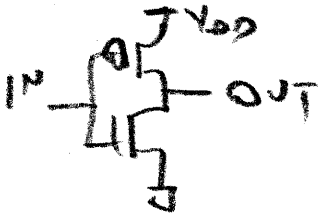
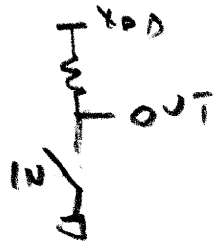
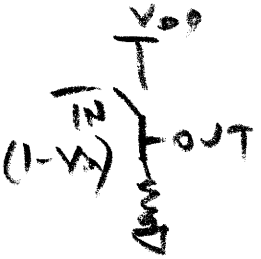
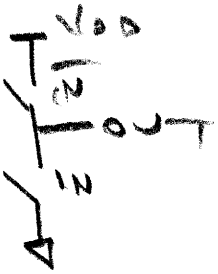
EHB 322E: Digital Electronic Circuits

SPRING 2015

INVERTERS

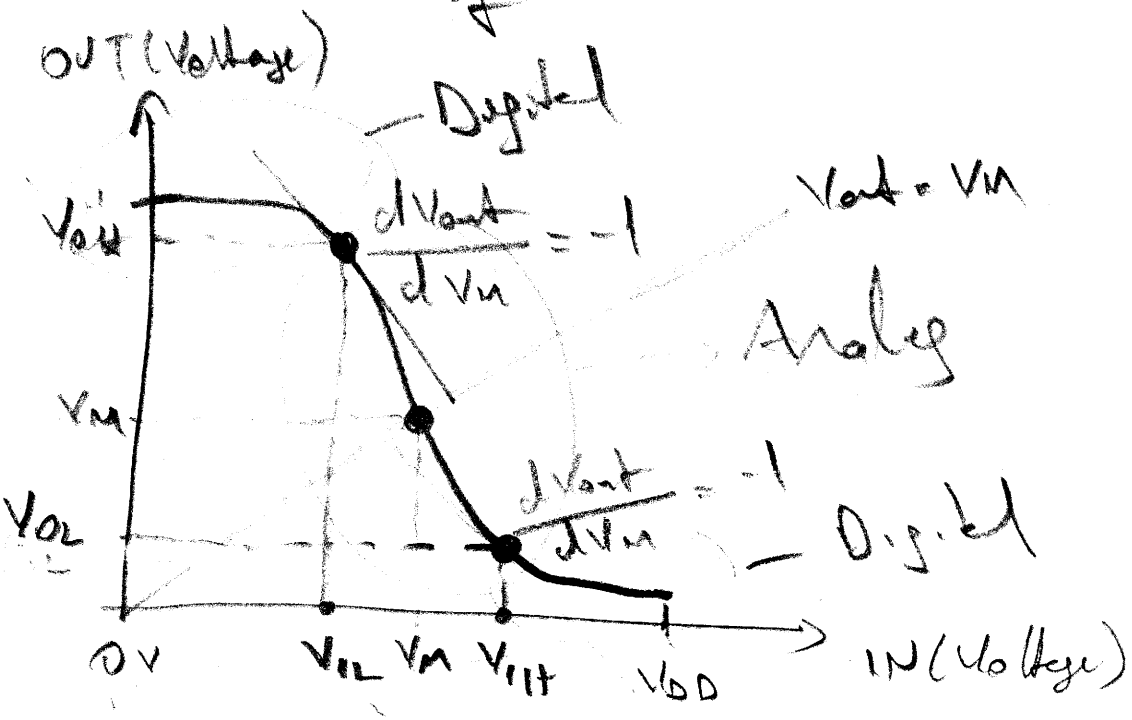
IN	OUT
logic 0 (≈0V)	logic 1 (≈5V)
logic 1 (≈5V)	logic 0 (≈0V)



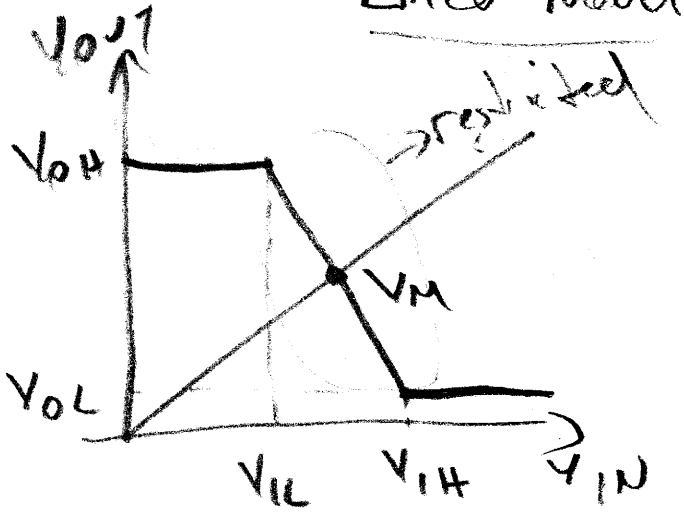
	NMOS	PMOS	CMOS
Circuit (transistor based)			
Circuit (switch based)			
INV's OUT	IN / OUT	IN / OUT	IN / OUT
V_{DD} = 5V	0V / V_{DD}	0V / ≈5V (<5V)	0V / 5V
GND = 0V	5V / ≈0 (>0)	5V / 0	5V / 0V
Static Power	> 0	> 0	= 0

Static behaviour of Inverters

Voltage Transfer Curve (VTC) of Inverters

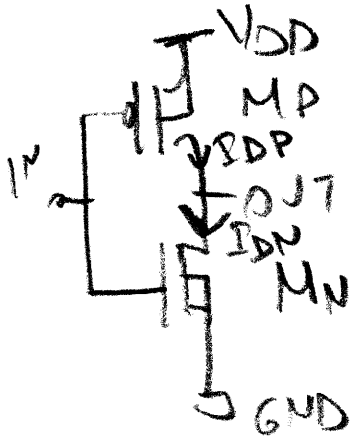


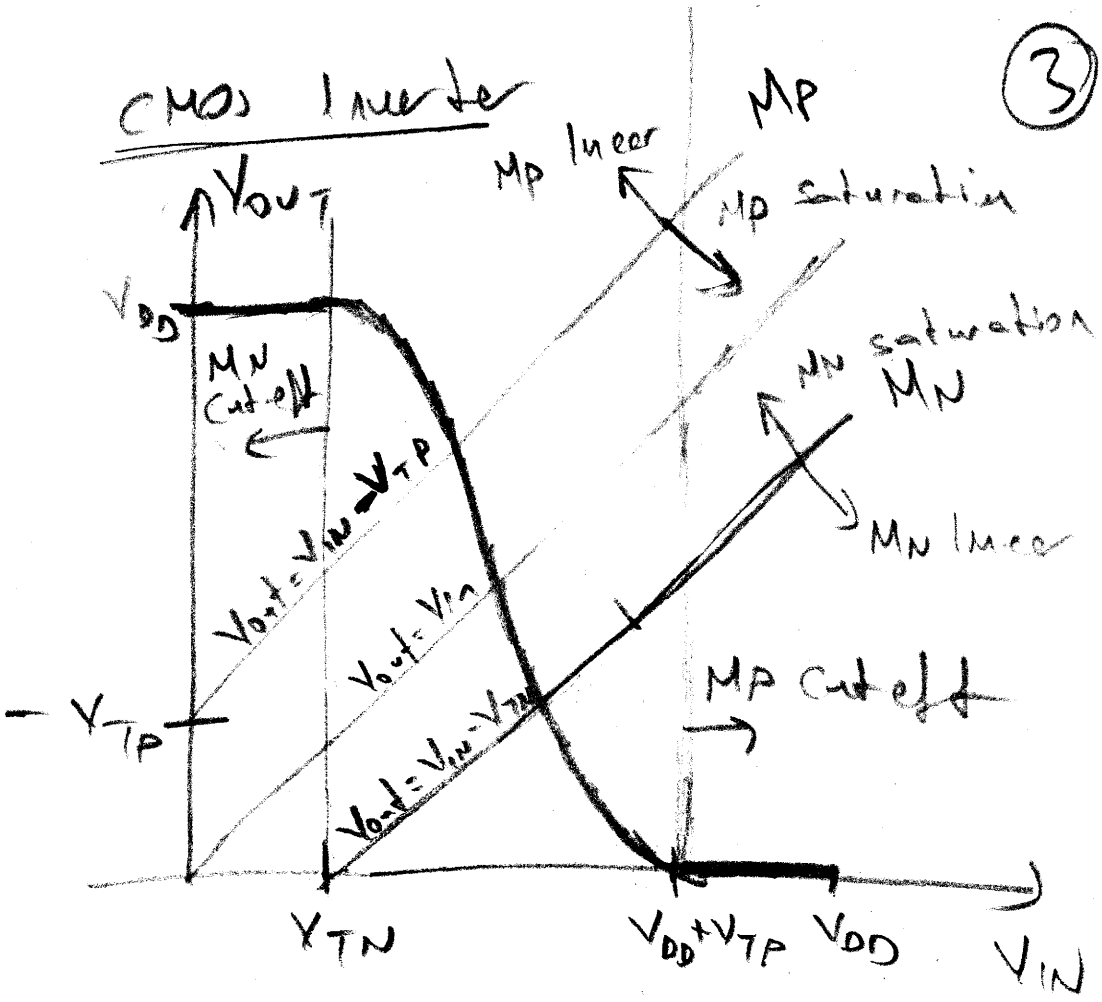
Linear Model



nMOS	pMOS	CMOS
$V_{OL} > 0$	$V_{OL} = 0$	$V_{OL} = 0$
$V_{OH} = V_{DD}$	$V_{OH} < V_{DD}$	$V_{OH} = V_{DD}$

CMOS Inverter





V_{TN} : Threshold voltage of MN (>0)

V_{TP} : Threshold voltage of MP (<0)

$V_{IN} = V_{GN} = V_{GP} \Rightarrow$ $\boxed{V_{GSN} = V_{IN}}$ $\boxed{V_{GSP} = V_{IN} - V_{DD}}$

$V_{OUT} = V_{DN} = V_{DP} \Rightarrow$ $\boxed{V_{DSN} = V_{OUT}}$ $\boxed{V_{DSP} = V_{OUT} - V_{DD}}$

$V_{GSN} \geq 0$ $\quad V_{GSP} \leq 0$

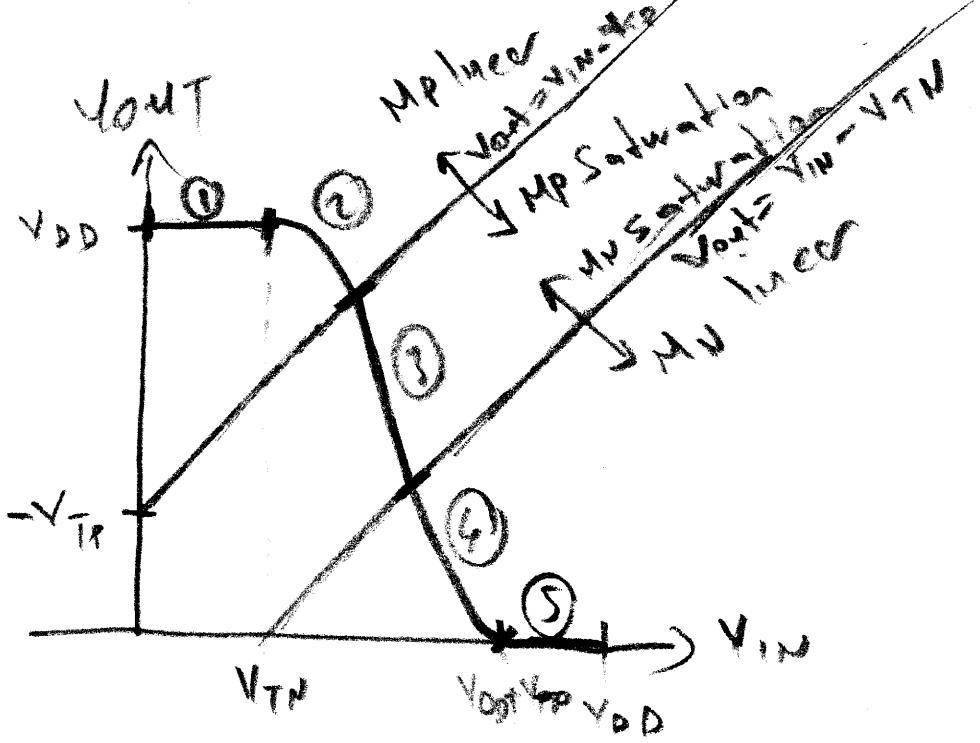
$I_{DN} = I_{DP}$ $\quad V_{DSN} \geq 0$ $\quad V_{DSP} \leq 0$

$V_{GSN} - V_{TN} = V_{DSN}$ (Saturation - linear edge of MN)

$\Rightarrow$ $\boxed{V_{OUT} = V_{IN} - V_{TN}}$ → MN line

$V_{GSP} - V_{TP} = V_{DSP}$ (Saturation - linear edge of MP)

$\Rightarrow V_{IN} - V_{DD} - V_{TP} = V_{OUT} - V_{DD} \Rightarrow$ $\boxed{V_{OUT} = V_{IN} - V_{TP}}$ → MP line



5 Regions

	Region	M_N	M_P
(1)	$0 \leq V_{IN} < V_{TN}$	Cut-off	Linear ($V_{DS}=0$)
(2)	$V_{TN} \leq V_{IN} < V_{OUT} + V_{TP}$	Saturation	Linear
(3)	$V_{OUT} + V_{TP} \leq V_{IN} < V_{OUT} + V_{TN}$	Saturation	Saturation
(4)	$V_{OUT} + V_{TN} \leq V_{IN} < V_{DD} + V_{TP}$	Linear	Saturation
(5)	$V_{DD} + V_{TP} \leq V_{IN}$	Linear ($V_{DS}=0$)	Cut-off

Switching Threshold (V_M)

V_M = ? Which region? → (3) both in sat.

$I_{DN} = I_{DP}$

$I_{DN} = K_N (V_{GSN} - V_{TN})^2 = K_N (V_{IN} - V_{TN})^2$

$I_{DP} = K_P (V_{GSP} - V_{TP})^2 = K_P (V_{IN} - V_{DD} - V_{TP})^2$

$V_{IN} = V_M$

$$\Rightarrow K_N (V_M - V_{TN})^2 = K_P (V_M - V_{DD} - V_{TP})^2$$

$$\Rightarrow V_M = \frac{V_{DD} + V_{TP} + \sqrt{\frac{K_N}{K_P}}\, V_{TN}}{1 + \sqrt{\frac{K_N}{K_P}}}$$

ex/ For symmetric operation V_M is selected as $V_{DD}/2$, and $V_{TN} = -V_{TP}$. Determine $\frac{K_N}{K_P}$.

Suppose that $R = \frac{K_N}{K_P}$

$$\frac{V_{DD}}{2} = \frac{V_{DD} - V_{TN} + R^2 V_{TN}}{1 + R^2}$$

$$\Rightarrow R^2 \left(\frac{V_{DD}}{2} - V_{TN}\right) = \left(\frac{V_{DD}}{2} - V_{TN}\right) \Rightarrow R = 1 \quad \frac{\frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_N}{\frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)_P} = 1$$

$$\frac{\mu_n}{\mu_p} = \frac{\left(\frac{W}{L}\right)_p}{\left(\frac{W}{L}\right)_N} \qquad L_p = L_N = L_{min}$$

$$\Rightarrow \frac{\mu_n}{\mu_p} = \frac{W_p}{W_N} \qquad \frac{\mu_n}{\mu_p} = 3 \Rightarrow \boxed{W_p = 3W_N}$$

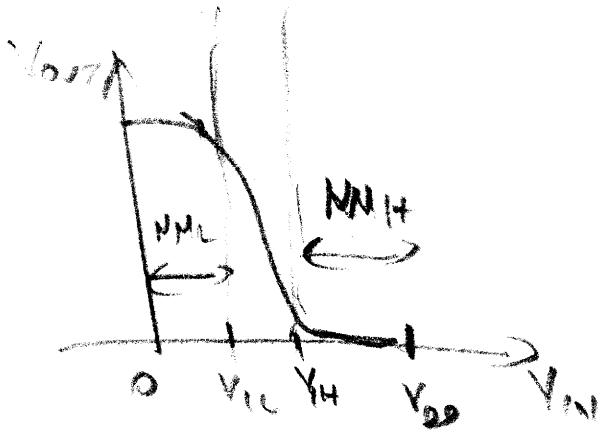
Noise Margin

$NM_L = V_{IL}$

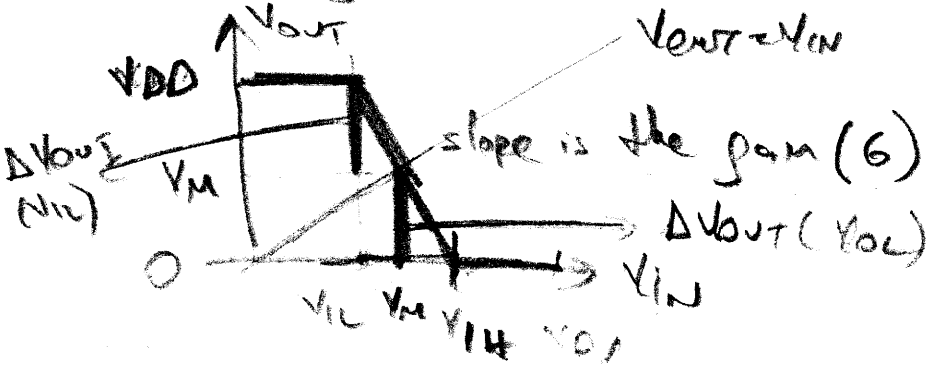
$NM_H = V_{DD} - V_{IH}$

NM_L and NM_H are maximum tolerable voltage values when $I_N = 0$ and $I_N = 1$, respectively

- If $V_{IN} > NM_L$ or $V_{OUT} < V_{DD} - NM_H$ then then V_{OUT} might be 0 or V_{DD} (unstable)



If using a linear model and V_M



$G = -\frac{dV_{out}}{dV_{IN}}$ (negative)

$$V_{IL} = V_M + \Delta V_{OUT} \frac{dV_{IN}}{dV_{out}}$$

$$V_{IL} = V_M + \frac{\Delta V_{OUT}}{G} = V_M + \frac{(V_{DD} - V_M)}{G}$$

$$\Rightarrow \boxed{NM_L = V_M + \frac{V_{DD} - V_M}{G}}$$

$$V_{IH} = V_M - \frac{V_M}{G}$$

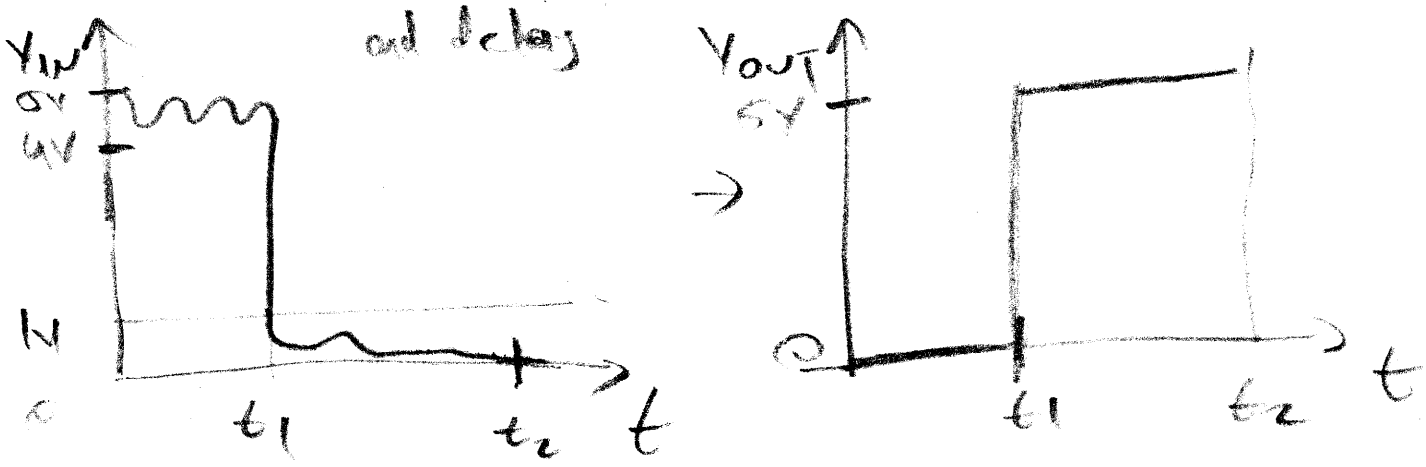
$$\Rightarrow \boxed{NM_H = V_{DD} - V_{IH} = V_{DD} - V_M + \frac{V_M}{G}}$$

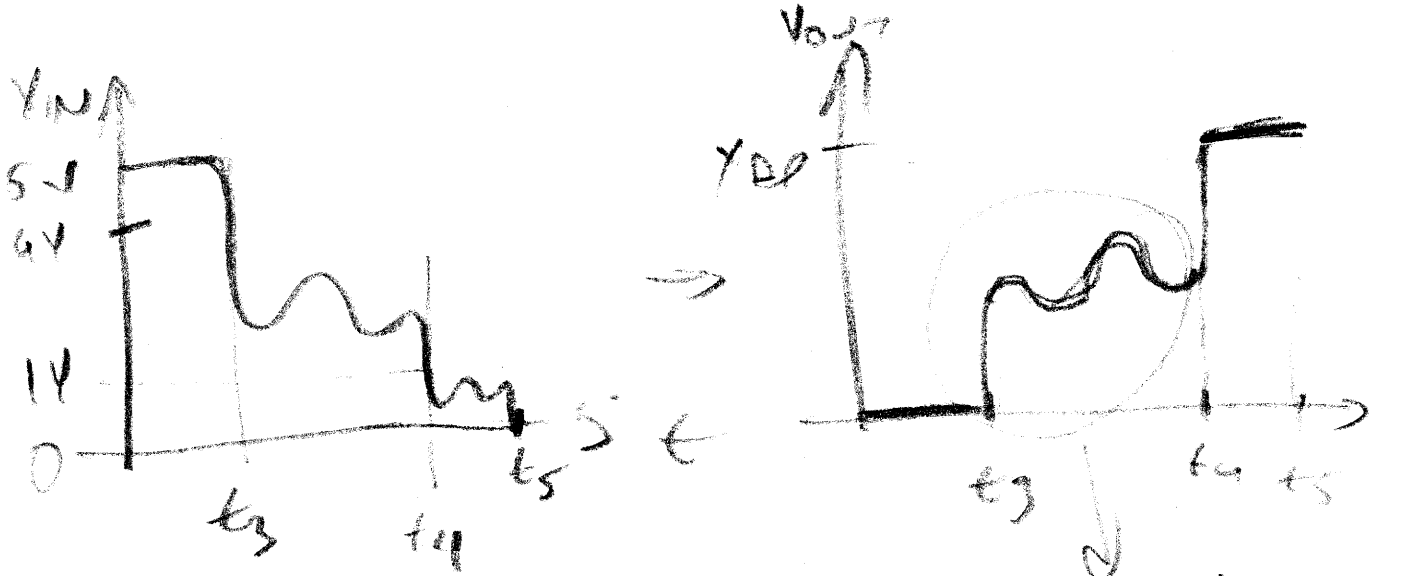
Ex/ For a CMOS inverter $V_{NL} = V_{NH} = 1\,V$ is desired. Determine V_M by using a linear VTC model. $V_{DD} = 5\,V$

$$1 = V_M + \frac{5 - V_M}{G} \qquad 1 = 5 - V_M + \frac{V_M}{G}$$

$$2 = 5 + \frac{5}{G} \Rightarrow G = -\frac{5}{3} \qquad V_M = 2.5\,V$$

Ex A CMOS inverter has $V_{DD} = 5V$, $NM_L = 1V$, and $NM_H = 1V$. Draw V_{out} vs. time. Suppose that there is no noise in the environment (ideal) and delay





problem

logic 0 or 1 ?

If $NM_L \uparrow$ or $NM_H \uparrow$ more tolerant to unwanted voltages

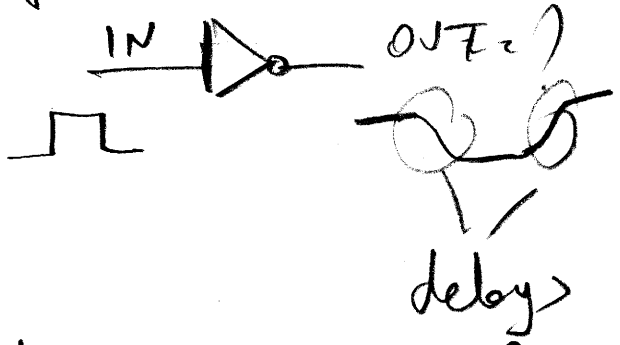
Dynamic behaviour of Inverters

Dynamic

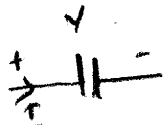
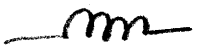
+ Considering delays
+ In time domain
+ Transient analysis
+ $V_{in} = 1.2V \Rightarrow V_{out} = 3V$

Static

+ Not considering delays (Instantaneous)
+ In voltage-current domain
+ DC analysis
+



How to model time delays in circuits?

Resistor	$V = I \cdot R$		
Capacitor	$I = C \frac{dV}{dt}$		$\Delta V \cong \frac{I \Delta t}{C}$
Inductor	$V = L \frac{dI}{dt}$		$\Delta I \cong \frac{V \cdot \Delta t}{L}$

Is it possible that there is no delay in a transition?

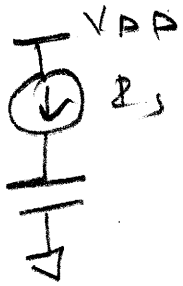
Ex

$V_C(t=0) = 0$

$I_S = 1\,mA$

$C = 1\,pF$

$V_{DD} = 5\,V$



a) Determine the time to make $V_C = 5\,V$

b) Determine the time to make $V_C = 2.5\,V$

$$I_C = C\frac{dV_C}{dt} \qquad I_C = I_S$$

$$\Rightarrow \frac{dV_C}{dt} = \frac{I_S}{C} = 10^9\ V/s$$

$$V_C = a\,t + b \Rightarrow a = 10^9$$

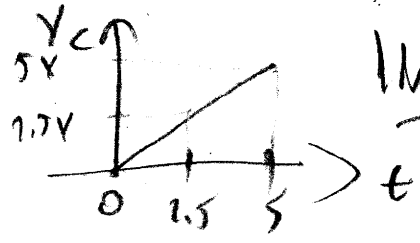
$$V_C(t=0) = b = 0 \Rightarrow b = 0$$

a) $V_C = 10^9 t$ and $V_C = 5\,V$

$\Rightarrow t = 5\,10^{-9}\,s = 5\,ns$ //

b) $V_C = 10^9 t$ and $V_C = 2.5\,V$

$\Rightarrow t = 2.5\,ns$ //



linear

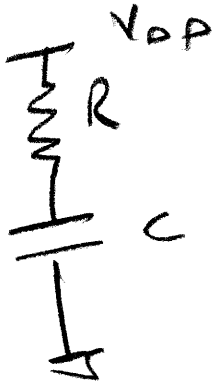
Rx

$V_C(t=0) = 0$

$R = 5k\Omega$

$C = 1pF$

$V_{DD} = 5V$



a) Determine the time to make $V_C = 5V$

b) Determine the time to make $V_C = 2,5V$

$$I_C = C\frac{dV_C}{dt} \qquad I_C = \frac{V_{DD} - V_C}{R} = \frac{5 - V_C}{5k}$$

$$\Rightarrow \frac{5 - V_C}{5k} = 1p\frac{dV_C}{dt} \qquad \left(\frac{dV_C}{dt} = \underbrace{k + l\,V_C}_{\text{constant}}\right)$$

$$\Rightarrow V_C = a + be^{ct}$$

$$\frac{5 - a - be^{ct}}{5k\,1p} = bc\,e^{ct}$$

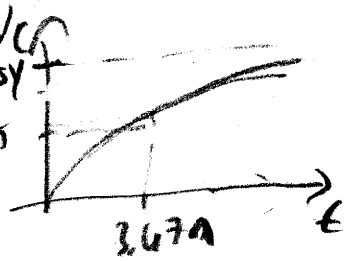
$$\Rightarrow 5 - a = 0 \Rightarrow \underline{a = 5} \quad , \quad \frac{-b}{5\,10^{-9}} = bc \Rightarrow c = \underline{0,2\,10^{9}}$$

$$V_C(t=\infty) = 0 \Rightarrow a + b = 0 \Rightarrow \underline{b = -5}$$

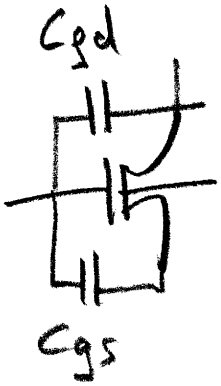
$$\boxed{V_C = 5 - 5e^{-2\,10^8 t}}$$

$$V_C = 5 \Rightarrow t = \infty$$

$$V_C = 2,5 \Rightarrow t = \frac{-\ln(0,5)}{2\,10^8} = 3,47\,ns$$



MOS Capacitors



4 terminals

$\binom{4}{2} = 6$ capacitors

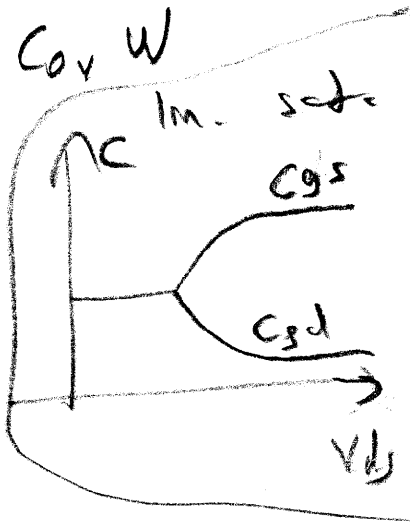
C_{gs} and C_{gd} are dominant ones. We only consider C_{gs} and C_{gd}

In linear region $C_{gs} \cong C_{gd} = \frac{W \cdot L \cdot C_{ox} + W C_{ov}}{2}$

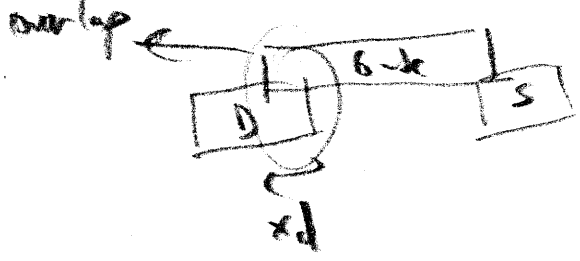
In saturation region $C_{gs} = \frac{2}{3} W \cdot L C_{ox} + W C_{ov}$

$C_{gd} = W C_{ov}$

In cut-off $C_{gs} = C_{gd} = C_{ov} W$



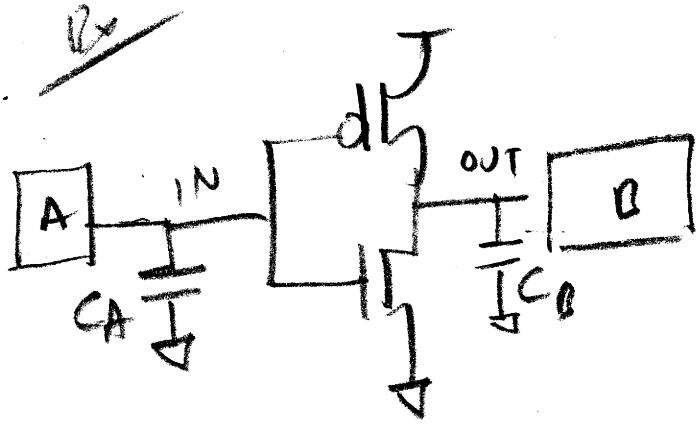
$C_{ov} = C_{ox} x_d$ overlap cap.



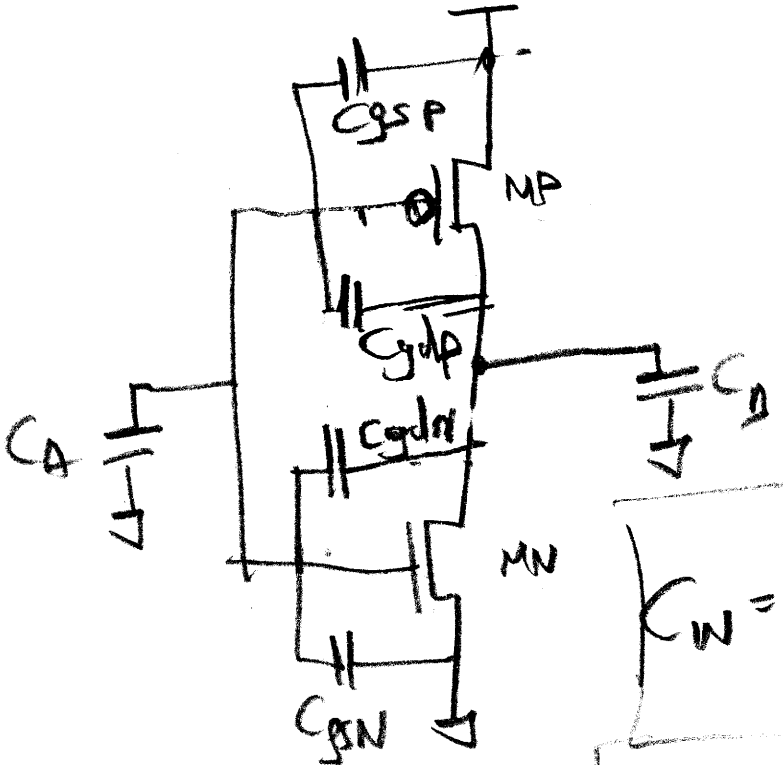
C_{ox} : cap. per area from gate across the oxide

- A node capacitor is the sum of all capacitors connected to the node

Ex



Calculate the equivalent input (C_{IN}) and output (C_{out}) node capacitors of the inverter.



$$C_{IN} = C_A + C_{gsP} + C_{gsN} + C_{gdP} + C_{gdN}$$

$$C_{out} = C_B + C_{gdP} + C_{gdN}$$