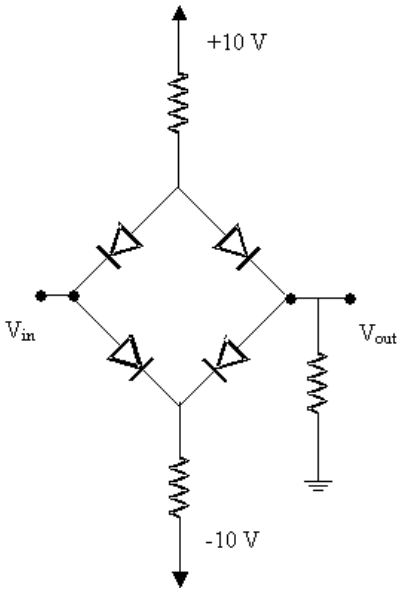
IMPORTANT: Besides your **calculator** and the sheets you use for calculations you are only allowed to have an A4 sized **"copy sheet"** during this exam. Notes, problems and alike are not permitted. **Please submit your "copy sheet" along with your solutions.** You may get your "copy sheet" back after your solutions have been graded. ***Do not forget to write down units and convert units carefully! Cell phones are not allowed and should be placed on the front desk before the exam.***

EHB222E INTRODUCTION TO ELECTRONICS (20727)
Midterm Exam #1 ✎ 23 March 2015 ⌛ 9.30-11.30
İnci ÇİLESİZ, PhD, Can ZOROĞLU, BS
EEF 2014

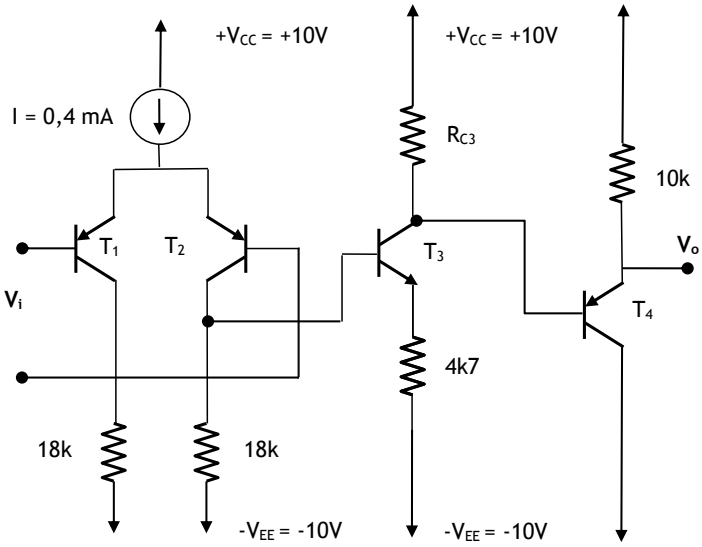
---

1. Assume you are have a diode made of n- and p-typed doped silicon with the following parameters: μ_n **= 1600 cm²/Vs,** μ_p **= 600 cm²/Vs.** n_i **= 1,5** 10^{10} **1/cm³,** **q = 1,602** 10^{-19} **C,** ε_r **= 12,** ε_o **= 8,85** 10^{-12} **F/m,** V_T **= 25 mV.**
   a. Find the dopant densities for n- and r-type silicon for specific resistances of 1 Ωcm and 0,5 Ωcm respectively. (6 points)
   b. Find the barrier voltage and saturation current for a junction area of **0,15 mm²**. (6 points)
      c. Determine the depletion zone width in **unbiased** state, when the junction is reverse biased at **2,5 V** and when it is forward biased at **0,25 V**. (9 points)
   d. Calculate the junction capacitances for the cases in (c). (9 points)



2. For the circuit shown on the right sketch V_{out} as a function of V_{in} for V_{in}: -10 V to +10 V assuming all three resistors are 10k and the voltage drop across conducting diodes are constant at 0,6 V. (30 points)
HINT: Analyze the circuit first at V_{in} = 0V; then at +10 V and –10 V, and finally at values in between.

3. Study DC characteristics of the 3-stage BJT amplifier circuit with $|V_{BE}|$ **= 0,6 V**, h_{FE} **= 200** for all four transistors. **Do not neglect base currents.**
   a. Design a current source that will provide **0,4 mA biasing current** to the differential stage. (10 points)
   b. Choose R_{C3} such that, waveform distortion at the output V_o is minimum and symmetrical, i.e., V_o **= 0V**? (30 points)



GOOD LUCK

SOLUTIONS:

1. Using Einstein Equation , i.e., $D_{p/n} = V_T \mu_{p/n} \Rightarrow D_p = 15\,\frac{cm^2}{s};\ D_n = 40\,\frac{cm^2}{s}$

   a. $\sigma_p = q \cdot \left(\frac{n_i^2}{N_A} \mu_n + N_A \mu_p \right) \cong q N_A \mu_p \Rightarrow N_A = \frac{\sigma_p}{q \mu_p} = \underline{\underline{2{,}08 \cdot 10^{16}\ / cm^3}}$

   $\sigma_n = q \cdot \left(N_D \mu_n + \frac{n_i^2}{N_D} \mu_p \right) \cong q N_D \mu_n \Rightarrow N_D = \frac{\sigma_n}{q \mu_n} = \underline{\underline{3{,}9 \cdot 10^{15}\ / cm^3}}$

   b. $V_B = V_T \cdot \ln\left(\frac{N_A \cdot N_D}{n_i^2} \right) = \underline{\underline{665 mV}}$ and $I_o = A \cdot q \cdot n_i^2 \cdot \left[\frac{D_p}{L_p N_D} + \frac{D_n}{L_n N_A} \right] = \underline{\underline{625 fA}}$

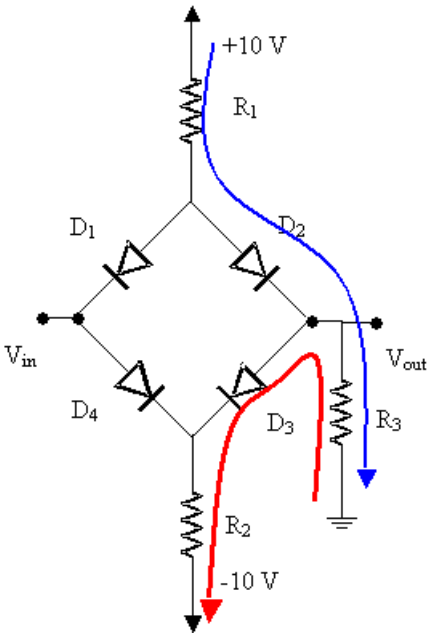
   c. unbiased $w_{dep} = \sqrt{\frac{2 \cdot \varepsilon_o \cdot \varepsilon_r \cdot V_B}{q} \left(\frac{1}{N_A} + \frac{1}{N_D} \right)} = \underline{\underline{0{,}51 \mu m}}$

   with reverse bias at 2,5 V, $w_{dep} = \sqrt{\frac{2 \cdot \varepsilon_o \cdot \varepsilon_r \cdot (V_B + V_{bias})}{q} \left(\frac{1}{N_A} + \frac{1}{N_D} \right)} = \underline{\underline{1{,}13 \mu m}}$

   with forward bias at 0,25 V, $w_{dep} = \sqrt{\frac{2 \cdot \varepsilon_o \cdot \varepsilon_r \cdot (V_B - V_{bias})}{q} \left(\frac{1}{N_A} + \frac{1}{N_D} \right)} = \underline{\underline{0{,}41 \mu m}}$

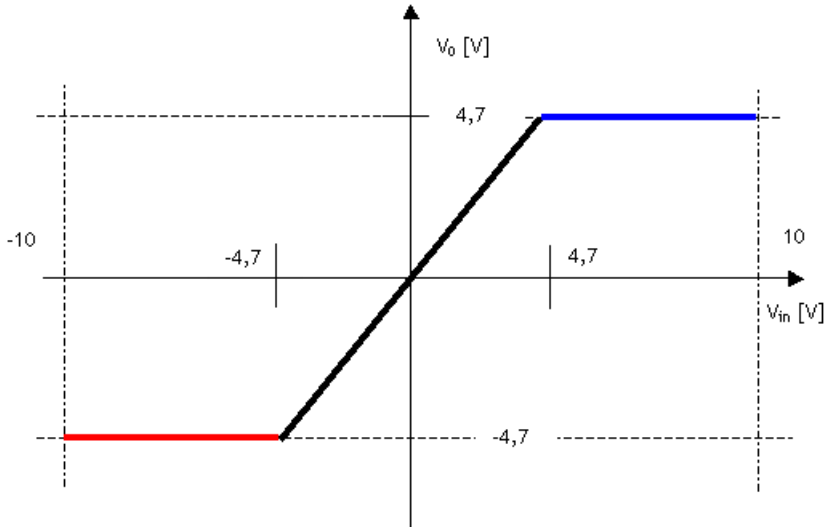
   d. Thus, $C = \varepsilon_o \cdot \varepsilon_r \frac{A}{w} = \begin{cases} \underline{\underline{30{,}74 pF, unbiased}} \\ \underline{\underline{14 pF, reverse@2{,}5V}} \\ \underline{\underline{38{,}9 pF,\ forward@0{,}25V}} \end{cases}$

2. Assume there is no V_{in}. V_{out} = 0V because of the symmetry of the circuit, and because all diodes are conducting. This is the same as V_{in} = 0V. Now assume V_{in} = 10V. We can easily see that D_1 and D_3 are reverse biased because most of the voltage drop from +10 V to –10 V is over the resistors R_1 and R_2. In other words, the anode of D_1 is much less than +10V whereas the cathode is at +10V (reverse bias). Also, D_4 is conducting, thus, the cathode of D_3 is at 9,4V wheras the anode of D_3 is much less than +9,4V. That means current flows (a) from +10V over R_1, D_2 , and R_3 to ground (**follow blue line**), and (b) from V_{in} over D_4 and R_4 to –10V. Since only 0,6V drops on the conducting diodes 9,4V drops over the two resistors R_1 and R_3. Since R_1 and R_3 have equal values, we divide the voltage drop by 2 and this is V_{out} = 4.7V.



   Now assume V_{in} = -10V. Similar to the observations above, D_4 and D_2 are reverse biased because most of the voltage drop from +10 V to –10 V is again over the resistors R_1 and R_2. In other words, the cathode of D_4 is much higher than -10V whereas the anode is at -10V (reverse bias again). Also, D_1 is conducting, thus, the anode of D_2 is at -9,4V whereas the cathode of D_2 is much higher than -9,4V. That means current flows (a) from the ground over R_3, D_3 , and R_2 to –10V (**follow red line**), and (b) from +10V over R_1 and D_1 to V_{in}. Since only 0,6V drops on the conducting diodes 9,4V drops over the two resistors R_2 and R_3. Since R_2 and R_3 have equal values, we divide the voltage drop by 2 and this is V_{out} = 4.7V.

Finally, we need to consider the output for 0V ≥ V_{in} ≥ -10V and 0V ≤ V_{in} ≤ +10V. One sees easily that when all the 4 diodes are conducting, the output V_{out} follows the input V_{in} because the circuit is symmetrical. When do all the 4 diodes conduct? See the sketch below….Capito????



3. DC characteristics are to be studied.
   a. You do your own design!
   b. Without neglecting the base currents of the differential (the very first) stage, for V_i = 0 V

$$I_{C1} = I_{C2} = \frac{h_{FE}}{h_{FE}+1} \cdot \frac{I_{ref}}{2} = \frac{200}{200+1} \cdot \frac{0{,}4mA}{2} \Rightarrow I_{C1} = I_{C2} = \underline{\underline{0{,}199mA}}$$

$$-(I_{C2} - I_{B3})18k + V_{BE3} + (h_{FE}+1)I_{B3}4k7 = 0$$

$$I_{C3} = h_{FE}\frac{18k * I_{C2} - V_{BE3}}{(h_{FE}+1)4k7 + 18k} = 200\frac{18k * 0{,}199mA - 0{,}6V}{(200+1)4k7 + 18k} = \underline{\underline{0{,}62mA}}$$

That the output voltage is in the middle of the power supply range (+10 V and -10 V), V_o = 0 V

$(h_{FE}+1)I_{B3}R_{E4} + V_{EB4} - (I_{C3} - I_{B4})R_{C3} = 0$, with $(h_{FE}+1)I_{B4}10k = 10V \Rightarrow I_{E4} = \underline{\underline{1mA}}$

$$(I_{C3} - I_{B4})R_{C3} = 10V + V_{EB4} \Rightarrow R_{C3} = \frac{10V + V_{EB4}}{I_{C3} - I_{B4}} = \underline{\underline{17k25}}$$