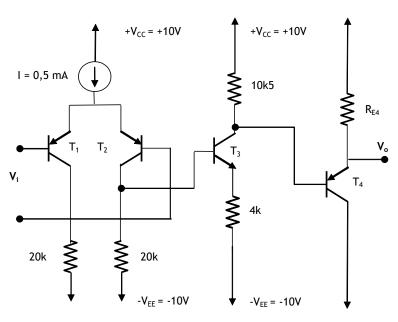
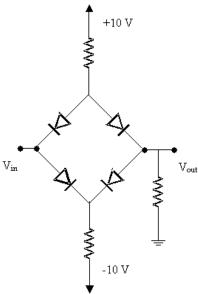
**IMPORTANT**: Besides your **calculator** and the sheets you use for calculations you are only allowed to have an A4 sized "**copy sheet**" during this exam. Notes, problems and alike are not permitted. **Please submit your "copy sheet" along with your solutions.** You may get your "copy sheet" back after your solutions have been graded. **Do not forget to write down units and convert units carefully! Cell phones are not allowed and should be placed on the front desk before the exam.** 

## EHB222E INTRODUCTION TO ELECTRONICS (21124) Midterm Exam #1 19 March 2018 9.30-11.30 inci ÇİLESİZ, PhD, M. Yasin ADIYAMAN EEF 5205

- 1. Compare and contrast conductors vs. semi-conductors. State similarities and differences. (10 p BONUS!)
- 2. Assume you have a diode made of n- and p-typed doped silicon with the following parameters  $N_D = 10^{16} \ 1/cm^3$  and  $N_A = 10^{17} \ 1/cm^3$ . You also know  $L_n = 10 \ \mu m$ ,  $L_p = 5 \ \mu m$ ,  $\mu_n = 1350 \ cm^2/Vs$ ,  $\mu_p = 480 \ cm^2/Vs$ .  $n_i = 1.5 \ 10^{10} \ 1/cm^3$ ,  $q = 1.602 \ 10^{-19} \ C$ ,  $\epsilon_r = 12$ ,  $\epsilon_0 = 8.85 \ 10^{-12} \ F/m$ ,  $V_T = 25 \ mV$ 
  - a. For the dark current (I<sub>o</sub>) to be under 100 fA how large should the junction area A be in mm<sup>2</sup>? (10)
  - b. If you cannot find A above, assume 0,5 mm<sup>2</sup> and calculate specific conductances of n and p type doped regions. (10)
  - c. Find depletion range width and junction capaticance in unbiased state. (10 puan)
- 3. For the circuit shown on the right sketch  $V_{out}$  as a function of  $V_{in}$  for  $V_{in}$ : -10 V to +10 V assuming all three resistors are 10k and the voltage drop across conducting diodes are constant at 0,6 V. (30 points) HINT: Analyze the circuit first at  $V_{in}$  = 0V; then at +10 V and -10 V, and finally at values in between.
- 4. Study DC characteristics of the 3-stage BJT amplifier circuit with  $|V_{BE}| = 0.6$  V,  $h_{FE} = 100$  for all four transistors.
  - a. Design a current source that will provide 0,5 mA biasing current to the differential stage. (10 p)





b. How should  $R_{E4}$  be chosen, such that, waveform distortion at the output is symmetrical, that is,  $V_0 = 0V$ ? If you cannot find take  $I_{C3} = 1$  mA. (30p)

## **SOLUTIONS:**

2.  $D_{p/n} = V_T \cdot \mu_{p/n}$  'thus  $D_p = 12$  cm<sup>2</sup>/s and  $D_n = 33.8$  cm<sup>2</sup>/s

$$\text{a.} \quad I_o = A \cdot q \cdot n_i^2 \cdot \left[ \frac{D_p}{L_p N_D} + \frac{D_n}{L_n N_A} \right] \quad \text{thus} \quad \text{if} \quad \text{I}_o \quad < \quad 100 \quad \text{fA} \quad \text{for} \quad \text{A} \quad < \quad 1,01 \quad \text{mm}^2.$$

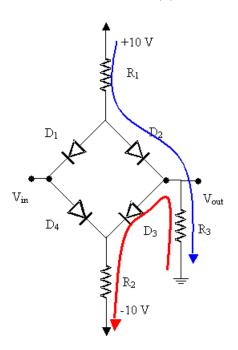
Thus I choose  $A = 1 \text{ mm}^2$ .

$$\text{b.} \quad \boldsymbol{\sigma}_{\boldsymbol{p}} = q \cdot \left( \frac{n_i^2}{N_{\scriptscriptstyle A}} \boldsymbol{\mu}_{\scriptscriptstyle n} + N_{\scriptscriptstyle A} \boldsymbol{\mu}_{\scriptscriptstyle p} \right) \! ; \quad \boldsymbol{\sigma}_{\scriptscriptstyle n} = q \cdot \left( N_{\scriptscriptstyle D} \boldsymbol{\mu}_{\scriptscriptstyle n} + \frac{n_i^2}{N_{\scriptscriptstyle D}} \boldsymbol{\mu}_{\scriptscriptstyle p} \right)$$

Thus  $\sigma_p = 7,69 \ 1/(\Omega \ cm)$   $\sigma_n = 2,16 \ 1/(\Omega \ cm)$ 

c. 
$$V_{B} = -V_{T} \cdot \ln \left( \frac{n_{i}^{2}}{N_{A} \cdot N_{D}} \right) \text{ thus V}_{\text{B}} = 728 \text{ mV and } w = \sqrt{\frac{2 \cdot \varepsilon_{o} \cdot \varepsilon_{r} \cdot V_{B}}{q \cdot}} \left[ \frac{1}{N_{A}} + \frac{1}{N_{D}} \right] \text{ thus}$$
 
$$\text{w}_{\text{dep}} = 3,26 \text{ } \mu\text{m and } C = \varepsilon_{o} \cdot \varepsilon_{r} \cdot \frac{A}{w} \text{ C} = 326 \text{ pF}$$

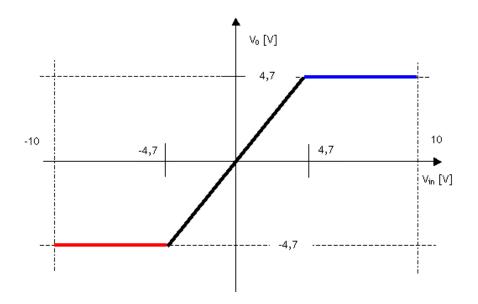
3. Assume there is no  $V_{in}$ .  $V_{out} = 0V$  because of the symmetry of the circuit, and because all diodes are conducting. This is the same as  $V_{in} = 0V$ . Now assume  $V_{in} = 10V$ . We can easily see that  $D_1$  and  $D_3$  are reverse biased because most of the voltage drop from +10 V to – 10 V is over the resistors  $R_1$  and  $R_2$ . In other words, the anode of  $D_1$  is much less than +10V whereas the cathode is at +10V (reverse bias). Also,  $D_4$  is conducting, thus, the cathode of  $D_3$  is at 9,4V wheras the anode of  $D_3$  is much less than +9,4V. That means current flows (a) from +10V over  $R_1$ ,  $D_2$ , and  $R_3$  to ground (follow blue line), and (b) from



 $V_{in}$  over  $D_4$  and  $R_4$  to -10V. Since only 0,6V drops on the conducting diodes 9,4V drops over the two resistors  $R_1$  and  $R_3$ . Since  $R_1$  and  $R_3$  have equal values, we divide the voltage drop by 2 and this is  $V_{out} = 4.7V$ .

Now assume  $V_{in}$  = -10V. Similar to the observations above,  $D_4$  and  $D_2$  are reverse biased because most of the voltage drop from +10 V to -10 V is again over the resistors  $R_1$  and  $R_2$ . In other words, the cathode of  $D_4$  is much higher than -10V whereas the anode is at -10V (reverse bias again). Also,  $D_1$  is conducting, thus, the anode of  $D_2$  is at -9,4V wheras the cathode of  $D_2$  is much higher than -9,4V. That means current flows (a) from the ground over  $R_3$ ,  $D_3$ , and  $R_2$  to -10V (follow red line), and (b) from +10V over  $R_1$  and  $D_1$  to  $V_{in}$ . Since only 0,6V drops on the conducting diodes 9,4V drops over the two resistors  $R_2$  and  $R_3$ . Since  $R_2$  and  $R_3$  have equal values, we divide the voltage drop by 2 and this is  $V_{out}$  = 4.7V.

Finally, we need to consider the output for  $0V \ge V_{in} \ge -10V$  and  $0V \le V_{in} \le +10V$ . One sees easily that when all the 4 diodes are conducting, the output  $V_{out}$  follows the input  $V_{in}$  because the circuit is symmetrical. When do all the 4 diodes conduct? See the sketch below....Capito????

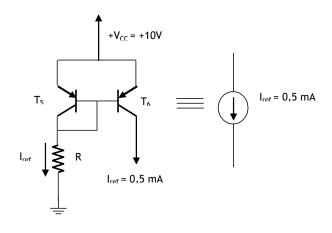


- 4. DC characteristics are to be studied.
  - a. See the sketch below. You should calculate the value of R, and make sure  $T_6$  operates in active mode.

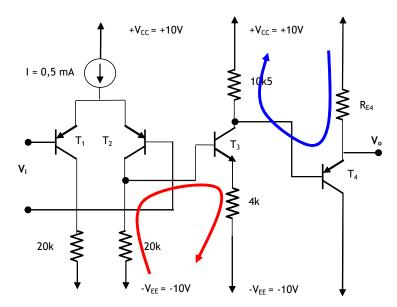
Without neglecting the base currents of the differential stage, for  $V_i = 0$ 

$$I_{C1} = I_{C2} = \frac{h_{FE}}{h_{FE} + 1} \cdot \frac{0.5mA}{2}$$

$$I_{C1} = I_{C2} = 0.248mA$$



b. Following the red loop  $-(I_{C2}-I_{B3})20k+V_{BE3}+(h_{FE}+1)I_{B3}4k=0$ 



$$I_{C3} = h_{FE} \frac{20k * I_{C2} - V_{BE3}}{(h_{FE} + 1)4k + 20k} = 100 \frac{20k * 0.248mA - 0.6V}{(100 + 1)4k + 20k} = \underbrace{1.028mA}_{}$$

## EHB222E INTRODUCTION TO ELECTRONICS (21124) Midterm Exam #1 – 19 March 2018

Following the blue loop and recalling that waveform distortion at the output should be minimum and symmetrical, i.e.,  $V_0$  = 0 V

$$\begin{split} &(h_{FE}+1)I_{B3}R_{E4}+V_{EB4}-(I_{C3}-I_{B4})10k5=0\,,\qquad \text{with}\qquad (h_{FE}+1)I_{B4}R_{E4}=10V\\ &10V+V_{EB4}-(I_{C3}-I_{B4})10k5=10V+0,&6V-(1,028\,mA-I_{B4})10k5=0\\ &I_{C4}=h_{FE}\Bigg[1,&028mA-\frac{10,&6V}{10k5}\Bigg]=\underbrace{1,87mA}_{E4}\text{ and }R_{E4}=\underbrace{\frac{10V}{(h_{FE}+1)I_{B4}}}=\underbrace{\frac{5k27}{E4}}_{E4} \end{split}$$