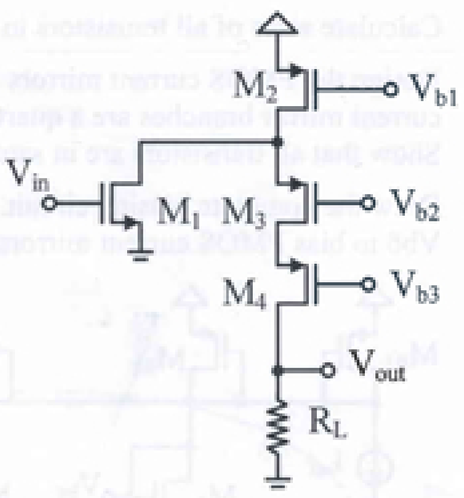
CMOS process parameters for all questions

V_{DD}=1.8V, C_{ox} = 10 fF/μm^2, μ_n = 2.5x10^{10} $\mu m^2 V^{-1} s^{-1}$, μ_p= 10^{10} $\mu m^2 V^{-1} s^{-1}$, V_{THN} = 0.4V, V_{THP} = -0.4V, λ_n=0.1V^{-1}, λ_p=0.2V^{-1}

1) Consider the folded cascode amplifier shown in figure 1. Please Express your answers in terms of small signal prameters of transistors.



a) Determine the output resistance (R_{out1}) of the folded cascode structure composed of M1, M2 and M3.

b) Determine the equivalent transconductance (G_{m1}) of the folded cascode structure composed of M1, M2 and M3.

c) Determine the output resistance (R_{out}) of the complete folded cascode structure composed of M1, M2, M3 and M4

d) Determine the equivalent transconductance (G_m) of the complete folded cascode structure.

e) Determine the voltage gain of the complete amplifier including R_L.

2) Consider the differential amplifier shown in figure 2. Amplifier is perfectly symmetrical (ie. M1 and M1a are identical, M2 and M2a are identical, etc..) A common mode feedback circuit keeps current through M3, M4, M5 and M6 constant under all operating conditions and DC level of the outputs is fixed at $V_{DD}/2$.

Overdrive voltage ($|V_{GS}|-|V_{TH}|$) is 100 mV for all transistors. Drain to source voltage is ±175 mV for M2, M3, M6, M7, M10 and M11. L=540nm for all transistors.

Ignore channel length modulation in all DC calculations. Use it only for small signal parameters.

$(W/L)_9=(W/L)_{10}=200$

$(W/L)_1=(W/L)_5=(W/L)_6=(W/L)_7=100$

$(W/L)_2=(W/L)_{11}=(W/L)_{12}=500$

$(W/L)_3=(W/L)_4=250$

a) Calculate V_{b1}, V_{b2}, V_{b3}, V_{b4}, V_{b5} and V_{b6}

c) Calculate the maximum voltage swing at the output node.

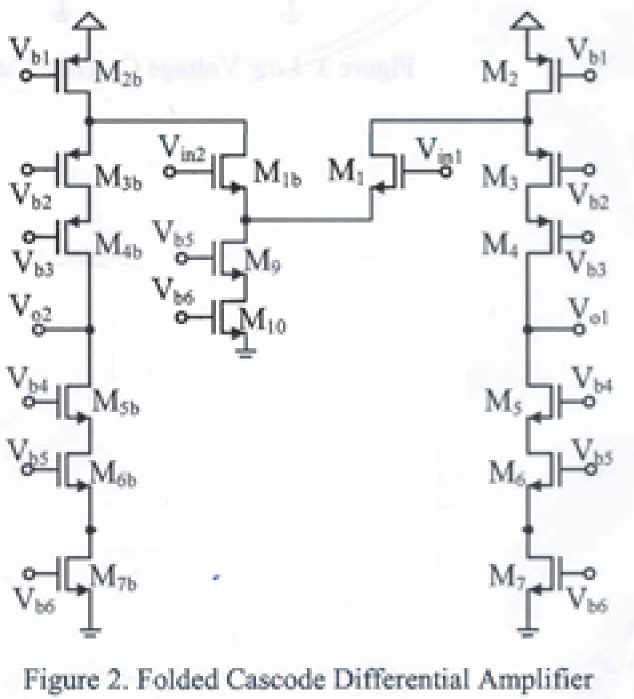


Figure 2. Folded Cascode Differential Amplifier

d) Calculate maximum and minimum value of common mode input voltage.
e) Calculate I_D for each transistor.
f) Calculate g_m and r_o for each transistor.
g) Use half circuit method to split the amplifier into 2. Replace the upper and lower circuits with equivalent Gm and Rout values you determined in question 1.
h) Calculate differential voltage gain. $(V_{o1}-V_{o2})/(V_{in1}-V_{in2})$ using half circuit method.

3) Current mirrors shown in figure 3 are used to generate the bias voltages Vb4, Vb5 and Vb6. M1, M2, M3 and M3a are identical transistors. MR1, MR2, MR3 and MR4 are identical transistors. Iref is half of ID7.

a) M1, M4 and M5 are actual diode connected transistors. In theory, same VGS voltages would be generated by M1 and M4 without M2, M3 and M3a. Explain why M2, M3 and M3a are placed in series with the actual diode connected transistors.
b) Calculate sizes of all transistors in current mirrors. Show that all transistors are in saturation.
c) Design the PMOS current mirrors to generate Vb1, Vb2 and Vb3. Currents flowing in all current mirror branches are a quarter of ID2. Calculate sizes of all transistors in current mirrors. Show that all transistors are in saturation.
d) Draw the complete biasing circuit. Use triple cascode current mirrors biased with Vb4, Vb5 and Vb6 to bias PMOS current mirrors.

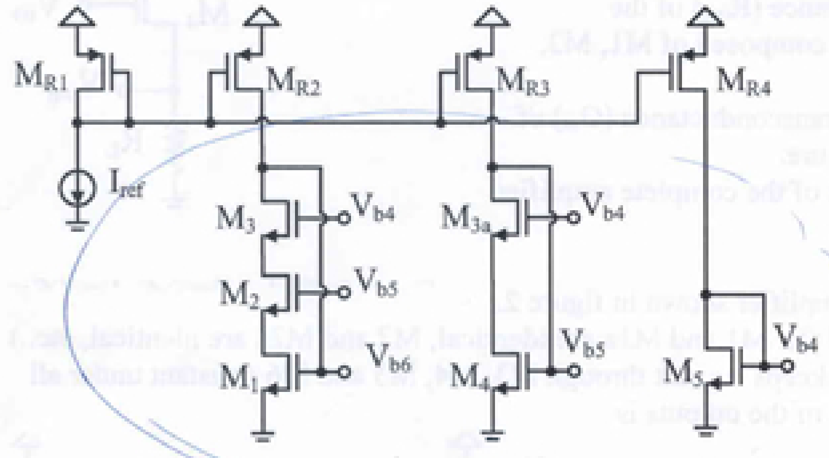


Figure 3. Low Voltage Cascode Current Mirror

1) a) $R_{out1} = (g_{m3} r_{o3} + 1)(r_{o1} \| r_{o2}) + r_{o3}$

b) $G_{m1} = g_{m1} \cdot \dfrac{R_{out1} - r_{o3}}{R_{out1}}$

c) $R_{out} = (g_{m4} r_{o4} + 1)(R_{out1}) + r_{o4}$

d) $G_m = G_{m1} \cdot \dfrac{R_{out} - r_{o4}}{R_{out}}$

e) $A_V = G_m \cdot (R_{out} \| R_L)$
$= \dfrac{G_{m1} \cdot (R_{out} - r_{o4}) R_L}{R_{out} + R_L}$
$= g_{m1} \cdot \dfrac{R_{out1} - r_{o3}}{R_{out1}} \cdot \dfrac{(R_{out} - r_{o4}) R_L}{R_{out} + R_L}$

2) a) $V_{b6} = V_{OD} + V_{TH7} = 500\ mV$

$V_{b5} = V_{OD} + V_{TH5} + V_{O7} = 675\ mV$

$V_{b4} = V_{OD} + V_{TH4} + V_{DS7} + V_{DS6} = 850\ mV$

$V_{b1} = V_{DD} - V_{OD} - |V_{TH2}| = 1.3V$

$V_{b2} = V_{DD} - V_{SD2} - V_{OD} - |V_{TH3}| = 1.125V$

$V_{b3} = V_D - V_{SD2} - V_{SD3} - V_{OD} - |V_{TH4}| = 950\ mV$

c) $V_{omax} = V_{b3} + |V_{TH4}| = 1350\ mV$

$V_{omin} = V_4 - V_{TH5} = 450\ mV$

$V_{swing} = 900\ mV$

d) $V_{D1} = 1.625V$

$V_{Gmax} = V_{D1} + V_{TH1} = 2.025V \rightarrow V_{CM,max} = 1.8V$

$V_{S1min} = V_{D9min} = V_{b5} - V_{TH9} = 275\ mV$

$V_{CM,min} = V_{G1min} = V_{S1min} + V_{GS1} = 0.275 + 0.5V = 0.775V$

e) $I_{10} = \frac{1}{2}(2.5 \times 10^{10})(10^{-14}) 200 (0.10)^2 = 2.5 \times 10^{-4}\ A$

$I_2 = \frac{1}{2}(10^{10})(10^{-14}) 500 (0.1)^2 = 2.5 \times 10^{-4}\ A$

$I_1 = \frac{I_{10}}{2} = 125\,\mu A$

$I_3 = I_2 - I_1 = 125\,\mu A \rightarrow$

$I_4 = I_5 = I_6 = I_7 = I_3 = 125\,\mu A$

f) all NMOS except 9 & 10 are same size with same V_{OD}.

M1-M5-M6-M7:

$g_m = \frac{2I_D}{V_{OD}} = \frac{250\times10^{-6}}{0.1} = 2.5\ mS$ $\quad r_o = \frac{1}{I_D\lambda_n} = \frac{1}{0.1(1.25\times10^{-4})} = 80k\Omega$

M9-M10

$g_m = \frac{2I_D}{V_{OD}} = 5\,mS$ $\quad r_o = \frac{1}{I_D\lambda_n} = \frac{1}{0.1(2.5\times10^{-4})} = 40k\Omega$

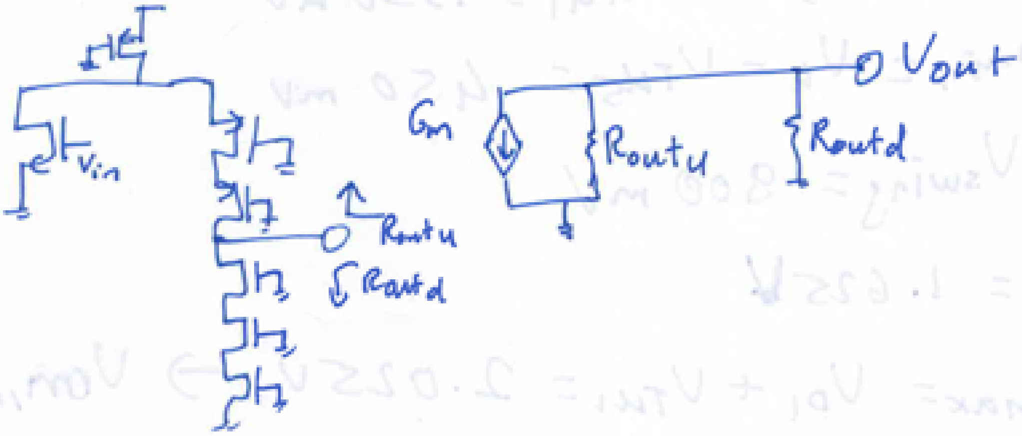
M2

$g_m = \frac{2I_D}{V_{OD}} = 5\,mS$ $\quad r_o = \frac{1}{I_D\lambda_p} = \frac{1}{0.1(2.5\times10^{-4})} = 20k\Omega$

M3-M4

$g_m = \frac{2I_D}{V_{OD}} = \frac{250\times10^{-6}}{0.1} = 2.5\,mS$ $\quad r_o = \frac{1}{I_D\lambda_p} = 40k\Omega$

g)



h)

From Q1

$R_{out1} = (2.5m(40k)+1)(80k \| 20k) + 40k = 101(16k) + 40k = 1656\,k\Omega$

$G_{m1} = g_{m1} \cdot \frac{R_{out1} - r_{o3}}{R_{out1}} = 2.5m\,\frac{1616k}{1656k} = 2.440\ mS$

$R_{out\,u} = (2.5m(40k)+1)(1656k) + 40k = 167.296\ M\Omega$

$G_m = G_{m1} \cdot \frac{167.256}{167.296} = 2.4394\ mS \Rightarrow$ we said if $r_{o1} \to \infty$, $g_{m1} = G_m$. This shows it

$$R_{out_d} = (g_{m5} r_{o5} + 1)\left[(g_{m6} r_{o6}+1) r_{o7} + r_{o6}\right] + r_{o5}$$

$$201\left(201(80k) + 80k\right) + 80k$$

$$= (201(202)+1)\,80k = 3248.240\ M\Omega$$

$$A_v = -G_m (R_{out_u} \,//\, R_{out_d}) = -2.4394\,mS\,(159.1017\ M\Omega)$$

$$= -388\,112.7\ V/V$$

3) a) Channel mod. effects current mirroring performance. That is why we use cascode current mirrors. M2 & M3 makes sure M1 has exactly same drain voltage M7 or M9 (in amp) has. M3a makes sure M4 has exactly the same drain voltage M6 & M9 has. (in amp.)

b) M1, M2, M3, M3a

If $I_{D1} = \dfrac{1.25\,\mu A}{2} = \dfrac{I_{D7}(amp)}{2}$

$$\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 = \left(\frac{W}{L}\right)_3 = \frac{100}{2} \rightarrow (W/L)_7\ (amp)$$

Because they have same V_{GS}.

$$(V_{GS_{4C}} - V_{TH}) = V_{b5} - V_{TH4} = 275\ mV$$

$$\frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_{4C}(275\,mV)^2 = \frac{\frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_7 (100\,mV)^2}{2}$$

$$\left(\frac{W}{L}\right)_{4C} = \frac{100}{2(2.75)^2} = 6.61$$

$$(V_{GS_{5C}} - V_{TH}) = V_{b6} - V_{TH6} = 450\,mV$$

$$(450\,mV)^2 \cdot \left(\frac{W}{L}\right)_{5C} = \frac{(W/L)_7\,(100\,mV)^2}{2} \rightarrow \left(\frac{W}{L}\right)_{5C} = \frac{50}{(4.5)^2}$$

$$\boxed{\left(\frac{W}{L}\right)_{5C} = 2.47}$$

3b) → cont ⇒ M3 is in SAT if

$V_{G4} - V_{TH} < V_{G6} \Rightarrow 850 - 400 = 450 < 500$

(If M3 is in SAT, M2 & M1 are also in SAT since their gate voltages & V_{th} are same as amplifier transistors.)

$V_{D2} = V_{G4} - V_{GS3} = 350\ mV$

$V_{G5} - V_{TH} = 275\ mV < 350\ mV$

$V_{D1} = V_{G5} - V_{GS2} = 175\ mV$

$V_{G6} - V_{TH} = 100\ mV < 175\ mV$

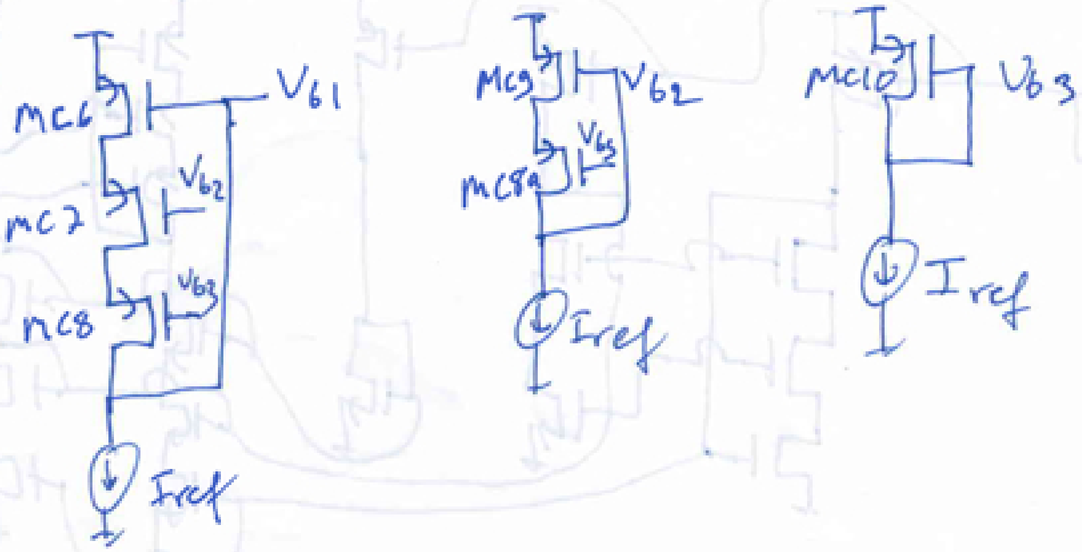
$V_{D3a} = V_{G5} = 675\ mV$

$V_{G4} - V_{TH} = 450\ mV < 675\ mV$

$V_{D4} = V_{G4} - V_{GS3a} = 350\ mV$

$V_{G5} - V_{TH} = 275\ mV < 350\ mV$

3) c)



$$\left(\frac{W}{L}\right)_{C6} = \left(\frac{W}{L}\right)_{C7} = \left(\frac{W}{L}\right)_{C8} = \frac{1}{4} \cdot \left(\frac{W}{L}\right)_2 = 125 = \left(\frac{W}{L}\right)_{C8a}$$

$2 \downarrow$ amp

$$V_{DD} - V_{b2} - |V_{TH}| = 275mV = V_{OD_{C9}}$$

$$\left(\frac{W}{L}\right)_{C9} \cdot (275mV)^2 = \frac{1}{4}\left(\frac{W}{L}\right)_2 (100mV)^2$$

$$\left(\frac{W}{L}\right)_{C9} = \frac{500}{4(2.75)^2} = 16.53$$

$$V_{OD_{C10}} = V_{DD} - V_{b3} - |V_{TH}| = 450mV$$

$$\left(\frac{W}{L}\right)_{C10} = \frac{500}{4(4.5)^2} = 6.17$$

$V_{DC8} = V_{b1} = 1300\ mV$ in SAT

$V_{b3} + |V_{TH}| = 950 + 400 = 1350mV > 1300\ mV$

$V_{DC8a} = V_{b2} = 1125mV$

$V_{b3} + |V_{TH}| = 1350mV > 1125mV$

others are all in SAT.

d)