IMPORTANT: Besides your **calculator** and the sheets you use for calculations you are only allowed to have an A4 sized **"copy sheet"** during this exam. Notes, problems and alike are not permitted. **Please submit your "copy sheet" along with your solutions.** You may get your "copy sheet" back after your solutions have been graded. ***Do not forget to write down units and convert units carefully! Cell phones are not allowed and should be placed on the front desk before the exam.***

ELE222E INTRODUCTION TO ELECTRONICS (10730)
Midterm Exam #1 ✎ 5 November 2013 ⌛ 16.30-18.30
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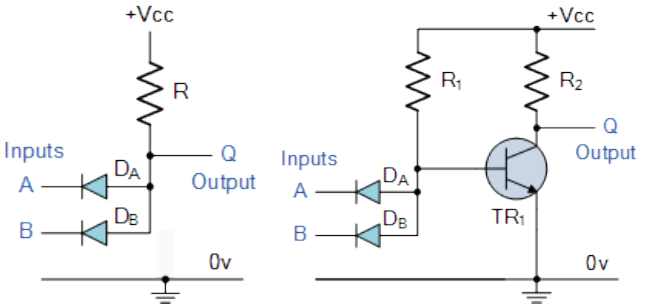
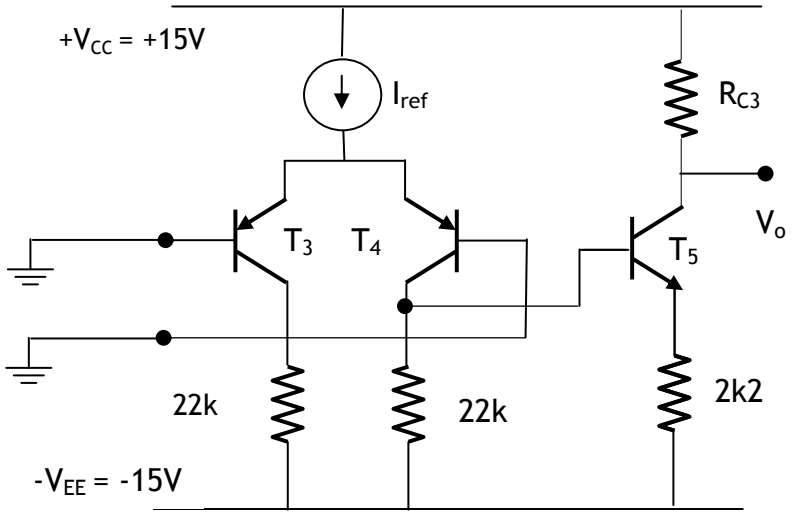
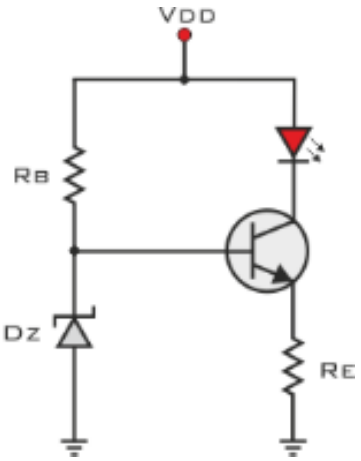
1. Calculate the current through a pn-junction with an area of 0,1 mm^2 forward biased with +0,7 V. Parameters you may need are ρ_n = 0,5 Ωcm, ρ_p = 0,75 Ωcm. Also you know $n_i = 1{,}5\ 10^{10}\ /cm^3$, $q = 1{,}602\ 10^{-19}$ C, $\varepsilon_r = 12$, $\varepsilon_o = 8{,}85\ 10^{-12}$ F/m, V_T = 25,2 mV, D_n = 36 cm^2/s, D_p = 16 cm^2/s, $\tau_n = \tau_p$ = 0,8 µsec. Finally calculate the junction capacitance when your pn-junction (diode) is reverse biased at +5 V. (25 points)

2. Look at the two logic circuits (gates) below. The simple 2-input ***Diode-Resistor Logic Gate*** on the left is converted into another logic gate by the addition of a single BJT transistor. Now complete look-up tables for each. Assume logic 0 ≡ low voltage; such as 0 V and logic 1 ≡ high voltage ; such as V_{CC} Which logic functions do these circuits realize? Analyze states for A < B, A > B, and A = B with V_D = 0,6 V. (20 points)

A↓\B→	Logic 0	Logic 1
Logic 0		
Logic 1		







3. In the figure to the right you see a ***Single Transistor Constant Current Driver*** with voltage regulation. V_Z = 5,1 V with a minimum Zener current of 1-2 mA. V_{BE} = 0,6 V, h_{FE} = 100, V_{DD} = 12 V. Find the resistor values to regulate the LED current at 20 mA. (20 points)

GOOD LUCK

4. Study DC characteristics of the 2-stage BJT amplifier circuit shown on the left with $|V_{BE}|$ = 0,6 V, and h_{FE} = 100 for all three transistors.

   Design a **current source** that will provide 0,4 mA biasing current to the differential stage. (T_1 and T_2 will be in that circuit!)(10 points)

How should R_{C3} be chosen, such that, waveform distortion at the output V_o is minimum and symmetrical, i.e. V_o = 0V?

Do NOT neglect base currents. (25 points)

SOLUTIONS:

1. Using Einstein relationship $V_T = \frac{D_n}{\mu_n} = \frac{D_p}{\mu_p} \Rightarrow \underline{\mu_n = 1430 cm^2/Vs; \mu_p = 634 cm^2/Vs}$

$$\sigma_p = \frac{1}{\rho_P} = q\mu_p N_A \Rightarrow \underline{N_A = 1{,}31 \cdot 10^{16}/cm^3}$$

$$\sigma_n = \frac{1}{\rho_n} = q\mu_n N_D \Rightarrow \underline{N_D = 8{,}75 \cdot 10^{15}/cm^3}$$

Using $L_n = \sqrt{\tau_n D_n}; L_p = \sqrt{\tau_p D_p} \Rightarrow \underline{L_n = 53{,}7\mu m; L_p = 35{,}8\mu m}$

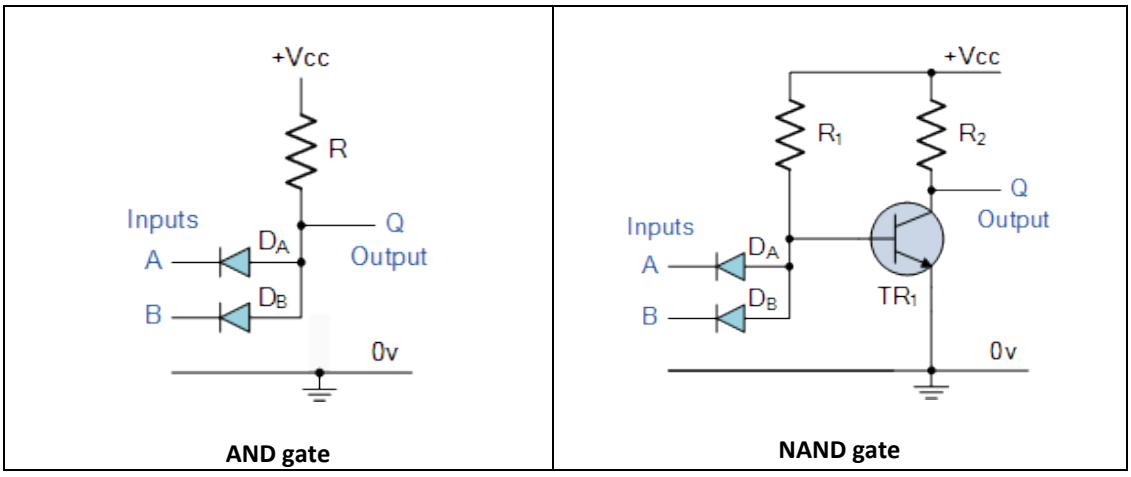
$$I_D(V = 0{,}7V) = A \cdot q \cdot n_i^2 \cdot \left[\frac{D_p}{L_p N_D} + \frac{D_n}{L_n N_A}\right]\left(e^{V/V_T} - 1\right) = \underline{41mA}$$

$$V_B = V_T \cdot \ln\left(\frac{N_A \cdot N_D}{n_i^2}\right) = \underline{680mV}$$

Using $w_{dep}(V_{reverse} = 5V) = \sqrt{\frac{2 \cdot \varepsilon_o \varepsilon_r}{q}(V_B + V)\left(\frac{1}{N_A} + \frac{1}{N_D}\right)} = \underline{1{,}2\mu m}$, thus

$$C(V_{reverse} = 5V) = \varepsilon_o \cdot \varepsilon_r \frac{A}{w} = \underline{8{,}87\,pF}$$

2. First have a look at the circuit w/o the BJT. With one or both of the inputs LOW (i.e., connected to ground, LOGIC 0), current will flow across R and the output voltage will drop close to 0, i.e., will be LOW. When both inputs are HIGH (LOGIC 1), the will be not current flow and thus output voltage will be equal to V_{CC}, i.e., HIGH.



AND gate **NAND gate**

A↓\B→	Logic 0	Logic1
Logic 0	0	0
Logic1	0	1

A↓\B→	Logic 0	Logic1
Logic 0	1	1
Logic1	1	0

Now the second one. With one or both of the inputs LOW, base voltage will be LOW, practically ZERO, and the BJT will be OFF. With no collector current on, the output will be HIGH. On the other hand, if both inputs are HIGH, they are reverse biased BUT the transistor is ON, V_{BE} biased by the current flowing through R_1 to BE.
For more information also look at http://www.electronics-tutorials.ws/logic/logic_1.html

3. http://www.pcbheaven.com/userpages/LED_driving_and_controlling_methods/?topic=worklog&p=2

$$V_E = V_B - V_{BE} = V_Z - V_{BE} = 5{,}1 - 0{,}6 = 4{,}5V$$

$$I_C = 20mA \Rightarrow I_E = \frac{h_{FE}+1}{h_{FE}} I_C = 20{,}2mA$$

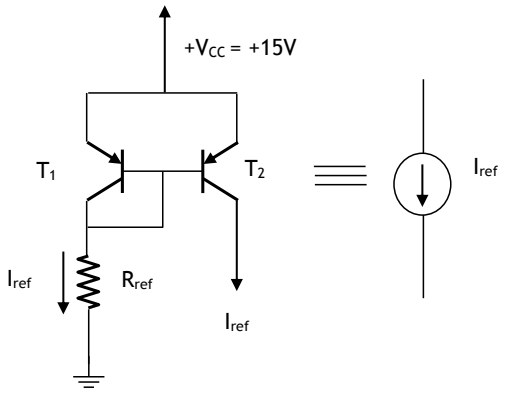
$$\Rightarrow R_E = \frac{V_E}{I_E} = \underline{\underline{222{,}7\Omega}}$$

Now assuming minimum Zener current of 2 mA (you could have assumed 1 or 2, or solve the problem for the Zener current somewhere between 1 and 2 mA):

$$R_B = \frac{V_{DD} - V_Z}{I_B + I_Z} = \frac{12V - 5{,}1V}{I_C / h_{FE} + I_Z} = \frac{12V - 5{,}1V}{200\mu A + 2mA} = \underline{\underline{3k14}} \text{ or}$$

$$R_B = \frac{V_{DD} - V_Z}{I_B + I_Z} = \frac{12V - 5{,}1V}{I_C / h_{FE} + I_Z} = \frac{12V - 5{,}1V}{200\mu A + 1mA} = \underline{\underline{5k75}}$$

4.



$$R_{ref} = \frac{15V - V_{EB1}}{I_{ref}} = \frac{15V - 0{,}6V}{0{,}4mA} = \underline{\underline{36k}}$$ However, we also need to make sure that T_2 operates in the normal operating region, i.e., $V_{C2} < V_{B2}$. The current mirror is connected to the common emitters of T_1 and T_2. The emitter voltage of the differential stage is $V_E = V_B + V_{EB} = 0 + 0{,}6V = 0{,}6V$.

On the other hand

$$V_{B2} = V_{CC} - V_{BE1} = 15V - 0{,}6V = 14{,}4V > 0{,}6V$$

This satisfies the condition $V_{C2} < V_{B2}$.

From the loop of 22k resistance connected to the collector of T_4, V_{BE5} and the 2k2 resistor:

$$-22k*(I_{C4} - I_{B5}) + V_{BE5} + 2k2*(1+h_{FE5})I_{B5} = 0$$

$$I_{C4} = \frac{I_{ref}}{2} \cdot \frac{h_{FE}}{h_{FE}+1} = \underline{\underline{0{,}198mA}}$$

$$I_{C5} = h_{FE5}\frac{22k * I_{C4} - V_{BE5}}{(h_{FE5}+1)2k2 + 22k} = 100\frac{22k * 0{,}198mA - 0{,}6V}{(100+1)2k2 + 22k} = \underline{\underline{1{,}78mA}}$$

Since $V_0 = +V_{CC} - R_{C3} * I_{C5} = 0V$ we find R_{C3} = <u>8k41</u> .

<u>Hereby note</u> we did NOT neglect the base currents of the differential stage because h_{FE} is only 100!