IMPORTANT: Besides your **calculator** and the sheets you use for calculations you are only allowed to have an A4 sized **"copy sheet"** during this exam. Notes, problems and alike are not permitted. **Please submit your "copy sheet" along with your solutions.** You may get your "copy sheet" back after your solutions have been graded. ***Do not forget to write down units and convert units carefully! Cell phones are not allowed and should be placed on the front desk before the exam.***

ELE222E INTRODUCTION TO ELECTRONICS (21454)
Midterm Exam #1 ✐ 31 March 2014 ⌛ 9.30-11.30

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EEF 5201 and 2014

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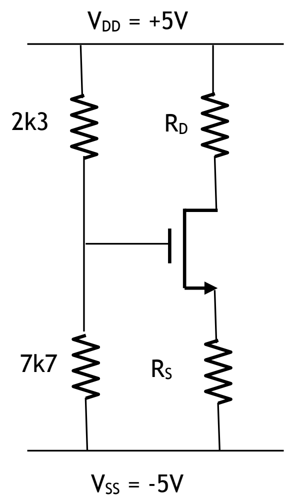
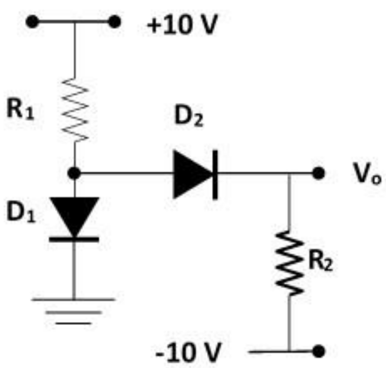
1. Assume you are to create a diode using n- and p-typed doped silicon with the following doping parameters: **N_D = 3 10^{17} /cm^3**, and **N_A = 10^{15} /cm^3**. You also know **L_n = 10 µm, L_p = 4 µm, μ_n = 1600 cm^2/Vs, μ_p = 600 cm^2/Vs. n_i = 1,5 10^{10} 1/cm^3, q = 1,602 10^{-19} C, ε_r = 12, ε_o = 8,85 10^{-12} F/m, V_T = 25 mV.**
   a. Find the barrier voltage and saturation current for a junction area of **0,1 mm^2**. (6 points)
   b. Calculate the specific conductivities of n- and p-type doped silicon. (6 points)
   c. Determine the depletion zone width in **unbiased** state, when the junction is reverse biased at **4,7 V** and when it is forward biased at **0,47 V**. (9 points)
   d. Calculate the junction capacitances for the cases in (c). (9 points)

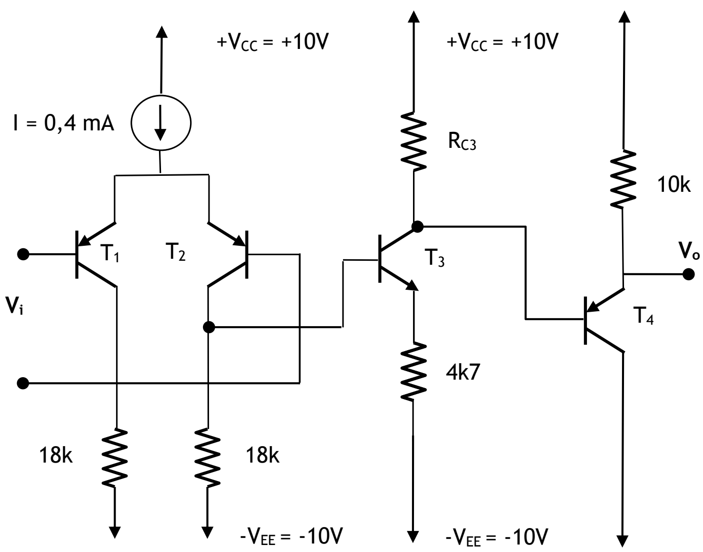


2. Assuming constant voltage drop in forward bias with the barrier potential found in **Problem 1** *(if you could not solve Problem 1 use 0,7 V)* calculate **V_o** and the <u>current flowing through D_1</u> (**I_{D1}**) for
   a. **R_1 = 10k** and **R_2 = 5k**, and (10 points)
   b. **R_1 = 5k** and **R_2 = 10k** (10 points).



3. The MOS transistor shown on the circuit to the left has the following properties: **V_T = 2 V,** $\mu_n C_{ox}\left(\frac{W}{L}\right) = 2\ mA/V^2$ Find the missing resistors values for the MOS to operate in saturation with **I_D = 1 mA**. (20 points).

4. Study DC characteristics of the 3-stage BJT amplifier circuit with **$|V_{BE}|$ = 0,6 V, h_{FE} = 200** for all four transistors. **Do not neglect base currents.**
   a. Design a current source that will provide **0,4 mA biasing current** to the differential stage. (10 points)
   b. Choose **R_{C3}** such that, waveform distortion at the output V_o is minimum and symmetrical, i.e., **V_o = 0V**? (30 points)



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SOLUTIONS:

1. Using Einstein Equation , i.e., $D_{p/n} = V_T \mu_{p/n} \Rightarrow D_p = 15\frac{cm^2}{s};\ D_n = 40\frac{cm^2}{s}$

   a. $V_B = V_T \cdot \ln\left(\frac{N_A \cdot N_D}{n_i^2}\right) = \underline{\underline{698mV}}$ and

   $$I_o = A \cdot q \cdot n_i^2 \cdot \left[\frac{D_p}{L_p N_D} + \frac{D_n}{L_n N_A}\right] = \underline{\underline{1{,}45pA}}$$

   b. $\sigma_p = q \cdot \left(\frac{n_i^2}{N_A}\mu_n + N_A \mu_p\right) \cong qN_A\mu_p = \underline{\underline{0{,}096/(\Omega cm)}}$

   $$\sigma_n = q \cdot \left(N_D \mu_n + \frac{n_i^2}{N_D}\mu_p\right) \cong qN_D\mu_n = \underline{\underline{76{,}9/(\Omega cm)}}$$

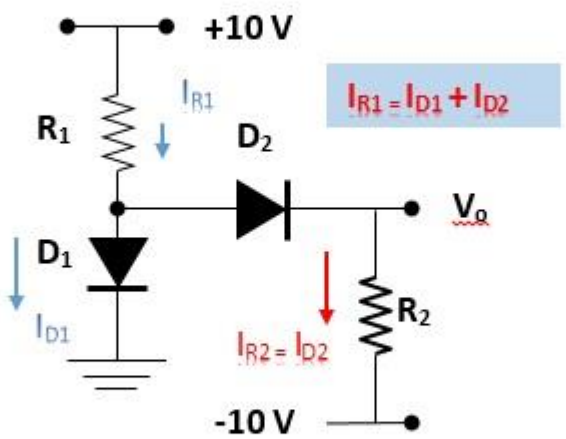
   c. unbiased $w_{dep} = \sqrt{\frac{2 \cdot \varepsilon_o \cdot \varepsilon_r \cdot V_B}{q}\left(\frac{1}{N_A} + \frac{1}{N_D}\right)} = \underline{\underline{0{,}963\mu m}}$

   with reverse bias at 4,7 V, $w_{dep} = \sqrt{\frac{2 \cdot \varepsilon_o \cdot \varepsilon_r \cdot (V_B + V_{bias})}{q}\left(\frac{1}{N_A} + \frac{1}{N_D}\right)} = \underline{\underline{2{,}68\mu m}}$

   with forward bias at 0,47 V, $w_{dep} = \sqrt{\frac{2 \cdot \varepsilon_o \cdot \varepsilon_r \cdot (V_B - V_{bias})}{q}\left(\frac{1}{N_A} + \frac{1}{N_D}\right)} = \underline{\underline{0{,}55\mu m}}$

   d. Thus, $C = \varepsilon_o \cdot \varepsilon_r \frac{A}{w} = \begin{cases} \underline{\underline{11pF}}, unbiased \\ \underline{\underline{3{,}96pF}}, reverse@4{,}7V \\ \underline{\underline{19{,}28pF}},\ forward@0{,}47V \end{cases}$

2. Pure mathematics assuming the directions given below yield the following results for currents through resistors and diodes:



R1 **R2**

a	1,00E+04	5,00E+03	**IR1**	9,30E-04	**ID2**	2,00E-03	**ID1**	**-1,07E-03**	NO WAY
b	5,00E+03	1,00E+04	**IR1**	1,86E-03	**ID2**	1,00E-03	**ID1**	8,60E-04	

INTERPRETATION:

a. That means, when R_1 = 10k and R_2 = 5k, D_2 is **NOT** conducting!
   THUS, $I_{D1} = I_{R1} = \frac{10-(-10)-0{,}7}{15k} = 1{,}28mA;\ V_o = -10V + 5k * 1{,}28mA = -2{,}87V$
b. When R_1 = 5k and R_2 = 10k , $I_{D1} = I_{R1} - I_{D2} = 0{,}86\ mA;\ V_o = 0V$

3. The MOS design looks very simple BUT many make mistakes. 2k3 and 7k7 resistors divide the 10 V voltage difference, such that $V_G = -5V + 7{,}7V = 2{,}7V$.

   From the given properties it is obvious that $V_{GS} - V_t = 1V$.

   Since we are working with NMOS $V_{GS} = 3V \Rightarrow V_S = V_G - V_{GS} = -0{,}3\ V \Rightarrow R_S = \frac{V_S - V_{SS}}{I_D} = \frac{4{,}7V}{1mA} = 4k7$

   For the NMOS to operate in saturation $V_{DS} = V_{GS} - V_t = 1V \Rightarrow V_D = V_S + 1V = -0{,}3 + 1 = 0{,}7\ V$

$$R_D = \frac{V_{DD} - V_D}{I_D} = \frac{5 - 0{,}7}{1mA} = 4k3$$

4. DC characteristics are to be studied.
   a. You do your own design!
   b. <u>Without neglecting</u> the base currents of the differential (the very first) stage, for V_i = 0 V

$$I_{C1} = I_{C2} = \frac{h_{FE}}{h_{FE}+1} \cdot \frac{I_{ref}}{2} = \frac{200}{200+1} \cdot \frac{0{,}4mA}{2} \Rightarrow I_{C1} = I_{C2} = \underline{\underline{0{,}199mA}}$$

$$-(I_{C2} - I_{B3})18k + V_{BE3} + (h_{FE}+1)I_{B3}4k7 = 0$$

$$I_{C3} = h_{FE}\frac{18k * I_{C2} - V_{BE3}}{(h_{FE}+1)4k7 + 18k} = 200\frac{18k * 0{,}199mA - 0{,}6V}{(200+1)4k7 + 18k} = \underline{\underline{0{,}62mA}}$$

That the output voltage is in the middle of the power supply range (+10 V and -10 V), V_o = 0 V

$$(h_{FE}+1)I_{B3}R_{E4} + V_{EB4} - (I_{C3} - I_{B4})R_{C3} = 0, \text{ with } (h_{FE}+1)I_{B4}10k = 10V \Rightarrow I_{E4} = \underline{\underline{1mA}}$$

$$(I_{C3} - I_{B4})R_{C3} = 10V + V_{EB4} \Rightarrow R_{C3} = \frac{10V + V_{EB4}}{I_{C3} - I_{B4}} = \underline{\underline{17k25}}$$