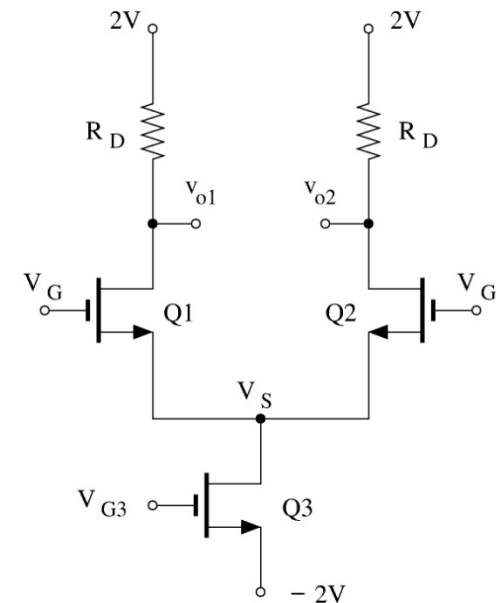


# **Exercises for Differential Amplifiers**

Exercise 1: Compute  $V_D$ ,  $V_S$ ,  $V_{DS}$  and  $V_{GS}$  if  $I_{D3} = 2 \text{ mA}$ ,  $R_D = 500 \Omega$ ,  $V_{OV3} = 0.5 \text{ V}$ , and identical Q1 & Q2 with  $\mu_n C_{ox} (W/L) = 8 \text{ mA/V}^2$ ,  $V_t = 0.5 \text{ V}$ ,  $\lambda = 0$ .  
 A) For  $V_G = 0$  and B) For  $V_G = 1 \text{ V}$ . Repeat the exercise for  $\lambda = 0.1 \text{ V}^{-1}$ .



- This exercise shows that precise biasing of Q1 and Q2 is not necessary as  $V_S$  adjusts itself automatically.
- Inclusion of channel-length modulation does not impact the bias points of Q1 and Q2 (which is set by the current source).

Ignoring channel-length modulation ( $\lambda = 0$ )

$$I_{D1} = I_{D2} = 0.5I_{D3} = 1 \text{ mA}$$

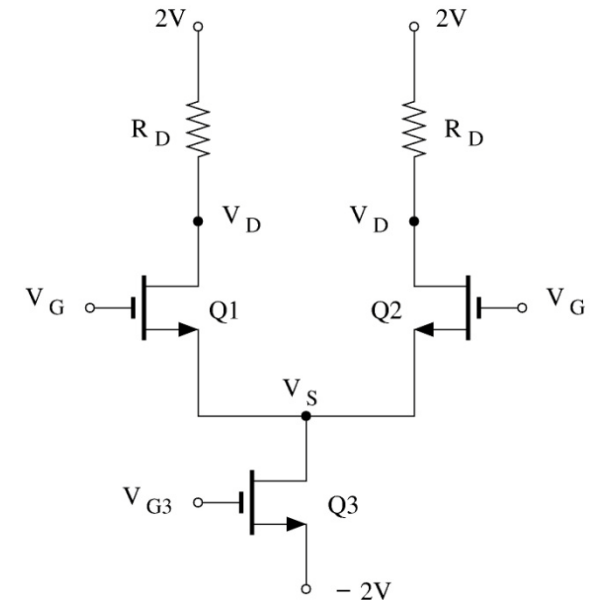
$$\text{KVL: } V_{D1} = 2 - R_D I_{D1} = 2 - 0.5 = 1.5 \text{ V}$$

Assume Saturation

$$1 \times 10^{-3} = I_{D1} = 0.5 \mu_n C_{ox} (W/L) V_{OV1}^2 = 4 \times 10^{-3} V_{OV1}^2$$

$$V_{OV1} = 0.5 \text{ V}$$

$$V_{GS1} = V_{OV1} + V_t = 1 \text{ V}$$



A)  $V_{G1} = 0$

$$V_S = V_{G1} - V_{GS1} = 0 - 1 = -1 \text{ V}$$

$$V_{DS1} = V_{D1} - V_S = 1.5 - (-1) = 2.5 \text{ V}$$

$$V_{DS3} = V_S - (-2) = -1 + 2 = 1 \text{ V}$$

$$V_{DS1} > V_{OV1} \text{ \& } V_{DS3} > V_{OV3} \Rightarrow \text{Saturation}$$

A)  $V_{G1} = 1$

$$V_S = V_{G1} - V_{GS1} = 1 - 1 = 0$$

$$V_{DS1} = V_{D1} - V_S = 1.5 - 0 = 1.5 \text{ V}$$

$$V_{DS3} = V_S - (-2) = 0 + 2 = 2 \text{ V}$$

$$V_{DS1} > V_{OV1} \text{ \& } V_{DS3} > V_{OV3} \Rightarrow \text{Saturation}$$

Note that as the bias voltage of Q1,  $V_{G1}$ , changes,  $V_S$  is adjusted automatically to get the necessary  $V_{OV1}$  and  $I_{D1}$

## Including channel-length modulation ( $\lambda = 0.1$ )

$$I_{D1} = I_{D2} = 0.5 I_{D3} = 1 \text{ mA}$$

$$\text{KVL: } V_{D1} = 2 - R_D I_{D1} = 2 - 0.5 = 1.5 \text{ V}$$

Assume Saturation

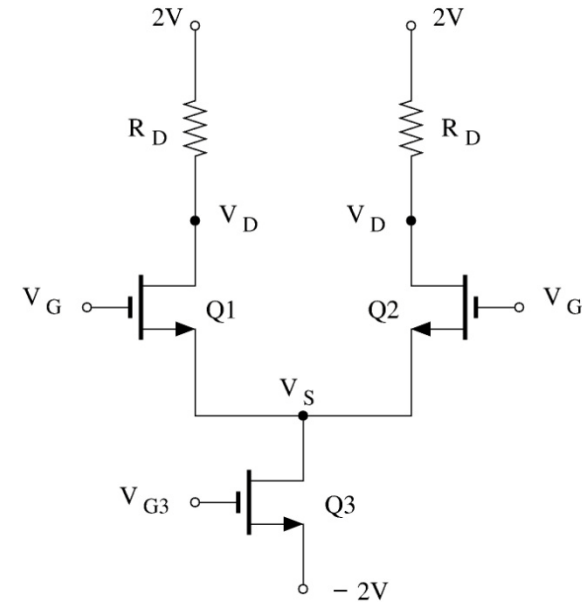
$$1 \times 10^{-3} = I_{D1} = 0.5 \mu_n C_{ox} (W/L) V_{OV1}^2 (1 + \lambda_n V_{DS1})$$

$$V_{OV1}^2 (1 + 0.1 V_{DS1}) = 0.25$$

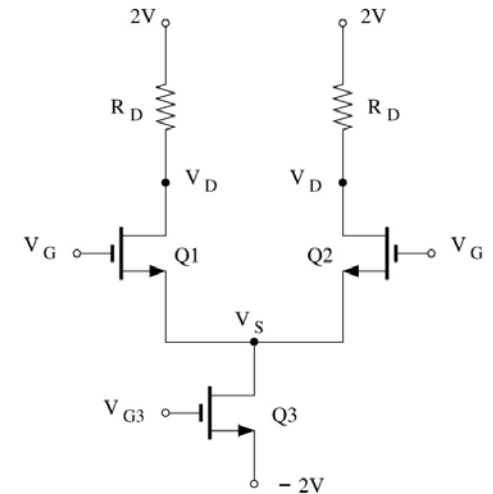
Need to write  $V_{DS1}$  in terms of  $V_{OV1}$ :

$$\begin{aligned} V_{DS1} &= V_{D1} - V_S \\ &= V_{D1} + (V_{GS1} - V_{G1}) \\ &= V_{D1} + (V_{OV1} + V_t) - V_{G1} \\ &= V_{OV1} + (V_{D1} + V_t - V_{G1}) \end{aligned}$$

For a given  $V_{G1}$ , we then substitute for  $V_{DS1}$  in  $I_D$  equation which leads to a cubic equation for  $V_{OV1}$



Including channel-length modulation ( $\lambda = 0.1$ )



$$V_{D1} = 1.5 \text{ V}$$

$$V_{OV1}^2 (1 + 0.1 V_{DS1}) = 0.25$$

$$V_{DS1} = V_{D1} + (V_{OV1} + V_t) - V_{G1}$$

C)  $V_{G1} = 0$

$$V_{DS1} = V_{OV1} + (1.5 + 0.5 - 0) = V_{OV1} + 2.0$$

$$V_{OV1}^2 [1 + 0.1(V_{OV1} + 2.0)] = 0.25$$

$$0.1V_{OV1}^3 + 1.2V_{OV1}^2 - 0.25 = 0$$

$$V_{OV1} = 0.448 \text{ V}$$

$$V_{GS1} = V_{OV1} + V_t = 0.948 \text{ V}$$

$$V_S = V_{G1} - V_{GS1} = 0 - 0.948 = -0.948 \text{ V}$$

$$V_{DS1} = 2.0 + V_{OV1} = 2.448 \text{ V}$$

$$V_{DS3} = V_S - (-2) = -0.948 + 2 = 1.052 \text{ V}$$

D)  $V_{G1} = 1 \text{ V}$

$$V_{DS1} = V_{OV1} + (1.5 + 0.5 - 1) = V_{OV1} + 1.0$$

$$V_{OV1}^2 [1 + 0.1(V_{OV1} + 1.0)] = 0.25$$

$$0.1V_{OV1}^3 + 1.1V_{OV1}^2 - 0.25 = 0$$

$$V_{OV1} = 0.467 \text{ V}$$

$$V_{GS1} = V_{OV1} + V_t = 0.967 \text{ V}$$

$$V_S = V_{G1} - V_{GS1} = 1 - 0.967 = +0.033 \text{ V}$$

$$V_{DS1} = 1.0 + V_{OV1} = 1.467 \text{ V}$$

$$V_{DS3} = V_S - (-2) = 0.033 + 2 = 2.033 \text{ V}$$

➤ Bias voltage of Q1 and Q2 ( $V_G$ ) does not affect  $I_{D1}$  as  $V_S$  adjusts itself automatically.  $V_G$  affects only  $V_{DS1}$  and  $V_{DS3}$  and precise biasing is NOT necessary.

**Ignore channel-length modulation**

**Include channel-length modulation**

$I_{D1} = I_{D2}$	$= 1.0 \text{ mA}$	1.0 mA	1.0 mA	1.0 mA	Specified parameters
$V_{OV1} = V_{OV2}$	$= 0.500 \text{ V}$	0.500 V	0.448 V	0.467 V	
$V_{G1} = V_{G2}$	$= 0 \text{ V}$	1.0 V	0	1.0 V	
$V_S$	$= -1.00 \text{ V}$	0	$-0.948 \text{ V}$	$0.033 \text{ V}$	
$V_{DS1}$	$= 2.50 \text{ V}$	1.50 V	$2.448 \text{ V}$	$1.467 \text{ V}$	
$V_{DS3}$	$= 1.00 \text{ V}$	2.0 V	$1.052 \text{ V}$	$2.033 \text{ V}$	

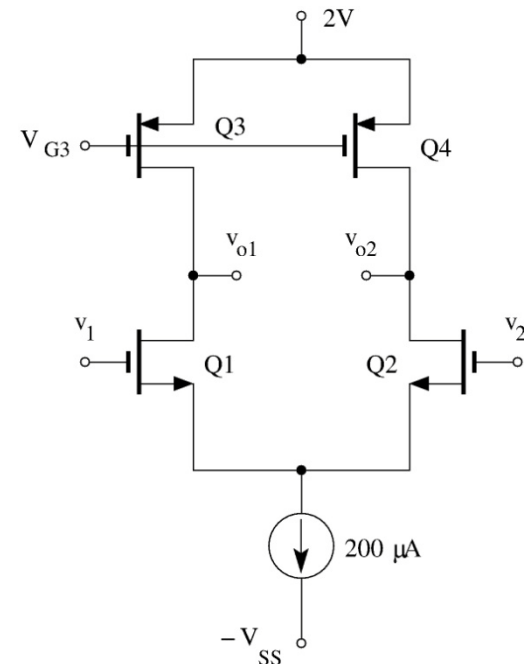
➤ Inclusion of channel-length modulation does not impact the bias points of Q1 and Q2 (which is set by the Q3 current source).

Exercise 2: Find the differential gain and ( $W/L$ ) of all transistors in the circuit below, Q3 & Q4 are matched, Q1 & Q2 are matched, all transistors have  $V_{OV} = 0.2$  V,  $\mu_n C_{ox} = 400 \mu\text{A}/\text{V}^2$ ,  $\mu_p C_{ox} = 100 \mu\text{A}/\text{V}^2$ , and  $V_{An} = |V_{Ap}| = 3.6$  V. Ignore channel-length modulation in biasing calculations.

**For symmetric circuits:**

$$v_{o2} = -v_{o1} \rightarrow v_{o,d} = v_{o2,d} - v_{o1,d} = -2v_{o1,d}$$

$$A_d = \frac{v_{o,d}}{v_d} = -2 \times \frac{v_{o1,d}}{v_d} = \frac{v_{o1,d}}{-0.5v_d}$$



Since transistors are matched and have the same  $V_{OV}$ :

$$I_{D1} = I_{D2} = I_{D3} = I_{D4} = 100 \mu\text{A}$$

$$100 \times 10^{-6} = I_{D1} = 0.5 \mu_n C_{ox} (W/L)_1 V_{OV1}^2$$

$$(W/L)_1 = 12.5 = (W/L)_2$$

$$100 \times 10^{-6} = I_{D3} = 0.5 \mu_p C_{ox} (W/L)_3 V_{OV3}^2$$

$$(W/L)_3 = 50 = (W/L)_4$$

$$A_d = \frac{v_{o,d}}{v_d} = \frac{v_{o,1d}}{-0.5v_d}$$

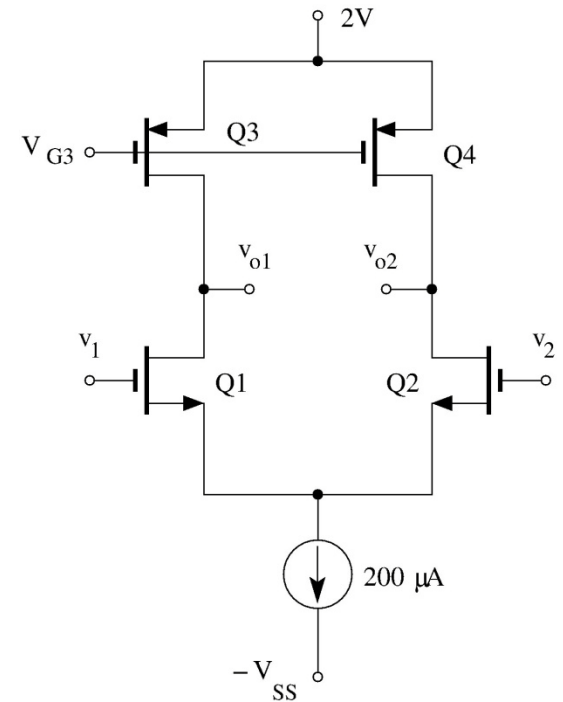
$$= -g_{m1}(r_{o1} \parallel r_{o3})$$

$$g_{m1} = \frac{2I_{D1}}{V_{OV1}} = 10^{-3} \text{ A/V}$$

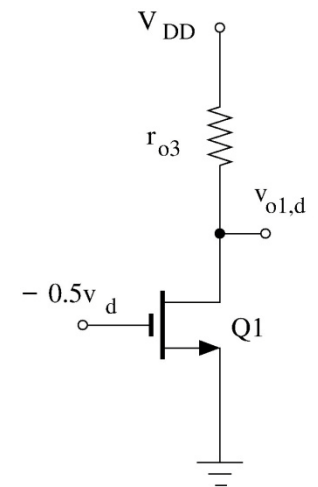
$$r_{o1} = \frac{V_{A1}}{I_{D1}} = 36 \text{ k}$$

$$r_{o3} = \frac{V_{A3}}{I_{D3}} = 36 \text{ k}$$

$$A_d = -g_{m1}(r_{o1} \parallel r_{o3}) = -10^{-3}(36 \text{ k} \parallel 36 \text{ k}) = -10^{-3} \times 18 \times 10^3 = -18$$



Differential Mode  
Half Circuit



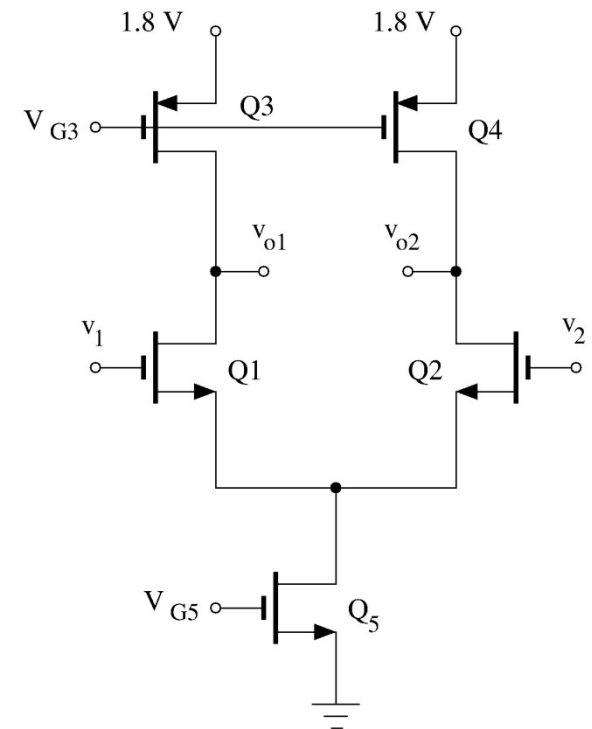


Exercise 3: The differential amplifier below should achieve a differential gain of 40 with a power consumption of 2 mW. All transistors operate with the same  $V_{OV}$ . Find  $(W/L)$  of all transistors,  $V_{G3}$ ,  $V_{G4}$ , and  $V_{G5}$ . ( $\mu_n C_{ox} = 400 \mu\text{A/V}^2$ ,  $\mu_p C_{ox} = 100 \mu\text{A/V}^2$ ,  $\lambda_n = 0.1 \text{ /V}$ ,  $\lambda_p = 0.2 \text{ /V}$ , and  $V_{tn} = |V_{tp}| = 0.4 \text{ V}$ . Ignore channel-length modulation in biasing.

Power Consumption:

$$P = 1.8 I_{D5} = 2 \times 10^{-3} \rightarrow I_{D5} = 1.11 \text{ mA}$$

$$I_{D1} = I_{D2} = I_{D3} = I_{D4} = 0.5 I_{D5} = 0.556 \text{ mA}$$



$$A_d = \frac{v_{o,d}}{v_d} = \frac{v_{o,1d}}{-0.5v_d}$$

$$= -g_{m1}(r_{o1} \parallel r_{o3})$$

$$r_{o1} = \frac{1}{\lambda_n I_{D1}}$$

$$r_{o3} = \frac{1}{\lambda_p I_{D3}} = \frac{1}{\lambda_p I_{D1}} = \frac{\lambda_n}{\lambda_p} \times \frac{1}{\lambda_n I_{D1}} = \frac{\lambda_n}{\lambda_p} \times r_{o1} = 0.5r_{o1}$$

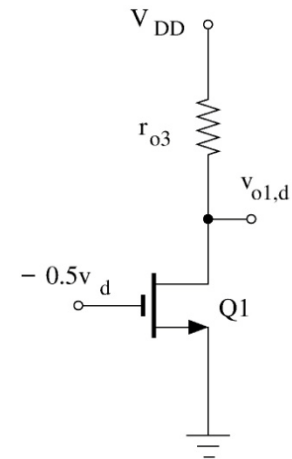
$$r_{o1} \parallel r_{o3} = \frac{r_{o1} \times (0.5r_{o1})}{r_{o1} + 0.5r_{o1}} = \frac{r_{o1}}{3}$$

$$|A_d| = +g_{m1}(r_{o1} \parallel r_{o3}) = \frac{1}{3} g_{m1} r_{o1}$$

$$= \frac{1}{3} \times \frac{2I_{D1}}{V_{OV1}} \times \frac{1}{\lambda_n I_{D1}} = \frac{2}{0.3V_{OV1}} = 40$$

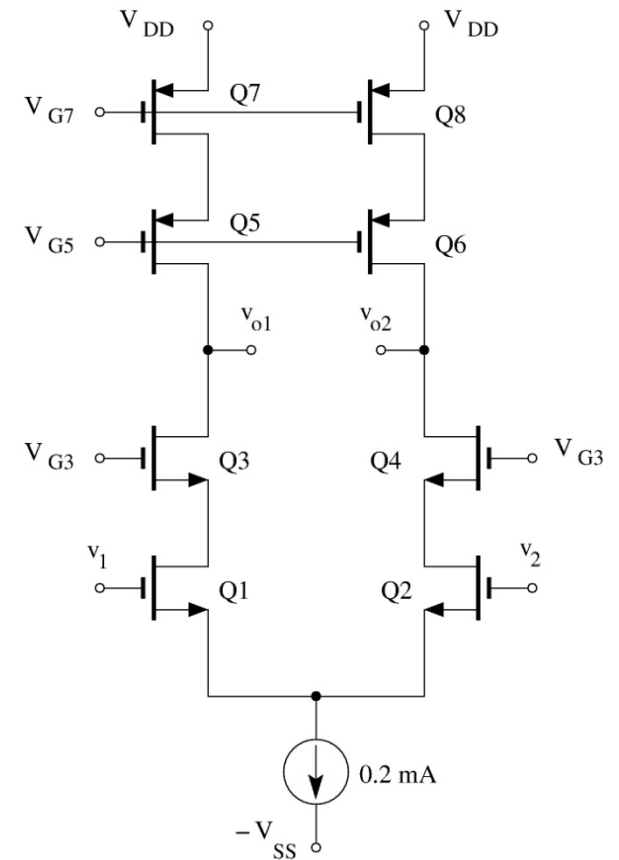
$$V_{OV1} = 0.167 \text{ V}$$

## Differential Mode Half Circuit





Exercise 4: The circuit below is fabricated with  $V_{An} = |V_{Ap}| = 3.6$  V,  $\mu_n C_{ox} = 100 \mu\text{A}/\text{V}^2$  &  $\mu_p C_{ox} = 25 \mu\text{A}/\text{V}^2$ . All transistors operate with  $V_{OV} = 0.5$  V. Find  $(W/L)$  of all transistors and the differential gain of the circuit.



$$\lambda_n = \lambda_p = \frac{1}{V_A} = \frac{1}{3.6} = 0.278 \text{ /V}$$

$$I_{D1} = I_{D2} = \dots = I_{D8} = 0.5 I_{D9} = 100 \text{ } \mu\text{A}$$

$$V_{OV1} = V_{OV2} = \dots = V_{OV8} = V_{OV9} = 0.5 \text{ V}$$

$$g_{m1} = g_{m2} = \dots = g_{m8} = \frac{2I_{D1}}{V_{OV1}} = \frac{2 \times 100 \times 10^{-6}}{0.5} = 0.4 \text{ mA/V}$$

$$r_{o1} = r_{o2} = \dots = r_{o8} = \frac{1}{\lambda I_{D1}} = \frac{1}{0.278 \times 100 \times 10^{-6}} = 36 \text{ k}$$

NMOS: Q1, Q2, Q3, & Q4:

$$I_{D1} = 0.5 \mu_n C_{ox} (W/L)_1 V_{OV1}^2$$

$$100 \times 10^{-6} = 0.5 \times 100 \times 10^{-6} (W/L)_1 \times (0.5)^2$$

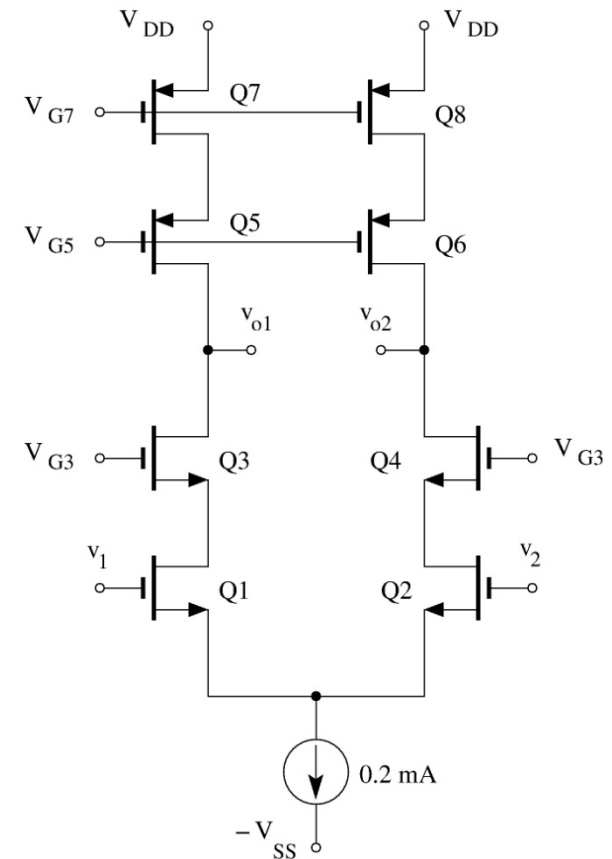
$$(W/L)_4 = (W/L)_3 = (W/L)_2 = (W/L)_1 = 8$$

PMOS: Q5, Q6, Q7, & Q8:

$$I_{D5} = 0.5 \mu_p C_{ox} (W/L)_5 V_{OV5}^2$$

$$100 \times 10^{-6} = 0.5 \times 25 \times 10^{-6} (W/L)_5 \times (0.5)^2$$

$$(W/L)_8 = (W/L)_7 = (W/L)_6 = (W/L)_5 = 32$$



$$A_d = \frac{v_{o,d}}{v_d} = -2 \times \frac{v_{o,1d}}{v_d} = \frac{v_{o,1d}}{-0.5v_d}$$

$$g_{m1} = g_{m2} = \dots = g_{m8} = 0.4 \text{ mA/V}$$

$$r_{o1} = r_{o2} = \dots = r_{o8} = 36 \text{ k}$$

Method 1: Use formula for Cascode Amplifier on Lecture Set 6, slide 14 (which assumes  $g_m r_o \gg 1$ ):

$$A_d = \frac{v_{o,1d}}{-0.5v_d} = -0.5 (g_m r_o)^2$$

$$A_d = -0.5(0.4 \times 10^{-3} \times 36 \times 10^3)^2 = -104$$

Method 2: Use multistage amplifier calculations (similar to Lecture Set 6, slide 14 but not assuming  $g_m r_o \gg 1$ ):

$$R'_L = r_{o5}(1 + g_{m5}r_{o7}) + r_{o7}$$

$$= 36 \times 10^3 \times (1 + 0.4 \times 36) + 36 \times 10^3 = 590 \text{ k}$$

$$A_{vQ3} = v_{o1,d} / v_1 \approx g_{m3}(r_{o3} \parallel R'_L)$$

$$= 0.4 \times 10^{-3} \times (36 \text{ k} \parallel 590 \text{ k}) = 13.6$$

$$R_{i3} = \frac{r_{o3} + R'_L}{1 + g_{m3}r_{o3}} = 40.6 \text{ k}$$

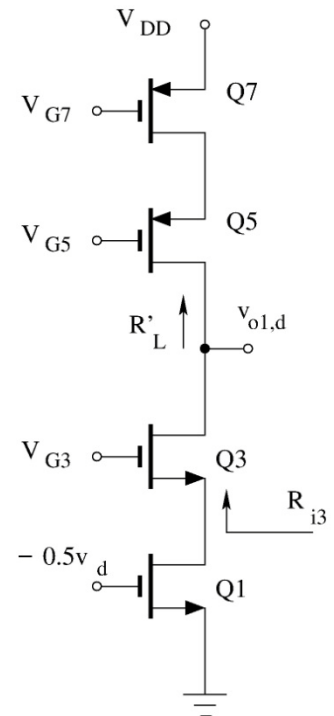
$$A_{vQ1} = v_1 / (-0.5v_d) = -g_{m1}(r_{o1} \parallel R_{i3})$$

$$= -0.4 \times 10^{-3} \times (36 \text{ k} \parallel 40.6 \text{ k}) = -7.63$$

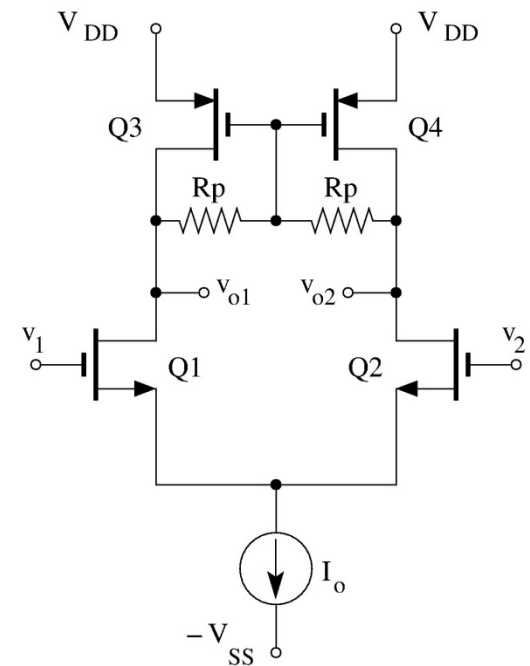
$$A_d = A_{vQ3} A_{vQ1} = -103.8$$

$g_m r_o \gg 1$  is a good approximation

Differential Mode Half Circuit



Exercise 5: Assume Q3 and Q4 as well Q1 and Q2 are identical. Compute the differential gain.



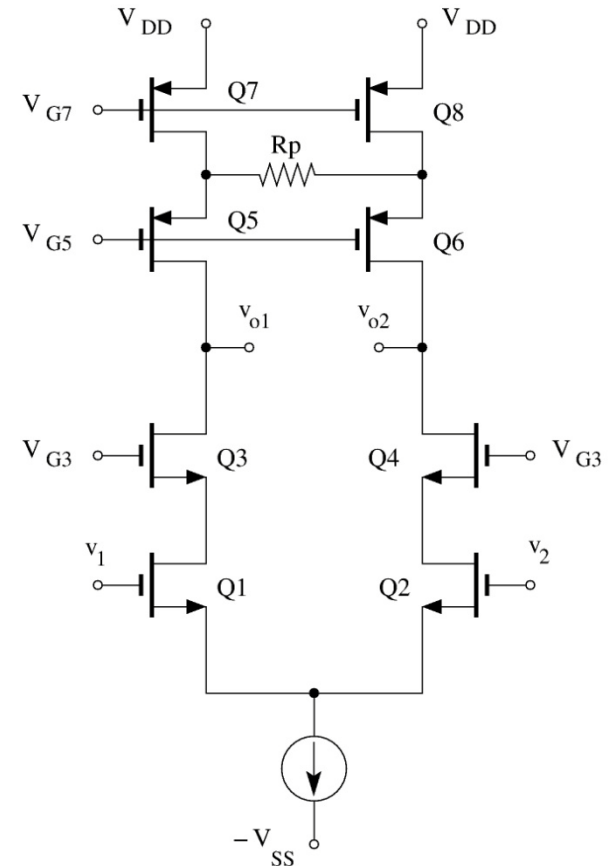
➤ This is a practice problem in constructing half-circuit.



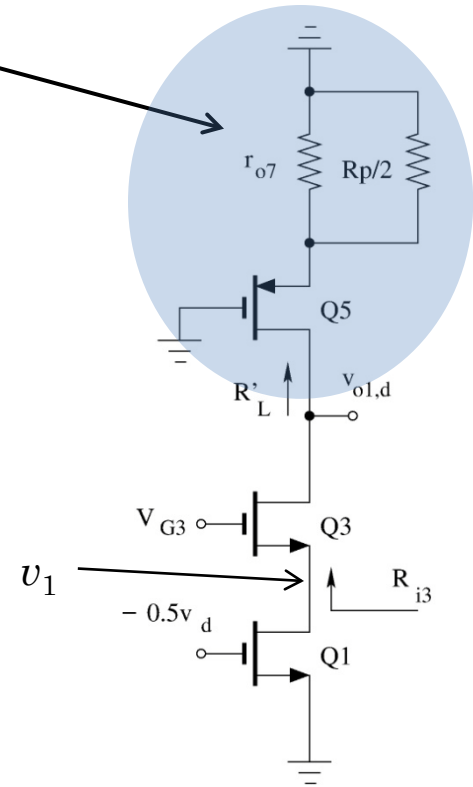
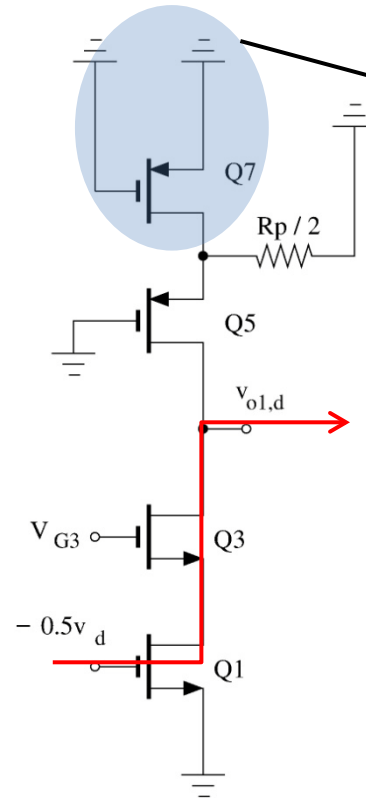
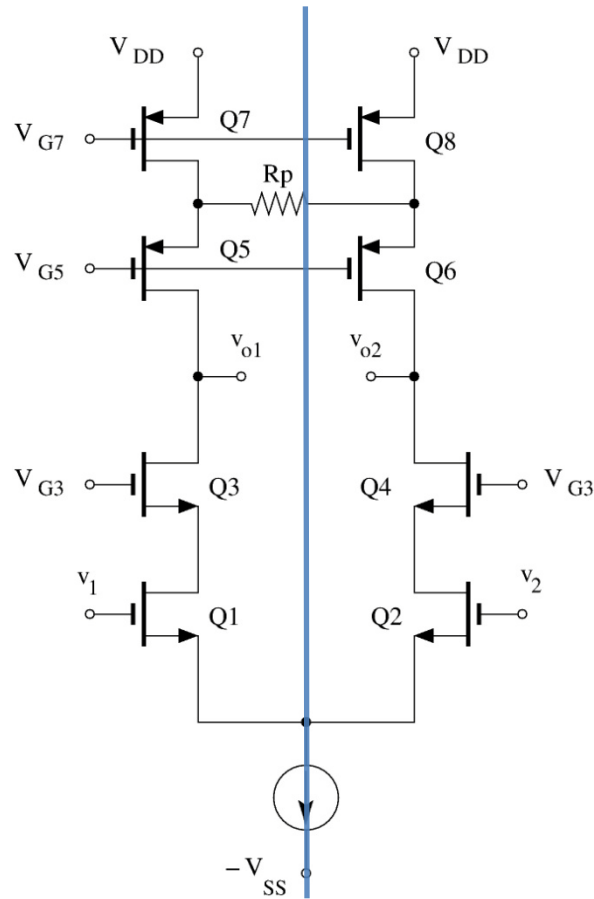


## Exercise 6: Compute the differential gain.

- This problem has it all, half circuit, constructing resistances from elementary R form, and Cascode amplifier.



## Differential-Mode half-circuit



$$R'_L = r_{o5}[1 + g_m(r_{o7} \parallel R_p/2)] + r_{o7} \parallel R_p/2$$

Since  $R_p$  value is not given, we cannot simplify  $R'_L$  expression using  $g_m r_o \gg 1$ .

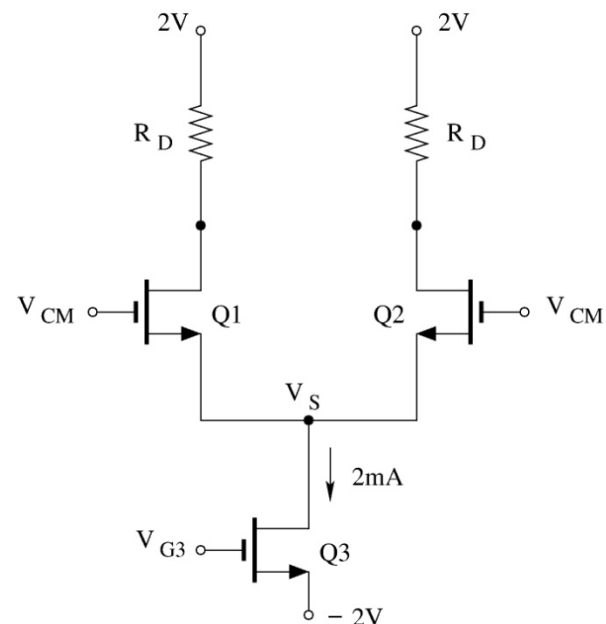
$$A_{vQ3} = v_{o1,d} / v_1 \approx g_{m3}(r_{o3} \parallel R'_L) \quad R_{i3} = \frac{r_{o3} + R'_L}{1 + g_{m3}r_{o3}} \quad A_{vQ1} = v_1 / (-0.5v_d) = g_{m1}(r_{o1} \parallel R_{i3})$$

$$A_d = A_{vQ3}A_{vQ1} = -g_{m1}g_{m3}(r_{o1} \parallel R_{i3})(r_{o3} \parallel R'_L)$$

Exercise 7: What is the input common-mode range in the circuit below. Q1 and Q2 are Identical and  $R_D = 500$ .

Use  $\mu_n C_{ox} (W/L) = 8 \text{ mA/V}^2$ ,  $V_t = 0.5 \text{ V}$  and  $V_{G3} = -1 \text{ V}$ .

- The input common-mode level is the range of DC values that can be applied to the gate of Q1 and Q2 (bias + signal) for which transistors remain in saturation.
  - Basically we are looking for range of DC voltages (i.e., bias) that can be applied to Q1 and Q2 while keeping them in saturation.
  - Then, for any given bias voltage, we can calculate the range of common-mode signals that can be applied to the circuit.
- There are two limits: 1) for Q1 and Q2 remain in saturation, 2) for Q3 to remain in saturation.
- It is straight forward to extend this to active loads.



Assume Q1 and Q2 in Saturation

$$1 \times 10^{-3} = I_{D1} = 0.5 \mu_n C_{ox} (W/L) V_{OV1}^2 = 4 \times 10^{-3} V_{OV1}^2$$

$$V_{OV1} = 0.5 \text{ V}$$

$$V_{GS1} = V_{OV1} + V_t = 1 \text{ V}$$

$$V_{D1} = 2 - R_D I_{D1} = 2 - 0.5 = 1.5 \text{ V}$$

$$V_{OV3} = V_{GS3} - V_t = V_{G3} - V_{S3} - V_t = -1 - (-2) - 0.5 = 0.5 \text{ V}$$

For Q3 in saturation:

$$V_{DS3} \geq V_{OV3}$$

$$V_{D3} - V_{S3} = V_S - (-2) \geq 0.5$$

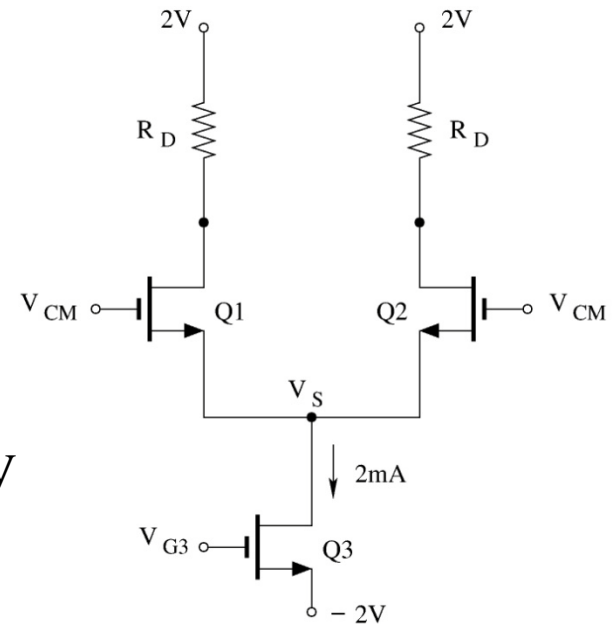
$$V_S \geq -2 + 0.5 = -1.5 \text{ V}$$

For Q1/Q2 in saturation:

$$V_{DS1} \geq V_{OV1}$$

$$V_{D1} - V_{S1} = 1.5 - V_S \geq 0.5$$

$$V_S \leq 1.5 - 0.5 = 1 \text{ V}$$



$$\boxed{-1.5 \leq V_S \leq 1 \text{ V}}$$

$$V_{GS1} = V_{CM} - V_S$$

$$V_S = V_{CM} - 1$$

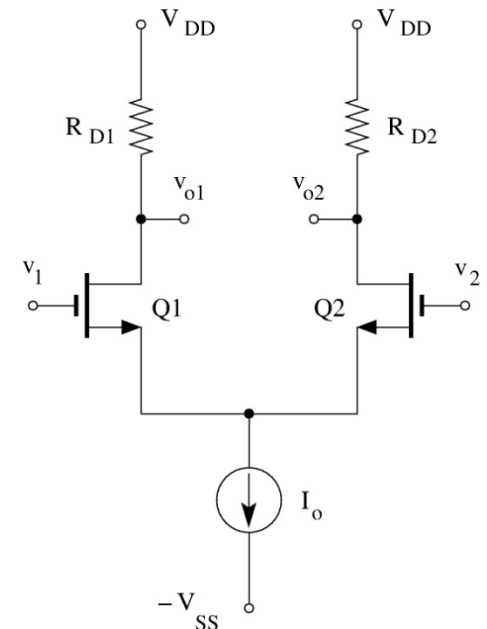
$$-1.5 \leq V_{CM} - 1 \leq 1$$

$$\boxed{-0.5 \leq V_{CM} \leq 2 \text{ V}}$$

Exercise 8: Circuit below is designed to operate at zero bias voltage at the gate of Q1 and Q2 (Q1 & Q2 are matched and  $\lambda = 0$ ). The practical circuit, however includes a slight mis-match of  $R_{D1} = R_D - 0.5 \Delta R_D$  and  $R_{D2} = R_D + 0.5 \Delta R_D$  ( $\Delta R_D / R_D$  is small).

- A) If  $v_1 = v_2 = 0$ , find  $V_o = v_{o2} - v_{o1}$  (Differential DC voltage at the output).  
 B) For what values of  $V_{OS} = v_2 - v_1$ , the DC output voltage will be zero. Ignore channel-length modulation.

- No amplifier chip can be manufactured with perfect symmetry. Mis-matches not only affect CMRR but DC voltages.
- Differential DC voltage at the output and the input offset voltage,  $V_{OS}$ , are important specs. Chips typically include pins for feedback to zero out these voltages.
- Note:  $v_1$  and  $v_2$  are DC values in this problem, they can be viewed either as mis-matched bias (and no signal) and/or signal (but with a matched “zero” bias).



A) If  $v_1 = v_2 = 0$ , find  $V_o = v_{o2} - v_{o1}$  (Differential DC voltage at the output):

$$R_{D1} = R_D - 0.5\Delta R_D \quad \& \quad R_{D2} = R_D + 0.5\Delta R_D$$

Since transistors are matched and  $V_{GS1} = V_{GS2}$  (because  $v_1 = v_2$ ):

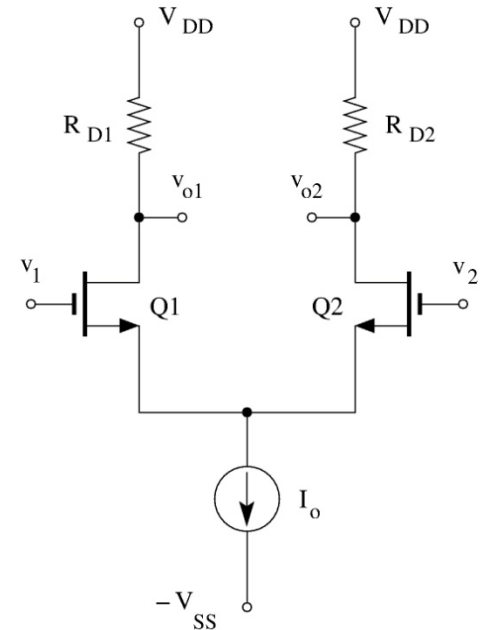
$$I_{D1} = I_{D2} = 0.5I_o$$

$$v_{o1} = V_{D1} = V_{DD} - R_{D1}I_{D1} = V_{DD} - 0.5I_o(R_D - 0.5\Delta R_D)$$

$$v_{o2} = V_{D2} = V_{DD} - R_{D2}I_{D2} = V_{DD} - 0.5I_o(R_D + 0.5\Delta R_D)$$

$$V_o = v_{o2} - v_{o1} = -0.5I_o\Delta R_D$$

Output Offset Voltage



B) For what values of  $V_{OS} = v_2 - v_1$ , the DC output voltage will be zero. Ignore channel-length modulation.

$$V_o = v_{o2} - v_{o1} = -0.5I_o\Delta R_D \quad \text{Output Offset Voltage}$$

$$I_{D1} = I_{D2} = 0.5I_o$$

Method 1: Viewing  $V_{OS}$  as the signal.

The bias voltages remain at zero and  $V_o$  has the above value. A differential signal  $v_d = V_{OS}$  is applied to the circuit leading to a differential output,  $v_{o,d}$ .

We want to find  $V_{OS}$  such that  $v_{o,d} + V_o = 0$

$$v_1 = -0.5V_{OS} \quad \text{and} \quad v_2 = +0.5V_{OS}$$

$$v_{o1,d} = -g_m R_{D1}(-0.5V_{OS}) = +0.5g_m R_{D1}V_{OS}$$

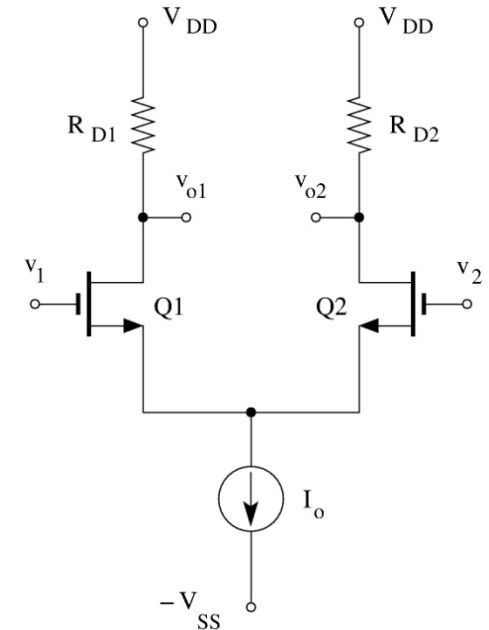
$$v_{o2,d} = -g_m R_{D2}(+0.5V_{OS}) = -0.5g_m R_{D2}V_{OS}$$

$$v_{o,d} = v_{o2,d} - v_{o1,d} = -0.5g_m V_{OS}(R_{D2} + R_{D1})$$

$$v_{o,d} = -0.5g_m V_{OS}[R_D + \Delta R_D + R_D - \Delta R_D]$$

$$v_{o,d} = -g_m V_{OS}R_D = -V_o$$

$$g_m R_D V_{OS} = -0.5I_o \Delta R_D \rightarrow \frac{2I_D}{V_{OV}} R_D V_{OS} = -I_{D1} \Delta R_D \quad \Rightarrow$$



Input Offset Voltage

$$V_{OS} = -0.5V_{OV1} \times \frac{\Delta R_D}{R_D}$$

## Method 2: Viewing $V_{OS}$ as the bias voltage:

For:  $V_{G1} = V_{G2} = 0 \Rightarrow I_{D1} = I_{D2} = 0.5I_o = 0.5\mu_n C_{ox} (W/L) V_{OV}^2$

Find:  $V_{G2} = +0.5V_{os}$  and  $V_{G1} = -0.5V_{os}$  such that  $V_o = v_{o2} - v_{o1} = 0$

$$I_{D1} = 0.5\mu_n C_{ox} (W/L) (V_{OV} - 0.5V_{OS})^2$$

$$\approx 0.5\mu_n C_{ox} (W/L) (V_{OV}^2 - V_{OS}V_{OV})$$

$$= 0.5\mu_n C_{ox} (W/L) V_{OV}^2 (1 - V_{OS}/V_{OV})$$

$$= 0.5I_o (1 - V_{OS}/V_{OV})$$

$$I_{D2} = 0.5\mu_n C_{ox} (W/L) (V_{OV} + 0.5V_{OS})^2 \approx 0.5I_o (1 + V_{OS}/V_{OV})$$

Dropping  $V_{OS}^2$  terms by  
assuming  $V_{OS} \ll V_{OV}$

$$v_{o1} = v_{o2} \rightarrow V_{DD} - R_{D1}I_{D1} = V_{DD} - R_{D2}I_{D2}$$

$$I_{D1}R_{D1} = I_{D2}R_{D2}$$

$$\cancel{0.5I_o} R_D (1 - V_{OS}/V_{OV}) (1 - 0.5\Delta R_D/R_D) = \cancel{0.5I_o} R_D (1 + V_{OS}/V_{OV}) (1 + 0.5\Delta R_D/R_D)$$

$$2(V_{OS}/V_{OV}) + \Delta R_D/R_D = 0$$

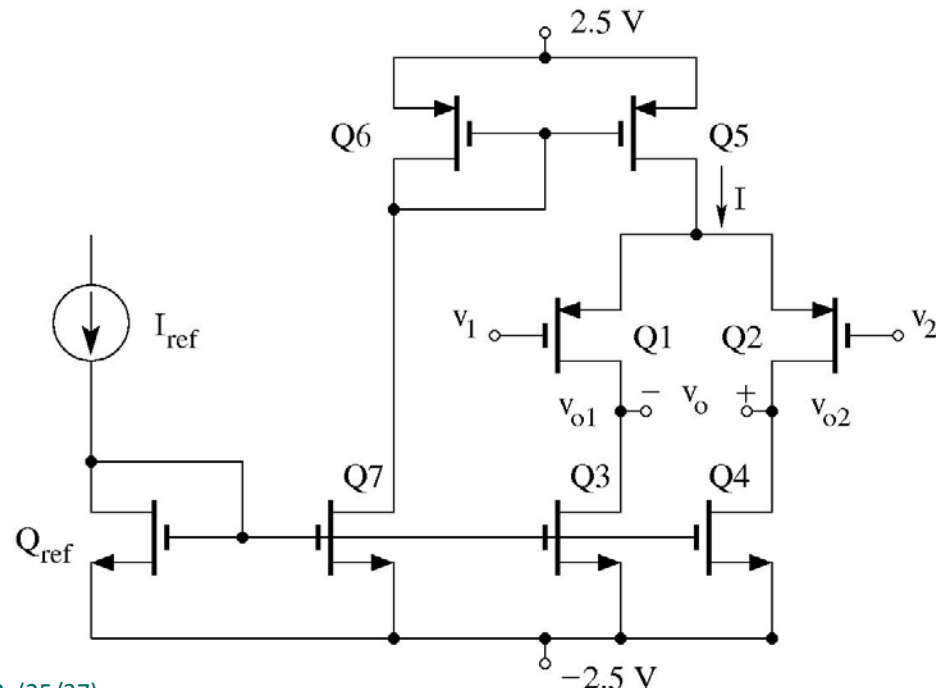


$$V_{OS} = -0.5V_{OV1} \times \frac{\Delta R_D}{R_D}$$



Exercise 9: Consider the circuit below with  $\mu_n C_{ox} = 90 \mu\text{A}/\text{V}^2$ ,  $\mu_p C_{ox} = 30 \mu\text{A}/\text{V}^2$ ,  $V_{tn} = -V_{pn} = 0.7 \text{ V}$  and  $V_{An} = -V_{Ap} = 20 \text{ V}$ . The circuit is to operate such that all transistors operate at  $V_{OV} = 0.5 \text{ V}$ ,  $I_{D1} = I_{D2} = I_{D3} = I_{D4} = I_{ref} = 0.2 \text{ mA}$ , and  $(W/L)_5 = (W/L)_6$ .

- Design the circuit (i.e., find  $(W/L)$  of all transistors).
  - Find the differential gain.
  - Find the common mode response at  $v_{o1}$  (i.e.,  $v_{o1}/v_{CM}$ ).
  - Find the input common-mode range
  - Find the allowable range of the output voltage.
- Ignore channel-length modulation in biasing calculations.





a) Find (W/L of all transistors)

$I_{D1} = I_{D2} = I_{D3} = I_{D4} = I_{ref} = 0.2 \text{ mA}$ ,  
and  $(W/L)_5 = (W/L)_6$ .

Step 1: Compute all currents.

$$I_{D5} = I = I_{D1} + I_{D2} = 0.4 \text{ mA}$$

$$I_{D6} = \frac{(W/L)_6}{(W/L)_5} \times I_{D5} = 0.4 \text{ mA}$$

$$I_{D7} = I_{D6} = 0.4 \text{ mA}$$

Step 2: Compute (W/L)s ( $V_{ov} = 0.5 \text{ V}$ )

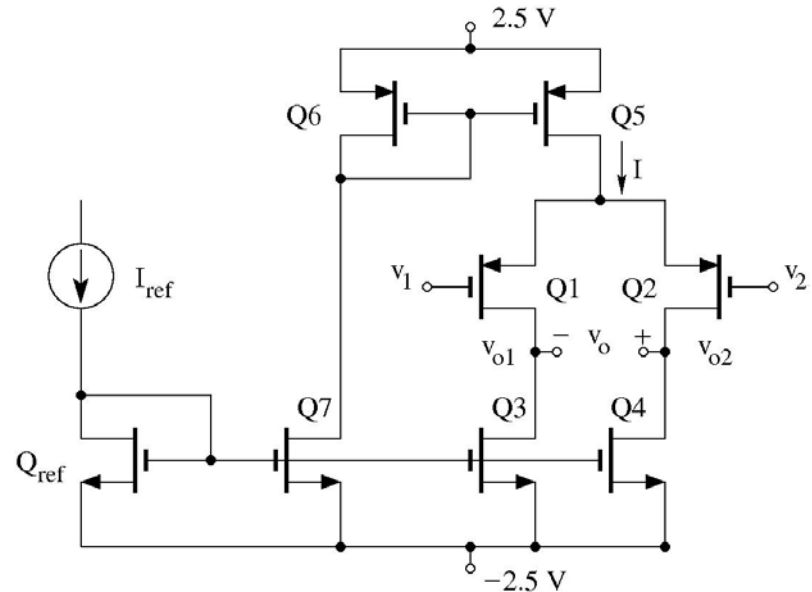
NMOS: Q<sub>ref</sub>, Q<sub>3</sub>, Q<sub>4</sub>, and Q<sub>7</sub>

$$0.2 \times 10^{-3} = I_{ref} = 0.5 \mu_n C_{ox} (W/L)_{ref} V_{OV}^2 = 0.5 \times 90 \times 10^{-6} (W/L)_{ref} (0.5)^2$$

$$(W/L)_{ref} = 17.8$$

$$I_{D3} = I_{D4} = I_{ref} = 0.2 \text{ mA} \Rightarrow (W/L)_3 = (W/L)_4 = (W/L)_{ref} = 17.8$$

$$I_{D7} = 2I_{ref} = 0.4 \text{ mA} \Rightarrow (W/L)_7 = 2(W/L)_{ref} = 35.6$$



PMOS: Q1, Q2, Q5, and Q6

$$0.2 \times 10^{-3} = I_{D1} = 0.5 \mu_p C_{ox} (W / L)_1 V_{OV}^2 = 0.5 \times 30 \times 10^{-6} (W / L)_1 (0.5)^2$$

$$(W / L)_1 = 53.3$$

$$I_{D2} = I_{D1} = 0.2 \text{ mA} \Rightarrow (W/L)_2 = (W/L)_1 = 53.3$$

$$I_{D5} = I_{D6} = 2I_{D1} = 0.4 \text{ mA} \Rightarrow (W/L)_5 = (W/L)_6 = 2(W/L)_1 = 107$$

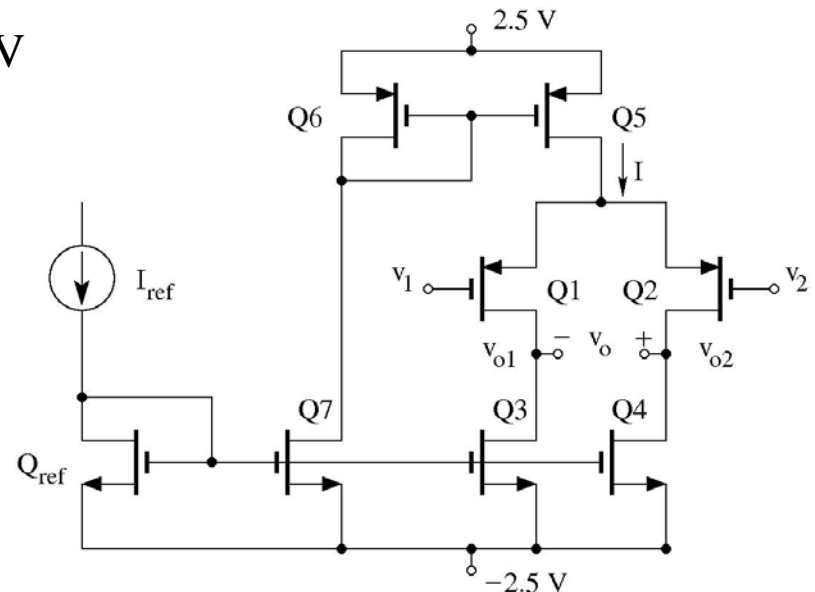
Small signal parameters:

$$g_{m2} = g_{m1} = \frac{2I_{D1}}{V_{OV1}} = \frac{2 \times 0.2 \times 10^{-3}}{0.5} = 8 \times 10^{-4} \text{ A/V}$$

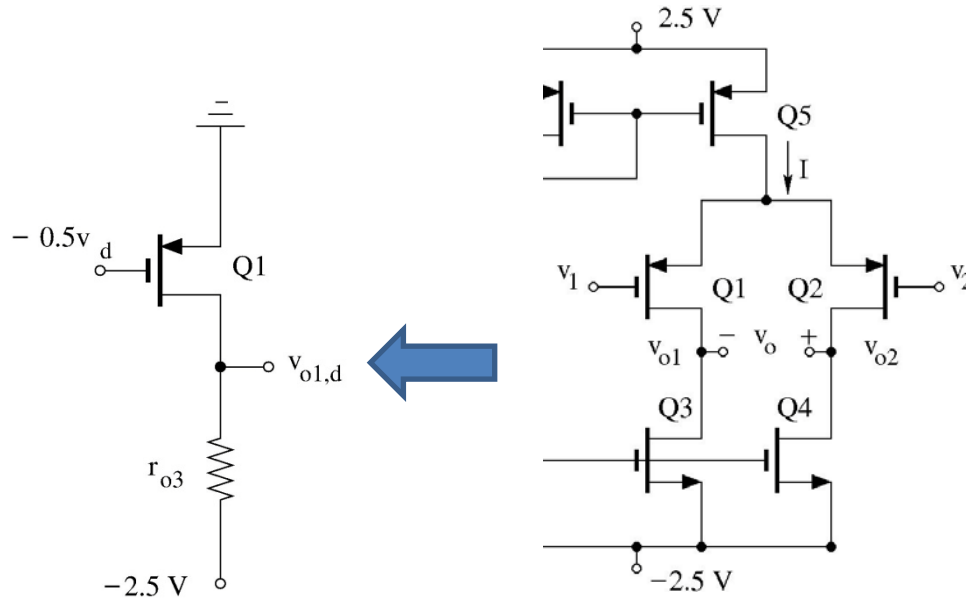
$$r_{o2} = r_{o1} = \frac{V_{A1}}{I_{D1}} = \frac{20}{0.2 \times 10^{-3}} = 100 \text{ k}$$

$$r_{o4} = r_{o3} = \frac{V_{A3}}{I_{D3}} = \frac{20}{0.2 \times 10^{-3}} = 100 \text{ k}$$

$$r_{o5} = \frac{V_{A5}}{I_{D5}} = \frac{20}{0.4 \times 10^{-3}} = 50 \text{ k}$$



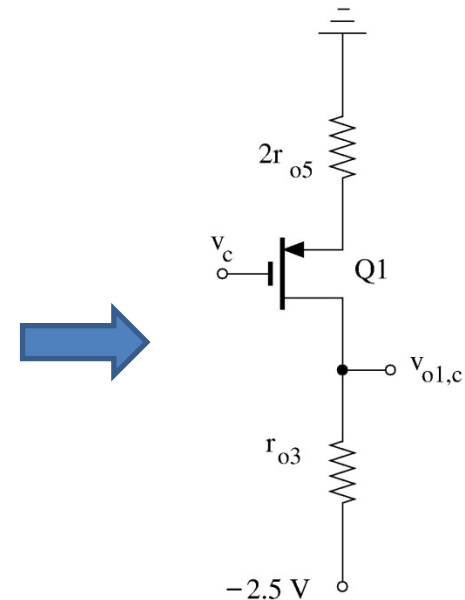
b) Find the differential gain:



$$A_d = \frac{v_{o1,d}}{-0.5v_d} = -g_{m1}(r_{o1} \parallel r_{o3})$$

$$A_d = -8 \times 10^{-4} (100\text{k} \parallel 100\text{k}) = -40$$

c) Find common mode response,  $v_{o1}$ :



$$\frac{v_{o1,c}}{v_c} = -\frac{g_{m1}r_{o3}}{1 + 2g_{m1}r_{o5} + r_{o3}/r_{o1}}$$

$$\frac{v_{o1,c}}{v_c} = -\frac{8 \times 10^{-4} \times 100 \times 10^3}{1 + 2 \times 8 \times 10^{-4} \times 50 \times 10^3 + 1}$$

$$\frac{v_{o2,c}}{v_c} = \frac{v_{o1,c}}{v_c} = -\frac{80}{1 + 80 + 1} = -0.98$$

d) Find input common mode range:

$$V_{S1} - V_{CM} = V_{OV} + |V_{tp}| = 1.2 \text{ V} \Rightarrow V_{S1} = V_{CM} + 1.2$$

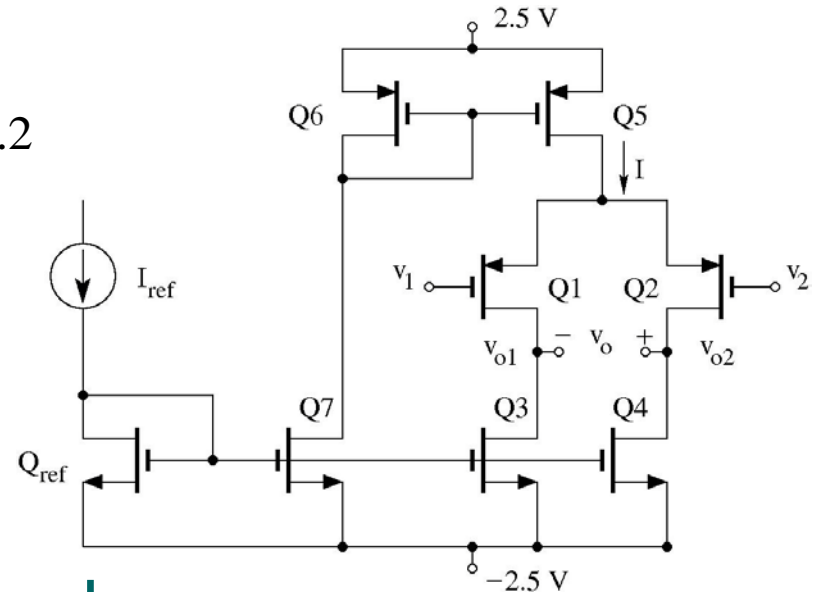
The above equation indicates  $V_{S1}$  changes and tracks  $V_{CM}$  as  $V_{CM}$  changes.  $V_{S1}$  is limited by two criteria below:

1) Q5 in saturation:

$$V_{SD5} = 2.5 - V_{D5} \geq V_{OV} \Rightarrow V_{S1} = V_{D5} \leq 2.5 - 0.5 = 2 \text{ V}$$

2) Q1/Q3 in saturation:

$$\left. \begin{array}{l} V_{SD1} \geq V_{OV1} \\ V_{DS3} \geq V_{OV3} \end{array} \right\} \begin{array}{l} V_{SD1} + V_{DS3} \geq V_{OV} + V_{OV} = 1 \text{ V} \\ V_{S1} - (-2.5) \geq 1 \Rightarrow V_{S1} \geq -1.5 \end{array}$$



$$-1.5 \leq V_{S1} \leq 2.0 \text{ V}$$

$$-1.5 \leq V_{CM} + 1.2 \leq 2.0 \text{ V}$$

$$-2.7 \leq V_{CM} \leq 0.8 \text{ V}$$

Note that the requirement on Q1/Q3 in saturation is usually more restrictive than above as Q1/Q3 do not usually reach saturation together (calculation above represents “the best case”). However, correct solution requires that we include channel-length modulation and calculate the relationship between  $V_{SD1}$  &  $V_{DS3}$  (same arguments apply to part e).

e) Find allowable range of output voltage:

1) Q3 in saturation:

$$V_{DS3} = v_{o1} - (-2.5) \geq V_{OV}$$

$$v_{o1} \geq -2.5 + 0.5 = -2 \text{ V}$$

2) Q1/Q5 in saturation:

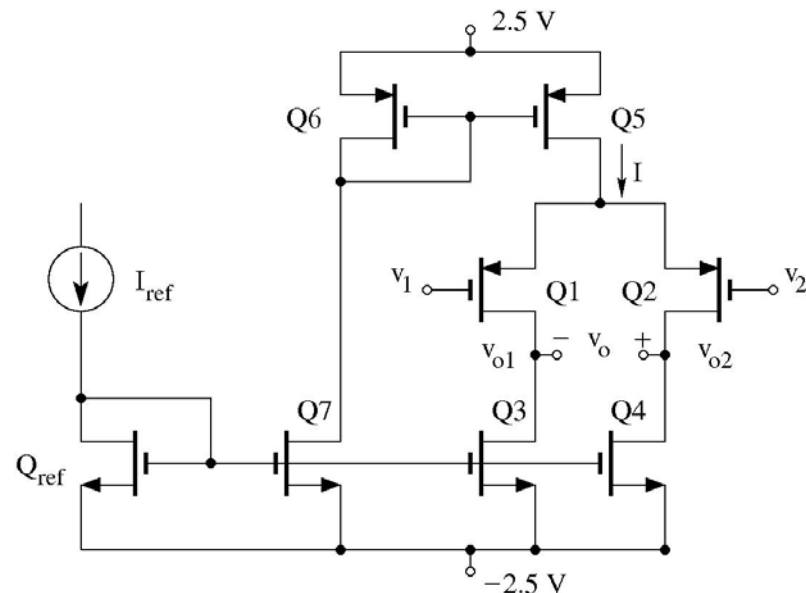
$$V_{SD1} \geq V_{OV}$$

$$V_{SD5} \geq V_{OV}$$

$$V_{SD5} + V_{SD1} \geq 2V_{OV} = 1 \text{ V}$$

$$V_{SD5} + V_{SD1} = 2.5 - v_{o1} \geq 1$$

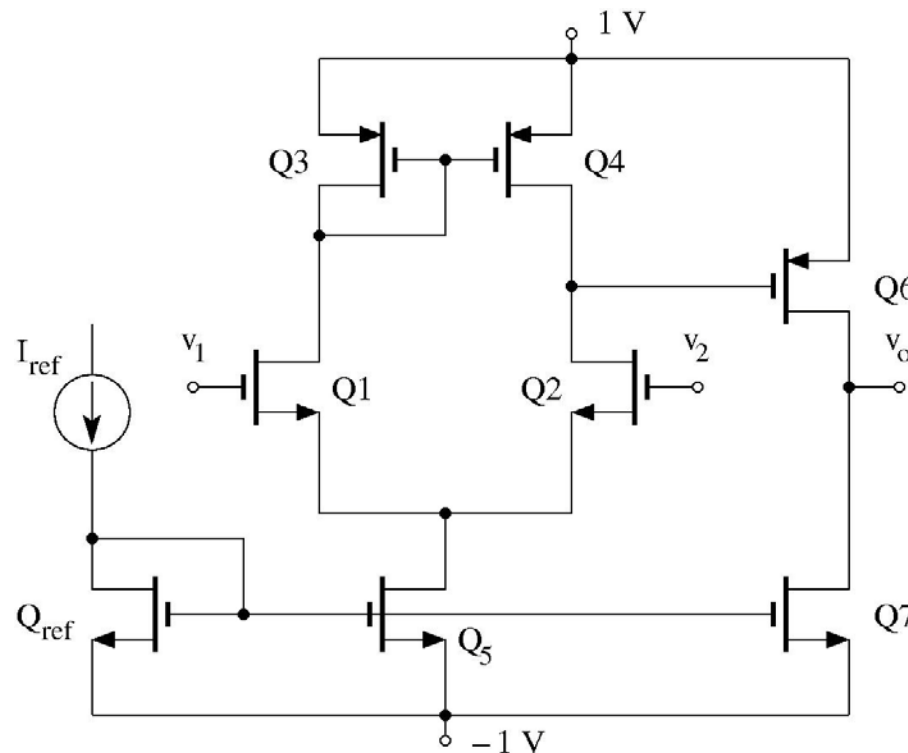
$$v_{o1} \leq 1.5 \text{ V}$$



$$-2.0 \leq v_{o1} \leq 1.5 \text{ V}$$

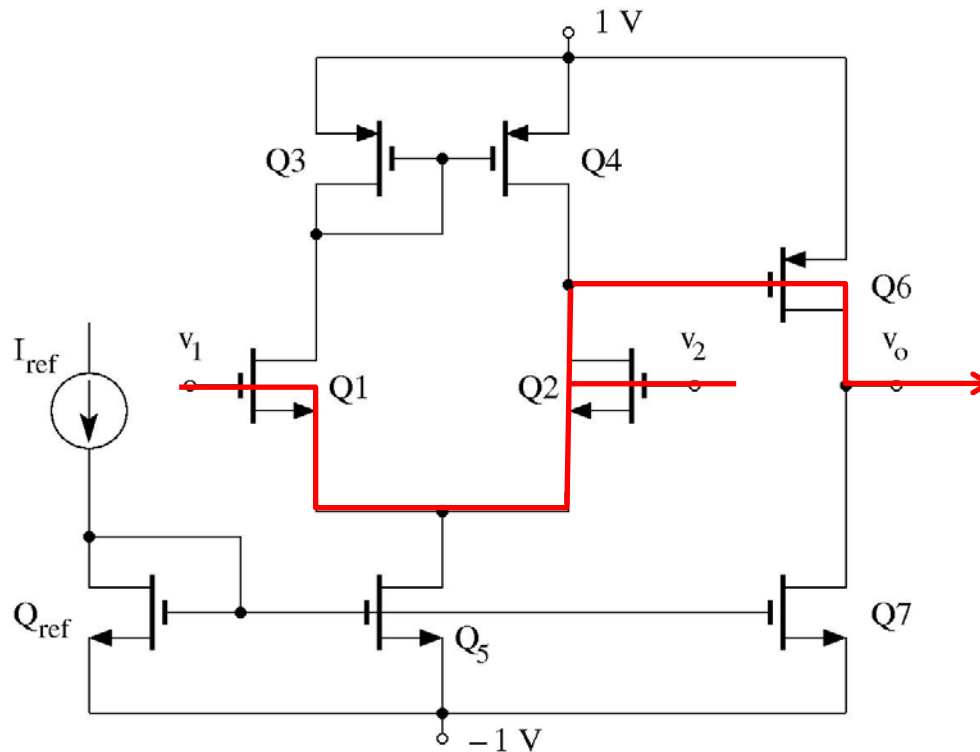
Exercise 10: Consider the circuit below with  $\mu_n C_{ox} = 400 \mu\text{A}/\text{V}^2$ ,  $\mu_p C_{ox} = 100 \mu\text{A}/\text{V}^2$ , and  $V_{tn} = -V_{pn} = 0.4 \text{ V}$ . All transistors operate at  $V_{OV} = 0.2 \text{ V}$  and  $I_{D1} = I_{D2} = I_{D3} = I_{D4} = I_{D6} = I_{ref} = 0.2 \text{ mA}$

- Design the circuit (i.e., find  $(W/L)$  of all transistors)
- Find the input common-mode range
- Find the differential gain ( $\lambda = 0.2 \text{ V}^{-1}$ )





5) Q3/Q4: asymmetric active load for differential amplifier



2) Q6: PMOS CS amplifier (2<sup>nd</sup> stage)

6) Q7: current-source/active load for Q6 CS amplifier

3) Q5: Current-mirror bias for differential

1) Q1 & Q2: NMOS Differential amplifier with single-ended output (1<sup>st</sup> stage)

4) Qref: The reference leg of current mirror for the circuit



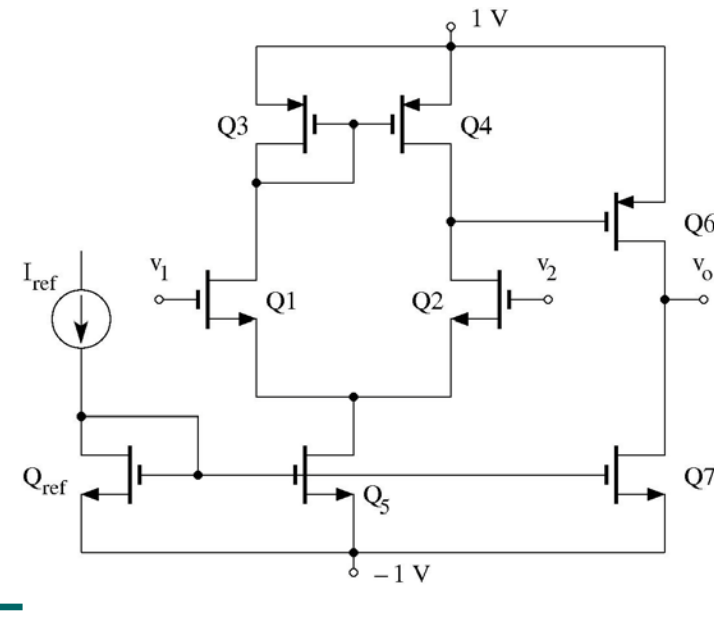
b) Find input common mode range:

$$V_{CM} - V_{S1} = V_{GS1} = V_{OV} + V_{tn} \Rightarrow V_{S1} = V_{CM} - 0.6 \text{ V}$$

Similar to problem 9, we look at  $V_{S1}$  limits:

1) Q5 in saturation:

$$V_{DS5} = V_{D5} - (-1) \geq V_{OV} \Rightarrow V_{S1} = V_{D5} \geq 0.2 - 1 = -0.8 \text{ V}$$



2) Q1/Q3 and Q2/Q4 in saturation (because the circuit is NOT symmetric, we need to consider both cases and choose the most restrictive one).

2A) Q1/Q3

$$V_{SD3} = V_{SG3} = V_{OV3} + |V_{tp}| = 0.6 \text{ V}$$

$$V_{SD3} = 1 - V_{D3} \Rightarrow V_{D3} = 0.4 \text{ V} = V_{D1}$$

$$V_{DS1} = V_{D1} - V_{S1} = 0.4 - V_{S1} \geq V_{OV} = 0.2 \text{ V}$$

$$V_{S1} \leq 0.2 \text{ V}$$

2B) Q2/Q4

$$V_{SG6} = V_{OV6} + |V_{tp}| = 0.6 \text{ V}$$

$$V_{SG6} = 1 - V_{G6} \Rightarrow V_{G6} = 0.4 \text{ V} = V_{D2}$$

$$V_{DS2} = V_{D2} - V_{S2} = 0.4 - V_{S1} \geq V_{OV} = 0.2 \text{ V}$$

$$V_{S1} \leq 0.2 \text{ V}$$

$$-0.8 \leq V_{S1} \leq 0.2 \text{ V} \Rightarrow -0.8 \leq V_{CM} - 0.6 \leq 0.2 \text{ V} \Rightarrow$$

$$-0.2 \leq V_{CM} \leq 0.6 \text{ V}$$

c) Find the differential gain ( $\lambda = 0.2 \text{ V}^{-1}$ ):

$$I_{D1} = I_{D2} = I_{D3} = I_{D4} = I_{D6} = 0.2 \text{ mA}$$

$$I_{D5} = I_{D1} + I_{D2} = 0.4 \text{ mA}$$

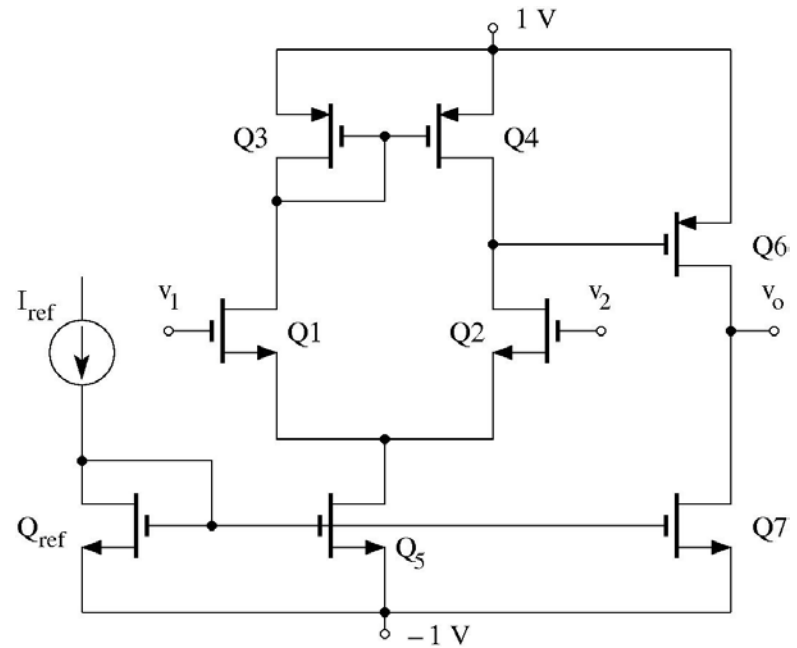
$$I_{D6} = I_{D7} = 0.2 \text{ mA}$$

$$g_{m2} = g_{m1} = \frac{2I_{D1}}{V_{OV1}} = \frac{2 \times 0.2 \times 10^{-3}}{0.2} = 2 \times 10^{-3} \text{ A/V}$$

$$r_{o2} = r_{o1} = \frac{1}{\lambda I_{D1}} = \frac{1}{0.2 \times 0.2 \times 10^{-3}} = 25 \text{ k}$$

$$r_{o4} = r_{o3} = \frac{1}{\lambda I_{D3}} = \frac{1}{0.2 \times 0.2 \times 10^{-3}} = 25 \text{ k}$$

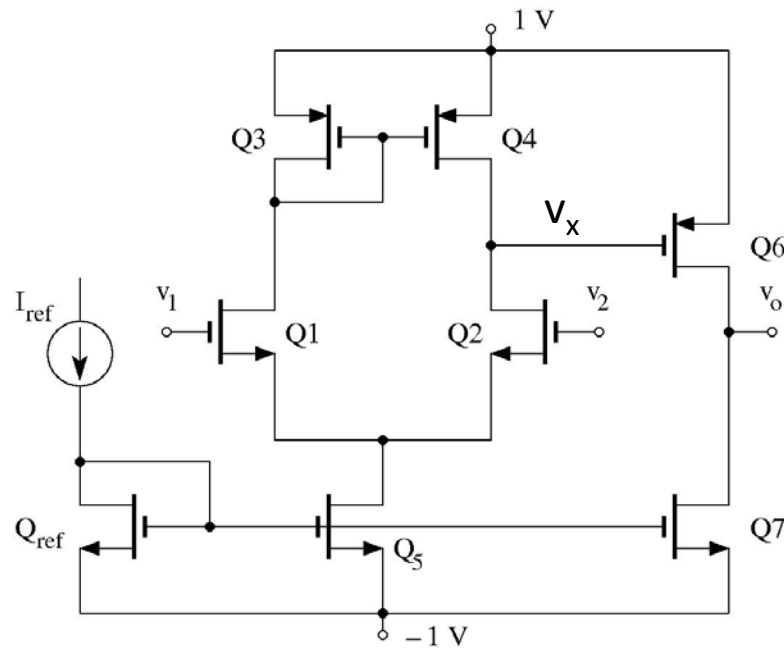
$$r_{o5} = \frac{1}{\lambda I_{D5}} = \frac{1}{0.2 \times 0.4 \times 10^{-3}} = 12.5 \text{ k}$$



$$g_{m6} = \frac{2I_{D6}}{V_{OV6}} = \frac{2 \times 0.2 \times 10^{-3}}{0.2} = 2 \times 10^{-3} \text{ A/V}$$

$$r_{o6} = \frac{1}{\lambda I_{D6}} = \frac{1}{0.2 \times 0.2 \times 10^{-3}} = 25 \text{ k}$$

$$r_{o7} = \frac{1}{\lambda I_{D7}} = \frac{1}{0.2 \times 0.2 \times 10^{-3}} = 25 \text{ k}$$



Q1 & Q2: NMOS Differential amplifier with single-ended output (1<sup>st</sup> stage)

Q6: PMOS CS amplifier (2<sup>nd</sup> stage)

$$\frac{v_x}{v_d} = -g_{m1}(r_{o1} \parallel r_{o3} \parallel R_L)$$

$$\frac{v_x}{v_d} = -2 \times 10^{-3}(25\text{k} \parallel 25\text{k}) = 25$$

$$\frac{v_o}{v_x} = -g_{m6}(r_{o6} \parallel r_{o7})$$

$$\frac{v_o}{v_x} = -2 \times 10^{-3}(25\text{k} \parallel 25\text{k}) = 25$$

$$R_{i2} = \infty$$

$$A_d = \frac{v_o}{v_d} = \frac{v_o}{v_x} \times \frac{v_x}{v_d} = 25 \times 25 = 625$$