Triangle-to-Sine Wave Conversion with MOS Technology

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Abstract—**This paper describes MOS circuit design techniques for nonlinear analog circuits that perform a triangle-to-sine wave conversion. These techniques may also be applied to synthesizing other functions. Design techniques for compensating the conversion for variations in temperature, processing, and triangle wave amplitude are also presented. Results from simulation and a monolithic circuit fabrication are reported which show that a sinusoidal approximation with a total harmonic content of 0.2 percent at 1 kHz is practical. The test circuit is powered from ±5-V supplies and displays a bandwidth of 1.1 MHz.**

I. INTRODUCTION

TRIANGLE-TO-SINE WAVE converters have been used for many years in function generators, phase-locked loops, and other types of communication circuits. The usefulness of this circuit function stems from the ease with which precision triangle waves can be generated over a wide range of frequencies by relaxation oscillators. The addition of a triangle-to-sine wave converter to such an oscillator allows a sinusoidal voltage to be realized, which is desirable in many systems. There are many practical difficulties in the design of an oscillator that directly generates a sine wave output over a wide frequency range. Triangle wave oscillators are easily tuned by a single electronic control. The amplitude of such an oscillator is controlled by a well-defined fast-limiting nonlinearity, and is largely independent of frequency. In practice, the generation of frequency-variable sine waves by feeding a triangle wave through a triangle-to-sine wave converter, as shown in Fig. 1, can lead to sine waves with less distortion than can be easily generated by a direct sine wave oscillator.

Resistor and diode circuits performing piecewise linear approximations to the ideal sinusoidal transfer characteristic have long been successfully used in discrete realizations of Fig. 1. In monolithic form the exponential transfer characteristic of the bipolar junction transistor has been exploited to approximate the sine function by continuous synthesis [1],[2]. The increasing use of MOS technology to perform analog functions has created demands for circuit functions such as triangle-to-sine wave conversion to that implemented in MOS technology. This problem is addressed in this paper.

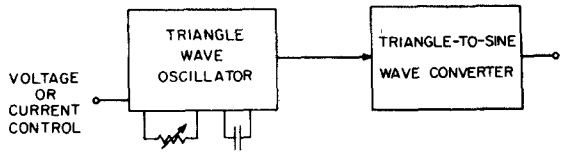

Fig. 1. Generation of frequency-variable sine waves.

Before discussing circuit design principles, it is useful to examine more closely the inherent limits to spectral purity of systems represented by Fig. 1. Even if the triangle-to-sine wave converter block could be designed to have an exact sinusoidal transfer function, the resultant output can include harmonic distortion if the triangle wave amplitude is not controlled precisely.

Consider the ideal ±90° transfer function of Fig. 2. As an example, this transfer function takes the form of a nonlinear voltage gain. That is, both input and output variables are voltages, related by

$$\text{output volts} = \begin{cases} -1 & \text{input volts} < -1 \\ \sin\left\{\frac{\pi}{2} \cdot \text{input volts}\right\} & -1 < \text{input volts} < 1 \\ +1 & 1 < \text{input volts.} \end{cases}$$

Accurate triangle waves of exactly 1-V (2-V·s peak-to-peak) amplitude, fed through this transfer function, would produce a spectrally pure sinusoid. However, significant harmonic content will be found in the output with even slight errors in the triangle wave amplitude.

A definition of the total harmonic distortion can be made in the usual way, that is

$$THD = \sqrt{\sum_n (HD_n)^2} \tag{1}$$

where the harmonic distortion terms are

$$HD_n = \frac{\text{amplitude of the } n\text{th harmonic}}{\text{amplitude of the fundamental}}$$

and the fundamental frequency is that of the incoming triangle wave. Fig. 3 plots this theoretical total harmonic distortion, up through the ninth harmonic, versus the amplitude of the triangle wave fed through the transfer function of Fig. 2. The case of an ideal transfer function that

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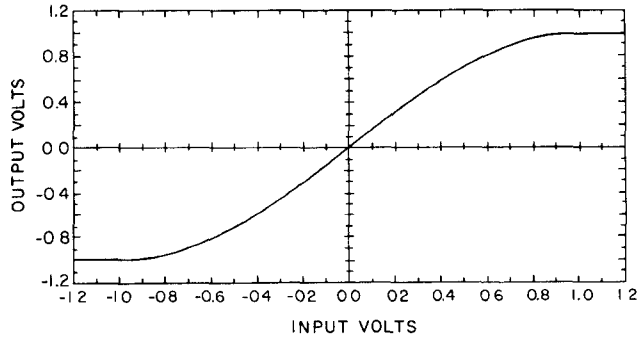


Fig. 2. Ideal triangle-to-sine transfer curve for $\pm 90°$ input range.

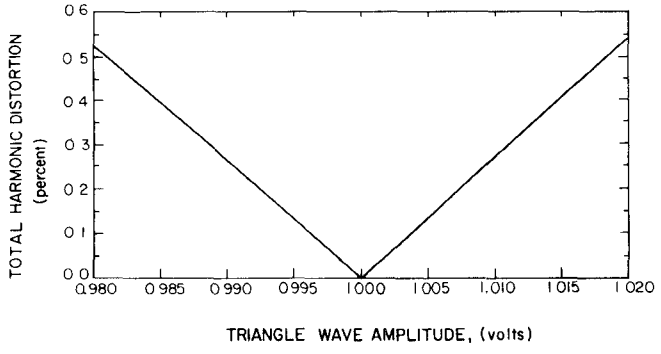


Fig. 3. THD of ideal converter based on transfer curve of Fig. 2 versus input triangle wave amplitude.

encompasses a wider angular input range, such as that of Fig. 4, yields a distortion characteristic almost identical to Fig. 3. A practical implementation of such a transfer function is described in [2].

Note that these distortions of the ideal sine wave output result from the triangle wave input failing to sweep the sinusoidal transfer function perfectly over a $\pm 90°$ range. The distorted output could be described as being either "clipped" or "pointed." Any deviation in the shape of the active region (between -1 and 1 V) of a practical approximation for Fig. 2 from its ideal sinusoidal contour would, in general, be responsible for yet higher harmonic content in the output than the theoretical limit of Fig. 3. The conclusion to be drawn here is that the design effort of a practical triangle-to-sine wave conversion system must be shared between both an accurate sinusoidal transfer function synthesis and a method of ensuring the correspondence of the active limits of that transfer function with the input triangle wave amplitude.

II. Synthesis Principles

The basic building block circuit for the synthesis technique described in this paper is the MOS differential pair, pictured in Fig. 5. For the purpose of analysis here, each MOS device is assumed to be in saturation and to obey a square-law model, that is

$$I_D = \begin{cases} 0 & V_{GS} \leq V_T \\ k(V_{GS} - V_T)^2 & V_{GS} > V_T \end{cases} \tag{2}$$

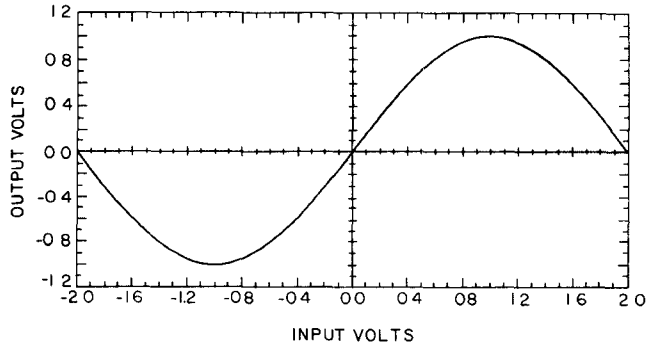


Fig. 4. Ideal triangle-to-sine transfer curve for $\pm 180°$ input range.

where

I_D	drain current,
V_T	threshold voltage for strong inversion,
V_{GS}	gate-to-source voltage,
k	$\frac{\mu_n C_{ox}}{2}(W/L)$,
μ_n	electron channel mobility,
C_{ox}	oxide capacitance per unit area,
W	effective channel width,
L	effective channel length.

A four-quadrant MOS analog multiplier was recently designed using this model, and fairly accurate agreement between designed performance and experimental results was shown [3]. Those results and the results of this investigation demonstrate that nonlinear MOS analog circuits capable of moderate precision can be designed without the need of more complex device modeling.

From (2), the nonlinear differential transconductance of the MOSFET pair in Fig. 5 can easily be derived. It is assumed that the value of the parameter k is identical for both devices. Defining

$$V_{\text{IN}} = V_{G1} - V_{G2}$$

and

$$I_{\text{OUT}} = I_{D1} - I_{D2}$$

then

$$I_{\text{OUT}} = \begin{cases} -I & V_{\text{IN}} < -\sqrt{\frac{I}{k}} \\ V_{\text{IN}}\sqrt{2kI - k^2V_{\text{IN}}^2} & -\sqrt{\frac{I}{k}} < V_{\text{IN}} < \sqrt{\frac{I}{k}} \\ +I & \sqrt{\frac{I}{k}} < V_{\text{IN}}. \end{cases} \tag{3}$$

This transfer function is graphed in Fig. 6.

Note that with first-order modeling, excluding subthreshold conduction, the bias current I can, with sufficiently high differential gate voltages, be diverted completely through each of the MOSFET's. This property is not changed significantly when subthreshold conduction is

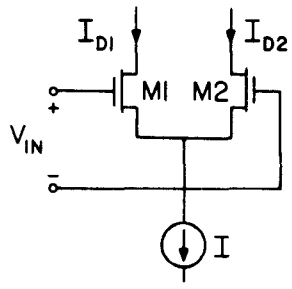


Fig. 5. MOS differential pair.

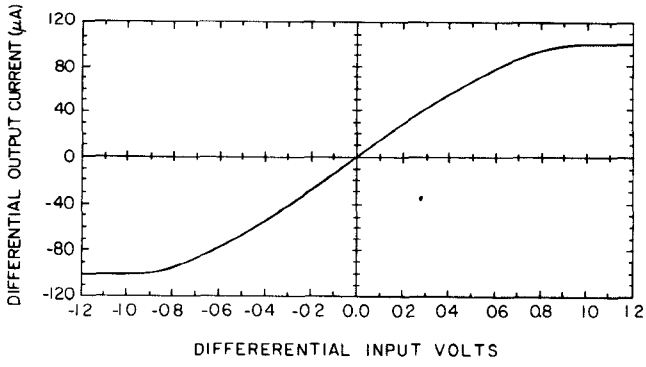


Fig. 6. Transfer characteristic of single MOS differential pair of Fig 5 with $I = 100\ \mu A$, $V_{SW} = 1$ V.

included in the MOSFET models. The differential input voltage required to completely switch the pair is defined as $\pm V_{SW}$, where $V_{SW} = \sqrt{I/k}$, and corresponds to $V_{GS} = V_T$ for one of the devices. Beyond this input voltage the differential output current saturates. The expression for differential output current can be rewritten with the differential input voltage normalized to V_{SW}, and is

$$I_{\text{OUT}} = \begin{cases} -I & V_{IN} < -V_{SW} \\ \left(\dfrac{V_{\text{IN}}}{V_{SW}} \cdot I\right)\left(2 - \left(\dfrac{V_{\text{IN}}}{V_{SW}}\right)^2\right)^{1/2} & -V_{SW} < V_{IN} < V_{SW} \\ +I & V_{SW} < V_{IN}. \end{cases} \tag{4}$$

Note that specifying the bias current I and the bilateral switching voltage V_{SW} of a differential pair is sufficient to completely characterize its nonlinear transconductance and to determine the necessary value of the parameter k.

Suppose that n differential pairs are connected with common inputs and outputs as in Fig. 7. Although the value of k is identical for both devices forming each pair, the value of k for each pair is arbitrary. The output drain leads of any pair may be cross connected (M_{1i} to node Y, M_{2i} to node X), as shown for pair i in the figure. In an expression for the total differential output current $I_X - I_Y$, the phase of each differential pair output connection can be absorbed into the sign of the bias currents. Although the physical values of the bias currents I_i remain positive, values of I_i expressed as negative correspond to cross-connected pairs, and

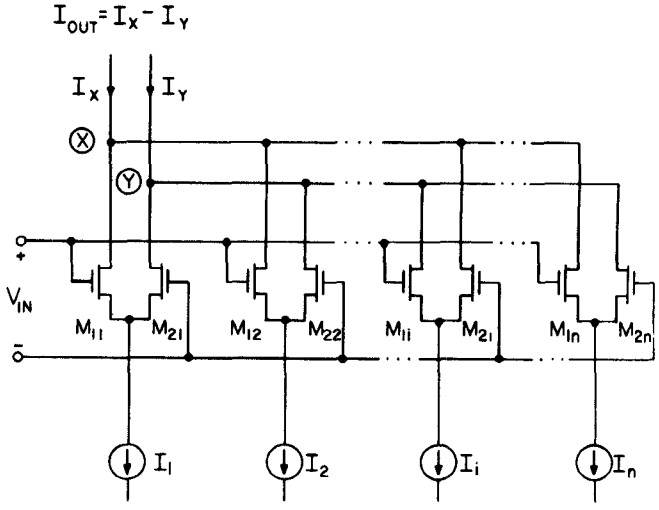


Fig. 7. Circuit with n differential pairs connected with common inputs and outputs.

$$I_{\text{OUT}} = \sum_{i=1}^{n} I_{\text{OUT}\,i} \tag{5}$$

where $I_{\text{OUT}\,i}$ is given by (4) for differential pair number i.

When designing a nonlinear function approximation, we have in mind an ideal desired odd transfer function, in this case a transconductance, which can be written as

$$I_{\text{OUT}\,des} = I_0 f\left\{\frac{V_{\text{IN}}}{V_0}\right\} \tag{6}$$

where

f an arbitrary odd function,

and

I_0, V_0 normalization constants.

For the matter at hand, triangle-to-sine wave conversion

$$I_{\text{OUT}\,des} = I_0 \sin\left\{\frac{\pi}{2}\,\frac{V_{\text{IN}}}{V_{PK}}\right\} \tag{7}$$

where

V_{PK} = peak value of the input triangle wave.

The process of design chosen here consists of specifying the parameters I_i and V_{SW_i}, for $i = 1, 2, \cdots, n$ in (5) so that (5) is a reasonable approximation to (7). Note that since (4) is odd with respect to V_{IN}, only odd functions may be approximated with this circuit topology.

At this point, we must choose a strategy for specifying the independent parameters in (5). One approach to a fairly precise approximation is to equate the first three nonzero coefficients in Taylor series expansions of (5) and (7). All differential pairs would be in their active region, that is $V_{SW_i} \geq V_{PK}$ for $i = 1, \cdots, n$. For each differential

pair

$$I_{\mathrm{OUT}\iota} = \left(\frac{V_{\mathrm{IN}}}{V_{SW\iota}} \cdot I_\iota\right)\left(2 - \left(\frac{V_{\mathrm{IN}}}{V_{SW\iota}}\right)^2\right)^{1/2}$$
$$\approx \beta_{1\iota} V_{\mathrm{IN}} + \beta_{3\iota} V_{\mathrm{IN}}^3 + \beta_{5\iota} V_{\mathrm{IN}}^5$$

where

$$\beta_{1\iota} = \sqrt{2}\,\frac{I_\iota}{V_{SW\iota}}$$

$$\beta_{3\iota} = -\frac{\sqrt{2}\, I_\iota}{4\, V_{SW\iota}^3}$$

and

$$\beta_{5\iota} = -\frac{\sqrt{2}\, I_\iota}{32\, V_{SW\iota}^5}.$$

Then $I_{\mathrm{OUT}} = \sum_{\iota=1}^{n} I_{\mathrm{OUT}\iota}$ is to be equated to

$$I_{\mathrm{OUT}des} = I_0 \sin\left(\frac{\pi\, V_{\mathrm{IN}}}{2\, V_{PK}}\right)$$
$$\approx \alpha_1 V_{\mathrm{IN}} + \alpha_3 V_{\mathrm{IN}}^3 + \alpha_5 V_{\mathrm{IN}}^5$$

where

$$\alpha_1 = I_0\left(\frac{\pi}{2V_{PK}}\right)$$

$$\alpha_3 = -\frac{I_0}{6}\left(\frac{\pi}{2V_{\mathrm{IN}}}\right)^3$$

and

$$\alpha_5 = -\frac{I_0}{120}\left(\frac{\pi}{2V_{PK}}\right)^5.$$

Choosing $n = 3$ gives six parameters to specify. Since there are but three equations to satisfy, one for each of the coefficients, this leaves three free parameters to adjust for an optimum solution. For example, the values of $V_{SW\iota}$ can be adjusted to find a preferred solution in terms of the bias currents I_ι.

Particular solutions may be ranked by merit in terms of both the spread required between the values of k for all the pairs, and how efficiently the total common-mode output current is used. Minimizing the k ratios between devices is important to keep total chip area small. A measure of common-mode current efficiency can be defined as

$$\eta = \frac{I_{\mathrm{OUT\,max}}}{\sum_{\iota=1}^{n} |I_\iota|} \tag{8}$$

where $I_{\mathrm{OUT\,max}}$ is the maximum differential output current used to approximate the desired function. $I_{\mathrm{OUT\,max}}$ would equal I_0 in the case of (7).

As an example, if $n = 1$ and a single differential pair transfer function of Fig. 6 were used to approximate Fig. 2, and if I_1 were equal to I_0 of (7), then η would equal 1. There will be more said regarding this case later.

In the case of multiple differential pairs ($n > 1$), η will be less than unity if the solution requires any of the currents I_ι to be negative, that is, any of the differential pairs to be cross connected. Reversing the phase of any of the outputs decreases $I_{\mathrm{OUT\,max}}$ while increasing the total common-mode drain currents of the MOSFET's. If η were too small, circuit design of additional complexity may be required to recover the small differential output signal from its large common mode vehicle.

When the strategy of equating Taylor series coefficients is applied to approximating the desired sine function of (7), a solution cannot be optimized to have a large enough value of η to be practical. The resulting low η values (well under 0.1) indicate that simultaneous solution requires near complete cancellation of the large series terms associated with each of the three differential pairs. This casts serious doubt on the validity of neglecting the resultant error from series terms beyond the first three nonzero terms. It also may require more precision from the MOSFET transfer characteristic model than is afforded by the first-order expression of (2).

However, when this circuit topology is used to approximate other functions, an adaptation of this Taylor series strategy may well be effective, particularly when the approximation need only be accurate over a limited function domain. For example, some application may demand an analog approximation to a portion of a logarithmic function for positive values of V_{IN}. Of course, circuits of this type would generate an odd-extension of this function for negative V_{IN} values.

Another example of a desirable function is a linear relation. This approximation would be useful as a part of frequency compensated operational amplifiers and continuous time analog filters. Often the stability or proper frequency domain characteristics of these circuits depend on an approximately constant small signal gain. A linear function synthesizer can widen the input voltage range over which the gain is constant to a much greater range than can be obtained with a simple differential pair.

Another possible strategy for designing the transfer characteristics of the n differential pairs of Fig. 7 can be extended from the design of diode shaping piecewise linear approximators. If the various $V_{SW\iota}$ values are distributed throughout the range of the input voltage, then the value of V_{IN} will determine which of the differential pairs are in their active region and which are saturated. A saturated pair contributes a constant value to the differential output current, namely plus or minus the value of the bias current. This allows the variation of output current between the values of the set of $V_{SW\iota}$ to be specified independent of the active characteristics of those pairs that are saturated. With this freedom, we can force the functional value of the output current to equal the desired relation at n discrete values of V_{IN}. It is convenient to establish this equality at the points $V_{\mathrm{IN}} = V_{SWj}$, $j = 1, \cdots, n$.

TABLE I
MULTIPLE DIFFERENTIAL PAIR WAVEFORM CONVERTER DESIGN SOLUTIONS

n	Equally Distributed V_{SW_i} Values (Initial Solution)		Optimized V_{SW_i} Values (Least Squared Deviation)	
1	$\frac{V_{SW1}}{V_{PK}} = 1$	$\frac{I_1}{I_0} = 1$	$\frac{V_{SW1}}{V_{PK}} = 0.9127$	$\frac{I_1}{I_0} = 0.9906$
	THD = 2.7%	$\eta = 1.00$	THD = 0.88%	$\eta = 1.00$
2	$\frac{V_{SW1}}{V_{PK}} = 0.5$	$\frac{I_1}{I_0} = 0.1349$	$\frac{V_{SW1}}{V_{PK}} = 0.5098$	$\frac{I_1}{I_0} = 0.06994$
	$\frac{V_{SW2}}{V_{PK}} = 1.0$	$\frac{I_2}{I_0} = 0.8651$	$\frac{V_{SW2}}{V_{PK}} = 0.9560$	$\frac{I_2}{I_0} = 0.9277$
	THD = 0.97%	$\eta = 1.00$	THD = 0.18%	$\eta = 1.00$
4	$\frac{V_{SW1}}{V_{PK}} = 0.25$	$\frac{I_1}{I_0} = 0.008416$	$\frac{V_{SW1}}{V_{PK}} = 0.2511$	$\frac{I_1}{I_0} = 0.004515$
	$\frac{V_{SW2}}{V_{PK}} = 0.50$	$\frac{I_2}{I_0} = 0.01568$	$\frac{V_{SW2}}{V_{PK}} = 0.5074$	$\frac{I_2}{I_0} = 0.03841$
	$\frac{V_{SW3}}{V_{PK}} = 0.75$	$\frac{I_3}{I_0} = 0.2206$	$\frac{V_{SW3}}{V_{PK}} = 0.7080$	$\frac{I_3}{I_0} = 0.09858$
	$\frac{V_{SW4}}{V_{PK}} = 1.00$	$\frac{I_4}{I_0} = 0.7553$	$\frac{V_{SW4}}{V_{PK}} = 0.9766$	$\frac{I_4}{I_0} = 0.8578$
	THD = 0.27%	$\eta = 1.00$	THD = 0.13%	$\eta = 1.00$

More precisely, assume that the pairs are numbered in increasing order of V_{SWi}, that is

$$V_{SW1} < V_{SW2} < \cdots V_{SWn}.$$

Then for the case of sine function approximation, the set of n equations

$$\sin\left(\frac{\pi}{2}\frac{V_{SWj}}{V_{PK}}\right) = \sum_{i=1}^{n}\left(\frac{I_i}{I_0}\right)\cdot\begin{cases}\left(\frac{V_{SWj}}{V_{SWi}}\right)\left(2-\left(\frac{V_{SWj}}{V_{SWi}}\right)^2\right)^{1/2} & V_{SWj} < V_{SWi} \\ 1 & V_{SWj} \geq V_{SWi}\end{cases}$$

$$\text{for } j = 1, \cdots, n \quad (9)$$

can be solved for the values of (I_i/I_0) given a set of values for V_{SWi}. These values of V_{SWi} can then be adjusted to optimize the functional fit between these anchor points.

This optimization was done numerically using a multidimensional version of the Newton–Raphson method, and minimizing the least-squared deviation between modeled and desired output currents. An initial starting solution was obtained by setting the V_{SWi} values to be equally distributed throughout the input voltage range, that is,

$$V_{SWi} = \frac{i}{n}V_{PK}, \qquad \text{for } i = 1, \cdots, n. \quad (10)$$

The numerical optimization routine then manipulated the V_{SWi} values giving a series of solutions in terms of the I_i currents. These solutions determined a series of transfer characteristics, each one of which anchored to the desired function at the V_{SWi} points, but converging to the transfer characteristic that best approximated the desired function over the entire range of V_{IN}. The results are presented in Table I and Fig. 8 for the three cases of $n = 1$, 2, and 4. Note that (fortunately) due to the shapes of Figs. 2 and 6, the solutions that emerge all have $\eta = 1$; that is, no differential pairs need be cross connected.

Table I also lists values of total harmonic distortion for the various circuits, in the form of Fig. 7, designed with the given solutions. These distortion values include the first nine harmonics of the fundamental, and are those reported by the circuit simulation program SPICE, Version 2G, with the second-order MOSFET model developed at the University of California at Berkeley. This model uses a more accurate expression for the drain current and incorporates the effects of short and narrow channels, back gate bias, channel length modulation, subthreshold conduction and other second-order factors.

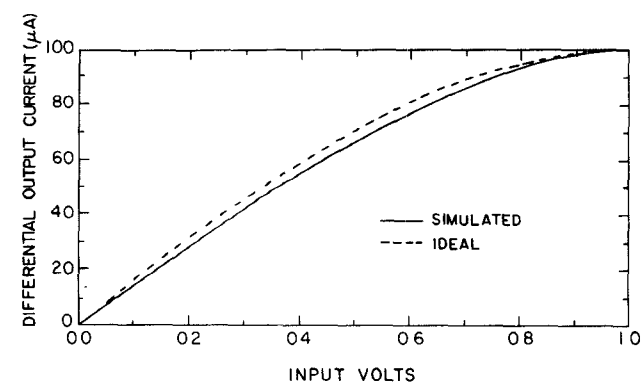
It is interesting to note that a single differential pair, properly driven, can generate a sinusoidal approximation with about 1-percent total harmonic content. For this result, the pair must be slightly "overdriven" into saturation by the input triangle wave, since $V_{SW1} = 0.9127V_{PK}$. Furthermore, the output current waveform, although in actuality clipped to $\pm I_1$, will appear to model a sinusoid of slightly greater amplitude, since $(I_1/I_0) = 0.9906$. For n greater than 2 the necessary bias current ratios become too large to implement with precision in a reasonable chip area.

III. PRACTICAL DESIGN

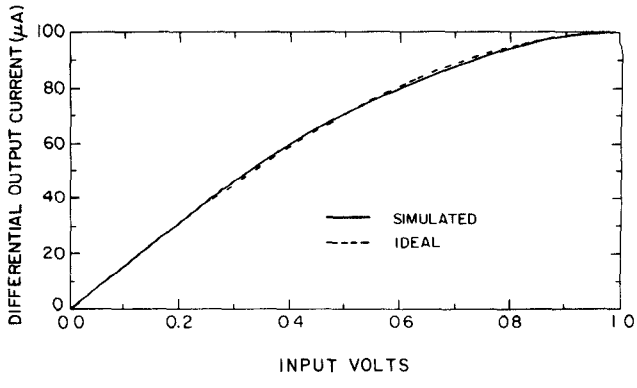
The solutions of the previous section illustrate the need for fairly accurate control over the relationships between the peak input triangle wave voltage and the switching voltages of the various differential pairs. Even small errors in these relationships could cause much higher harmonic distortion than in the optimum case, as demonstrated in Section I. The value of V_{SWi} for each differential pair depends on the MOSFET model parameter k, which in turn depends on the channel mobility and oxide capacitance. As these depend strongly on temperature, oxide thickness, and other factors, the V_{SWi} values cannot be assumed constant. A mechanism is needed to set the proper ratio of the switching voltage to the triangle wave amplitude for each differential pair independent of the k parameter. This can be accomplished by adjusting the bias currents I_i with a replica bias circuit [4],[5].

Consider the circuit of Fig. 9. Assume that V_{BIAS}, the differential voltage that drives the bias circuit, is equal to V_{PK}, the peak differential voltage of the triangle wave that is fed to the sine wave converter. M_{1B} and M_{2B} have identical k parameters, referred to as k_B. The operational amplifier, by controlling the drain currents, enforces the same condition on M_{1B} and M_{2B} as would be present if they composed a differential pair, namely that their source voltages are identical. This adjustment is made, however, with the constraint that I_D of M_{2B} is a times that of M_{1B} (I in Fig. 9), where $a < 1$. This constraint is enforced by appropriate device size ratios. From the first-order MOSFET model, the current I will reach equilibrium at

$$I = \frac{1}{(1-\sqrt{a})^2}\cdot k_B V_{PK}^2. \quad (11)$$



(a)



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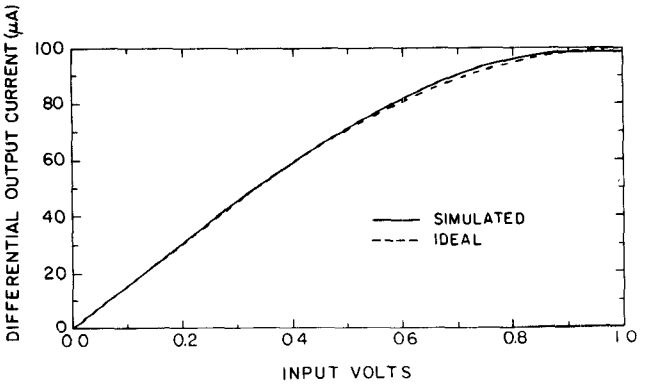

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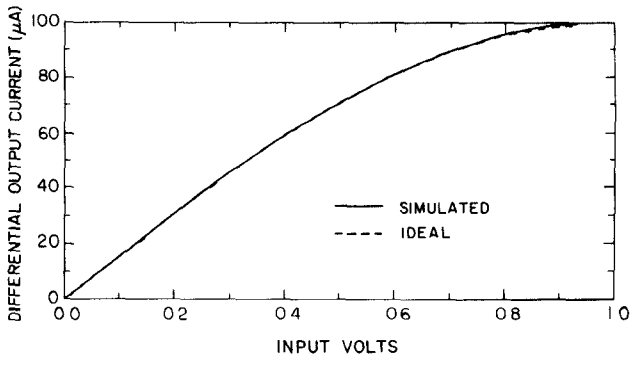

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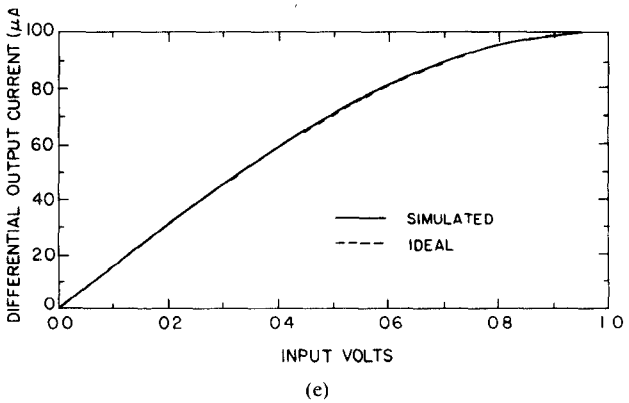

(e)

Fig. 8. Simulated transfer characteristic of triangle-to-sine wave converters compared with ideal curve of Fig. 2. (a) $n=1$ and equally spaced V_{SW_i} values. (b) $n=1$ and optimized V_{SW_i} values. (c) $n=2$ and equally spaced V_{SW_i} values. (d) $n=2$ and optimized V_{SW_i} values. (e) $n=4$ and equally spaced V_{SW_i} values.

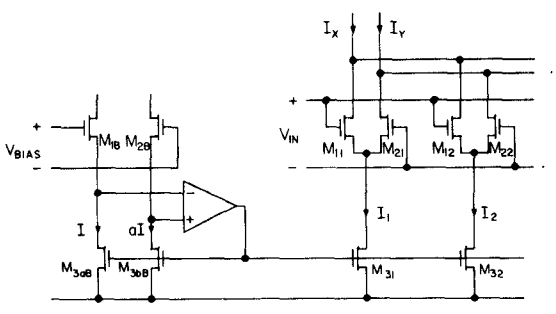

Fig. 9. Replica bias circuit with wave converter.

Suppose that k_{31} were equal to $(1-\sqrt{a})^2 \cdot k_{3aB}$ and that k_{11} and k_{21} were both equal to k_B. Then the switching voltage of the M_{11}, M_{21} pair $(\sqrt{I_1/k_B})$ would be set to V_{PK}. By designing proper device size ratios between M_{31} and M_{3aB}, and between the pairs M_{11}, M_{21} and M_{1B}, M_{2B}, any relationship between switching voltage and V_{PK} can be realized, independent of the magnitude of the bias current I_1. More differential pairs can be added to this bias generator, with bias currents supplied by additional MOSFET's as shown. Proper ratios between these current source devices can implement any desired ratio between bias currents.

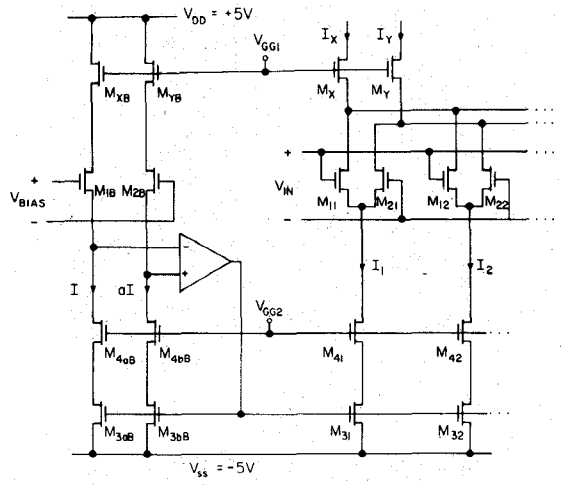

Fig. 10. Complete schematic of the wave converter.

TABLE II
MOSFET DIMENSIONS AND SUPPLY VOLTAGES FOR THE TEST CIRCUIT

MOSFETs	$\left(\frac{W}{L}\right)$	W (μm)	L (μm)
M_{11} M_{21}	4	80	20
M_{12} M_{22}	15	300	20
M_{31}	1	20	20
M_{32}	13.25	265	20
M_{1B} M_{2B}	13.75	275	20
M_{3aB}	21.5	430	20
M_{3bB}	1	20	20
M_{41}	1	20	20
M_{42}	13.25	265	20
M_{4aB}	21.5	430	20
M_{4bB}	1	20	20
M_X M_Y	13.25	265	20
M_{XB}	21.5	430	20
M_{YB}	13.25	265	20

Supply	Voltage
V_{DD}	5
V_{SS}	-5
V_{GG1}	4
V_{GG2}	-1.5

In this manner, a bias generator and waveform converter circuit can be designed so that it is optimally driven by a dc differential bias voltage equal to the triangle wave amplitude. Conversely, given a dc voltage of V_{PK} applied to it, such a bias generator will establish bias currents in the converter of exactly the values needed to convert a triangle wave of amplitude V_{PK} into a sine wave with minimum distortion.

This dc voltage can be obtained directly from the triangle wave oscillator. It may be present as a bias voltage applied to the comparator that signals the time for the triangle wave to reverse its ramp direction. Alternatively, V_{BIAS} may be generated externally by a peak detector.

A complete triangle-to-sine wave converter for the case of $n = 2$ is shown in Fig. 10. Note the inclusion of cascode devices to more closely preserve the proper current ratios between the various bias current source devices, and also to ensure that the transfer function of the differential pairs is not affected by channel-length modulation. Table II gives

TABLE III
MEASURED NMOS DEVICE PARAMETERS

Parameter	Value
V_T	0.95 V
k	13.6 $\frac{\mu A}{V^2}$
γ	0.55 $\sqrt{V}$

appropriate values of the (W/L) ratio for each device. These ratios are for a value of $1/21.5$ for the bias generator parameter a, chosen so that some device size ratios could be duplicated.

IV. EXPERIMENTAL RESULTS

The performance of the circuit of Fig. 10 was extensively simulated with SPICE. The operational amplifier in the bias generator was modeled by an ideal gain block with a voltage gain of 1000. After promising results were shown, a monolithic test circuit was laid out and fabricated. Some measured process model parameters are listed in Table III. Only the individual MOSFET's shown in Fig. 10 were included in this test circuit, and a commercial LF356 operational amplifier was added externally to complete the bias generator.

The MOSFET channel widths and lengths listed in Table II are mask dimensions. The precision with which sine waves can be generated with this circuit is dependent on the accuracy with which ratios between effective device dimensions can be realized. Designing all active devices with the same mask channel lengths makes these ratios first-order independent of lateral diffusion and other variable factors controlling effective channel length. The mask width values include an extra 1-μm allowance for the loss of effective channel width due to the gradually pitched walls of local oxidation windows. Devices M_{3aB}, M_{31}, M_{11}, and M_{21} are actually composed of four devices each that can be interconnected in various combinations. This allows trimming of the critical width ratios in the test version of this circuit around the nominal values given in Table II. Also listed in the table are the values used for the bias voltage sources V_{GG1} and V_{GG2}.

The long channels indicated in Table II were chosen so that this test circuit actually tested the principles of function synthesis outlined in Section II. Avoiding strong influence from short and narrow channel effects helps make the MOSFET's more closely follow the first-order model of (2), on which the aforementioned principles are based. These somewhat oversized test devices occupy a total active area of 1840 μm by 720 μm. There is much room for further refinements of monolithic versions of this circuit, and almost assuredly dramatic reductions in the active area could be achieved. Scaling down device sizes may also yield a higher frequency response than that of the test chip designed here. Fig. 11 is a photograph of one of the fabricated dice.

Fig. 12 is a graphical comparison between the observed amplitudes of the first eleven harmonics produced by the circuit and the first nine predicted by SPICE. Total

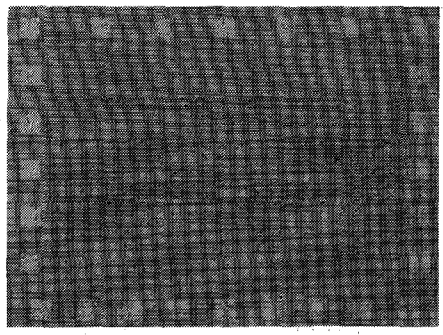

Fig. 11. Die photograph of the test circuit.

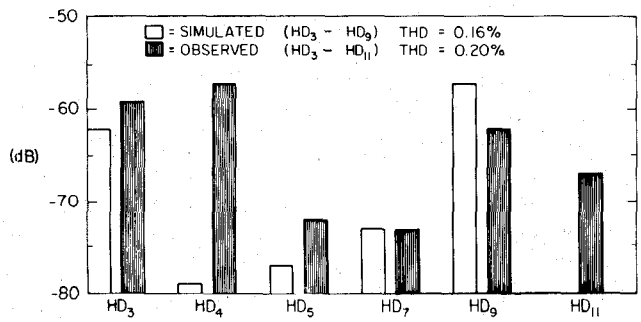

Fig. 12. Simulated and observed harmonic distortion of output sinusoid.

harmonic distortion figures are also given. For this test, the converter was driven by a 1-kHz triangle wave of amplitude 1 V, and a 1-V dc bias was applied as V_{BIAS} to the bias generator. An oscilloscope photograph of input and output waveforms and a spectrum analysis of the output sinusoid approximation under these conditions can be found in Figs. 13 and 14, respectively. The major part of any slight input offset voltage of the MOS differential pairs was nulled out in the testing procedure. Although the total harmonic content was fairly well predicted by simulation, the numerical MOS models are clearly not precise enough to accurately estimate the contribution of each harmonic. The significant fourth harmonic contribution in Fig. 12 also appeared in computer simulations when a small internal offset voltage between the two differential pairs was introduced. This offset cannot be externally nulled. Three different fabricated dice were bonded and tested, all giving essentially the same performance.

As a comparison, the simple bipolar circuit described in [11] generates sine waves with 0.2-percent THD at 100 kHz, while the more complex design reported in [2] achieves 0.017-percent THD at 10 kHz.

In practice, the waveform converter may be driven with a triangle wave whose amplitude V_{PK} is not exactly equal to V_{BIAS}. With a bias error voltage defined as

$$\text{error voltage} = V_{PK} - V_{\text{BIAS}}$$

the dependence of the resulting observed total harmonic distortion on this error voltage is graphed in Fig. 15. The three curves correspond to three different values of amplitude. Note the similarity between each curve and the ideal limit of Fig. 3, although each observed curve's minimum is not, of course, at zero THD. The dislocation of two of the

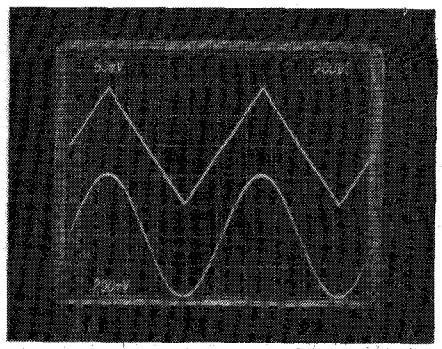

Fig. 13. Measured input and output waveforms of the wave converter at 1 kHz. Top trace 500 (mV/div), bottom trace 200 (mV/div).

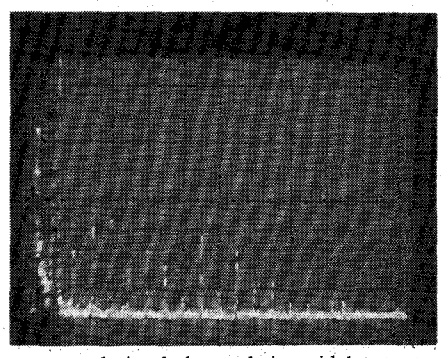

Fig. 14. Spectrum analysis of observed sinusoidal output at 1 kHz. 10 (dB/div) vertical, 2 (kHz/div) horizontal.

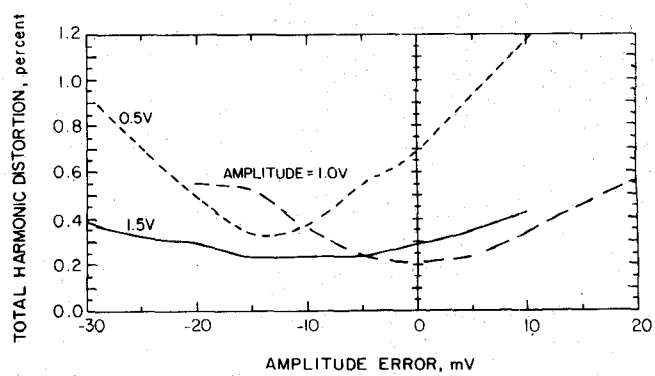

Fig. 15. Observed THD versus amplitude error for three values of triangle wave amplitude at 1 kHz.

minima from zero error voltage is due to small deviations in bias generator device width ratios from the exact ratios designed in Section III.

The fundamental frequency at which the output amplitude dropped by 3 dB from its value at 1 kHz was found to be 1.1 MHz. Fig. 16 plots the test circuit THD as a function of ambient temperature. The small rise in THD at low temperatures is also due to slight device size errors. Fig. 17 shows the temperature dependence of the sinusoidal differential output current amplitude. These curves were measured at 1 kHz and 1-V input amplitude, and with V_{BIAS} held constant. The temperature dependence of the output amplitude is an inherent characteristic of the temperature compensating mechanism of this wave converter. With a constant V_{BIAS}, the bias generator will scale the differential pair bias currents to keep distortion minimized.

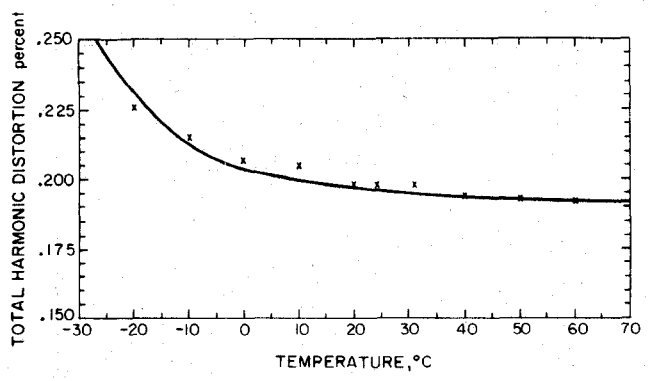

Fig. 16. THD versus ambient temperature, 1-V triangle wave amplitude at 1 kHz.

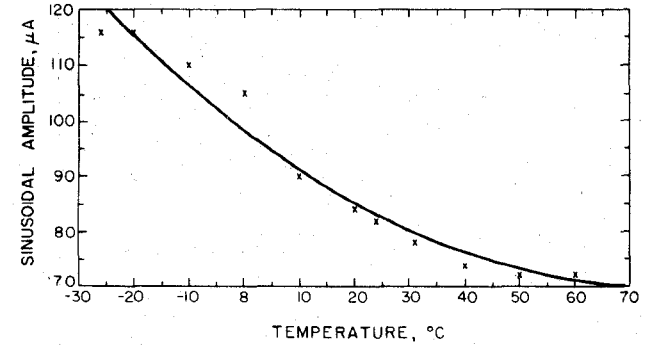

Fig. 17. Output sinusoid amplitude versus ambient temperature, 1-V input amplitude at 1 kHz and V_{BIAS} held constant.

Therefore the differential pair output amplitudes must vary when the device characteristics drift with temperature. To compensate for this dependence the wave converter can be followed by a gain stage designed with the inverse temperature characteristic.

V. Conclusion

General techniques for designing nonlinear MOS analog circuits for function approximation have been presented in this paper. These techniques have been applied to the case of triangle-to-sine wave conversion and a simple circuit design developed. The effectiveness of this design has been demonstrated by simulation and by testing of a fabricated monolithic circuit. A total mid frequency harmonic content of 0.2-percent and a bandwidth of 1.1 MHz have been shown to be achievable in practice with these simple techniques. In addition, a replica bias circuit design for preserving this spectral purity over temperature, processing, and triangle wave amplitude variations has been described.

References

[1] R. G. Meyer, W. M. C. Sansen, S. Lui, and S. Peeters, "The differential pair as a triangle-sine wave converter," *IEEE J. Solid-State Circuits*, vol. SC-11, pp. 418–420, June 1976.

[2] B. Gilbert, "A monolithic microsystem for analog synthesis of trigonometric functions and their inverses," *IEEE J. Solid-State Circuits*, vol. SC-17, pp. 1179–1191, Dec. 1982.

[3] D. C. Soo and R. G. Meyer, "A four-quadrant NMOS analog multiplier," *IEEE J. Solid-State Circuits*, vol. SC-17, pp. 1174–1178, Dec. 1982.

[4] D. Senderowicz, D. A. Hodges, and P. R. Gray, "High performance NMOS operational amplifier," *IEEE J. Solid-State Circuits*, vol. SC-13, p. 763, Dec. 1978.

[5] A. Young, "A high-performance all-enhancement NMOS operational amplifier," *IEEE J. Solid-State Circuits*, vol. SC-14, pp. 1073–1074, Dec. 1979.

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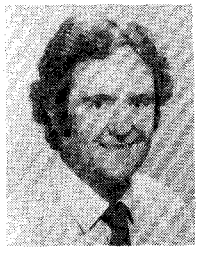

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