

# Correspondence

## The Differential Pair as a Triangle-Sine Wave Converter

ROBERT G. MEYER, WILLY M. C. SANSEN, SIK LUI,  
AND STEFAN PEETERS

**Abstract**—The performance of a differential pair with emitter degeneration as a triangle-sine wave converter is analyzed. Equations describing the circuit operation are derived and solved both analytically and by computer. This allows selection of operating conditions for optimum performance such that total harmonic distortion as low as 0.2 percent has been measured.

### I. INTRODUCTION

The conversion of triangle waves to sine waves is a function often required in waveshaping circuits. For example, the oscillators used in function generators usually generate triangular output waveforms [1] because of the ease with which such oscillators can operate over a wide frequency range including very low frequencies. This situation is also common in monolithic oscillators [2]. Sinusoidal outputs are commonly desired in such oscillators and can be achieved by use of a nonlinear circuit which produces an output sine wave from an input triangle wave.

The above circuit function has been realized in the past by means of a piecewise linear approximation using diode shaping networks [1]. However, a simpler approach and one well suited to monolithic realization has been suggested by Grebene [3]. This is shown in Fig. 1 and consists simply of a differential pair with an appropriate value of emitter resistance  $R$ . In this paper the operation of this circuit is analyzed and relationships for optimum performance are derived.

### II. CIRCUIT ANALYSIS

The circuit to be analyzed is shown in Fig. 1(a). The sinusoidal output signal can be taken either across the resistor  $R$  or from the collectors of  $Q1$  and  $Q2$ . The current gain of the devices is assumed large so that the waveform is the same in both cases.

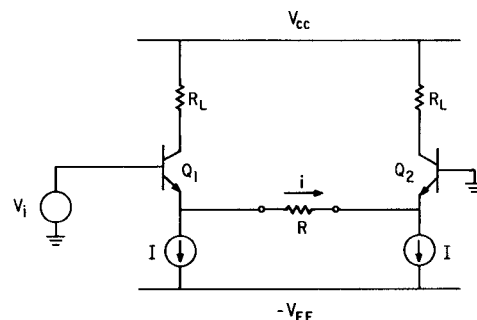
The operation of the circuit can be understood by examining the transfer function from  $V_i$  to current  $i$  flowing in  $R$ . This is shown in Fig. 1(b) and has the well-known form for a differential pair. The inclusion of emitter resistance  $R$  allows the curvature to be adjusted for optimum output waveform, as will be seen later.

When a triangle wave input of appropriate amplitude is applied as shown in Fig. 1(b), the output waveform is flattened

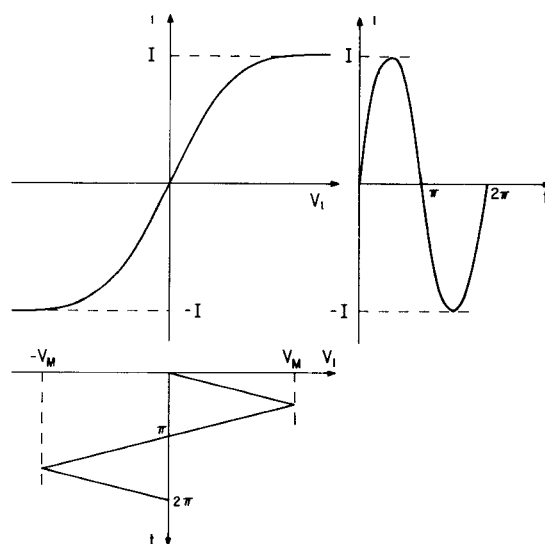
Manuscript received August 4, 1975; revised December 15, 1975. Research by R. G. Meyer and S. Lui was sponsored by the U.S. Army Research Office, Durham, NC, under Grant DAHC04-74-G0151. Research by W. M. C. Sansen and S. Peeters was sponsored respectively by the Belgian National Science Foundation (NFWO) and the Belgian National Fund for Scientific Research (IWONL).

R. G. Meyer and S. Lui are with the Department of Electrical Engineering and Computer Sciences and the Electronics Research Laboratory, University of California, Berkeley, CA 94720.

W. M. C. Sansen and S. Peeters are with the Laboratorium Fysica en Elektronica van de Halfgeleiders, Katholieke Universiteit, Leuven, Belgium.



(a)



(b)

Fig. 1. Triangle-sine wave converter. (a) Circuit schematic. (b) Transfer function.

by the curvature of the characteristic and can be made to approach a sine wave very closely. As with all such circuits, the distortion in the output sine wave is dependent on the input amplitude and this must be held within certain limits for acceptable performance.

In the following analysis,  $Q1$  and  $Q2$  are assumed perfectly matched, although in practice mismatches will occur and give rise to second-order distortion (typically less than 1 percent). However, introduction of an input dc offset voltage has been found to reduce second-order distortion terms to negligible levels and they will be neglected in this analysis. The presence of such an offset does not affect the following analysis. From Fig. 1(a)

$$V_i = V_{BE1} + iR - V_{BE2} \quad (1)$$

but

$$V_{BE1} = V_T \ln \frac{I_{C1}}{I_K} \quad (2)$$

$$V_{BE2} = V_T \ln \frac{I_{C2}}{I_K}$$

where

$$V_T = \frac{kT}{q}.$$

Substitution of (2) and (3) in (1) gives

$$V_i = iR + V_T \ln \frac{I_{C1}}{I_{C2}}.$$

If  $\alpha \approx 1$  for  $Q1$  and  $Q2$  then

$$I_{C1} = I + i$$

$$I_{C2} = I - i.$$

Substitution of (6) and (7) in (5) gives

$$\frac{V_i}{V_T} = \frac{i}{I} \left( \frac{IR}{V_T} \right) + \ln \frac{1 + \frac{i}{I}}{1 - \frac{i}{I}}.$$

Equation (8) is expressed in normalized form and shows that the output signal  $i/I$  normalized to  $I$  depends only on normalized input voltage  $V_i/V_T$  and factor  $IR/V_T$ . Because of the small number of parameters in (8), it is readily solved in normalized form by computer to yield a series of curves specifying the circuit performance. Before this is pursued however, it is useful to consider an approximate analytical solution of (8) which gives some insight into the circuit operation.

The log term in (8) can be expanded as a power series

$$\ln \frac{1 + \frac{i}{I}}{1 - \frac{i}{I}} = 2 \frac{i}{I} + \frac{2}{3} \left( \frac{i}{I} \right)^3 + \frac{2}{5} \left( \frac{i}{I} \right)^5 + \dots \quad (9)$$

for

$$\frac{i}{I} < 1. \quad (10)$$

Substitution of (9) in (8) for the circuit transfer function gives

$$\frac{V_i}{V_T} = \left( \frac{IR}{V_T} + 2 \right) \frac{i}{I} + \frac{2}{3} \left( \frac{i}{I} \right)^3 + \frac{2}{5} \left( \frac{i}{I} \right)^5 + \dots \quad (11)$$

This can be expressed as

$$\begin{aligned} \frac{1}{\frac{IR}{V_T} + 2} \frac{V_i}{V_T} &= \frac{i}{I} + \frac{2}{3} \frac{1}{\frac{IR}{V_T} + 2} \left( \frac{i}{I} \right)^3 \\ &+ \frac{2}{5} \frac{1}{\frac{IR}{V_T} + 2} \left( \frac{i}{I} \right)^5 + \dots \end{aligned} \quad (12)$$

The desired transfer function for the circuit is [see Fig. 1(b)]

$$i = K_1 \sin K_2 V_i \quad (13)$$

where  $K_1$  and  $K_2$  are constants, and thus

$$K_2 V_i = \arcsin \frac{i}{K_1}. \quad (14)$$

Expansion of (14) in a power series gives

$$K_2 V_i = \frac{i}{K_1} + \frac{1}{6} \left( \frac{i}{K_1} \right)^3 + \frac{3}{40} \left( \frac{i}{K_1} \right)^5 + \dots \quad (15)$$

By comparison of (12) and (15) it is apparent that in order to realize the desired transfer function, it is necessary (but not sufficient) that

$$K_1 = I \quad (16)$$

$$K_2 = \frac{1}{\frac{IR}{V_T} + 2} \frac{1}{V_T}. \quad (17)$$

Equation (16) shows that the peak value of the output current should equal the current source value  $I$ . If the input triangle wave has peak value  $V_M$  then (13) indicates that for a perfect sine wave output it is necessary that

$$K_2 V_M = \frac{\pi}{2}. \quad (18)$$

Substitution of (17) in (18) gives

$$\frac{V_M}{V_T} = 1.57 \frac{IR}{V_T} + 3.14. \quad (19)$$

Equation (19) gives the normalized input triangle wave amplitude for minimum output distortion.

The circuit transfer function given by (12) is to be made as close as possible to the arcsin expansion of (15). If we equate coefficients of third- and fifth-order terms in (12) and (15) we obtain  $IR/V_T$  equal to 2 and 3.33, respectively. It is thus expected that the best performance of the circuit will occur for this range of values, and this is borne out by experiment and computer simulation.

### III. COMPUTER SIMULATION AND EXPERIMENTAL RESULTS

The solution of (8) was obtained by computer simulation for various values of  $V_M/V_T$  (normalized triangle wave amplitude) and factor  $IR/V_T$ , and the output signal was analyzed into its Fourier components. Third-harmonic distortion ( $HD_3$ ) is defined as the ratio of the magnitude of the signal at the third harmonic frequency to the magnitude of the fundamental. Total harmonic distortion (THD) is  $\sqrt{HD_3^2 + HD_5^2 + \dots}$ . A typical plot of  $HD_3$  and THD is shown in Fig. 2 for  $IR/V_T = 2.5$ . It can be seen that the THD null and the  $HD_3$  null occur at about the same value of  $V_M/V_T$ , and this is true for any value of  $IR/V_T$ . The measured points in Fig. 2 show good agreement with the computed curves and both show a minimum value of THD of about 0.2 percent for  $V_M/V_T \approx 6.6$ . This corresponds to  $V_M \approx 175$  mV for  $V_T = 26$  mV.

The effect of variations in  $IR/V_T$  on the minimum value of THD is illustrated by the computed curve of Fig. 3. At each point on this curve,  $V_M/V_T$  was adjusted for minimum distortion. This curve shows that best performance is obtained for  $IR/V_T \approx 2.5$ , and this is within the range of 2–3.3 predicted earlier. These results were verified by experimental data.

The effect of temperature variation on circuit performance was investigated by setting  $IR/V_T = 2.5$  at room temperature and holding  $I$ ,  $R$ , and  $V_M$  constant as  $T$  was varied. Measured and computed THD were less than 1 percent from 0° to 55°C. The measured rms output amplitude decreased 5 percent over this temperature range.

The results described above were measured and computed at low frequencies. The measurements were made at frequencies of the order of 100 kHz where the distortion was still frequency independent. Computer simulation neglected all capacitive effects in the transistors. In order to investigate the performance of the circuit at frequencies where charge storage

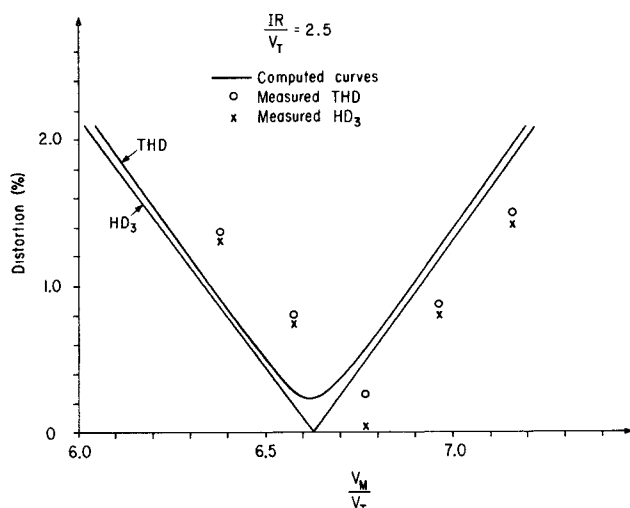


Fig. 2. Computed and measured distortion versus normalized input voltage of the circuit of Fig. 1(a) with  $IR/V_T = 2.5$ .

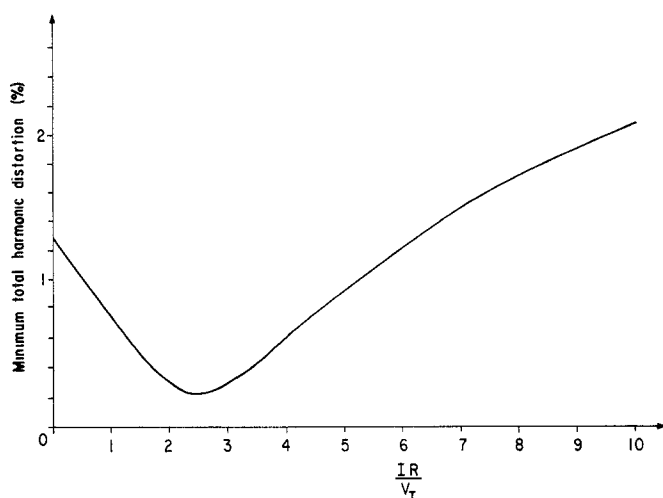


Fig. 3. Computed minimum total harmonic distortion versus  $IR/V_T$  for the circuit of Fig. 1.

in the transistors is important, computer simulation was used with input frequencies up to 10 MHz and including a complete, large-signal high-frequency device model. The results showed that THD was independent of frequency up to about 1 MHz. Above this frequency, THD increased rapidly due to irregularities in the peaks of the output sinusoid. This is due to the fact that at the signal peaks, the output current  $i$  approaches the current source value  $I$  [see (16)], and thus  $Q1$  and  $Q2$  alternately approach cutoff. The  $f_T$  of the transistors in this condition is quite low and they are unable to follow the input signal.

#### IV. CONCLUSIONS

The performance of a differential pair with emitter degeneration as a triangle-sine wave converter has been approached by forming a nonlinear equation in three normalized parameters. The output normalized waveform  $i/I$  is a function only of the input amplitude  $V_M/V_T$  of the triangle wave, and factor

$IR/V_T$ . Computer solution shows that the output sine wave THD has a minimum of about 0.2 percent for  $IR/V_T = 2.5$  and  $V_M/V_T = 6.6$ .

#### ACKNOWLEDGMENT

The authors wish to thank Dr. A. B. Grebene for suggesting to them the potential of the differential pair as a triangle-sine wave converter.

#### REFERENCES

- [1] E. H. Heflin, "Compact function generator with enhanced capability-cost ratio," *Hewlett-Packard J.*, pp. 15-20, July 1973.
- [2] A. B. Grebene, *Analog Integrated Circuit Design*. New York: Van Nostrand Reinhold, 1972, p. 313.
- [3] —, "Monolithic waveform generation," *IEEE Spectrum*, pp. 34-40, Apr. 1972.

### Integrated TV Tuning System

W. JOHN WU AND ERIC G. BREEZE

**Abstract**—This paper presents a frequency synthesized digital tuning system for UHF/VHF TV receivers and the integrated circuits developed to implement this scheme. The design and performance of the  $1\text{ GHz} \div 248/256$  programmable prescaler is described in detail.

Recent trends in the consumer and communication industry toward more cost effective and more reliable systems place the following requirements on advanced TV tuning systems: meet new FCC regulations; tune all channels (VHF and UHF) individually without complex alignment; be capable of interfacing with digital displays and remote control circuits; have keyboard entry for channel selection; and allow provisions for fine tuning. This correspondence presents a frequency synthesizer which meets all the above requirements and is highly accurate as the phase-locked loop is self-compensating for parameter drifts and component tolerance.

Fig. 1 gives the block diagram of the frequency synthesizer. The dotted block represents a standard VHF or UHF varactor tuner. An amplifier is connected to the VCO output of the tuner to increase the voltage to the acceptable level to drive the digital prescaler. The purpose of the prescaler is to divide down the local oscillator high frequencies to a range that can be processed and counted by TTL or MOS logic circuits. Output of the prescaler is then fed to the programmable counter programmed by the keyboard entry. The output is then compared with a crystal controlled reference frequency. The phase/frequency comparator drives an integrator which in turn provides voltage control to the varactor tuner input [1]. Physical implementation of this scheme requires 5 integrated circuits and will precisely tune 99 channels, the air channels (2 through 83), and the cable channels (84 through 99). The fine tuning provides  $\pm 1$  MHz in 128 steps. It also has the capability of keyboard entry, channel searching, and channel number display.

The  $1\text{ GHz} \div 248/256$  prescaler is designed for this specific

Manuscript received December 28, 1975.

The authors are with Fairchild Semiconductor, Mountain View, CA 94042.