NPTEL Workshop: Test 1

Wadhwani Electronics Lab, IIT Bombay

8th July 2022

Important Instructions:

1. Total Marks: 20
   Vhdl Code and simulations (10 Marks), Demo on Krypton board (5 Marks), Scan chain output (5 Marks).
2. Duration: 2 hrs
3. Use structural modelling for this experiment; means instantiate components and use port map to connect those components.
4. For implementing basic gates (AND, OR, NOT, NAND, NOR, XOR and XNOR), you are allowed to use only the components in Gates.vhdl and your own VHDL descriptions in the experiments/homework problems so far.
5. Perform RTL and Gate-level simulation using the provided testbench and tracefile. Demonstrate the simulations to your TA.
6. Perform the experiment on Krypton board.
7. Perform scan chain for the experiment.

Submissions:
You have to submit your **handwritten design** on sheet and **quartus project via. google form** in a single zip file. The design and project files should contain:

1. Design: Your neatly handwritten/hand drawn design comprising of truth-tables, K-maps, Boolean equations, justifications for the boolean equations by inspection (as the case may be) to explain your approach along with the entities of the overall design and the decomposed components.
2. Quartus Project folder: After successful demonstration, compress your whole project directory into zip file (including all design files (vhd/vhdl), .qpf file, scanchain output.txt file) and submit with name "NPTEL_test1_StudentName.zip".

Problem Statement:

1. Design the logic circuit to meet the specifications as follows

   (a) The circuit has one 4-bit input A(A3A2A1A0) and one bit output Y. The Tracefile format is : ($< A3\ A2\ A1\ A0 >\ \ < Y >\ \ 1$)

   (b) Design any one of the three blocks(BCD; ONES; DIV 3_5) as mentioned below:

      i. BCD: This outputs 1 if the four bit input A is valid BCD number. The output should be 0 otherwise.
      Tracefile
      ii. ONES: This outputs 1 if the number of ones in 4-bit input A is equal to 3. The output should be 0 otherwise.
      Tracefile
      iii. DIV 3_5: This outputs 1 if the four bit input A is divisible by 3 or 5 or both. The output should be 0 otherwise.
      Tracefile

2. Write VHDL description for these blocks.

3. Demonstrate the RTL and Gate Level simulation for complete design to your TA using the generic Testbench and the given Tracefile.

4. Perform experiment on Krypton board and also do the scan chain and demonstrate it to your TA.

5. Submit the handwritten design and upload zipped Quartus project directory via. google form.

6. Google form link for submission: **NPTEL_Test1**

7. Those who are done with one block can try doing rest two blocks for bonus marks.