NPTEL Workshop: Homework 2

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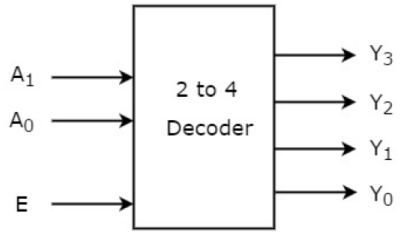
Instructions:

1. Use structural modelling for this experiment; means instantiate components and use port map to connect those components.
2. Perform RTL and Gate-level simulation using the provided testbench and tracefile.
3. Demonstrate the simulations to your TA on next day.

Problem Statement:

1. **Part-A: 2 to 4 decoder**
   (a) Design: Design a 2 to 4 decoder with enable input as shown in figure below. Use only 2 input gates and inverters given in Gates.vhdl. (Assume enable as active high input)
   INFO: Decoders are combinational circuit which takes in binary information in the form of N input lines and change the binary information into 2^N output lines. Hint: See Tracefile to understand the functionality of decoder

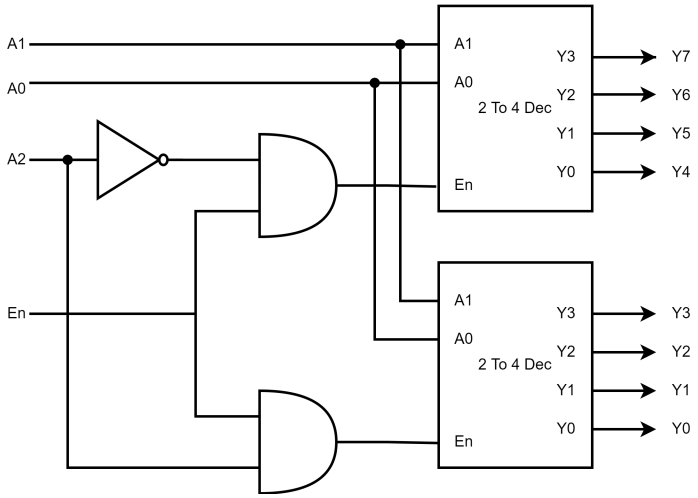


   (b) VHDL description: Describe a 2 to 4 decoder with enable input in VHDL.

   (c) Simulation: Simulate the decoder using the generic testbench to confirm the correctness of your description.
   NOTE: To do this, you need to use the given tracefile and modify the testbench given to you appropriately.
   Tracefile format: ($< A1\ A0 >< E >\ < Y3\ Y2\ Y1\ Y0 >\ \ 1111$) Tracefile

2. **Part-B: 3 to 8 decoder**
   (a) VHDL description: Describe a 3 to 8 decoder with enable input in VHDL using 2 to 4 decoder of part A.
   INFO: 3 data input, 1 enable input, $2^3 = 8$ output lines

(b) Design: Designing of 3 to 8 decoder with enable input using 2 to 4 decoder is shown below:



(c) Simulation: Simulate the decoder using the generic testbench to confirm the correctness of your description. To do this, you need to use the given tracefile and modify the testbench given to you appropriately. Tracefile format: $(A2\ A1\ A0 >< E > \ < Y7\ Y6\ Y5\ Y4\ Y3\ Y2\ Y1\ Y0 > \ \ 11111111)$ Tracefile