NPTEL Workshop: Homework 3

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Instructions:

1. Use structural modelling for this experiment; means instantiate components and use port map to connect those components.
2. Perform RTL and Gate-level simulation using the provided testbench and tracefile.
3. Demonstrate the simulations to your TA on next day.
4. Perform this experiment on Krypton board.

Problem Statement: Vowel Detector

1. Design: The English language has 26 alphabets, which are classified into vowels and consonants. Let us assume that we have only the first 16 letters of the English alphabets (i.e. A to P) Let 0000 represent A, 0001 represent B and so on.
   Design a system that gives output as '1' when a given alphabet is a vowel, and '0' in other cases.

   Note: You are only allowed to use pre-designed gates using port maps (NO DATAFLOW STATEMENTS). Make an attempt to minimize the number of logic gates used.

2. VHDL description: Describe your designed vowel detector in VHDL.

3. Simulation: Simulate the vowel detector using the generic testbench to confirm the correctness of your description.
   NOTE: To do this, use the tracefile given below and modify the testbench given to you appropriately.
   Tracefile format: ($< x3\ x2\ x1\ x0 >\ \ < Y >\ \ 1$) Tracefile

4. Perform the experiment in the Krypton board. Inputs can be given using four switches corresponding to binary representation of alphabets (for example to give input B, four switch combination will be 0001). One LED will turn ON when given input alphabet has three points.