NPTEL Workshop: Homework 4

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Instructions:

1. Use Behavioral and Dataflow modelling for this experiment.
2. Perform RTL and Gate-level simulation using the provided testbench and tracefile.
3. Demonstrate the simulations to your TA.

Problem Statement

1. Describe the given ALU using VHDL. This ALU circuit performs various functions based on select lines.

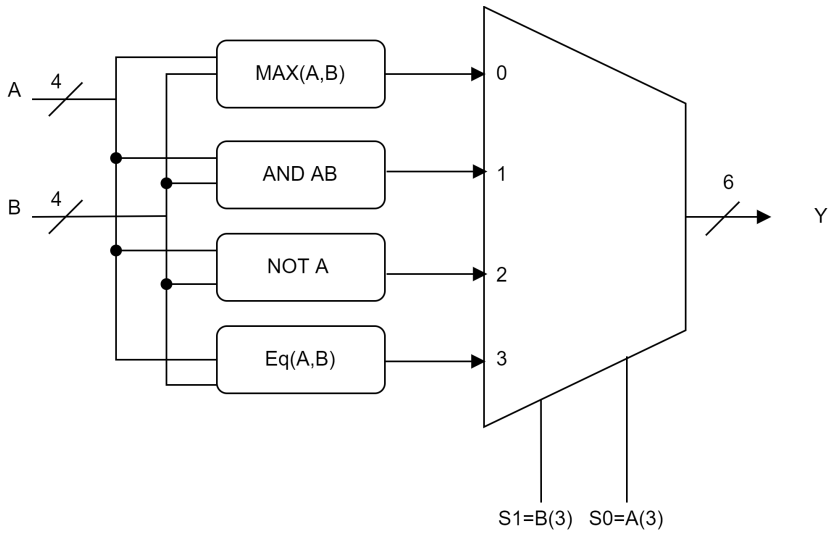

Figure 1: ALU with 4 functions

S1 S0	ALU Output
0 0	MAX(A,B): This block outputs larger number between A and B else outputs 0000.
0 1	AND A B: This block performs AND operation between A , B.
1 0	NOT A: This block performs NOT operation of A.
1 1	Eq(A,B): This block outputs the number whenever A=B else it should output 0000.

- In this problem MSB of inputs A and B are also working as selection lines. S1 is connected to MSB of input B [i.e. B(3)] and S0 is connected to MSB of input A [i.e. A(3)].
- Simulate your design using the generic testbench to confirm the correctness of your description.
- Tracefile format $< A3\,A2\,A1\,A0\,B3\,B2\,B1\,B0 >< Y5\,Y4\,Y3\,Y2\,Y1\,Y0 >$ 1 1 1 1 1 1