# NPTEL Workshop: Homework 6 (Bonus)

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## 1 Problem statement

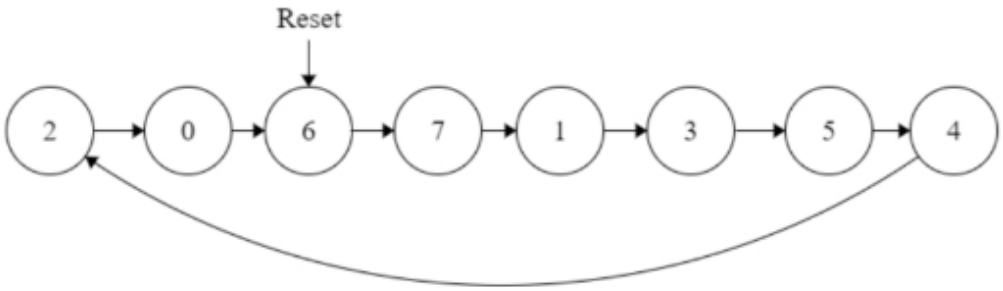
Consider the following Sequence generator which generates a certain sequence upon every input clock pulse and on reset the sequence will go into default sequence i.e 6 in this case.

Design and implement both structural and behavioral below sequence generator and Perform RTL and Gate level simulation and scanchain with the given TRACEFILE.

**Note**: The reset is asynchronous in nature i.e reset effects the output sequence irrespective of the input clock arrival.

Inputs: Reset, clock

Output(3 bit):Y2Y1Y0




Tracefile format: ($< reset >< clock >$ $< y2y1y0 >$ $< MaskBits >$) Tracefile