NPTEL Workshop: Experiment 5

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Instructions:

1. Use structural modelling for this experiment; means instantiate components and use port map to connect those components.
2. Perform RTL and Gate-level simulation using the provided testbench and tracefile.
3. Demonstrate the simulations to your TA.
4. Perform this experiment on Krypton board.
5. Perform scan-chain and demonstrate to your TA.

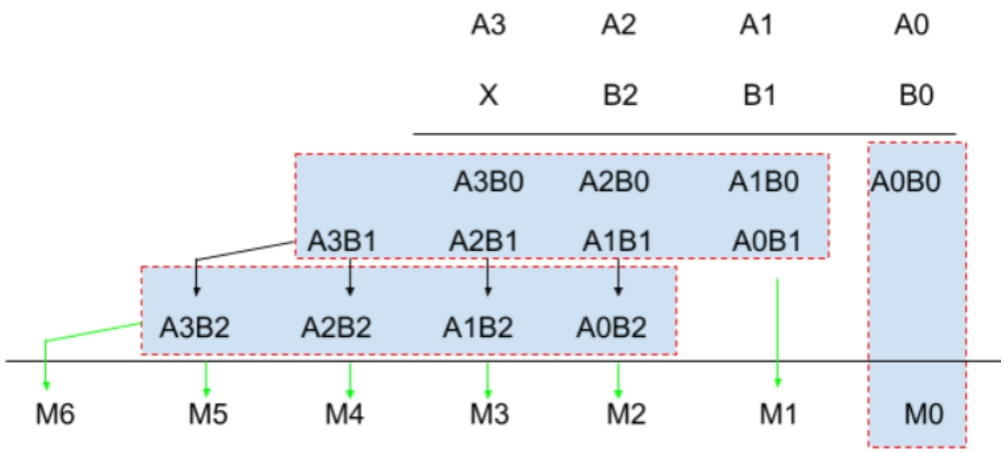
Problem Statement: Multiplier

1. Design: Design a multiplier circuit with one 4-bit input and one 3-bit input.

2. VHDL description: Describe your designed circuit in VHDL.

3. Try it using Generate for Bonus Marks.
   Generate statements are used to replicate Logic in VHDL. The generate keyword is always used in a combinational process or logic block. If the digital designer wants to create replicated or expanded logic in VHDL, the generate statement with a for loop is the way to accomplish this task.

4. Syntax for Generate:
   label : for $<$ *parameter* $>$ in $<$ *range* $>$ generate
   $<$ *declarations* $>$
   begin
   $<$ *concurrent statements* $>$
   end generate label;



5. Simulation: Simulate your design using the generic testbench to confirm the correctness of your description.
   NOTE: To do this, use the tracefile given below and modify the testbench given to you appropriately.

6. Scanchain: Test the correctness of your design using Scanchain
   Tracefile format: ($< A3\ A2\ A1\ A0\ B2\ B1\ B0 >\ < M6\ M5\ M4\ M3\ M2\ M1\ M0 >\ \ 1\ 1\ 1\ 1\ 1\ 1\ 1$)
   Tracefile