NPTEL Workshop: Homework 1

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Instructions:

1. Use structural modelling for this experiment; means instantiate components and use port map to connect those components.
2. Perform RTL and Gate-level simulation using the provided testbench and tracefile.
3. Demonstrate the simulations to your TA on next day.

Problem Statement: 4-bit Adder-Subtractor

1. VHDL Description: Using the full adder and XOR gate as a component, describe a 4-bit ripple carry adder-subtractor in VHDL.

   INFO: 4-bit ripple carry adder-subtractor has following parts
   (a) Two 4-bit inputs : A (A3 A2 A1 A0) , B (B3 B2 B1 B0)
   (b) One 1-bit input: M
   (c) One 4-bit output : S (S3 S2 S1 S0)
   (d) One 1-bit output: Cout

   NOTE: It is a simple binary adder-subtractor that can be implemented by cascading four full adders such that the carry generated by the addition of lower significant bits forms the incoming carry for addition of the next significant bits.

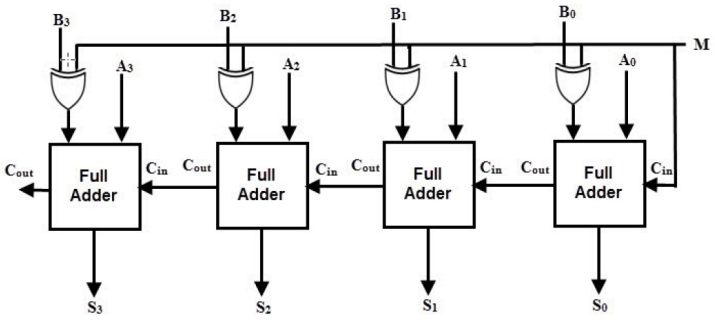

Figure 1: Design of 4 Bit Adder-Subtractor

2. Simulation: Simulate the design using the generic testbench to confirm the correctness of your description.
   NOTE: To do this, you need to use the given tracefile and modify the testbench given to you appropriately.
   Tracefile format: $(< a3\,a2\,a1\,a0 >< b3\,b2\,b1\,b0 >< M > \; < Cout >< S3\,S2\,S1\,S0 > \quad 11111)$ Tracefile

3. Expected Simulation Result of 4 Bit Adder-Subtractor:

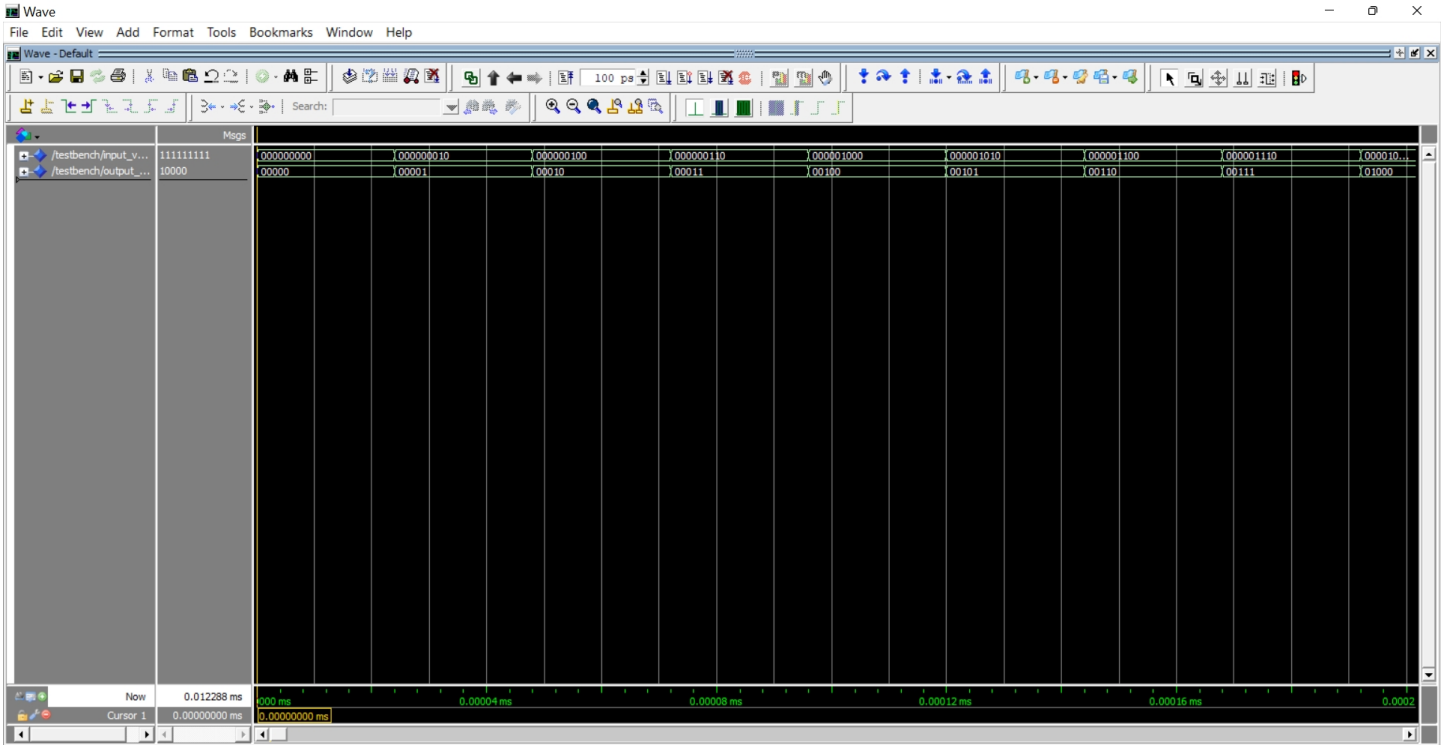

Figure 2: 4 Bit Adder-Subtractor Simulation Result