NPTEL Workshop: Experiment 4

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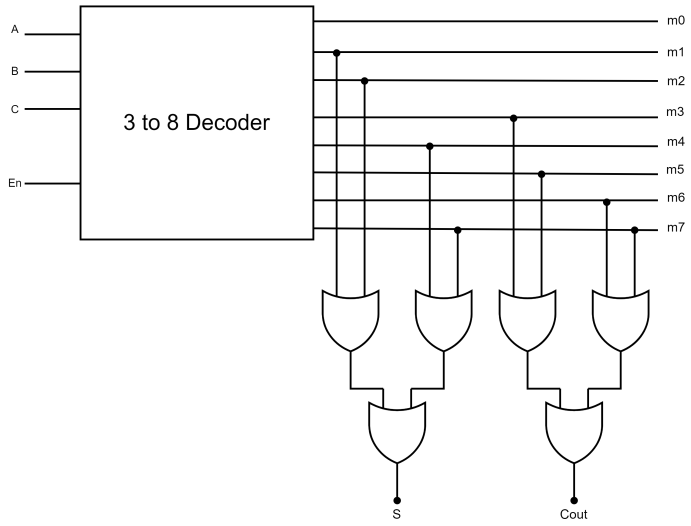
Instructions:

1. Use structural modelling for this experiment; means instantiate components and use port map to connect those components.
2. Perform RTL and Gate-level simulation using the provided testbench and tracefile.
3. Demonstrate the simulations to your TA.
4. Perform this experiment on Krypton board.
5. Perform scan-chain and demonstrate to your TA.

Problem Statement: Full adder using 3 to 8 decoder

1. VHDL description: Describe full adder using 3 to 8 decoder (designed on day2) in VHDL.

   INFO: Design of full adder using 3 to 8 decoder is shown below:
   Make Enable = '1'



2. Simulation: Simulate this full adder using the generic testbench to confirm the correctness of your description.
   NOTE: To do this, use the given tracefile and modify the testbench given to you appropriately.
   Tracefile format: ($< A\ B\ Cin >\ \ < S\ Cout >\ \ 11$) Tracefile