

BA2 DSD Résumé

Logical operators: conjunction "and", disjunction "or", exclusive or (logic exclusion)

n inputs	→ 2 ⁿ combinations	A	B	A · B	A + B	"xor"	= $\bar{A} \cdot B + A \cdot \bar{B}$	A ⊕ B = $(\neg A \wedge B) \vee (\neg B \wedge A)$
"not"	A → \bar{A}	0	0	0	0	0	\bar{A}	$\Delta A \oplus (B \cdot C) \neq (A \oplus B) \cdot (A \oplus C)$
A → $\neg A$	1	0	0	1	1	1	\bar{A}	$A \cdot (\bar{B} + C) = (A \cdot \bar{B}) + (A \cdot C)$
1	0	0	1	1	1	1	$A + (\bar{B} + C) = (A + \bar{B}) \cdot (A + C)$	$A \cdot (\bar{B} \oplus C) = (A \cdot \bar{B}) \oplus (A \cdot C)$
0	1	1	1	1	0	0	$\Delta A \oplus (B \cdot C) \neq (A \oplus B) \cdot (A \oplus C)$	$A \oplus (B \otimes C) = (A \oplus B) \otimes (A \oplus C)$

first $\rightarrow (\cdot) \cdot \oplus +$ last ANSI IEC

Analog: range of values
Digital: two values (1, 0)
 $O \cdot F$ 1.T

Result = 1: minterms
Result = 0: maxterms
 \downarrow : positive edge, \uparrow : negative edge

Properties:

- $A \cdot A = A$ $A + A = A$ $A \oplus A = 0$ $A \cdot 0 = 0$ $A \cdot 1 = A$ $A + 0 = A$ $A + 1 = 1$ $A \oplus 0 = A$ $A \oplus 1 = \bar{A}$
- $A \cdot (A+B) = A$ $A + (AB) = A$ $A \cdot \bar{A} = 0$ $A + \bar{A} = 1$ $A \oplus \bar{A} = 1$ $\bar{A} = A$
- $A \cdot (B+C) = (A \cdot B) + (A \cdot C)$ $A + (B \cdot C) = (A + B) \cdot (A + C)$ $A \cdot (B \oplus C) = (A \cdot B) \oplus (A \cdot C)$ $A \oplus (B \otimes C) = (A \oplus B) \otimes (A \oplus C)$

Karnaugh groups: 2^m minterms/maxterms → m variables don't care (Symmetry) (E)
Var E is don't care when 2^{m-1} minterms/maxterms where E=1 and 2^{m-1} where E=0
Var. E influences when all 2^m minterms/maxterms are where E=1 or where E=0

Circuits: SR-Latch, D-Latch, D-Flip-Flop

R S	Q	R S	Q	E Q	D	C Q	D
0 0	Q	0 0	Q	1 D	0 a	1 D	0 a
1 1	Q	0 1	Q	0 1	1 Q	0 1	0 Q
1 0	Q	1 0	Q	1 0	0 Q	1 0	0 Q
0 1	Q	0 1	Q	0 1	0 Q	0 1	0 Q

Data 0 Store 0 Data 0 Clock 0

Operations: $111_2 + 101_2 = 1000_2$, carry Adder $768_{10} + 2145_{10} = 2913_{10}$, borrow Subtract $111_2 - 101_2 = 100_2$

Div.: $1011_2 / 101_2 = 10_2$, Overflow 1, Mult. $0101_2 \times 111_2 = 0101_2$, Underflow 1, negative result Overflow 1111

Representations: nibble: 4 bits, byte: 8 bits, MSB...LSB, encoding: thermometer: 00011111_b, one-hot: 00100000_b, 5 decimal: 00000001_b, 0 decimal: 00000000_b, binary $[0, 2^k - 1]$

Sign & Magnitude: 00b+0, invert 00b+0 add 2 numbers -MSB 00b+0, one's comp. 11b+0 and + carry, two's comp. 1011b-5, excess N 01b-N, Fixed point 11.01 3,25

CT: code table to binary State → Code, TT: State → Code, maps current outputs + inputs to new outputs, OT: Output Table, output IRL

FSM: CT + TT: Medvedev + OT: Moore, + to output logic: Mealy

encoding n states: $\lceil \log_2(n) \rceil$ bits, unused codes: ghost states, CMOS: Complementary metal oxide Semiconductor

None Ideal behavior: TTL: transistor to transistor logic, Hazards: gates have delay ⇒ don't work, D signal must be stable during t_{setup} → Metastability or 1

Programmable Logic: ASIC: Application Specific Integrated Circuit, PAL: Programmable Array Logic, OTP: one-time programmable, GAL: Generic Array Logic

CPLD: Complex Programmable Logic Device, IOB: Input Output Block, FPGA: Field Programmable Gate Array, LUT: Look up Table, P&R software → bit-file, RAM: random access memory, SOC: System on chip

VHDL: case-insensitive, comments --, Entity: black-box, Architecture: functionality, std_logic: a bit, std_logic_vector(n-1 DOWNTO 0): n bits vector, bit value E '0' '1' 'U' 'X' '-'

RTL: register transfer level: from combinational logic - connect with wires, Gates: AND NAND OR NOR NOT XOR XNOR, Sensitivity: signals on the right of <= sensitivity list (should put all),

CONSTANT: undefined → unknown (short circuit), don't care → explicit

VHDL

```

library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;

entity entity_name is
    generic(k: unsigned;
            L: std_logic := '0'); -- default MSB      LSB
    port(clock, reset: in std_logic;           -- (n-1) downto 0
          Y: out std_logic_vector(0 to 7)); -- 0      to (n-1)
                                         LSB      MSB
end entity_name;

architecture arch_name of entity_name is
    -- Declaration
    type state is (IDLE, UPDATE, DONE); -- local to arch
    -- hex X"EF", bin: "11101111", macro: (y =>'0', others =>'1')
    signal s_Y_data: std_logic_vector(7 downto 0) := "00000000"; -- default value
    signal s_A, s_B, s_C: std_logic;
    signal s_D, s_E: unsigned(5 downto 0);
    constant c_PI: std_logic := '1';

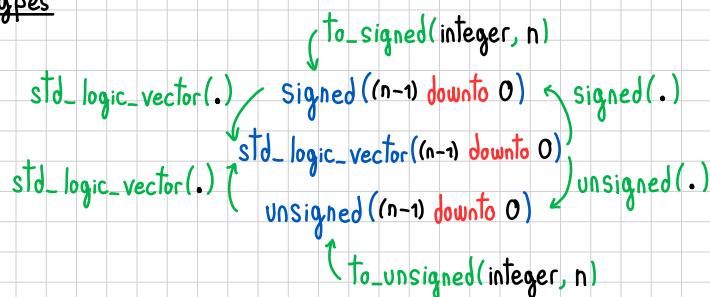
    component component_entity is
        generic(c0: integer;
                P: std_logic_vector(2 downto 0));
        port(A, B: in std_logic;
              Y: out std_logic);
    end component;

```

Help

Decimal	Bin	Hex
0	0000	0
1	0001	1
2	0010	2
3	0011	3
4	0100	4
5	0101	5
6	0110	6
7	0111	7
8	1000	8
9	1001	9
10	1010	A
11	1011	B
12	1100	C
13	1101	D
14	1110	E
15	1111	F

Types



```

begin
    -- Description (don't read from output!)
    -- Implicit process
    Y <= (s_Y_data(0) or (s_Y_data(2) and (not s_Y_data(3)))) & s_Y_data(6 downto 0);
    s_B <= c_PI when s_Y_data(5)='1' else '-' when s_Y_data(6)=L else '0';
    with s_Y_data(4) select s_D <= -- puts value in s_D
        to_unsigned(0,6) when s_Y_data(0), -- tests data[4]=data[0]
        to_unsigned(1,6) when s_Y_data(2),
        to_unsigned(2,6) when others;
    -- Explicit process (latest assign matters/don't assign both in implicit and explicit)
    p-process_name: process(reset, clock, s_Y_data(1)) is
        begin
            -- D-FlipFlop
            -- Async reset
            if reset='1' then s_A <= '0'; -- reset value
            elsif rising_edge(clock) then s_A <= s_B, -- Falling-edge(clock)
            end if;
            -- Sync reset
            if rising_edge(clock) then
                if reset='1' then s_A <= '0';
                else s_A <= s_B xor s_A; -- Allowed read and write to signal
                end if;
            end if;
            case s_Y_data(1) is
                when s_Y_data(0) => -- can use if/else here
                    s_E <= to_unsigned(0,6),
                    s_A <= '0',
                when s_Y_data(2) => s_E <= to_unsigned(1,6);
                when others => s_E <= k;
            end case;
        end process p-process_name;
    pm-do. component_entity
        generic map(O=>g,
                    P=>"001");
        port map(A=>s_A, B=>s_B, Y=>s_C);
    end arch_name;

```