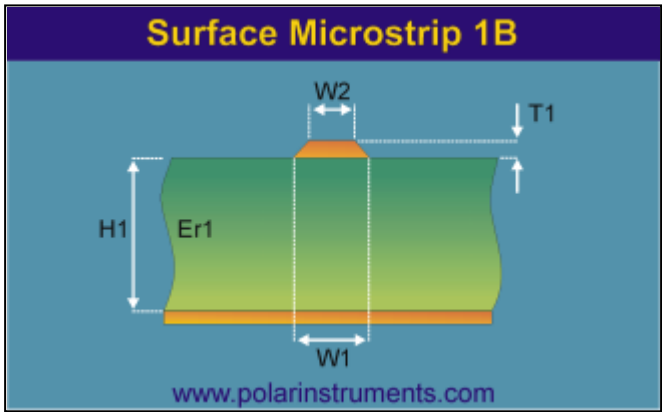
Polar Si9000 PCB Transmission Line Field Solver



				Tolerance	Minimum	Maximum
Substrate 1 Height	H1	13.0000	+/-	0.0000	13.0000	13.0000
Substrate 1 Dielectric	Er1	4.2000	+/-	0.0000	4.2000	4.2000
Lower Trace Width	W1	23.5000	+/-	0.0000	23.5000	23.5000
Upper Trace Width	W2	23.5000	+/-	0.0000	23.5000	23.5000
Trace Thickness	T1	2.3500	+/-	0.0000	2.3500	2.3500
Impedance	Zo	50.23		------	50.23	50.23
Delay (ps/in)	D	148.398		------	148.398	148.398
Inductance (nH/in)	L	7.454		------	7.454	7.454
Capacitance (pF/in)	C	2.954		------	2.954	2.954

Notes: (First 5 lines will print)

[1] 吴川斌的博客. PCB叠层设计及阻抗计算[M].
第2.1节