journal

J. Am. Ceram. Soc., 74 [11] 2739-46 (1991)

Degradation of Multilayer Ceramic Capacitors with Nickel Electrodes

Shigekazu Sumita,* Masaaki Ikeda, Yukie Nakano, Kousuke Nishiyama, and Takeshi Nomura*

Materials Research Center, TDK Corporation, Narita 286, Japan

The mechanism of degradation, or *IR* drop, of $BaTiO_3$-based Ni-electrode chip capacitors has been studied, with special attention to the microstructure. Degradation occurred mainly at the center of the capacitors. Longer-life capacitors were obtained under conditions of low oxygen partial pressure, 10^{-12} atm, during sintering, and had larger grain sizes and smaller quantities of grain boundary phase. The existence of oxygen vacancies in the grain boundary phase was confirmed by cathode luminescence measurement. Double layers along the surfaces of the Ni electrodes were also related to the life of the capacitors. [Key words: multilayer capacitor, nickel, electrodes, degradation, microstructure.]

I. Introduction

MULTILAYER ceramic chip capacitors have been profoundly important surface mount devices (SMDs) in several areas of electronics such as personal computers, automobiles, VCRs, TVs, radios, watches, and communication networks. Currently, reduction of production costs is required for wider applications of capacitors with high reliability. However, precious metals such as platinum, palladium, silver, and their alloys are still used as interleaved electrodes that make up a large part of the production costs of capacitors. Under such circumstances, replacing those precious metals with a base metal like nickel has been attempted;[1,2] in fact, Ni-electrode chip capacitors are increasingly being produced. However, the Ni electrode is easily oxidized during the firing process. Consequently, low oxygen partial pressure (P_{O_2}) during firing is indispensable.[3,4] A reducing atmosphere may cause the formation of oxygen vacancies in the ceramic bodies of capacitors. For that reason, in this experiment, annealing as the sequential process of sintering was carried out in order to reoxidize the ceramic bodies. Nevertheless, Ni-electrode chip capacitors still have the weakness of short life spans; in other words, degradation occurs quickly. The definition of degradation is an *IR* drop of the capacitors from 10^{12}–10^{13} to 10^5–10^7 $\Omega \cdot$cm under the accelerating conditions of 200°C–200 VDC or 4 times the rated voltage of each capacitor. The goal of this study, therefore, was to elucidate the degradation mechanism and related phenomena of Ni-electrode multilayer chip capacitors in order to prolong their lives.

II. Experimental Procedure

A cross section of a multilayer chip capacitor is shown in Fig. 1. The monolithic chip capacitors investigated in this set of experiments were C3216-Y5V type with interleaved Ni electrodes. The mother ceramic material was perovskite structure (ABO_3) $BaTiO_3$-based dielectric whose chemical formula had an A-site rich nonstoichiometry of $(Ba_{1-x}Ca_x)_m(Ti_{1-y}Zr_y)O_3$ ($1.000 < m < 1.005$) with additives of SiO_2 and MnO. Calcium oxide was partially substituted for BaO to maintain the resistance of the capacitors under the essential condition of low oxygen partial pressure (P_{O_2}) during sintering[5–7] to avoid oxidation of the Ni electrodes. Barium zirconate was used for reducing the Curie temperature from around 120°C to room temperature. Silicon oxide was used as a sintering aid and the role of manganese oxide was to lengthen the life of the capacitors.[8–10]

(1) Degraded Layer of Chip Capacitors

Each chip capacitor, which has a dielectric thickness of 27 μm, was fixed with epoxy resin. One end of the capacitor (end terminal: vertical direction of interleaved electrodes) was polished with diamond paste with a final diameter of 0.25 μm to reveal the cross section of the capacitor. The other end was bonded to a conductive wire connected to an ohmmeter. The resistance of all the layers of each capacitor was measured by using an extremely sharp needle which also was connected to the ohmmeter. While observing each specimen under an optical microscope, we measured the resistance of each layer by touching the tip of the probe needle, to all of the Ni electrodes one by one. The resistance of the individual electrodes was not measured since it was extremely difficult to polish both ends of the chip capacitors and to measure the resistance by controlling two needles under the optical microscope. However, measuring the resistance of the dielectric layers was accomplished by one-needle measurement in the system.

(2) Effects of Oxygen Partial Pressure

Chip capacitors were put onto a ZrO_2 setter which was then inserted into an electric tube furnace. The oxygen partial pressure was controlled by the equilibrium of H_2 and H_2O; i.e., the water vapor pressure was adjusted by bubbling a hydrogen/nitrogen mixture through water at a controlled tem-

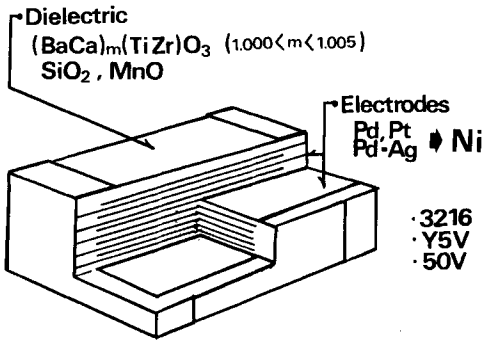

Fig. 1. Cross section of a ceramic multilayer chip capacitor.

W. A. Schulze—contributing editor

Manuscript No. 197398. Received August 2, 1990; approved July 24, 1991.
Presented at the 92nd Annual Meeting of the American Ceramic Society, Dallas, TX, April 23, 1990 (Symposium on Dielectric and Capacitor Composition II, Paper No. 35-E-90).
*Member, American Ceramic Society.

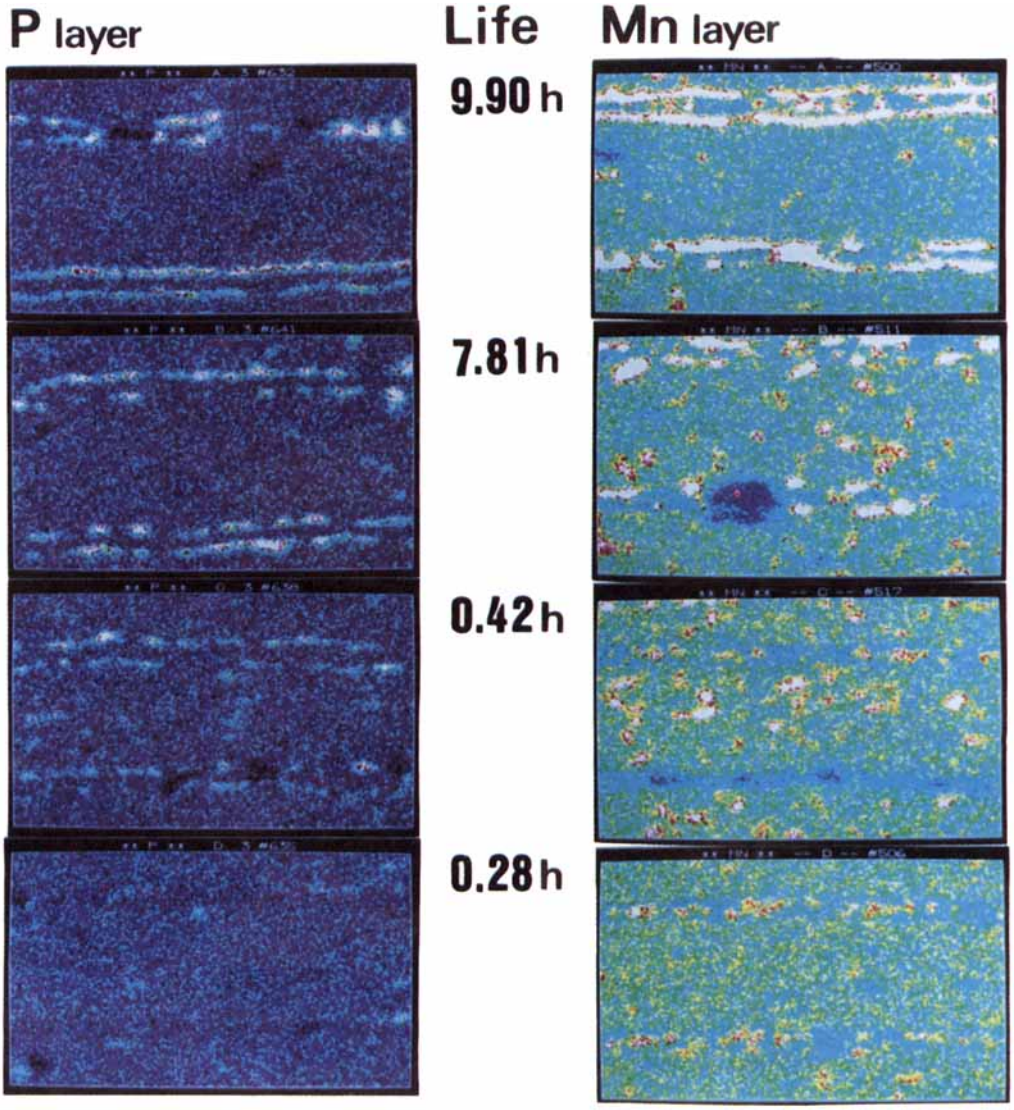

Plate 1. Relation among Mn layer, P layer, and the life of the chip capacitor.

perature. Binder burnout was carried out at 800°C for 2 h and the conditions for sintering and annealing were 1340° and 1000°C, respectively, both for 2 h. After the firing process, liquid In–Ga was painted on both end terminals of each capacitor in order to achieve ohmic contact. Conditions of 200°C–200 VDC were applied to each capacitor to conduct a high-temperature, highly accelerated life test (HALT). The temperature of 200°C was more severe than the general HALT temperature of 140°C. At least three capacitors, which had been processed under exactly the same firing schedule, were tested.

(3) Microstructure of Dielectric

The capacitor was polished with 0.25-μm-diamond paste and then chemically etched with HCl + HF solution to reveal the grains. Carbon deposition or gold sputtering was applied on the surface of the samples for microstructural observation by scanning electron microscope (SEM: Hitachi S-800). Then the area of the grain boundary phase (GBP) was quantitatively evaluated by using an image processor (Nikon LUSEX IID). SEM micro-observation, particularly along the surfaces of the Ni electrodes, was carried out to study the formation of double layers, and the relationship to the lives of the capacitors.

(4) Oxygen Vacancy in the Grain Boundary Phase

Sample preparation was the same as in the previous section. Cathode luminescence (CL) images were observed at exactly the same microarea of the secondary electron image of the dielectric by CL attached SEM (Shimadzu EMX-SM7).

(5) Corona Current

The end terminals of Ni-electrode, Pd-electrode, and metallized-polypropylene capacitors (film capacitors) were fixed with conductive wires and then were settled into inert solution (3M Fluorinert) in order to measure the electrical corona of each capacitor. The measuring voltage was swept from 0 to 130 VAC.

(6) Quantitative Analysis of the Grain Boundary Phase

The quantitative analysis of the GBP composition was carried out by means of a scanning transmission electron microscope (STEM) with an energy dispersion X-ray (EDX) spectrometer. The diameter of the electron beam was approximately 30 nm. The peak separation of overlapped spectra of Ba and Ti emission lines, for example, was carried out by the best-fit method for the combination of BaO and TiO_2 standard spectra.

III. Results and Discussion

(1) Degraded Layer of Chip Capacitors

Some papers have referred to the degradation of chip capacitors;[11–15] however, no report has discussed the degraded zone, or the degraded layer, of multilayer ceramic capacitors. Our first task was to answer the question of whether degradation occurred at one zone of the capacitor or at random. In order to determine the degraded area, the resistance of all of the layers of each capacitor was measured. The distribution of degraded layers of the capacitors is shown in Fig. 2. The "X" marks indicate degraded layers. When the needle is in contact with electrode 6, for example, both layers between electrodes 5 and 6, and electrodes 6 and 7, are measured. Thus, X's are marked on both layers. It must also be noted that electrodes 6 and 12, for example, are equivalent because of the symmetry of the capacitor. A couple of significant conclusions can be made: (1) Degradation occurred in one layer of each chip capacitor. (2) Degradation occurred mainly at the center of the capacitors.

Only one layer of each capacitor showed the lowest resistance of around 10^5 to 10^7 Ω·cm; other layers maintained a high resistance of 10^{12} to 10^{13} Ω·cm. It is thus believed that

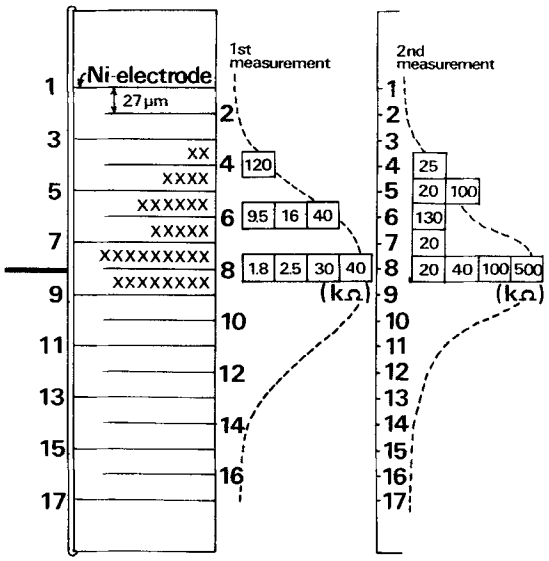

Fig. 2. Distribution of degraded part in chip capacitors with interleaved Ni electrodes. (Note: the vertical direction of the chip capacitor is exaggerated to show "X" marks in degraded layers.)

the degraded layer, or central area of each capacitor, was not adequately reoxidized during annealing. In this experiment, the resistance of Ni electrodes, which are indicated by odd numbers in Fig. 2, was less than 10^{-1} Ω·cm; the equivalent series resistance (ESR) showed no resistance change during the degradation. Furthermore, the small resistance value of less than 10^{-1} Ω·cm was negligible for the degradation measurement. Result 1 agreed with expectations because it was not difficult to suppose that the weakest layer would be preferentially degraded. After the main path of electrical conduction was established in one degraded layer, other layers had little chance of secondary degradation.

As shown in Fig. 2, degradation occurred primarily near the center layer but not in outer layers. This is a significant result which suggests that the oxygen partial pressure during sintering and annealing affected the position of the degraded layer since the surface of the chip capacitors was directly influenced by the atmosphere during firing. Therefore, studying the relation between the life of the capacitors and the firing process is of prime importance.

The applied condition of 200°C was higher than that of the general HALT condition of 140°C. In order to enlarge the accelerating coefficient, however, a higher temperature of 200°C was intentionally applied. The best condition of HALT is still under consideration. Thus high-temperature HALT will be discussed in a future paper.

(2) Effect of Oxygen Partial Pressure

Figure 3(A) shows the effects of oxygen partial pressure (P_{O_2}) on binder burnout and of sintering on the life of the capacitors. The life was extended by decreasing the water temperature, in other words, by decreasing P_{O_2} during sintering. As for the binder burnout, the life also was extended, but by increasing the water temperature or increasing P_{O_2}. The concentration of the residual carbon after 800°C binder burnout was nearly 250 ppm. This is a fairly small value compared with 500 to 600 ppm residual carbon after 500° to 600°C binder burnout in air. Thus, the life of the capacitors clearly depended on the P_{O_2} during binder burnout and during sintering, but in opposite manners. Presumably, the binder decomposed sufficiently at relatively higher P_{O_2} and Ni electrodes were less oxidized under the low P_{O_2} or around 10^{-12} atm.

The life of the capacitor as a function of annealing time is shown in Fig. 3(B). An annealing temperature of 1000°C was selected under the same water temperature of each sintering condition. When the annealing temperature was high (1200°C), the oxidation of Ni electrodes was remarkable;

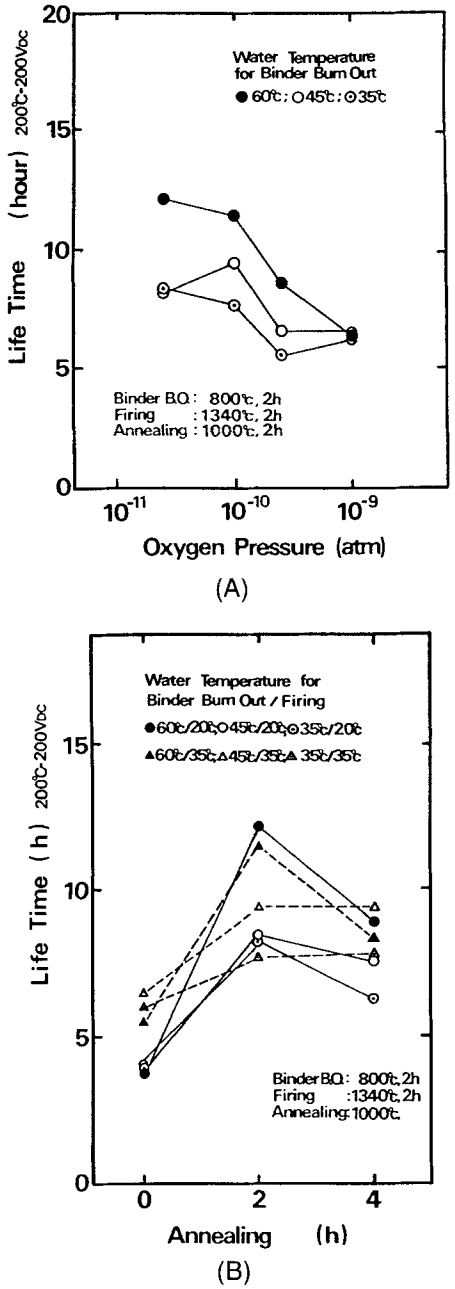

Fig. 3. Effects of (A) the oxygen partial pressure during sintering, and (B) the annealing time, on the life of the chip capacitor.

when a low annealing temperature of 800°C was applied, the ceramic body was not adequately reoxidized. Therefore, an effective annealing temperature between 900° and 1100°C must have been used. The lives of six kinds of chip capacitors that had different histories of binder burnout and sintering showed a common tendency; 2 h of annealing significantly enhanced the lives of the capacitors, but excess annealing showed no effect or reduced the life.

We conclude that oxygen vacancies form in the ceramic dielectric under the severe condition of low P_{O_2} which is disadvantageous to the life of the capacitors,[16,17] although it is advantageous to prevent the oxidation of Ni electrodes. The life of the capacitor is enhanced by compensatory oxygen to the vacancy for a suitable annealing time of 2 h at 1000°C; excess annealing probably causes oxidation of Ni electrodes while reducing the life.

(3) Microstructure of Dielectric

In order to study the difference between a long-life chip capacitor and a short-life one, the microstructures of polished and chemically etched surfaces of the capacitors were observed by SEM as shown in Fig. 4. All of the green chips had the same dielectric thickness because the chips were cut from the same multilayer green sheet. However, the dielectric thickness of the polished surfaces in Fig. 4 was not the same since the chips were intentionally leaning in the epoxy resin for creating an expanded view of the area between electrodes.

The most noticeable difference was the grain size of the dielectric bodies. The long-life chip capacitor, which was obtained at a lower P_{O_2} of 10^{-12} atm, had a large grain size. On the other hand, the short-life chip capacitor sintered at 10^{-9} atm had a small grain size. Observing hundreds of SEM photomicrographs, it was confirmed that the difference of the grain size was remarkably related to the oxygen partial pressure. The SEMs revealed another significant difference in the area of the GBP. Figure 5 shows differences in GBPs; the

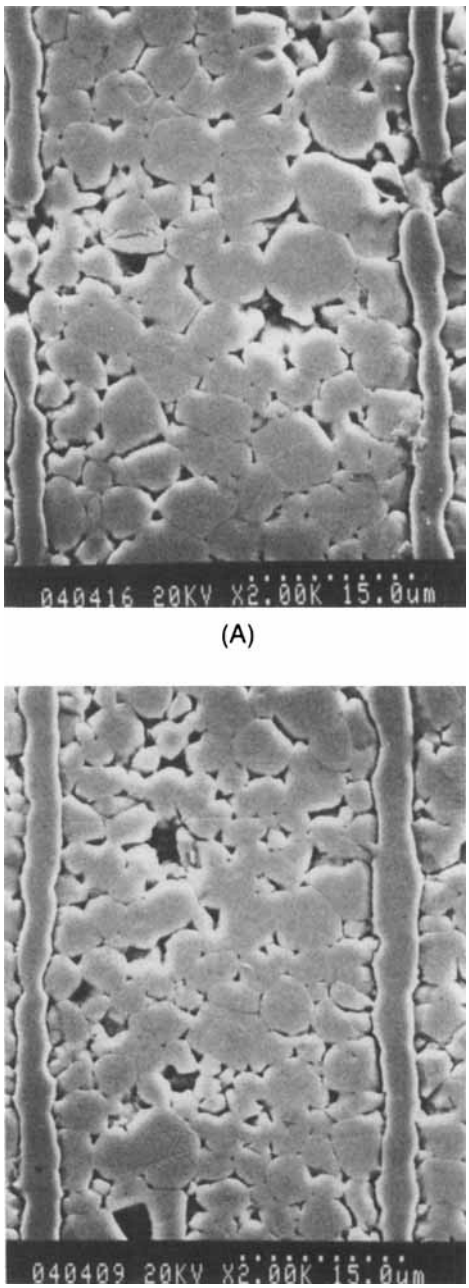

Fig. 4. SEM photomicrographs of polished and chemically etched surfaces of chip capacitors: (A) long life: 12.2 h, and (B) short life: 4.0 h, under the accelerating conditions of 200°C–200 VDC.

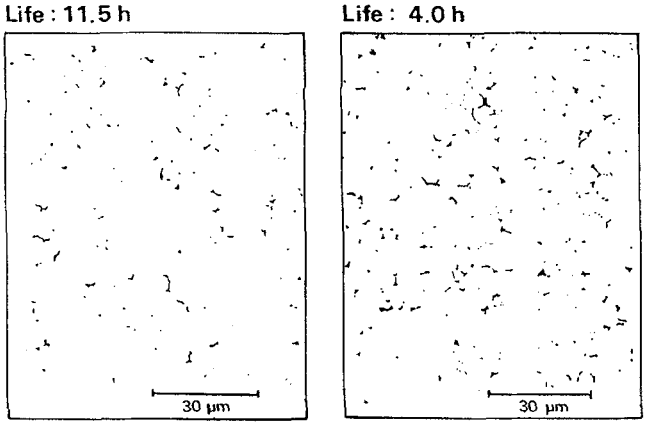

Fig. 5. Comparison of the area of grain boundary phase in the polished surfaces of the dielectric with the life of the capacitors.

number and quantity of GBPs in the long-life chip capacitor were smaller than in the short-life one. At the same time, the grain boundary surface area per unit volume of the microstructure decreased as the grain size increased. It was, therefore, concluded that as the P_{O_2} during sintering was reduced, the area of the GBP became smaller and the life of the capacitor grew longer. In other words, the GBP was isolated by the grain growth and the number and the size of GBP precipitates were reduced under the conditions of lower P_{O_2}.

As shown in Fig. 6, the life of the capacitor is given as a function of the quantity of GBP in the dielectric. The GBP is presumably the main path of electrical conduction. That is why as the path (GBP) became narrower, the life of the capacitor became longer. For the prolongation of the life, therefore, it is necessary to minimize the GBP under conditions of a low P_{O_2} of 10^{-12} atm and to isolate the GBP by grain growth of the dielectric ceramic.

(4) Oxygen Vacancy in the Grain Boundary Phase

In the previous sections, the influence of the quantity of GBP on the life of the capacitor was emphasized, suggesting the vital role of oxygen vacancies in the degradation mechanism. In fact, oxygen diffusion is often enhanced in grain boundaries since oxygen vacancies are largely implicated in the degradation behavior of barium titanate, especially in oxygen-deficient materials.[3,8,16,17] It is the purpose of this section to distinguish the properties of the GBP from those of grains in terms of the number of oxygen vacancies.

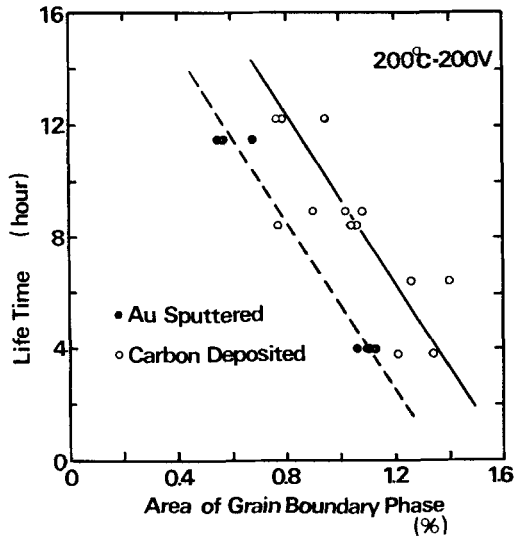

Fig. 6. Life of chip capacitor as a function of quantity of grain boundary phase.

SEM and CL photomicrographs of the same microarea of a $BaTiO_3$-based dielectric are shown in Fig. 7. It is remarkable that CL radiation was observed at the GBP and pores, although grains did not give off any radiation. A model of the radiative recombination process in $BaTiO_3$ as revealed by spectral CL measurement was presented by Koschek and Kubalek[18] as shown in Fig. 8. The binding energy levels of oxygen and barium vacancies exist between those of conduction and valence bands. The emission energies that are the origins of CL radiation are 2.6, 2.3, and 2.1 eV. On the other hand, CL spectra consisting of three peaks were observed in this experiment (Fig. 8(B)). The energy unit of those wavelengths was converted to electronvolts; the values of 475 nm (2.6 eV), 540 nm (2.3 eV), and 590 nm (2.1 eV) showed good

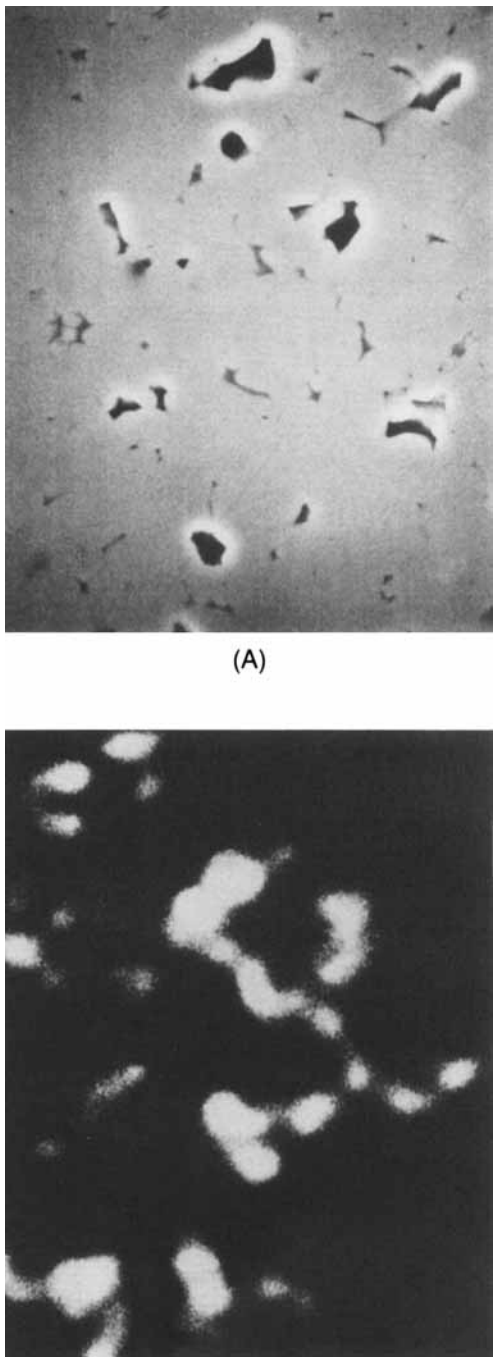

Fig. 7. (A) SEM and (B) cathode luminescence (CL) micrographs of dielectric.

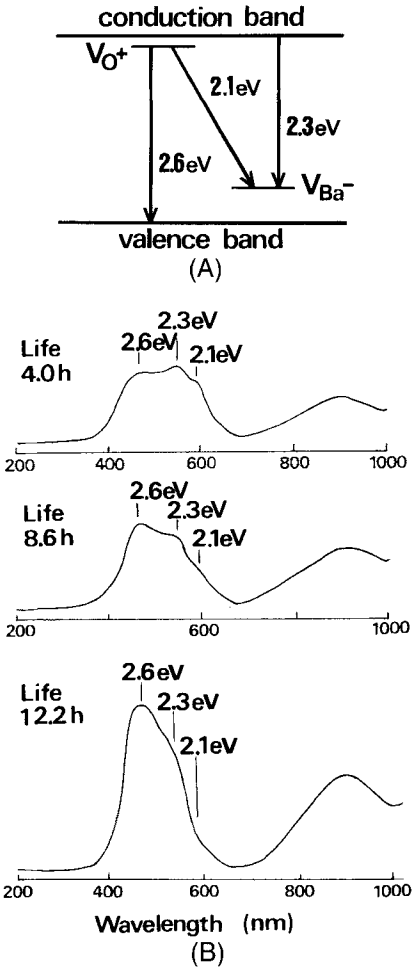

Fig. 8. (A) Radiation recombination process in $BaTiO_3$, as revealed by spectral CL measurement (Koschek and Kubalek, *J. Am. Ceram. Soc.*, **68**, 582–86 (1985)). (B) CL spectra of this experiment. (Note: The vertical scale of the bottom datum is twice as large as that of the top and middle data.)

agreement with the model. The result of CL measurement consequently supported the conclusion that oxygen and barium vacancies formed in the GBP but not in grains of $BaTiO_3$-based dielectric. It was also found that CL radiation was not observed near the surface of the capacitors. This phenomenon indicates that oxygen fills in the vacancies during annealing from the surface to the center of the capacitors.

Another interesting feature was that as the life of the capacitor became shorter, the emission intensities of 2.3 and 2.1 eV became stronger, as shown in Fig. 8(B). It seemed that the formation of barium vacancies slightly took priority over that of oxygen vacancies in the GBP of the short-life capacitor. No reasonable explanation for this phenomenon, however, is offered at this point.

Figure 9 compares the CL radiation with the life of the capacitors. A Pd electrode capacitor which had been fired in an air atmosphere and had an extremely long life of more than 100 h under the accelerating conditions of 200°C–200 VDC did not show any CL radiation. On the other hand, Ni electrode capacitors fired at a low P_{O_2} of 10^{-10} atm showed CL radiation here and there from the GBP; an enormous number of radiating areas were observed in the dielectric of the shortest-life capacitors among the three specimens. This result is proof that oxygen vacancies in the GBP formed when low P_{O_2} was used for sintering. The interesting point was that the rate of radiation from the GBP also related to the life of the capacitors. Therefore, the CL measurement supports the significant fact that vacancies in the GBP markedly affect the life of capacitors whether noble metal or base metal is used for the interleaved electrodes.

(5) Quantitative Analysis of Grain Boundary Phase

Table I gives the results of STEM microanalysis of GBP. It cannot be denied that the A/B analytical values of 11.17 at 10^{-12} atm and 6.39 at 10^{-8} atm are significant, since the difference was reproducible ($n = 4$ and 7, respectively), although the spatial resolution of EDX chemical analysis was not highly accurate. The first important point was the change of Ni concentration in the GBP. The longer-life chip capacitor had lower Ni concentration. Thus migration or diffusion of Ni from the electrodes tended to occur mainly at higher oxygen partial pressure. The second point was the change in the A/B ratio of the ABO_3 perovskite structure. In this case, A-site elements were Ba and Ca; B-site elements were Ti and Zr. The longer-life chip capacitor had a larger A/B value in the GBP. Even as SiO_2 was added to the B-site elements, the tendency of the A/B value was the same. Therefore, the Ni concentration and the A/B ratio in the GBP are also of prime importance.

(6) Corona Current

Figure 10 shows Lissajous figures of corona current at 130 VAC. The palladium-electrode chip capacitor and metal-

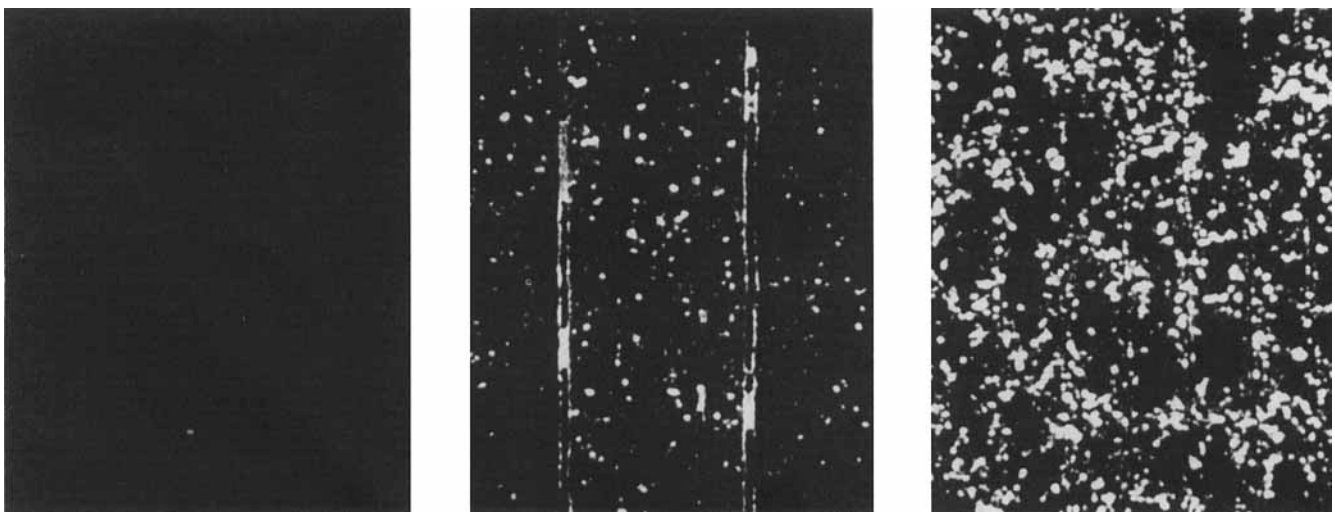

Fig. 9. Cathode luminescence image of multilayer chip capacitors: (A) Pd electrode, fired in air, extremely long life; (B) Ni electrode, fired in low P_{O_2}, long life with 0.25 wt% MnO; and (C) Ni electrode, fired in low P_{O_2}, short life with 0.15 wt% MnO.

Table I. STEM Quantitative Microanalysis of Grain Boundary Phase

P_{O_2} (atm)	Life	n	Composition (wt%)									A/B
			Ba	Ti	Ca	Al	Si	Zr	Mn	Ni	P	
10^{-12}	Long	4	40.7	1.26	0.05	12.0	13.4	0.03	0.43	0.09	0.10	11.17
10^{-10}	Mid	7	44.0	1.44	0.13	10.9	12.5	0.09	0.29	0.13	0.12	10.41
10^{-8}	Short	7	40.9	2.07	0.23	11.5	12.8	0.39	0.42	0.19	0.00	6.39

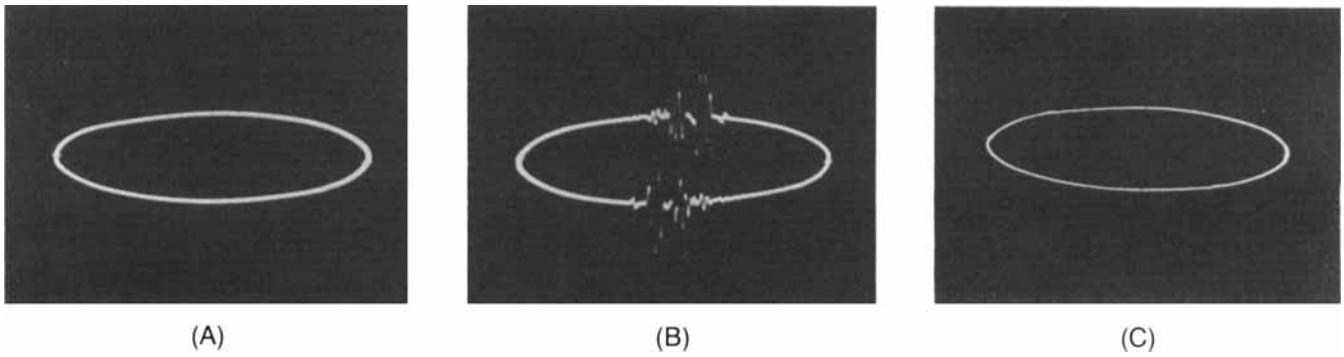

Fig. 10. Lissajous figures of corona current: (A) Pd-electrode chip capacitor, (B) Ni-electrode chip capacitor, and (C) metallized polypropylene capacitor. Note: Horizontal and vertical directions of the Lissajous show ac voltage and current, respectively.

lized polypropylene capacitor (film capacitor) showed perfect rings; this means that corona currents did not occur in those capacitors. On the other hand, however, electric corona was observed in Ni-electrode chip capacitors, showing an indentation in the Lissajous ring; i.e., the corona current was a characteristic phenomenon of the Ni-electrode chip capacitors with exceedingly good reproducibility. In general, an electric corona was observed through the medium of air between a needle electrode and a flat one.[19] Therefore, pore size in the dielectric is probably one of the most important factors indicating the electric corona. In fact, the ceramic body of Ni-electrode capacitors had big pores, as shown in Figs. 4 and 7. Cathode luminescence was characteristic of not only the GBP but also some pores in the Ni-electrode chip capacitor. At this stage, however, the relation between the corona current and the life of the capacitor is not explained clearly.

(7) Layer Structure on the Surface of Ni Electrodes

As shown in Fig. 11, segregated layers were found, after the sintering process, along the surface of interleaved Ni electrodes when the P_{O_2} during sintering was less than 10^{-12} atm. The microstructural analysis by STEM proved that the nearest layer of the Ni electrode was a Ba-rich layer which contained Ba and P; the next nearest layer of the electrode was a Ti-rich layer whose constituent elements were Ti, Mn, Fe, and Ni, although quantitative values of the constituent elements of the layers were not analyzed. The formation mechanism of the layer structure is not explained at this stage. It is, however, confirmed that the double layer was found only in the long-life capacitors that had been sintered at low P_{O_2} of less than 10^{-11} atm.

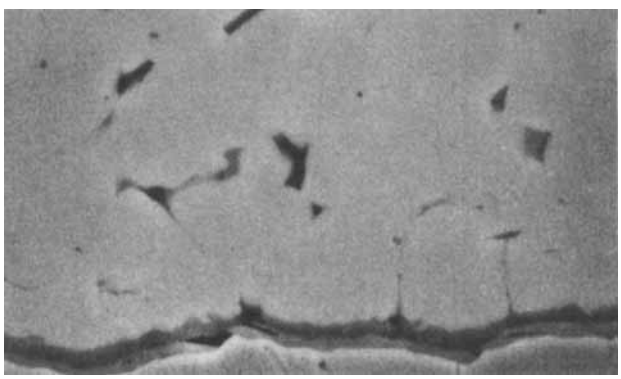

Fig. 11. SEM photomicrograph of a segregation layer along the surface of Ni electrode.

The thickness of the each layer was about 0.5 μm but depended on its position in the chip capacitor; near the center of the capacitor, in general, the layer was thinner of faded out. This result indicates that degradation occurred mainly at the center of the capacitors. Therefore, the existence of the double layer is also one of the predominant factors in the prolongation of the life of the capacitors.

Plate 1 shows the effect of the presence of Mn layers and P layers on the life of the chip capacitor. The concentration of Mn additive in the dielectric was ca. 2000 ppm and that of P impurity was 240 ppm detected by ICP measurement. The unknown amounts of impurities of Mn and P were also contained in the Ni paste for screen printing. Ni electrodes were sandwiched by the double layers of Mn and P. When the accelerating life was reduced from 9.9 to 7.8 h, Mn layers became thinner or faded out but P layers showed almost no change. As the life fell only 0.4 h, the Mn layers disappeared but P layers still existed. In this specimen, the existence of the Mn was detected mainly at the triple points of the grain boundaries in $BaTiO_3$ dielectric. Eventually, the P layers also diminished at a life of less than 0.3 h. This result led to the conclusion that the life of the capacitors is related to the existence of Mn layers. Formation of the layers along the surface of Ni electrodes is essential for maintaining the long life of the capacitors.

IV. Conclusions

The degradation mechanism of multilayer chip capacitors with interleaved Ni electrodes has been studied.

(1) Degradation occurs in one layer of each chip capacitor. Degradation occurs mainly at the center of the capacitor.

(2) A long-life chip capacitor is produced under conditions of a low oxygen pressure of 10^{-12} atm during sintering. The longer-life chip capacitor has a larger grain size and has a smaller quantity of grain boundary phase.

(3) The grain boundary phase, with the presence of oxygen vacancies confirmed by cathode luminescence measurement, is probably the main path of electrical conduction. Presumably, the Ni migrates from the interleaved electrodes.

(4) An electrical corona is a characteristic phenomenon of Ni-electrode chip capacitors since big pores exist in the

dielectric. However, the relation between corona current and the life of the capacitor cannot be clearly explained.

(5) Segregation layers are observed along the surface of interleaved electrodes in long-life chip capacitors. Near the center of the capacitors, the double layers become thinner or fade out. Mn layers are strongly related to the life of the chip capacitors.

(6) Formation of oxygen vacancies in grain boundary phases is the key to elucidate the degradation mechanism of Ni electrodes in multilayer ceramic chip capacitors.

Acknowledgments: We thank J. Iteguchi and S. Itoh for their helpful comments. We gratefully acknowledge the microstructural analysis by A. Nakata, Y. Izumi, and Y. Taguchi.

References

[1]J. M. Herbert, "High-Permittivity Ceramics Sintered in Hydrogen," *Trans. Br. Ceram. Soc.*, **62** [8] 645–58 (1963).

[2]J. M. Herbert, "Thin Ceramic Dielectrics Combined with Nickel Electrodes," *Proc. IEEE*, **112** [7] 1474–77 (1965).

[3]I. Burn and G. H. Maher, "High Resistivity $BaTiO_3$ Ceramics Sintered in CO–CO_2 Atmospheres," *J. Mater. Sci.*, **10**, 633–40 (1975).

[4]H.-J. Hagemann, "Electrical Properties of Acceptor-Doped $BaTiO_3$ Ceramic," *Ber. Dtsch. Keram. Ges.*, **55** [7] 353–55 (1978).

[5]Y. Sakabe, "Dielectric Materials for Base-Metal Multilayer Ceramic Capacitors," *Am. Ceram. Soc. Bull.*, **66** [9] 1338–41 (1987).

[6]Y. H. Han, J. B. Appleby, and D. M. Smyth, "Calcium as an Acceptor Impurity in $BaTiO_3$," *J. Am. Ceram. Soc.*, **70** [2] 96–100 (1987).

[7]X. W. Zhang, Y. H. Han, M. Lal, and D. M. Smyth, "Defect Chemistry of $BaTiO_3$ with Addition of $CaTiO_3$," *J. Am. Ceram. Soc.*, **70** [2] 100–103 (1987).

[8]J. Rodel and G. Tomandl, "Degradation of Mn-Doped $BaTiO_3$ Ceramic under a High D. C. Electric Field," *J. Mater. Sci.*, **19**, 3515–23 (1984).

[9]I. Burn, "Mn-Doped Polycrystalline $BaTiO_3$," *J. Mater. Sci.*, **14**, 2454–58 (1979).

[10]J. Iteguchi, "Ceramic Dielectric Material," Jpn. Pat. No. 109104, 1985.

[11]H.Y. Lee and L. C. Burton, "Charge Carriers and Time Dependent Currents in $BaTiO_3$-Based Ceramic," *IEEE Trans. Components, Hybrids, Manuf. Technol.*, **CHMT-9** [4] 469–74 (1986).

[12]K. Lehovec and G. A. Shirn, "Conductivity Injection and Extraction in Polycrystalline Barium Titanate," *J. Appl. Phys.*, **33** [6] 2036–44 (1962).

[13]U. Bast, G. Tomandl, and L. Hanke, "The Influence of the Ti-Rich Secondary Phase $Ba_6Ti_{17}O_{40}$ on the Reduction Behavior of Undoped Barium Titanate Ceramics," *Silic. Ind.*, **49** [9] 191–96 (1984).

[14]M. S. Dakhiya, V. A. Zakrevskii, and A. I. Slutsker, "Accumulation Processes in the Mechanism of Electrical Damage to Ceramics," *Sov. Phys — Solid State (Engl. Transl.)*, **28** [9] 1513–16 (1986).

[15]W. A. Bahn and R. E. Newnham, "Microdefect in $BaTiO_3$ Capacitors," *Mater. Res. Bull.*, **21**, 1073–82 (1986).

[16]H.-J. Hagemann and D. Hennings, "Reversible Weight Change of Acceptor-Doped $BaTiO_3$," *J. Am. Ceram. Soc.*, **64** [10] 590–94 (1981).

[17]G.V. Lewis and C. R. A. Catlow, "Defect Studies of Doped and Undoped Barium Titanate Using Computer Simulation Techniques," *J. Phys. Chem. Solids*, **47** [1] 89–97 (1986).

[18]G. Koschek and E. Kubalek, "Grain-Boundary Characteristics and Their Influence on the Electrical Resistance of Barium Titanate Ceramics," *J. Am. Ceram. Soc.*, **68** [11] 582–86 (1985).

[19]Y. Toriyama, T. Sakai, and Y. Murooka, *High Voltage Technology*; pp. 96–120. Corona Publishing Co. Ltd., Tokyo, Japan, 1980. □