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Finite Element Analysis and Design of Thermal–Mechanical Stresses in Multilayer Ceramic Capacitors

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A three-dimensional finite element model describing the thermal–mechanical stress distribution in multilayer ceramic capacitors (MLCCs) during termination firing, soldering, and bending tests is presented. Numerical results indicate that the thermal residual stresses originating from the soldering process are approximately one-fifth to half of the magnitude of the flexural stresses at the crack occurrence during the board flex test. The peak tensile stress from numerical simulations correlates with the crack initiation site observed *in situ* in board flex tests. The effects of inner electrode number, solder wicking height, lateral margin length, and the thickness of nickel in the termination component on mechanical failure during the board flex test are also investigated. Numerical results demonstrate that the maximum tensile stress could be effectively relieved by increasing the length of the lateral margin. In addition, a judicious combination of the solder wicking height and nickel termination thickness can further diminish the peak tensile stress during the board flex test. Finally, better design criteria are also developed by modifying the geometric parameters of MLCCs using Taguchi orthogonal arrays to decrease the peak tensile stresses that occur during board flex tests.

Introduction

Multilayer ceramic capacitors (MLCCs) are layered composite structures consisting of alternating layers of metal inner electrodes and dielectric ceramics sandwiched between two ceramic cover layers. Because of their high capacitance per volume and excellent high-frequency characteristics, MLCCs play important roles in a number of applications, such as telecommunications, automotive engineering, and aeronautics. During manufacturing and operation especially in automobile, however, the components of MLCCs are stressed by mechanical, thermal, and electrical loads. Therefore, multiple reliability tests including thermal shock, board flex (bending), and biased humidity tests, are typically required to ensure the reliability of MLCCs for some high end applications.

Among those reliability tests, the board flex test[1] is mainly used to evaluate the mechanical resistance of MLCCs to cracking. In the board flex test, one MLCC is first soldered onto printed circuit board (PCB) which is then subjected to three-point or four-point bending, as shown in Fig. 1. When the stress in the capacitor body exceeds the tensile strength of the dielectric ceramics, the capacitor will eventually crack, because the ceramic dielectric material is the brittlest constituent within the MLCC. The stress at which the MLCC cracks is dependent on the material properties of the constituent components (i.e., the dielectric ceramics, the metal inner electrodes, the solders, and the termination materials), the geometries of the components (i.e., the solder fillets, the widths of the housing and lateral margins (see definition of the term in Fig. 2), the thicknesses of the electrode and dielectric materials, etc.), the thermal residual stresses within the MLCC during manufacturing and soldering, and macro defects within the ceramic materials.

A complicated internal residual stress state develops during manufacturing, termination firing, and soldering processes, owing to the varying thermal contraction behavior of each of the different materials present, such

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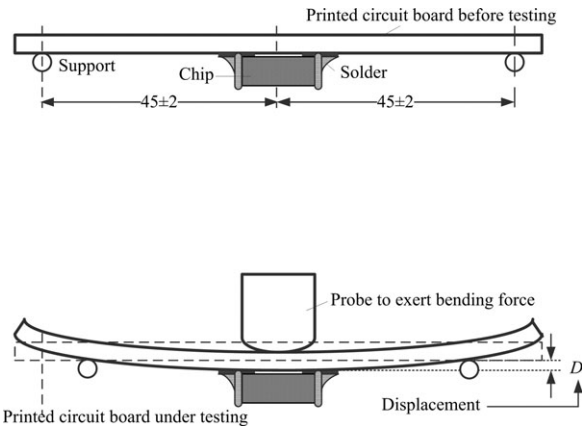

Fig. 1. Schematic drawing of the board flex test.

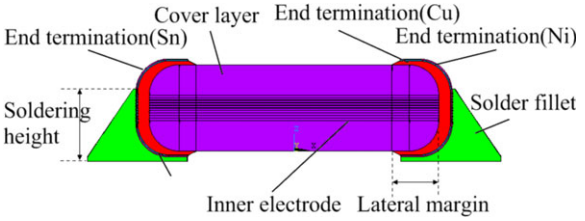

Fig. 2. Schematic structure of a multilayer ceramic capacitor (MLCC).

as the dielectric ceramic and the metal inner electrodes. As the importance of miniaturization of the MLCC chip, the number of capacitor layers must also increase and the thicknesses of the ceramic/electrode layers must decrease. The characterization of residual stresses in MLCCs has been presented in a number of studies[2–13]; however, most were primarily concerned with the residual stresses induced by the cooling process that follows sintering. Few groups have investigated the influences of the residual stresses induced by the termination firing and soldering processes, which are required to mount the MLCC onto the circuit board.[14,15] In addition to such thermal residual stresses, higher stress levels are imposed on the MLCC when a bending load is applied. Further investigation into the aforementioned stresses is therefore warranted because cracking of the MLCC depends on the resultant stress in the system.

A thorough understanding of the stress distribution in MLCC structures is essential to improve their performance and lifetime. The stresses in MLCCs can be simulated through the finite element method (FEM),[16–20] calculated by analytical models,[2,4] measured by X-ray diffraction (XRD),[7,13,16] or from sharp indentation techniques such as nanoindentation.[6,12] Compared with other techniques, the FEM provides a convenient approach to analyze detailed local stress information within MLCCs under different thermal/mechanical/electrical loadings.[3,17,18,20] This particular approach can overcome the constraints of preparing specimens with different MLCC geometries and is suitable for parametric studies of complex structures. However, previous research often used two-dimensional models or simplified three-dimensional models without actually considering details of MLCCs. To further understanding the influences of different design parameters, it is necessary to set up three-dimensional finite element models with detailed geometries.

In this study, the mechanism of stress development in MLCCs under board flex tests is investigated using three-dimensional finite element analyses (FEA). Both the thermal residual stresses caused by the soldering process and the flexural stresses resulting from bending tests are taken into account. By including detailed information regarding the active region, the termination region, and the solder materials, the proposed three-dimensional finite element models more accurately resemble actual MLCCs. A telemicroscope was used to perform *in situ* inspection of cracking when the MLCC was subjected to the board flex test. The crack initiation site was identified and compared with the stress field obtained from the finite element analysis.

Furthermore, the effects of four design parameters, including the number of metal inner electrodes, the lateral margin widths, the nickel termination thickness, and the solder wicking height, on how to diminish the peak tensile stress during the board flex test are herein discussed. The Taguchi L9 method is adopted to analyze the effects of the aforementioned four design parameters on the peak tensile stresses as well as to determine the optimal design parameters necessary to minimize the peak tensile stress in the dielectric ceramics. Numerical results are also presented to support the proposed design.

Numerical Analysis and Design

The MLCC discussed in this study consists of $BaTiO_3$-based dielectric ceramics, metal inner electrodes, and the termination structure as shown in Fig. 2. The $BaTiO_3$-based dielectric ceramics are prepared according to the Electronics Industry Association (EIA) specification X7R. The dimensions of the selected MLCC, X7R0805, are 1850 × 1150 × 550 μm. Eleven layers of nickel with thicknesses of 2 μm constitute the metal inner electrodes. The thickness of the dielectric ceramic layers is 14 μm, and the dimensions of the lateral margin, housing margin, and cover margin of the MLCC are 300, 300, and 194 μm, respectively, as specified in Fig. 2. The termination component consists of layers of

copper, nickel, and tin (from the end of the dielectric ceramic to the top surface of the MLCC) with thicknesses of 25, 6, and 6 μm in the transverse direction of the MLCC, respectively. In addition, the thicknesses of the termination layers (from the end of the dielectric ceramic to the top surface of the MLCC) in the longitudinal direction of the MLCC are 75, 6, and 6 μm, respectively. The cover length of the termination in the longitudinal direction is equal to the lateral margin.

The MLCC is soldered to the PCB at 216.9°C and subsequently cooled to room temperature. The solder material is assumed to be a wedge attached to the termination of the MLCC as shown in Fig. 2. The soldered device is then loaded for the board flex test using the displacement control method. The dimensions of the PCB are 900 × 46 × 1.6 mm, and the material properties of the PCB are assumed to be independent of temperature, with the elastic modulus and Poisson's ratio being 23 GPa and 0.25,[16] respectively. According to IPC/JEDEC standard 9702,[21] four-point bending is employed in the board flex test, as shown in Fig. 3, consisting of two concentrated loads applied at 10 mm from the middle point on each side of the PCB. In addition, two roller supports are set at 20 mm from the middle point on each side of the PCB. It is worth emphasizing that the dimensions of the MLCC and the PCB are not shown to scale in Fig. 3 because the actual dimensions of the PCB are much larger than those of the MLCC.

The deformation behavior of the dielectric and the board is assumed to be elastic, and the plastic deformation of the metals is described by a bilinear kinematic hardening law.[16] The parameters are the temperature-dependent yield stress and the tangent modulus, which is fixed in accordance with FEM practices at 10% of the temperature-dependent elastic modulus. Time-dependent deformation (creep) is neglected. The material data used for the simulations are summarized in Tables I–IV.[16]

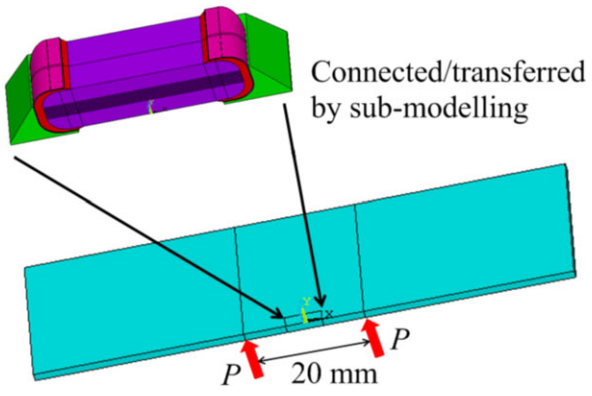

Fig. 3. Three-dimensional finite element model of the multilayer ceramic capacitor (MLCC) board flex test.

The three-dimensional numerical model used for this simulation was developed using ANSYS FEM software.[22] Because of the symmetric geometry, only half of the soldered device is modeled as depicted in Fig. 3. The PCB is composed of about 28,000 hexagonal elements while the MLCC is composed of about 220,000 hexagonal and 75,000 tetrahedral elements in the proposed finite element model. As the dimensions of the PCB (900 × 46 × 1.6 mm) are much larger than the dimensions of the MLCC (1.850 × 1.150 × 0.550 mm), the mesh density (depending on the element sizes) of the PCB is different to that of the MLCC.

In order to calculate the thermal residual stresses that form in the MLCC during the soldering and cooling processes, the temperature of the entire meshed model was initially set to 25°C and then increased to 216.9°C, which corresponds to the melting point of the weld bonding, and then finally decreased to 25°C. The assumptions used in the simulation are (i) the MLCC was stress-free at the initial temperature of 25°C; (ii) perfect bonding exists between different materials, such as the dielectric ceramics and the metal inner electrodes, the dielectric ceramic and the termination layer of the MLCC, and the solder material and the PCB; (iii) the thermal residual stress results from the different coefficients of thermal expansion of the materials employed; and (iv) no heat convection and radiation effects originating from the soldering process are taken into account.

Following the heating and cooling processes, the soldered device is subjected to the board flex test. To eliminate the influence of the test indenter radius, four-point bending of the soldered MLCC devices is performed in the FEA. It is worthwhile to note that the PCB and the MLCC are simulated in separate models. However, for the flex test modeling, the PCB and MLCC are connected by the sequential submodeling approach with a continuous displacement condition. The detailed stress distributions that occur where the MLCC is soldered to the PCB are obtained from previously generated global solutions through the submodeling technique.

In summary, the FEA considers three successive (and combined) steps: (i) the weld-bonding and heating process, (ii) the cooling process, and (iii) the bending process. Furthermore, the deflection at the external load points of the PCB in the FEA is set to a prescribed value to address the flexural stresses under different deflections. The flowchart of the proposed analysis procedure is described in Fig. 4.

The MLCCs were provided by YAGEO (Taipei, Taiwan, Republic of China) with X7R dielectric type and 0805 size that have a length of 0.08 inch and a

Table I. Properties of the Internal Electrodes at Various Temperatures (Nickel)

Properties	Value			
	25°C	100°C	200°C	300°C
Elastic modulus	207 GPa	205 GPa	203 GPa	200 GPa
Poisson's ratio	0.31	0.31	0.31	0.31
Yield stress	148 MPa	155 MPa	145 MPa	143 MPa
Thermal expansion coefficient	13.3×10^{-6}/K	13.5×10^{-6}/K	13.8×10^{-6}/K	14.1×10^{-6}/K

Table II. Properties of the Layered Termination Components (Copper and Tin)

Properties	Value			
	25°C	100°C	200°C	300°C
Copper				
Elastic modulus	207 GPa	205 GPa	203 GPa	200 GPa
Poisson's ratio	0.31	0.31	0.31	0.31
Yield stress	148 MPa	155 MPa	145 MPa	143 MPa
Thermal expansion coefficient	13.3×10^{-6}/K	13.5×10^{-6}/K	13.8×10^{-6}/K	14.1×10^{-6}/K
Tin				
Elastic modulus	54 GPa	48.4 GPa	35.5 GPa	35.5 GPa
Poisson's ratio	0.33	0.33	0.33	0.33
Yield stress	14.5 MPa	11.0 MPa	4.5 MPa	4.5 MPa
Thermal expansion coefficient	25.6×10^{-6}/K	30.0×10^{-6}/K	38.9×10^{-6}/K	38.9×10^{-6}/K

Table III. Properties of the $BaTiO_3$-based X7R Dielectric at Various Temperatures

Properties	Value			
	25°C	100°C	150°C	300°C
Elastic modulus	91 GPa	108 GPa	175 GPa	175 GPa
Poisson's ratio	0.33	0.33	0.33	0.33
Thermal expansion coefficient	7.6×10^{-6}/K	8.0×10^{-6}/K	7.8×10^{-6}/K	9.8×10^{-6}/K

Table IV. Properties of the Solder

Properties	Value		
	0°C	50°C	100°C
Elastic modulus	26.5 GPa	12.5 GPa	2.9 GPa
Poisson's ratio	0.36	0.36	0.36
Yield stress	36.4 MPa	15.2 MPa	5.8 MPa
Thermal expansion coefficient	24.7×10^{-6}/K	24.7×10^{-6}/K	24.7×10^{-6}/K

width of 0.05 inch. A soft solder was used to mount the MLCC at the center of PCB. After assembling, the PCB was subjected to deflection based on IPC/JEDEC standard 9702 by four-point bending, and MTS criterion tabletop test system was used to perform this test. The inner load span was 20 cm, and the outer support span was 40 cm.

The loading condition used in this study was displacement control with the cross-head moving to a specified displacement at the speed of 0.1 mm/s, holding at

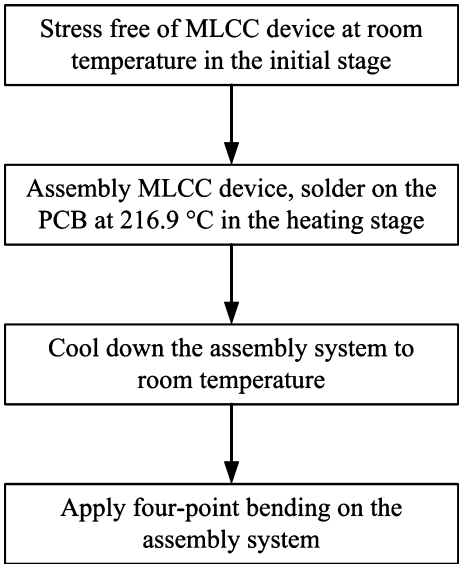

Fig. 4. Flowchart of the proposed finite element analyses (FEA).

the specified displacement for 5 s, and then unloading to origin at the same speed. The contact between the bending fixture and the PCB was lubricated to minimize the frictional stress. Optem Zoom 125 telemicroscope, with a working distance of 10 cm, was used to perform the *in situ* observation of cracking of MLCC during the test. In order to facilitate the observation, the mounted PCB was cut and polished prior to the test. The experimental setup is illustrated in Fig. 5.

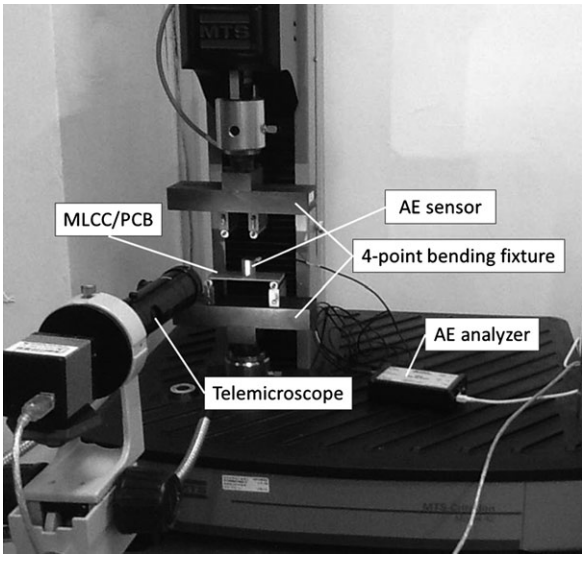

Fig. 5. The setup of the in situ crack observation system of the four-point bending test.

To avoid tensile cracking during the board flex test, different design rules are investigated using the design of experiment (DOE) method. Contrast to the one-factor-at-a-time approach, the DOE method takes the interaction between factors into consideration. In this study, a fractional factorial experiment design, standard Taguchi L9 (3^4) design method, is chosen for the investigation because it can account for the four parameters at three different levels.[23] Instead of 3^4(=81) experiments in the traditional full factorial design, a Taguchi L9 design method needs only nine experiments with statistical considerations. This format is chosen from preliminary works that identified four relevant design parameters, namely (A) the number of inner electrodes, (B) the height of the soldering material, (C) the length of the lateral margin, and (D) the thickness of the nickel layer in the termination component.

Details of the effects of different parameters on the experimental results are obtained by considering three values for each parameter. The corresponding values in each of the three levels, listed in Table V, all are manufactured solutions in YAGEO. The effect of each parameter level can be estimated as the following:

$$m_{X_i} = \frac{1}{3}\sum_{j=1}^{3} Y_j \mid_{X=X_i} \quad (1)$$

where the subscript X_i represents the design parameter X at the i-th level and Y is the desired performance value of the experiment at $X = X_i$. Note that the effect of each parameter at each level can be calculated by the above equation according to the Taguchi orthogonal array as shown in Table VI. The overall mean of the nine experiments can then be determined by:

$$m = \frac{1}{9}\sum_{j=1}^{9} Y_j \quad (2)$$

Then, the analysis of mean and analysis of variance were employed to identify the sensitive and passive parameter for each property.[23]

Table V. Chosen Parameters and their Levels

	Level		
Parameter	**1**	**2**	**3**
A: electrode number	5	9	13
B: solder wicking height (μm)	200	350	500
C: lateral margin length (μm)	250	300	350
D: termination thickness of nickel (μm)	2	4	6

Table VI. Taguchi L9 Orthogonal Array Design and the Computed Maximum Principal Stresses (unit: MPa)

Exp.	A	B	C	D	σ_1 (Soldering)	σ_1 (Bending)
1	5	200	250	2	44.98	200.39
2	5	350	300	4	49.79	93.42
3	5	500	350	6	60.85	92.43
4	9	200	300	6	44.74	113.72
5	9	350	350	2	51.28	89.29
6	9	500	250	4	53.21	159.71
7	13	200	350	4	42.30	92.61
8	13	350	250	6	45.72	120.13
9	13	500	300	2	57.14	141.59

Finally, a confirmation experiment was carried out to verify the reliability and feasibility of the Taguchi design method. As the sensitive parameters and the corresponding optimal levels have been obtained, the summary optimal condition can be calculated as:

$$Y_{\text{opt}} = m + \sum_{X \in \text{sensitiveparameters}} (m - m_{X_{\text{opt}}}) \qquad (3)$$

where m is the overall mean and $m_{X_{\text{opt}}}$ is the mean effect of sensitive parameters at the optimal level.

It is worth noting that the thicknesses of the dielectric ceramic layers in the active region have to be changed accordingly in the nine experiments even though thicknesses are not a selected design parameter. The thicknesses of the dielectric ceramic layers in the active region are modified, so that the height of the MLCC is constant while the thickness of the cover margin remains unchanged. To avoid tensile cracking in the MLCC, the maximum principal stress, σ_1, in the dielectric ceramic layers under 3 mm deflection in the board flex test is chosen to evaluate the performance of different experiments.

Results

As the soldering procedure, which includes both heating and cooling processes, is identical for all bending tests, solely the case of 3 mm deflection is herein discussed. In addition, because flexural cracks occur only in the dielectric ceramics ($BaTiO_3$ layers), the stresses in the dielectric ceramics are investigated to avoid brittle fracture hereafter.

The maximum and minimum principal stress distributions of the ceramics during the soldering process are shown in Figs. 6a–d, respectively. Throughout the weld-bonding and heating process, the maximum and minimum principal stresses in the active region of the dielectric ceramic approach zero, which implies that most of the dielectric ceramic is stress-free. High tensile stress occurs at the top and bottom rounded corners of the outer surface of the dielectric ceramic, corresponding to points labeled A and B in Fig. 6a. The peak value of the maximum principal stress was 45.78 MPa which occurs at point A. In addition, as shown in Fig. 6b, compressive stress is observed at the outer surface of the cross-section defined by points C and D.

Following the cooling process, the maximum principal stresses, σ_1, throughout most of the ceramic are negative, which implies that the ceramic is under compression. From Figs. 6c, d, most of the dielectric ceramic is stress-free with only little compressive residual stresses in the lower region of the structure. The maximum tensile stress is 56.73 MPa observed at the outer surface in the upperpart of the ceramic near point C shown in Fig. 6c. The thermal residual stresses result from the difference in the thermal expansion coefficients of the dielectric ceramic layers ($BaTiO_3$) and the nickel electrode.

The distribution of maximum principal stresses that result from weld-bonding and heating, cooling, and bending processes under different deflections is shown in Fig. 7. From Fig. 7a, it is evident that the location of maximum tensile stress changes from the upperpart (end of the soldering process) to the lower part of the dielectric ceramic under 3 mm deflection at the outer surface of the dielectric ceramic. In addition, the compressive stress occurs at the lower part of the dielectric ceramic close to the symmetric plane (i.e., *XZ* plane) while the inner part of dielectric ceramic has little tensile stress as shown in Fig. 7b.

Moreover, comparing Fig. 7a with Fig. 7c, one can find that the area subjected to tensile stress spreads when the deflection is increased from 3 to 4 mm. The corresponding peak value of σ_1 increases from 90.72 to 100.67 MPa as the deflection increases. The area experiencing high tensile stress covers nearly the entire region, where the termination layer attaches to the outer surface of the dielectric ceramic. On the other hand, the rounded corners in the upperpart of the dielectric ceramic are also under compression. When deflection is increased, the area under compression is reduced and concentrated at regions prementioned before.

The peak values of maximum principal stress, σ_1, in the dielectric ceramics from nine tests following soldering and bending processes are listed in Table VI. The peak values of σ_1 during the soldering process are approximately one-fifth to half of that which occurs throughout the soldering and bending process. Therefore, only the final results after soldering and bending flexural stresses are included in this study. The factor effect of the peak maximum principal stress during the board flex test is carried out by averaging the numerical results from nine test runs

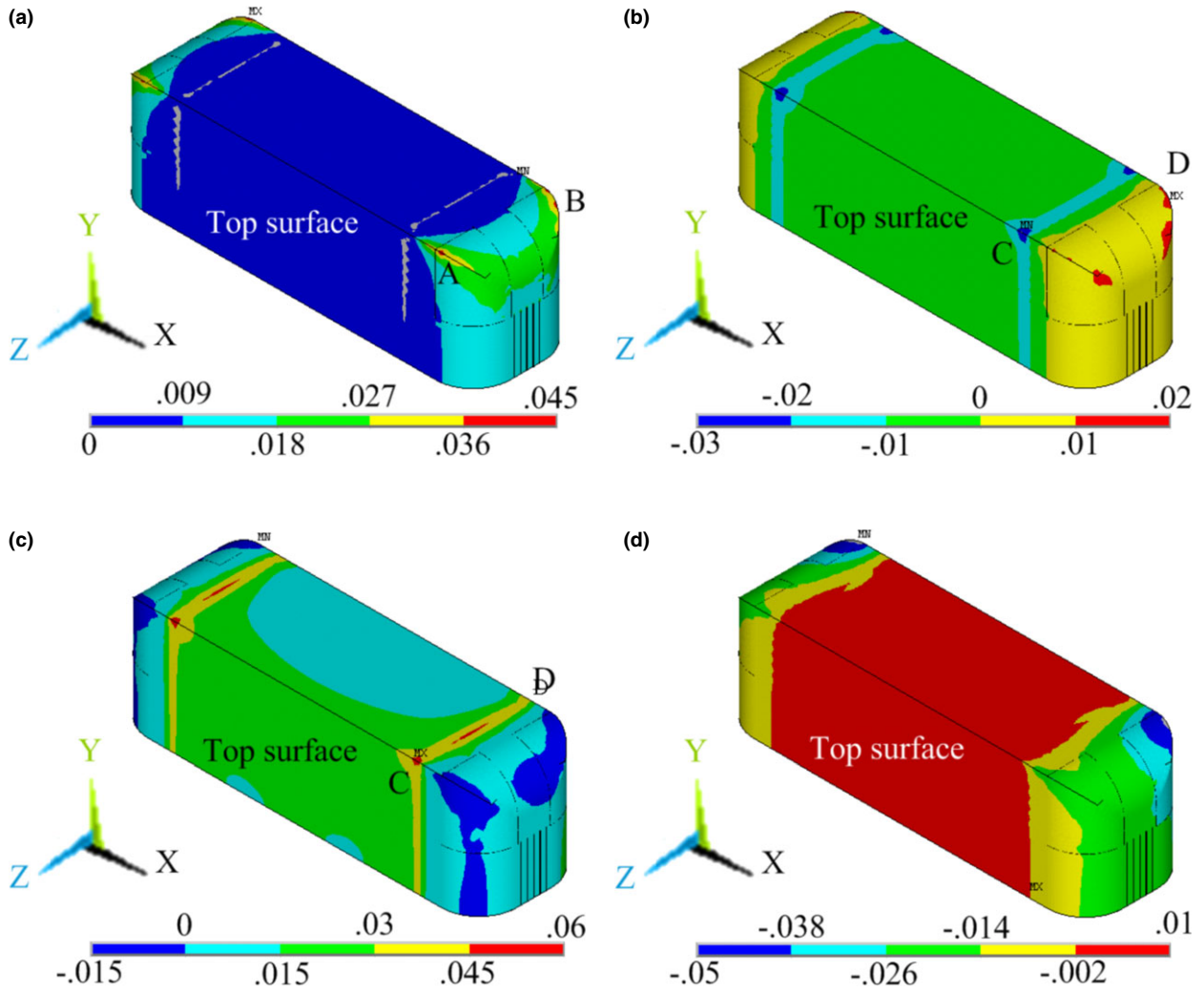

Fig. 6. Maximum and minimum principal stress contours operative during the soldering process (unit: GPa) ([a] Maximum principal stress [heating]; [b] Minimum principal stress (heating); [c] Maximum principal stress [cooling]; [d] Minimum principal stress [cooling]).

corresponding to each level of each parameter and is plotted in Fig. 8. Figure 8 shows the relationship between peak values of σ_1 and the chosen parameters. It is worth noting that the peak value of σ_1 is mainly influenced by the length of the lateral margin in the MLCC. In addition, the thickness of the termination (nickel) and the height of the soldering material are subordinary factors. Furthermore, the number of metal inner electrodes has less effect on the peak value of σ_1 than the previous three parameters.

By increasing the length of the lateral margin in the MLCC, the peak value of σ_1 in the dielectric ceramic decreases and tensile cracking in the dielectric ceramics can be avoided. The peak value of σ_1 for the lateral margin at level 3 is only 57.1% of the same parameter at level 1. In addition, the peak value of σ_1 in the dielectric ceramic can also be decreased by increasing the thickness of the nickel layer in the termination component. Similarly, the peak value of σ_1 for the nickel thickness at level 3 is only 75.7% that of the same parameter at level 1. Furthermore, the peak value of σ_1 in the dielectric ceramic is decreased when the height of the soldering takes on the value for level 2. Finally, the maximum principal stress, σ_1, in the dielectric ceramic is further decreased by increasing the number of metal inner electrodes in the MLCC.

Discussion

Following cooling from the soldering temperature, FEA demonstrate that the tensile stresses concentrate in

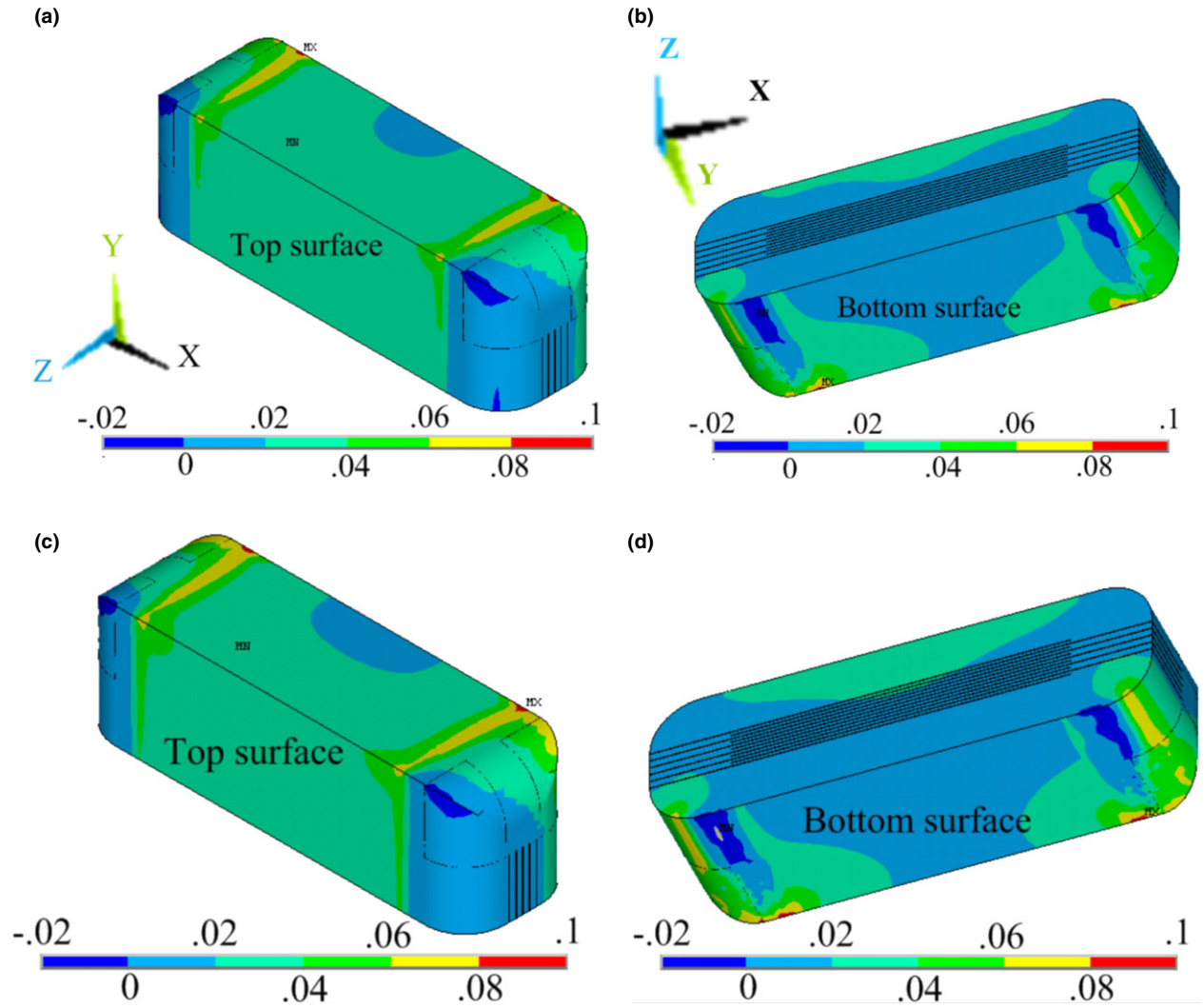

Fig. 7. Maximum principal stress contour under different deflections during the board flex test (unit: GPa) ([a] Deflection = 3 mm [oblique view 1]; [b] Deflection = 3 mm [oblique view 2]; [c] Deflection = 4 mm [oblique view 1]; [d] Deflection = 4 mm [oblique view 2]).

the upper cover layer of the dielectric ceramic and compressive stresses concentrate in the lower cover layer. Numerical results reveal that thermal residual stresses in the dielectric ceramic show in-plane compressive values of up to 52.14 MPa (as shown in Fig. 6d), which are consistent with values (60 MPa) obtained from X-ray diffractometry measurements.[13,16] Numerical results further indicate that the location of maximum tensile stress changes from the upperpart of the dielectric ceramic during the soldering process to the lower part throughout the board flex tests. This implies that the thermal residual stress from soldering could compensate, to some extent, the flexural stresses of the bending test. However, the thermal tensile residual stresses are about one-fifth to half of the bending flexural stresses that occur during the board flex tests in the nine test experiments. Therefore, the flexural stresses that result from the bending process still dominate the stress distribution in the dielectric ceramic. In other words, the soldering process does not cause significant thermal residual stress except at the lower corners of the MLCC.

The board flex test was performed 10 times for X7R0805 MLCCs while the average deflection corresponding to the initial crack occurrence was 4.4 mm. These cracks typically originated near the edge of the termination margin from top or bottom surface and then extended across the dielectric ceramic. A typical example of a flex crack at one of the MLCC end terminations is shown in Fig. 9. The locations of peak tensile stresses from numerical simulations coincide with the crack initiation

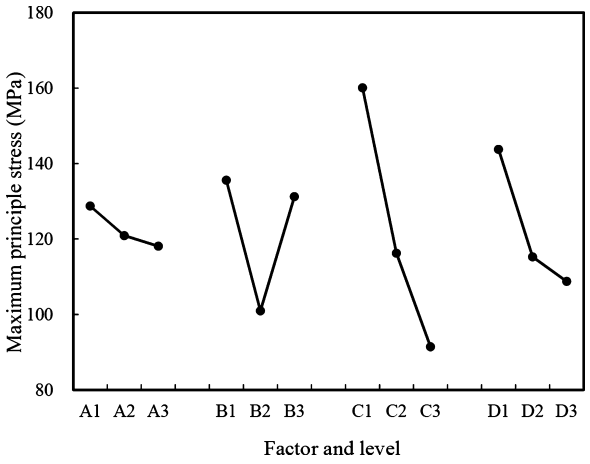

Fig. 8. The effect of parameters on the maximum principal stress.

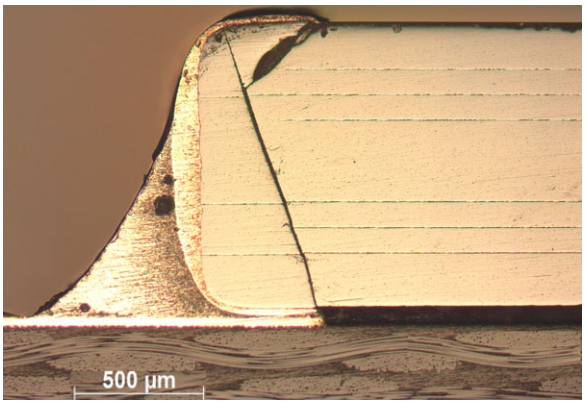

Fig. 9. In situ observed bending crack in the multilayer ceramic capacitor (MLCC) during the board flex test.

sites observed in flex tests. Areas subjected to high tensile stress display the same trend with crack patterns. Numerical simulations further demonstrate that the peak tensile stresses occur at the outer surface of dielectric ceramic and the inner part has little tensile stress.

The effects of the four design parameters, which again include the number of metal inner electrodes, the lateral margin width, the thickness of nickel in the termination layer, and the solder wicking height, on the peak tensile stress following board flex tests were parametrically investigated. Firstly, numerical results show that the peak value of σ_1 is mainly influenced by the length of the lateral margin in the MLCC under the constraint of a fixed housing margin width. It is interesting that peak values of σ_1 increase monotonically during the soldering process as the width of the lateral margin increases, while peak values of σ_1 are relieved monotonically by the bending process as the width of the lateral margin increases. The variation in thermal residual stress displays the same trend as those found in the sintering process.[9] Secondly, different solder heights, which are measured from the base of the dielectric ceramic to the uppermost point of the solder, influence the peak value of σ_1. Franken *et al.*[16] showed that the failure probability increases as the solder heights decrease, which is consistent with our results. Our simulation results also indicate that both overly low and overly high solder heights induce high tensile stress during the bending process. Thirdly, the MLCC termination simulations indicate that thicker layers of nickel are associated with lower values of tensile stress. Finally, a minor influence is also observed by varying the number of inner electrodes. The reason of little influence of the number of inner electrodes could be resorted to small variation at each level of this parameter. A trend toward declining maximum principal stress values with an increasing number of inner electrodes is observed, which could be employed to decrease the failure probability of MLCCs.

As shown in Fig. 8, the optimum conditions for minimizing the peak value of σ_1 are A3B2C3D3, which corresponds to the greatest number of inner electrodes, a moderate value for the solder wicking height, the greatest value of the lateral margin, and the largest value of the nickel thickness considered herein. According to Eq. (3), the corresponding maximum principal stress is predicted to be 77.61 MPa with the major contributing factors being parameters C and D. A confirmatory virtual experiment was carried out to verify the reliability of Taguchi's method; the result obtained from FEA is 80.33 MPa, which is consistent with the predicted optimum value of the maximum principal stress.

Conclusions

A parameter-based numerical model for simulation of the soldering and bending of MLCCs was presented. The effects of thermal residual stresses resulting from the soldering process were discussed within the framework of three-dimensional FEA. Compared with the flexural stress resulting from board flex tests, the thermal residual stress contributes less to the maximum tensile stress. For a MLCC (X7R 0805) of specific dimensions, the effects of four selected design parameters were investigated using the Taguchi orthogonal design. The results show that manipulation of the length of the lateral margin most significantly influences the maximum principal stress experienced in MLCCs during flex tests. In addition, the nickel termination thickness and the solder height also contribute to the tensile stress that occurs in the bending process. Consequently, optimal MLCC design criteria based on Taguchi orthogonal arrays were proposed.

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