Gambali Seshasai Chaitanya

Bachelor of Technology
Electronics and Communication Engineering
Indian Institute of Technology (BHU) Varanasi

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Education

Degree	Institute	Board / University	CGPA/Percentage	Year
B.Tech ECE	Indian Institute of Technology (BHU) Varanasi	IIT (BHU) Varanasi	8.45 (Till 6th Sem)	2022-2026
Senior Secondary	St. Francis School, Indirapuram	CBSE	96.8%	2021
Matriculation	St. Francis School, Indirapuram	CBSE	97%	2019

Experience

- **Jaguar Land Rover** *May 2025 - July 2025*
  Embedded Systems Intern Bengaluru, Karnataka
  - Designed and implemented a **secure two-stage bootloader architecture** with Root of Trust and Digital Signature verification, incorporating **AES decryption** capabilities to protect sensitive IP in compiled firmware binaries.
  - Optimized the bootloader design for low runtime memory usage and heap utilization for running in highly resource constrained environments.

- **RISC-V International @ Linux Foundation Mentorship 2025** *March 2025 - June 2025*
  Project Mentee Remote
  - Developed a **Hardware Abstraction Layer Transitional Library for Software to Hardware Posits For RISC-V** under the mentorship of Prof. Joshua Gyllinsky, the RISC-V foundation. Selected as a mentee for the Spring term of the Linux Foundation Mentorship Program, Spring 2025
  - Improved and delivered a new version of the SoftPosit-cpp Library that provides native support for posit arithmetic. Implemented math functions for 8, 16 and 32-bit posits with benchmarks, unit tests.
  - Created CI/CD pipelines for automating building and packaging, developed a Python Wrapper for SoftPosits and created a debian Package.

- **Google Summer of Code, 2025** *June 2025 - September 2025*
  Software Development Intern Remote
  - Contributing to **OpenROAD**, an Open Source RTL2GDSII flow for digital IC design. Working on implementing support for polygonal floorplans inside the flow. Modifying the user facing tcl scripts, intermediate SWIG wrappers and the backend C++ logic to support polygonal floorplans.

- **Indian Institute of Technology Bombay** *May 2024 - July 2024*
  Summer Research Intern (with Prof. Sandip Mondal) Bombay, India
  - Developed Verilog and Embedded C-based applications using Vivado and Xilinx SDK to run on a Digilent Zybo FPGA board for developing an **FPGA based controller** to perform Read, Write and Erase Operations on 2D and 3D SLC and MLC Raw **NAND Flash** Chips.
  - Used bit-banging to precisely control the onboard GPIO pins to interface with the Raw NAND using the ONFI Consortium Protocol. Developed programs in Embedded C to run on **Embedded Linux** on an Altera DE1 SoC.

- **Google Summer of Code, 2024** *May 2024 - August 2024*
  Software Development Intern Remote
  - Contributed to **Apertium**, an open source machine translation platform. Developed core tools with command line utilities for automated bidirectional dictionary generation from a set of parallel translated texts.
  - Experimented with and employed various methods for word alignment in parallel translated texts, such as Bayesian models with Markov Chain Monte Carlo and Graph Neural Networks for multiparallel word alignment.

- **University of Michigan** *November 2024 - March 2025*
  Software Development Intern (with Prof. Mehdi Saligane) Remote
  - Worked on creating an ABC script to improve synthesis options in Yosys for creating a balanced synthesis plan, balancing between Speed and Area optimized synthesis. Integrated this new tool with the OpenRoad flow for Power Performance and Area analysis of Verilog Modules.

- **Indian Institute of Technology Roorkee** *January 2024 - March 2025*
  Project Intern Remote
  – Worked on SPICE simulations of crossbar arrays with interconnect models for interconnect-aware analysis and evaluation of thermal effects on crossbar performance. Simulations were performed using industry-based Verilog-A models of FeFET devices and interconnects.

- **Anonimo Interactive** *May 2024 - August 2024*
  Machine Learning Intern Remote
  – Trained Machine Learning models using state-of-the-art approaches for Options Market Forecasting, Market Swing Prediction and Implied Volatility Prediction. Developed a portal to fetch live market data from the Zerodha API and run inference on it for market predictions
  – Developed a RAG-based Sales Assistant for answering consumer queries with product-specific information sourced from catalogues. Created a backend server and APIs for access from a customer-facing frontend.

Conferences and Publications

–Gambali Seshasai Chaitanya, Ankit Arora, *"A Non-Volatile ReRAM and Subthreshold-FET-Based Kernel for Energy-Efficient Temporal Signal Processing Using Reservoir Computing"*, 23rd Non Volatile Memory Technology Symposium (NVMTS 2025, Poster Presentation)

–Gambali Seshasai Chaitanya, Shubham Pande, Ankit Arora, *"ReRAM-based Crossbar Compatible Equality Checker for Neuromorphic Applications"*, 8th Students' Conference on Engineering & Systems (SCES-2024, Oral Presentation)

–Gambali Seshasai Chaitanya, Vaseekaran Elangovan, *"ReRAM Crossbar Compatible Efficient Equality Checker and Half Adder Implementation,"* XXII International Workshop on Physics of Semiconductor Devices (Oral Presentation)

–Gambali Seshasai Chaitanya, Arin Weling, Sandip Mondal, *"Stress Induced Failure Mechanism in NAND Flash Memory Devices,"* Electronic Materials Conference 2025 (Poster Presentation)

–Arin Weling, Gambali Seshasai Chaitanya, Sandip Mondal, *"Thermal-Induced Threshold Voltage Distribution Changes in 3D NAND Flash Cells: Experimental Characterization,"* Electronic Materials Conference 2025 (Oral Presentation)

–Asifa Khatun, Gambali Seshasai Chaitanya, Sandip Mondal, *"Page and Block-wise Program Disturb Operation in NAND Flash Memory,"* Electronic Materials Conference 2025 (Poster Presentation)

Projects

- **RISC-V CPU Implemented in Verilog HDL** *Jan 2024 - Apr 2024*
  – Designed and implemented a RISC-V CPU from scratch using Verilog as the hardware description language.
  – Worked on creating a microarchitecture, implementing the instruction set architecture (ISA), optimizing performance, and debugging the design through simulation tools.
- **Neural Network Inference on FPGAs** *Jan 2024 - Apr 2024*
  Dr. Sonam Jain
  – Developed a Convolutional Neural Network and ran inference on FPGAs for Edge Computing
  – Implemented a behavioural model of a neuron in Verilog and used it to construct a fully connected network
- **Systolic Hardware Accelerator for Vector Matrix Operations** *March 2024*
  IChip, Udyam'24, IIT (BHU) Varanasi
  – Designed a Hardware accelerator that efficiently performs Matrix multiplications and Convolutions
  – Connected various components using an AXI-4 Interrupt controlled interface and Implemented the project in Verilog.

Achievements

- 3rd prize winner in the National Level Digital Design Hackathon conducted by the Ministry of Electronics & Information Technology of India (MeitY) under the Chips to Startup (C2S) Program.
- International Finalist in Google Code-In 2019, out of 14,798 participants from 117 countries
- Winner of the 'Startup with German' Scholarship, awarded by Goethe Institute. Felicitated by **Angela Merkel**
- Winner of Times Scholar 2019, Felicitated by the then Vice President of India, **Shri Venkiah Naidu**
- National Finalist in Hack AI, an AI/ML based Hackathon, Techfest, IIT Bombay
- 2nd in FPGA-based round in I-Chip, a Verilog-based event in Udyam'24, EES IIT (BHU) Varanasi
- Finalist in Digisim, a Digital Electronics Event, Udyam'24, EES IIT (BHU) Varanasi