EE 241 MIDTERM 1 FAll 2021

Name :

Number :

1) (10 p)Implement the boolean equation

$$\overline{((AB+CDE)F+G)}$$

using complemantary CMOS.

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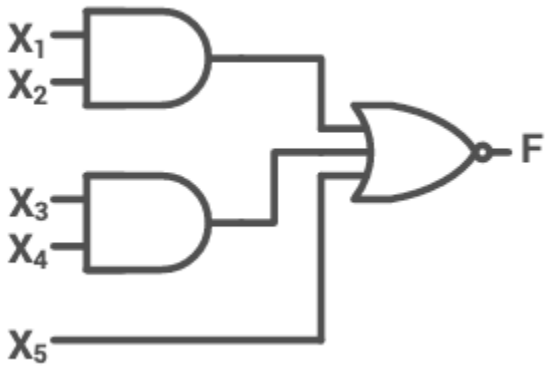
2)(20) Given the curcuit below



a) Drive the Sop

b) implement the sop using complemantary CMOS

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3) Given the truth table below:

X	Y	B_{IN}	D	B_{OUT}
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

a)(5) Drive sop for Bout (use k-maps)

c)(5)implement Bout in 8-to-1 mux

d)(10)implement Bout in 4-to-1 mux. Hint : use x and y as select signals and attach each input to the appropriate choice of 0,1 or Bin

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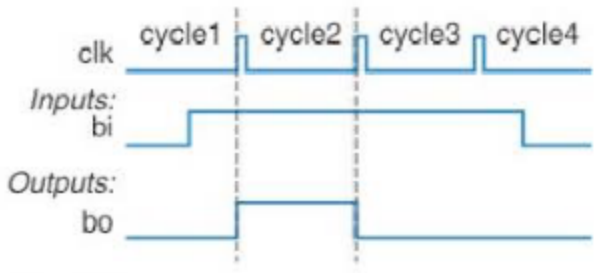
4)(25) You are to design a system that synchronizes a button press to a clock signal: when you press the button your output should be high only for one cycle. A sample timing diagram is shown below where bi is system input and bo is system output.



a) (5) Draw the state diagram.

b) (5)Write down the truth table for fsm

c) (5)Calculate output and next state logic.

d) (10)Implement your FSM in verilog using behavioral blocks.

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5)(25) Table 1: Truth Table.

Table 1: Truth Table.

sw[2]	sw[1]	sw[0]	led[2]	led[1]	led[0]
0	0	0	0	1	0
0	0	1	0	0	0
0	1	0	1	1	0
0	1	1	1	0	0
1	0	0	1	1	0
1	0	1	0	0	1
1	1	0	0	1	0
1	1	1	0	0	1

a)(5) For the truth table of Table 1. Use Karnaugh Map to simplify the Output LED.

b) (5)Draw logic gates circuit for the simplified output LED from your answer in (a).

c) (5)Write a Verilog design source module of the simplified output LED using dataflow modelling.

d) (10)Write a Testbench module that simulates all combinations of the output LED.

Good Luck