EE241 Fall 2022 Final

1)

You will design and implement the following modules which have two 8 bit inputs (a and b) and outputs a 1 if

a) (10) a=b

b) (10) a>b

c)(10) a<b

For each option deliver your verilog project with test bench.

2)

Recal that multiplacation is repetetive additon:

4 x 3 = 4+4+4 = 3+3+3+3

C snippet below shows an implementation

int n=4; int m=3; do {m=m+m; n=n-1;} } while (n!=0);

a)(5) identify the operations you need in datapath

b) (15) Design (draw) the datapath

c)(20) implement and test your datapath design in verilog

d) (10) Draw the high level fsm and covert it to a fsm state chart.

e) (20) implement and test both the controller and the datapath in a module named mymultiplier.