EE 241 Fall 2022 RECit

1) (20)ou are given the following multiplication module module unsigned_mult (out, a, b); output [15:0] out; input [7:0] a; input [7:0] b;

```
    assign out = a * b;
```

endmodule

Write down a test bench to test the module Deliverables Your Verilog Project

2) 80 Exponentiation is defined as

$$b^n = \underbrace{b \times b \times \cdots \times b \times b}_{n \text{ times}}.$$

You are to design and implement a system in verilog which can calculate b^n where b and n are 4bit unsigned integers.

a) 10 pseudo code or c code b) draw the datapath clearly c)implement the datapath and a proper test bench in verilog d) draw high level fsm state chart for the controller and convert it to fsm state chart e) implement the controller and a proper test bench in verilog f) implement the overall sytem which has two inputs (other than reset and clk) b and n and one output b^n