EE241 Midterm2

Q1: (35)

You are to design a baby as an fsm. Your baby has three states : Sleeping (also initial), Hungry and Crying. Your baby's interface to the world is via three signals: green, yellow, red. She sets green high when sleeping, yellow high when hungry and red high when crying. She stays in the state crying unless she is fed and returns to sleeping state when fed.

a) Draw the block diagram of your baby module

b) drive the truth table

c) drive the next state and output logic.

d) implement your baby in Verilog

e) write the test bench and prove that your system is working by simulation.

Q2: 35

You are to design a mother as finite state machine. Mother has three inputs green,yellow,red. Mother is initially in birth state then she makes a transition to Content state. She stays in that state as long as the input to the module is green. if not her state changes to observant State. In the observant state if she receives a green input she returns back to the Content state and if not she passes to feeding state. Mother states in the feeding state as long as she recives a green. She has only one output: milk. She sets milk high in the feeding state.

a) Draw the block diagram of your baby module

b) drive the truth table

c) drive the next state and output logic.

d) implement your baby in Verilog

e) write the test bench and prove that your system is working by simulation.

Q3: -(100010)

You are to design a sytem named Habitat. Habitat has only clock input and an output named alarm.It consists of two modules mother and child. İt sets alarm high when mother is feeding.

a) Draw the block diagram of your baby module

b) drive the truth table

c) drive the next state and output logic.

d) implement your baby in Verilog

e) write the test bench and prove that your system is working by simulation.

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