**EE241 Digital Curcuits**

**Goals:** The aim of this course is to provide the students with the knowledge of digital circuit components and the principles of logic circuit design.

**Content:** This course covers; analog and digital signals, number systems, coding, binary numbers and arithmetic, digital logic circuits, Boolean arithmetic, logical design, Karnaugh maps, digital integrated circuits, combinational logic circuits, flip-flops, sequential logic, digital devices, counters,

recorders and memory elements.

**Textbook:** UNSALAN CEM,Tar Bora, Digital System Design with FPGA: Implementation using Verilog and VHDL, New York. 2017.,

Charles Roth, Lizy K. John, Byeong Kil Lee - Digital Systems Design Using Verilog-CL Engineering ,

Introduction to Logic Circuits & Logic Design", by Brock J. LaMeres published by Springer International in 2016.

**Additional Resources**

Lecture notes: will be published on yulearn

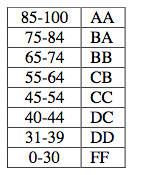
Videos for the text book titled "Introduction to Logic Circuits & Logic Design", by Brock J. LaMeres published by Springer International in 2016.

https://www.youtube.com/playlist?list=PL643xA3Ie\_Et2uM4xu1yFk-A5ZQQ8gQ5e

| **ASSESSMENT** | | |
| --- | --- | --- |
| **IN-TERM STUDIES** | **NUMBER** | **PERCENTAGE** |
| Midterms | 2 | 25 |
| Laboratory | 10 | 10 |
| Homework/quiz | 1 | 10 |
| **Total** |  | **70** |
| **CONTRIBUTION OF FINAL EXAMINATION TO OVERALL GRADE** | 1 | 30 |
| **CONTRIBUTION OF IN-TERM STUDIES TO OVERALL GRADE** |  | 70 |
| **Total** |  | **100** |

| **COURSE CONTENT** | | |
| --- | --- | --- |
| **Week** | **Topics** | **Study Materials** |
| 1 | Digital System, Analog - Digital Signals, Digital Coding, Representation of Numbers, Conversion from decimal to other number bases | Lecture Notes, text book |
| 2 | Binary to decimal base conversion, Octal/hexadecimal to binary base conversion and re-conversion, Displayed Signed Numbers | Lecture Notes, text book |
| 3 | Binary Logic and Gates, Binary Variables, Truth Tables, Boolean Algebra, Evaluation of Boolean Functions | Lecture Notes, text book |
| 4 | Verilog: Introduction | Lecture Notes, text book |
| 5 | Logic gates, circuit diagrams and logical expressions | Lecture Notes, text book |
| 6 | Implementation of basic logic gates with Verilog | Lecture Notes, text book |
| 7 | Midterm 1 | Lecture Notes, text book |
| 8 | Design of combinational logic circuits | Lecture Notes, text book |
| 9 | Combinational logic implementation with Verilog | Lecture Notes, text book |
| 10 | Latches and flip-flops, analysis of synchronous sequential logic circuits | Lecture Notes, text book |
| 11 | Midterm 2 | Lecture Notes, text book |
| 12 | Verilog: Latch and flip-flop implementation | Lecture Notes, text book |
| 13 | Synchronous sequential logic circuit design | Lecture Notes, text book |
| 14 | Verilog: Implementation of sequential logic circuits | Lecture Notes, text book |
| 15 |  |  |

Below table will be used for the determination of letter grades. The table is fixed and will NOT be modified in any case.



It is a must to get a min. 30 in the Final Exam. In any case (even their in-term mark is greater than 30), when the final exam score is <=30, these students will get FF as the letter mark.

They will have the chance to attend the ReSit exams (Bütünleme Sınavı). There is no min. limit for the ReSit exams.

It is a MUST for students to attend the Final exam and midterms. Otherwise, they will NOT have the right to attend the Resit Exam, and they will be evaluated as FA.

It is also necessary to attend all LABORATORY sessions (you will only have 1 make Up session to compensate for the missing laboratory. When you fail from the laboratory, you will be evaluated as FA independent from the other works you performed.

6Attendace is also a MUST (min 80% attendance). Otherwise, you will be evaluated with FA.