Computer Architecture Lab (CS 341)

Assignment 7: MIPS Pipeline Simulator Due Date: 01/11/20

(Lab Assignment 4)

For this and the remaining two assignments, you are free to work individually or in a team. Ideally, if you work in a team, it would be the same team (or subteam) as in the course project. In any case, clearly spell out the team members involved in this assignment.

Questions 1 and 2 are related to ONLY single cycle instructions, i.e., instructions that require just 1 cycle to be executed (in the EX stage).

1. Craft a sequence of 4-5 MIPS instructions that you think best illustrates the need for data forwarding. Feed the instructions to the pipeline simulator. Report the total execution times of the instructions without and with forwarding.
2. Design your own experiments with the pipeline simulator to figure out:
   (a) The stage in which the branch target address is computed
   (b) The stage in which the branch condition is evaluated
   (c) The number of stalls due to a taken branch without a branch delay slot
   (d) The number of stalls due to a taken branch with a branch delay slot

   Report your results for each of the above and anything else of interest you may have noticed.

The remainder of the questions are related to the MIPS processor with multiple functional units which are supported by the pipeline simulator. Note that some of these are multi-cycle execution units – further, some of them may be pipelined and at least one is not.

3. Craft a sequence of instructions that uses ALL functional units, i.e., there is at least one cycle during which all functional units are simultaneously busy. Report the instruction sequence and the cycle.
4. Can two or more instructions finish execution during the same cycle? If so, which gets promoted to the MEM stage? Craft and report the sequence of instructions to support your answer.
5. Can structural hazards occur on the processor being simulated? If so, which component (or components) cause the structural hazard. Report the sequence of instructions that illustrates this.
6. Can a WAW hazard occur? If so, report the code sequence that best depicts this together with the pipeline timing diagram generated by the simulator.
7. Can a WAR hazard occur? If so, report the code sequence that best depicts this together with the pipeline timing diagram generated by the simulator.