Computer Architecture Theory + Lab (CS 305/341)

Assignment 8: Memory Hierarchy Due Date: 10/11/20

(Theory Assignment 4)

1. A machine has two levels of cache. The miss rates of L1 and L2 are respectively 40 and 20 per 1000 memory references. (Of the 40 references missed by L1 and picked up by L2, 20 are missed). The hit times of L1 and L2 are respectively 1 and 10 cycles while the miss time of L2 is 200 cycles. Assume that 50% of all instructions executed are Load/Store.
   (a) The average memory access time of L1 cache is _____ cycles .
   (b) The average memory access time of L2 cache is _____ cycles .
   (c) The average number of stalls per instruction is _____ cycles.
   (d) The average number of stalls per instruction assuming the presence of only L1 but not L2 is _____ cycles .

   Explain clearly how each answer was obtained.

2. Consider a toy 32-byte D-cache accessed using physical addresses. Assume the replacement policy is LRU and the MM update policy is write back with write allocate on a write miss.

```
        li    $2, 0
        addi  $3, $0, 5
here:   lw    $1, arr($2)
        addi  $2, 4
        sw    $1, arr($2)
stride: addi  $2, 16
        addi  $3, -1
        bnez  $3, here
```

   Assume that the start address (physical) of array, arr is 0x100 and that the width of the physical address is 16 bits on this toy machine. The questions below pertain to the execution of the above program on this machine.
   (i) The number of D-cache misses assuming D-cache is direct-mapped with line size = 4 bytes is _____ .
   (ii) The number of D-cache misses assuming D-cache is direct-mapped but with line size = 8 bytes is _____ .
   (iii) In the instruction at label “stride”, if 16 were replaced by 12, the answer to (ii) above would be _____.

(iv) The number of D-cache misses assuming D-cache is 3-way set associative with line size = 4 bytes is _____ .

(v) On program termination, the values of the tags in the set bearing index value = 1 in case (iv) above is/are

_____ .

Express tag values in decimal above.

Explain clearly how each answer was obtained.